SSC2101S

Power Factor Correction Continuous Conduction Mode Controller

Features and Benefits

- Interleaved Discontinuous Conduction Mode (DCM) operation: low peak current, low ripple current, and low noise; for medium- to high-power applications
- Constant Voltage Mode control: no auxiliary windings required on inductors because of the built-in arithmetic circuit; achieves a simple PFC system
- Maximum on-time: 15 µs (typ)
- Built-in Soft Start function: reduces stress on power devices at startup
- Built-in High Speed Response (HSR): suppression of output voltage changes during dynamic load transients
- Error Amplifier reference voltage: 3.5 V (typ)

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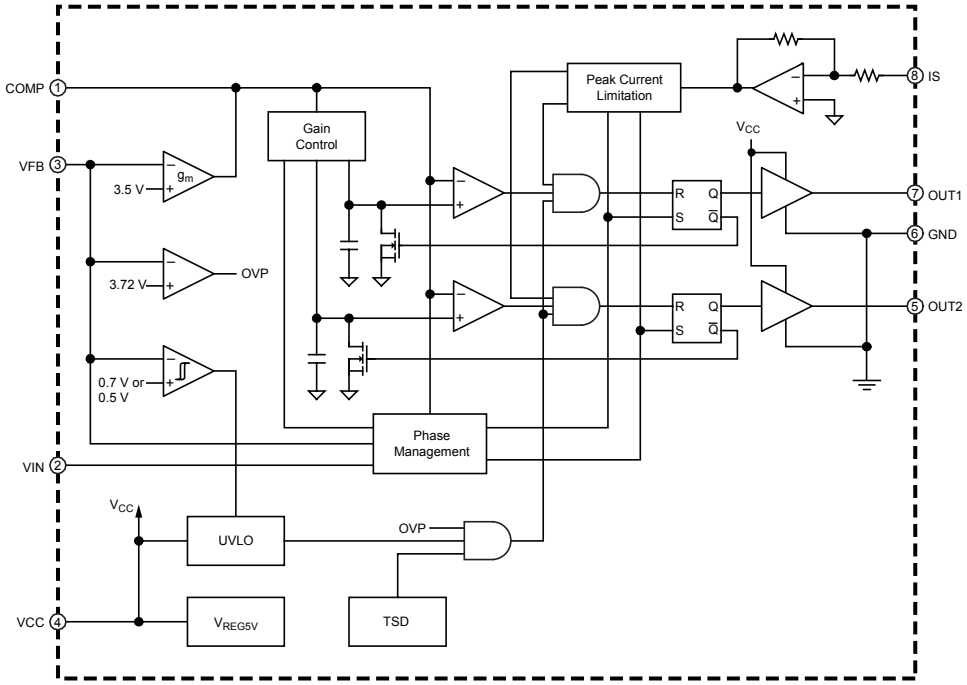
Package: SOP8

Description

The SSC2101S is a controller IC intended to implement a Discontinuous Conduction Mode (DCM) interleaved Power Factor Correction (PFC) circuit. Using the two-phase interleaved control incorporated in this IC, it is possible to achieve a low cost, high performance PFC system with low input/output ripple currents, low noise, and few external components.

Functional Block Diagram



Features and Benefits (continued)

- Protection Functions
  - Soft Overvoltage Protection (SOVP): output voltage reduction
  - Output Overvoltage Protection (OVP): gate drive on/off on a pulse-by-pulse basis, with auto-restart
  - Overcurrent Protection (OCP): dual-level OCP, with auto-restart
  - Output Open Loop Detection (OLD): switching operation stop and transition to standby mode
  - Open Terminal Protection (OTP): switching operation stop or output voltage reduction, during open condition on VFB, VIN, or IS terminals
  - Thermal Shutdown (TSD): auto-restart with hysteresis

Selection Guide

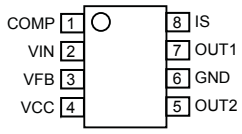
Part Number
SSC2101S

Absolute Maximum Ratings* T_A = 25°C unless otherwise specified

Characteristics	Symbol	Notes	Terminals	Rating	Unit
VCC Terminal Voltage	V_{CC}		4 – 6	−0.3 to 30	A
COMP Terminal Voltage	V_{COMP}		1 – 6	−0.3 to 5.5	A
VFB Terminal Voltage	V_{FB}		3 – 6	−0.3 to 5.5	V
VFB Terminal Current	I_{FB}		3 – 6	−1 to 1	mA
VIN Terminal Voltage	V_{IN}		2 – 6	−0.3 to 5.5	V
VIN Terminal Current	I_{IN}		2 – 6	−1 to 1	mA
IS Terminal Voltage	V_{IS}		8 – 6	−16.0 to 5.5	V
IS Terminal Current	I_{IS}		8 – 6	−1.75 to 1	mA
OUT2 Terminal Voltage	V_{OUT2}		5 – 6	−0.3 to 30	V
OUT1 Terminal Voltage	V_{OUT1}		7 – 6	−0.3 to 30	V
Operating Frame Temperature	T_{FOP}		–	−40 to 85	°C
Storage Temperature	T_{stg}		–	−40 to 125	°C
Junction Temperature	T_j		–	−40 to 125	°C

*Current polarity is defined relative to the IC: sink as positive, source as negative.

Pin-out Diagram



Terminal List Table

Name	Number	Function
1	COMP	Error Amplifier output and phase compensation terminal
2	VIN	AC mains rectified voltage monitoring input terminal
3	VFB	Feedback control terminal, input for: Constant Voltage Mode control signal, Overvoltage Protection signal, and Open Loop Detection signal
4	VCC	IC power supply input terminal
5	OUT2	Gate drive 2 output terminal
6	GND	IC ground terminal
7	OUT1	Gate drive 1 output terminal
8	IS	Peak current detection signal input terminal

ELECTRICAL CHARACTERISTICS Valid at T_A = 25°C, unless otherwise specified

Characteristics	Symbol	Test Conditions	Terminals	Min.	Typ.	Max.	Unit
Power Supply Start-up Operation							
VCC Operation Start Voltage	$V_{CC(ON)}$		4 – 6	10.8	11.6	12.4	V
VCC Operation Stop Voltage	$V_{CC(OFF)}$		4 – 6	9.8	10.6	11.4	V
VCC Undervoltage Lockout Hysteresis	$V_{CC(HYS)}$		4 – 6	0.8	1.0	1.2	V
VCC Circuit Current in Pre-operation	$I_{CC(OFF)}$		4 – 6	–	40	100	µA
VCC Circuit Current in Operation	$I_{CC(ON)}$		4 – 6	–	11.0	15.0	mA
VCC Circuit Current During OVP	$I_{CC(OVP)}$		4 – 6	–	8.0	10.0	mA
VCC Circuit Current During Standby	$I_{CC(Standby)}$		4 – 6	–	100	200	µA
Oscillator Operation							
Maximum On-Time	t_{ONMAX}		7 – 6	14	15	16	µs
OUT1 to OUT2 On-Time Matching	t_{RATIO}		5 – 6 7 – 6	−5	0	5	%
OUT1 to OUT2 Phase Difference	Δ_{PHASE}		5 – 6 7 – 6	170	180	190	deg.
Protection Operation							
VFB Output Open Loop Stop Voltage	$V_{FB(OLDL)}$		3 – 6	0.46	0.50	0.54	V
VFB Output Open Loop Start Voltage	$V_{FB(OLDH)}$		3 – 6	0.64	0.70	0.76	V
VFB Output Overvoltage Protection Voltage	$V_{FB(OVP)}$		3 – 6	3.64	3.72	3.80	V
VFB Output Soft Overvoltage Protection Voltage	$V_{FB(SOVP)}$		3 – 6	3.60	3.68	3.76	V
IS Lower Overcurrent Protection Voltage	$V_{IS(OCPL)}$		8 – 6	−0.48	−0.42	−0.36	V
IS Upper Overcurrent Protection Voltage	$V_{IS(OCPH)}$		8 – 6	−0.62	−0.55	−0.48	V
COMP Sink Current During Protection Mode	$I_{COMP(SK)}$		1 – 6	80	100	120	µA
Upper Thermal Shutdown Protection Threshold Temperature	T_{JTSDH}	Not tested, guaranteed by design	–	150	–	–	°C
Lower Thermal Shutdown Protection Threshold Temperature	T_{JTSDL}	Not tested, guaranteed by design	–	140	–	–	°C
Thermal Shutdown Protection Hysteresis	$T_{JTSDHYS}$	Not tested, guaranteed by design	–	–	10	–	°C
Error Amplifier Operation							
VFB Error Amplifier Reference Voltage	$V_{FB(REF)}$		3 – 6	3.4	3.5	3.6	V
VFB Error Amplifier Transconductance Gain	g_{mEA}		–	80	100	120	µS
COMP Error Amplifier Maximum Source Current	$I_{COMP(SO)}$		1 – 6	–36	–30	–24	µA
COMP Error Amplifier Maximum Output Voltage	$V_{COMP(MAX)}$		1 – 6	4.00	4.12	4.25	V
VFB High Speed Response Enable Voltage	$V_{FB(HSR)enable}$	Not tested, guaranteed by design	3 – 6	3.3	3.4	3.5	V

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ELECTRICAL CHARACTERISTICS (continued) Valid at T_A = 25°C, unless otherwise specified

Characteristics	Symbol	Test Conditions	Terminals	Min.	Typ.	Max.	Unit
VFB High Speed Response Active Voltage	$V_{FB(HSR)active}$		3 – 6	3.1	3.2	3.3	V
COMP High Speed Response Source Current	$I_{COMP(SOHSR)}$		1 – 6	–120	–100	–80	µA
VFB Input Bias Current	$I_{FB(bias)}$		3 – 6	–	–	1.5	µA
COMP Voltage During Output Open Loop Detection	$V_{COMP(OLD)}$		1 – 6	0.7	0.9	1.1	V
Drive Circuit							
OUTx Gate Voltage (Low)	$V_{OUT(L)}$		5 – 6 7 – 6	–	–	0.3	V
OUTx Gate Voltage (High)	$V_{OUT(H)}$		5 – 6 7 – 6	–	10.2	–	V
OUTx Rise Time	t_r		5 – 6 7 – 6	–	70	–	ns
OUTx Fall Time	t_f		5 – 6 7 – 6	–	35	–	ns
OUTx Peak Source Current	$I_{OUT(SO)}$	Not tested, guaranteed by design	5 – 6 7 – 6	–	–0.5	–	A
OUTx Peak Sink Current	$I_{OUT(SK)}$	Not tested, guaranteed by design	5 – 6 7 – 6	–	0.5	–	A

*Current polarity is defined relative to the IC: sink as positive, source as negative.

Thermal Characteristics Valid at T_A = 25°C

Characteristics	Symbol	Test Conditions	Terminals	Min.	Typ.	Max.	Unit
Package Thermal Resistance (Junction to Internal Leadframe)	$R_{\theta JF}$	Internal leadframe temperature (T_F) is measured at the root of pin 6, the GND terminal.	–	–	65	85	°C/W

Functional Description

Interleaved Discontinuous Conduction Mode (DCM)

The well-known single-phase Discontinuous Conduction Mode (DCM) technique achieves low switching noise because the drain current increase starts at zero when a power MOSFET turns on, and the rate of drain current increase is not steep, as shown by the waveforms in Figure 1. However, the usable power level of single-phase DCM is limited by the very high input / output ripple currents that are generated.

The SSC2100 series provides two-phase interleaved DCM (see Figure 2). This advanced technique incorporates two boost converters working together to cancel input ripple currents and to reduce output ripple currents. This result is based on a phase difference of 180° between the two converters.

Interleaved DCM also achieves a PFC system with lower switching noise and smaller input filter footprint in comparison to single-phase DCM. This is because reducing input / output ripple currents increases the filtering effectiveness of the EMI filter and also reduces switching noise.

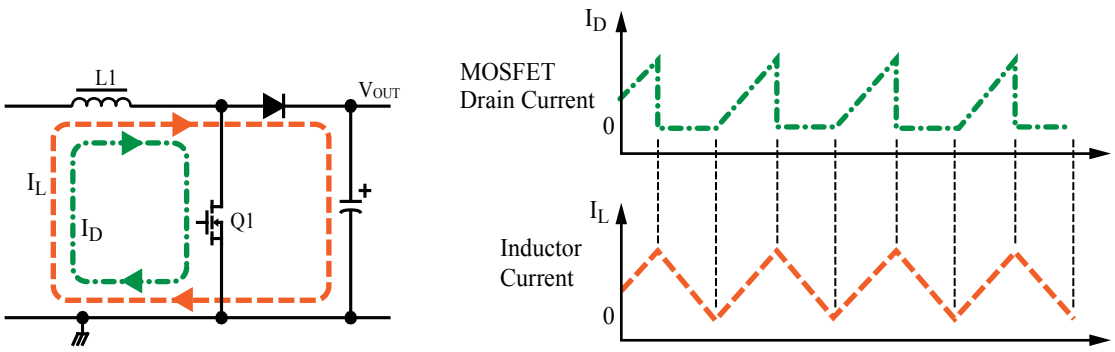


Figure 1. External circuit and current waveforms for single-phase DCM

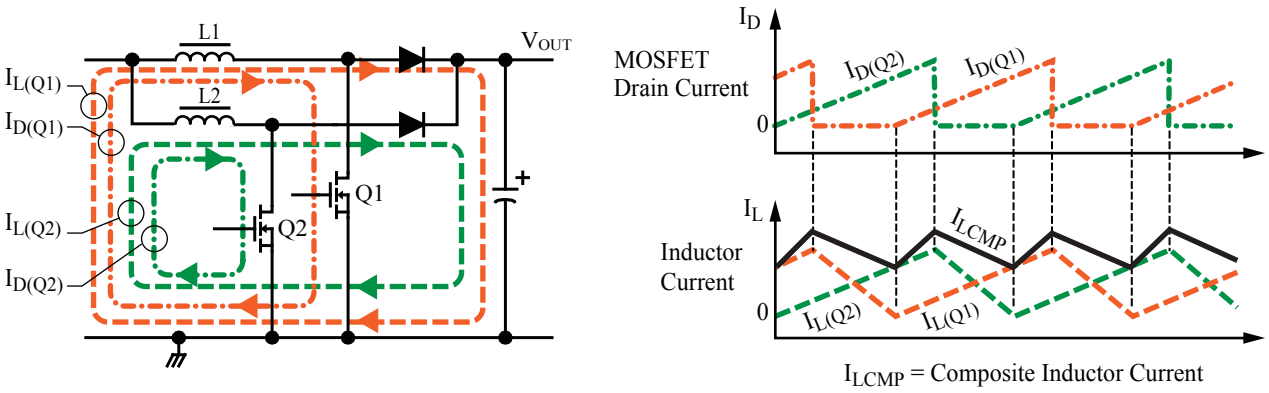


Figure 2. External circuit and current waveforms for two-phase interleaved DCM

Startup Operation

VCC is the external power supply input to the SSC2100 IC. The external circuit for the VCC terminal is shown in Figure 3.

When AC mains and VCC external voltage are applied, after the VFB terminal voltage increases to $V_{FB(OLDH)}$ = 0.7 V (typ) or more and the VCC terminal voltage increases to $V_{CC(ON)}$ = 11.6 V (typ) or more, the control circuit starts switching operation.

Note: One of the startup conditions is that the input voltage must reach 20% or more of the rated value for V_{OUT}. This value of V_{OUT} is equivalent to approximately $V_{FB(OLDH)}$ = 0.7 V (typ).

When the VCC terminal voltage subsequently decreases to $V_{CC(OFF)}$ = 10.6 V (typ) or less, the control circuit stops switching operation. It does so by enabling the UVLO (undervoltage lockout) circuit, and then reverting to the standby mode that is the state of the IC before startup.

When the VFB terminal voltage subsequently decreases to $V_{FB(OLDL)}$ = 0.5 V (typ) or less, the control circuit stops switching operation and reverts to pre-startup standby mode, even if VCC terminal voltage has increased to $V_{CC(ON)}$ or more.

Because the regulation range of the VCC internal circuit is very wide, between $V_{CC(OFF)}$ = 11.4 V (max) and the V_{CC} absolute maximum rating of 30 V (max), a wide input voltage range from the external power supply can be applied. The behaviors of ICC during startup and when switching is stopped are shown in Figure 4.

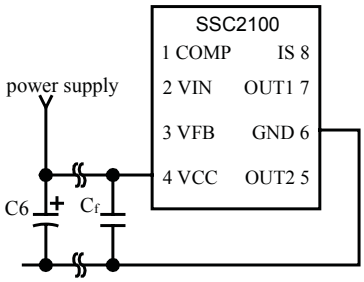


Figure 3. External circuit of VCC terminal

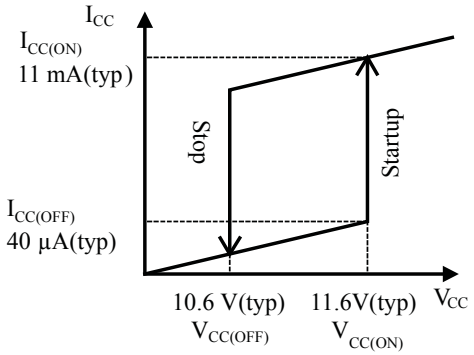


Figure 4. Relationship of V_{CC} and I_{CC} at startup and stopping

Soft Start Function

Soft start is adjusted by the external circuits on the VFB and COMP terminals, as shown in Figure 5. At startup, when the input voltage increases to approximately 20% of the rated output voltage, V_{OUT}, and the VCC terminal voltage increases to $V_{CC(ON)}$ = 11.6 V (typ), soft start operation begins.

As shown in Figure 6, during the soft start period, the COMP terminal is charged by $I_{COMP(SO)}$ = −30 µA. In this way, the output power increases gradually, reducing stress on the power devices.

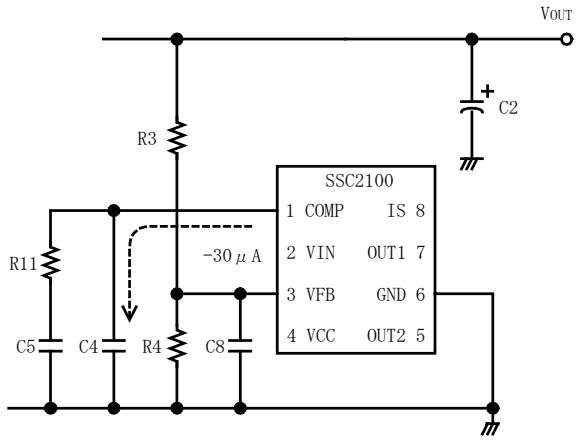


Figure 5. External circuits of VFB and COMP terminals

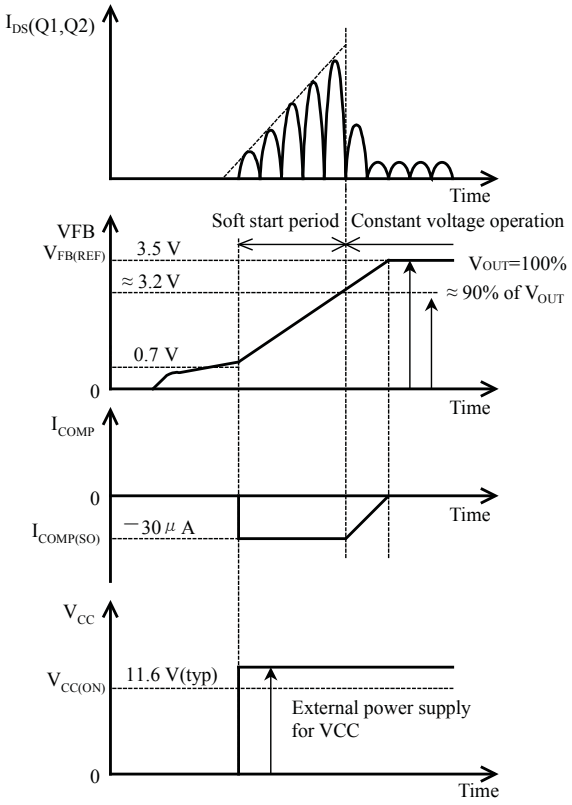


Figure 6. Soft Start operation

Voltage Control Operation

A generic PFC circuit for implementing single-phase DCM is shown in Figure 7. The circuit is composed of a boost inductor (L1), a switching device (Q1), a rectifier diode (D2), and an output capacitor (C2). A control circuit would monitor the C2 voltage and generate an error amplifier output signal to operate Q1. When the control circuit detects an off-time at the L1 Zero Current Detection (ZCD) winding, it turns on Q1 for a period of time. When Q1 is later turned off, the energy stored in L1 is transferred through D2 to C2. After all of the energy stored in L1 is transferred to C2, the control circuit would again turn on Q1, repeating the process.

The SSC2100 series two-phase interleaved DCM uses the VIN terminal to monitor the AC mains rectified input voltage, the VFB terminal to monitor output voltage, and the COMP terminal to monitor phase compensation. This IC internally generates the on-time, t_{ON}, and off-time, t_{OFF}, and it controls output voltage using the voltage-mode control method. Thus, a PFC system used with this IC has no requirement for an auxiliary winding to detect zero crossings of the inductor current. This allows simple circuits with few external components.

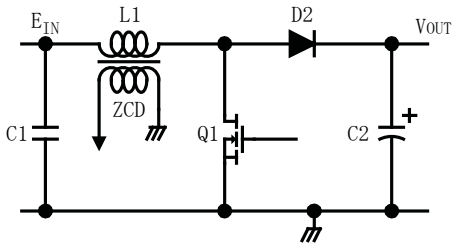


Figure 7. PFC circuit with generic single-phase DCM

In the boost PFC converter, t_{ON} is a function of load power and t_{OFF} is a function of both the input voltage, E_{IN}, and the rated output voltage, V_{OUT}. The relationship between t_{ON} and t_{OFF} is given by the following:

$$t_{OFF} > \frac{E_{IN}}{V_{OUT} - E_{IN}} \times t_{ON} \quad (1)$$

The VIN terminal voltage is monitored internally and used to calculate the internal t_{OFF}. The typical relationship between t_{ON} and the VIN terminal voltage, V_{IN}, is shown in Figure 8. The maximum t_{ON} occurs at $V_{IN} = 0$ V. The values shown assume $V_{COMP} = 4$ V, where V_{COMP} is the COMP terminal voltage.

As shown in Figure 9, the rectified input voltage is divided by R1 and R2, and input to the VIN terminal. The output voltage is divided by R3 and R4, and input to the VFB terminal. Because of the way in which the VIN terminal voltage and the VFB terminal voltage are used for internal calculations, the two dividers should be well matched. Thus, the R1, R2, and C7 values of the input portion should be equal to the R3, R4, and C8 values of the output portion.

R1 is recommended to be a high-value resistor, in the range from several hundred kΩ to several MΩ, ±1% tolerance, and of an anti-electromigration type, such as metal oxide film.

C8, if necessary to reduce high frequency noise, is recommended to have a capacitance of in the range of 0.1 to 10 nF.

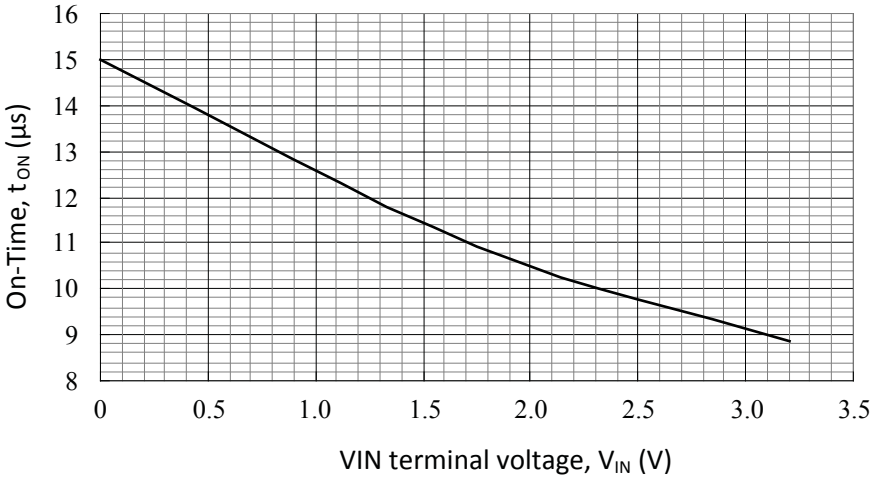


Figure 8. Typical relationship between V_{IN} and t_{ON}

High Speed Response Function (HSR)

The boost PFC converter is supplied by an AC sinusoidal waveform at the local commercial mains input voltage and frequency. However, the IC voltage control circuit, described above, characteristically responds at a relatively slow rate. As a result, the dynamic load response of the IC would be slow, and could cause the output voltage to drop too quickly.

The innovative built-in High Speed Response (HSR) function reduces variation of the output voltage under dynamic load change conditions. As shown in Figure 10, when the VFB terminal voltage increases to $V_{FB(HSR)enable}$ = 3.4 V (typ) or more, the control circuit enables the HSR operation. If the VFB terminal voltage subsequently decreases to $V_{FB(HSR)active}$ = 3.2 V (typ) or less, whether due to dynamic load change or other conditions, the control circuit activates the HSR operation.

When HSR is in active operation, the COMP terminal charges by $I_{COMP(SOHSR)}$ = −100 µA (typ) and the output power increases until the COMP terminal voltage increases to 3.2 V (typ). $V_{FB(HSR)active}$ = 3.2 V (typ) is equivalent to approximately 91.4% of the rated output voltage, V_{OUT}.

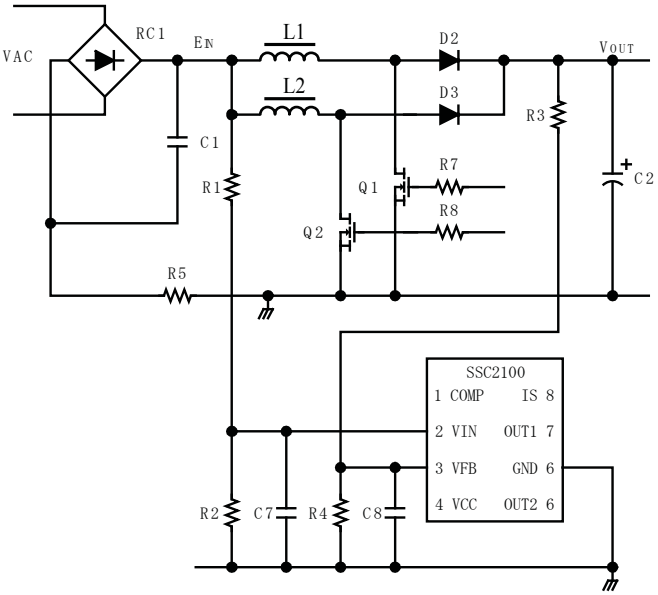


Figure 9. External circuits for VIN and VFB terminals

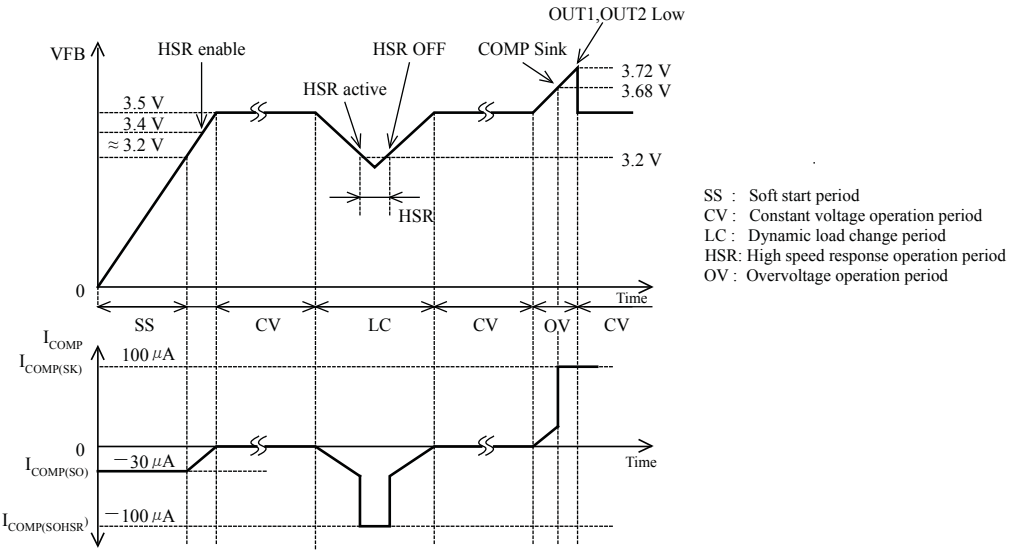


Figure 10. VFB terminal voltage waveforms

Gate Drive

The OUT1 and OUT2 terminals each directly drive an external power MOSFET. Currents and voltages are set as follows:

Peak Current		Gate Voltage	
Source	Sink	Low	High
–0.5 A (typ)	0.5 A (typ)	0.3 V (max)	10.2 V (typ)

Resistors R7, R8, R9, and R10 in Figure 11 should be selected for performance in the actual application, because these values relate to the individual board layout patterns and power MOSFET capacities. The gate resistors, R7 and R8, are recommended to be in the range of several ohms to several tens of ohms, and should be selected to reduce gate voltage ringing and EMI noise. R9 and R10 help to prevent malfunctions caused by steep dV/dt during power MOSFET turn-off. The recommended values are in the 10 to 100 kΩ range. These components should be placed close to the gate and source terminals of the corresponding power MOSFET.

Error Amplifier Phase Compensation

The phase compensation circuit is connected between the COMP and GND terminals, as shown in Figure 12. The COMP terminal is the output of the internal Error Amplifier. The Error Amplifier circuit, which implements the enhanced response functions, consists of a transconductance amplifier and switched current sources. The Error Amplifier response is set below 20 Hz to maintain power factor correction at standard commercial power frequencies of 50 or 60 Hz.

The phase compensation components, C4, C5, and R11 (see Figure 12), have typical recommended values shown below, but should be selected for performance in the application: to reduce ripple, or to enhance transient load response at the rated output voltage.

- C4: 0.047 to 0.47 µF
- C5: 0.47 to 10 µF
- R11: 10 to 100 kΩ

Thermal Shutdown Protection (TSD)

When the temperature of the IC increases to T_{JTSDH} = 150°C (min) or more, the control circuit stops switching operation. Conversely, when temperature decreases to T_{JTSDL} = 140°C or less, the control circuit restarts switching operation. The hysteresis of the detection temperature, $T_{JTSDHYS}$, is 10°C (typ).

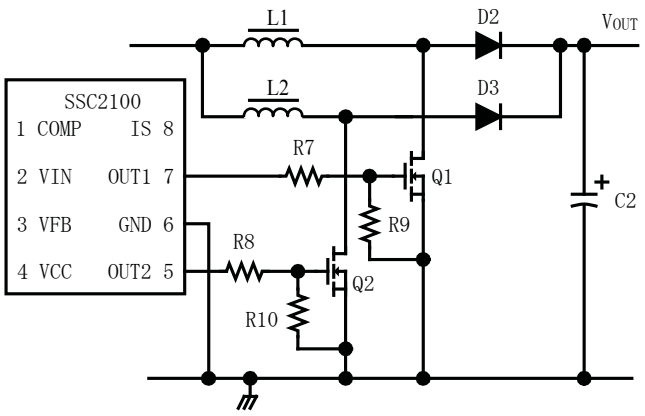


Figure 11. External circuits for OUTx terminals

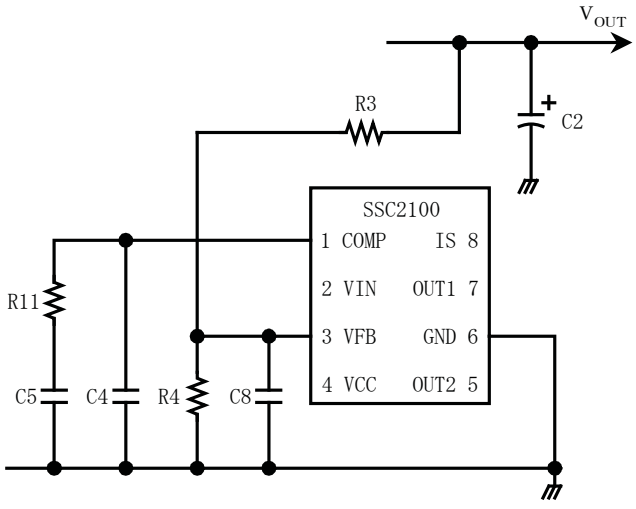


Figure 12. Phase compensation circuit (external COMP terminal circuit)

Overcurrent Protection (OCP)

The inductor current of both inductors is monitored by the detection resistor, R5, and is input to the IS terminal, as shown in Figure 13.

The overcurrent protection function has two stages, IS Lower OCP, and IS Upper OCP, described below.

IS Lower Overcurrent Protection, $V_{IS(OCPL)}$ When the inductor current is increasing and if the IS terminal voltage decreases to $V_{IS(OCPL)} = -0.42$ V (typ), the control circuit limits the output power by turning off either one or both power MOSFETs, according to the output states of both OUT1 and OUT2, as follows:

• If either one of OUT1 or OUT2 is high when the fault occurs, that output is now set low (so both outputs are off). Figure 14 is an example. Where the IS terminal voltage falls to $V_{IS(OCPL)}$ or lower while OUT1 is high (Q1 is ON) and OUT2 is low, under this condition, OUT1 is set to low.

• If both OUT1 and OUT2 are high when the fault occurs, the output that went high earlier than the other output (considering the current pulses only) is now set low (the other output remains high). Figure 15 is an example where both OUT1 and OUT2 are high (Q1 and Q2 are on), and the IS terminal detects $V_{IS(OCPL)}$ or lower. Under this condition, because OUT1 was set high before OUT2 was, OUT1 is now set low (and OUT2 remains high).

R5 (see Figure 13) should be selected for performance in the actual application, such that IS terminal voltage reaches $V_{IS(OCPL)}$ or lower under the conditions of minimum input voltage and peak load.

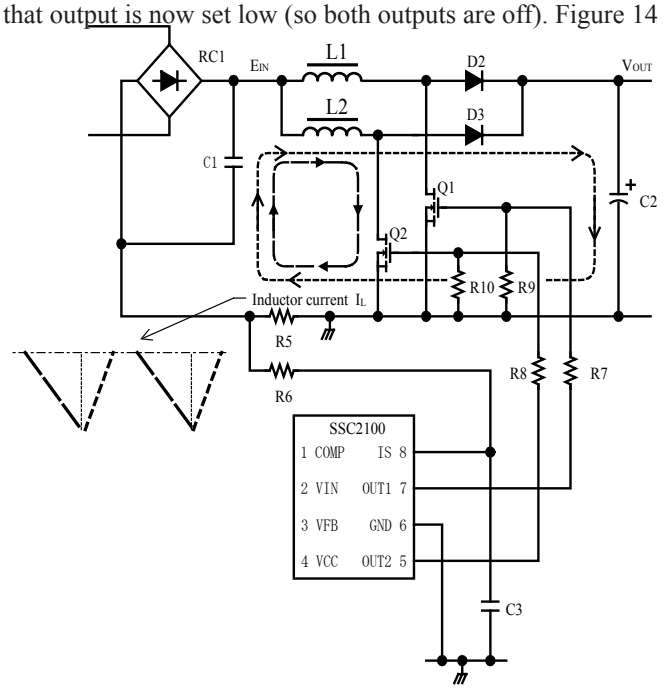


Figure 13. External circuits for IS and OUTx terminals

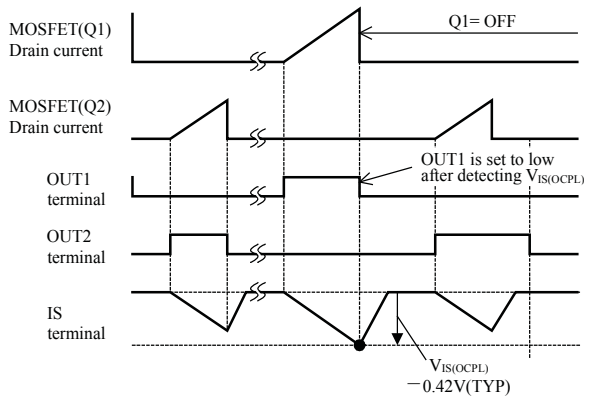


Figure 14. $V_{IS(OCPL)}$ operation waveform after OUT1 is set to high and OUT2 is set to low

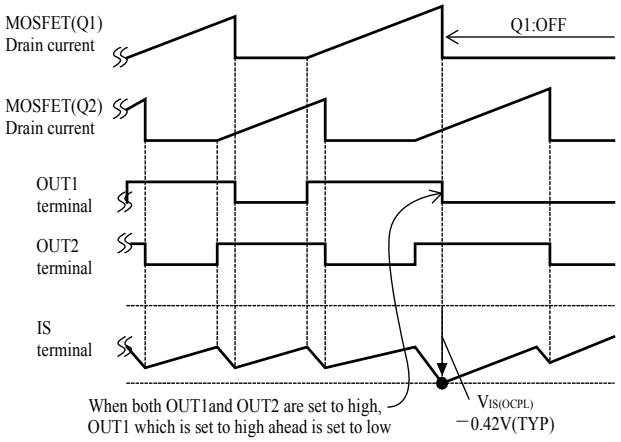


Figure 15. $V_{IS(OCPL)}$ operation waveform after both OUT1 and OUT2 are set to high

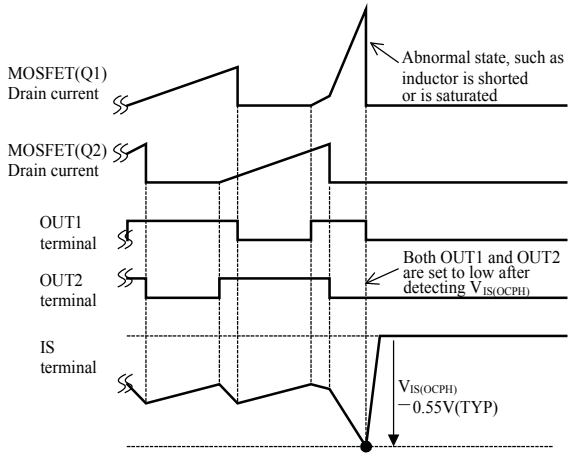


Figure 16. Phase compensation circuit (external COMP terminal circuit)

R6 is a damping resistor, which buffers IS terminal current against surge currents, such as inrush currents. It is recommended to have a value of 100 Ω.

C3, if necessary to reduce high frequency noise, is recommended to have a capacitance of in the range of 0.1 to 10 nF.

IS Upper Overcurrent Protection, $V_{IS(OCPH)}$ If the IS terminal voltage decreases to $V_{IS(OCPH)} = -0.55$ V (typ) or lower, the control circuit limits the output power on a pulse-by-pulse basis by setting both OUT1 and OUT2 low, which turns off both power MOSFETs. This is shown in Figure 16. This protection function operates under abnormal conditions such as when an inductor is shorted or is saturated.

Overvoltage Protection (OVP)

The overvoltage protection function has two stages, Soft OVP, and OVP, illustrated in Figure 17 and described below.

VFB Output Soft Overvoltage Protection, $V_{FB(SOVP)}$ When VFB terminal voltage increases to $V_{FB(SOVP)} = 3.68$ V (typ), Soft Overvoltage Protection is activated. This discharges the COMP terminal by $I_{COMP(SK)} = 100$ µA (typ) and the output voltage is decreased. $V_{FB(SOVP)} = 3.68$ V (typ) is equivalent to about 105% of the rated output voltage, V_{OUT}.

The output voltage threshold that initiates Soft Overvoltage Protection, is calculated approximately as follows:

$$V_{OUT(SOVP)} \approx \frac{V_{OUT(norm)}}{V_{FB(REF)}} \times V_{FB(SOVP)} \quad (2)$$

where $V_{OUT(norm)}$ is V_{OUT} under normal operating conditions, and $V_{FB(REF)}$ is the Error Amplifier reference voltage, 3.5V (typ).

VFB Output Overvoltage Protection, $V_{FB(OVP)}$ When the VFB terminal voltage increases to $V_{FB(OVP)} = 3.72$ V (typ), both OUT1 and OUT2 are set low on a pulse-by-pulse basis, which stops the output supply by turning off the power MOSFETS. When VFB terminal voltage decreases to $V_{FB(SOVP)}$, the control circuit stops discharging from the COMP terminal and restores switching operation.

The output voltage threshold that initiates Overvoltage Protection, is calculated approximately as follows:

$$V_{OUT(OVP)} \approx \frac{V_{OUT(norm)}}{V_{FB(REF)}} \times V_{FB(OVP)} \quad (3)$$

where $V_{OUT(norm)}$ is V_{OUT} under normal operating conditions, and $V_{FB(REF)}$ is the Error Amplifier reference voltage, 3.5V (typ).

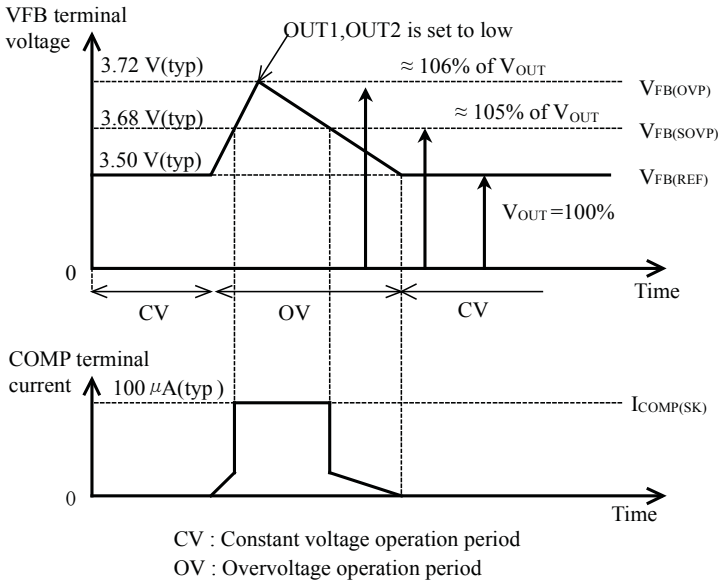
R3 is recommended to be a high-value resistor, in the range from several hundred kΩ to several MΩ, ±1% tolerance, and of an anti-electromigration type, such as metal oxide film.

C8 is recommended if necessary to reduce high frequency noise, and should have a rating of 0.1 to 10 nF.

Open Loop Detection (OLD)

In the event that the output voltage detection resistor, R3 (see Figure 18), opens and VFB terminal voltage decreases to $V_{FB(OLDL)} = 0.5$ V (typ) or less, the control circuit stops the switching operation and enters standby mode. $V_{FB(OLDL)} = 0.5$ V (typ) is equivalent to about 14.3% of the rated output voltage, V_{OUT}.

When the VFB terminal voltage subsequently increases to $V_{FB(OLDH)} = 0.7$ V (typ) or more, the control circuit restores switching operation. $V_{FB(OLDH)} = 0.7$ V (typ) is equivalent to about 20% of the rated output voltage, V_{OUT}.



CV : Constant voltage operation period
OV : Overvoltage operation period

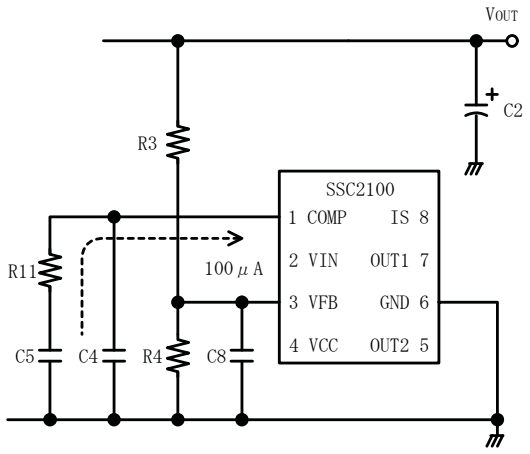


Figure 17. Overvoltage operation waveform and external circuit

Open Terminal Protection (OTP)

The VFB, IS, and VIN terminals each have dedicated internal Open Terminal Protection functions.

VFB Open Protection The VFB terminal is internally connected with a pull-up current source. In the event that the VFB terminal is open, VFB terminal voltage is pulled-up to the internal supply voltage, the IC overvoltage protection is activated, and both OUT1 and OUT2 are set low, decreasing the output voltage.

IS Open Protection The IS terminal is internally connected with a pull-up current source. In the event that the IS terminal is open, the IS terminal voltage is pulled-up to the internal supply voltage, the IC overcurrent protection is activated, and both OUT1 and OUT2 are set low, decreasing the output voltage.

VIN Open Protection The VIN terminal is internally connected with a pull-up current source. In the event that the VIN terminal is open, the VIN terminal voltage is pulled-up to the internal supply voltage, and the control circuit limits IC operation or stops it.

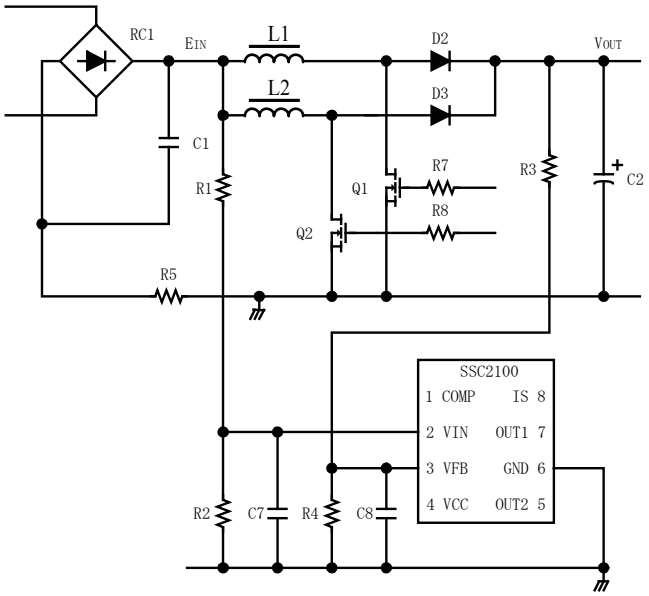


Figure 18. External VFB terminal circuit

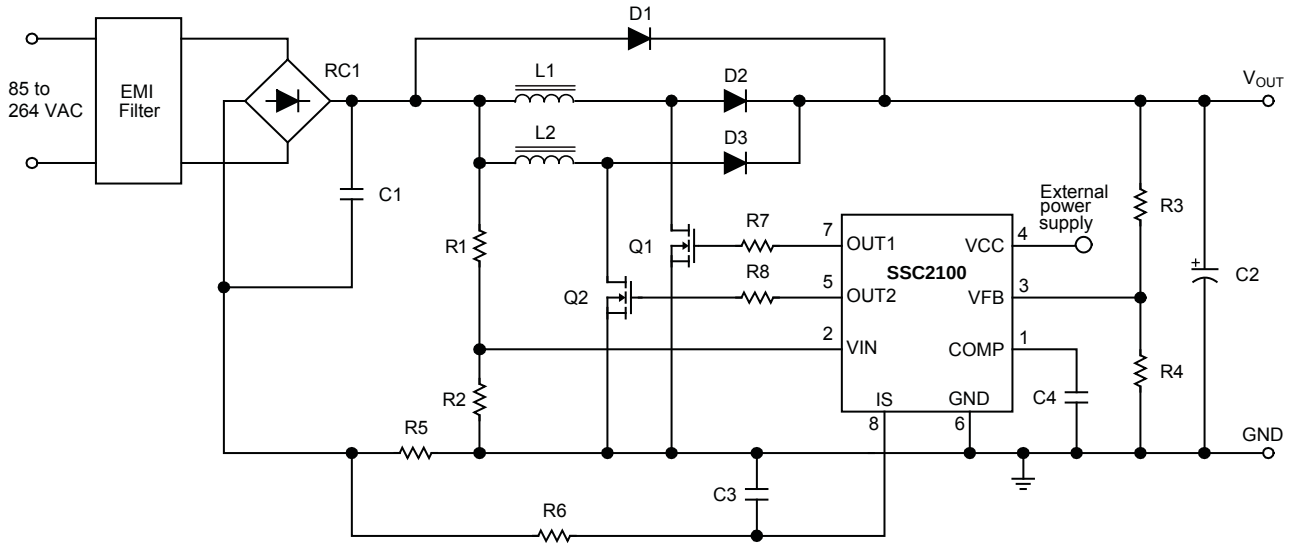
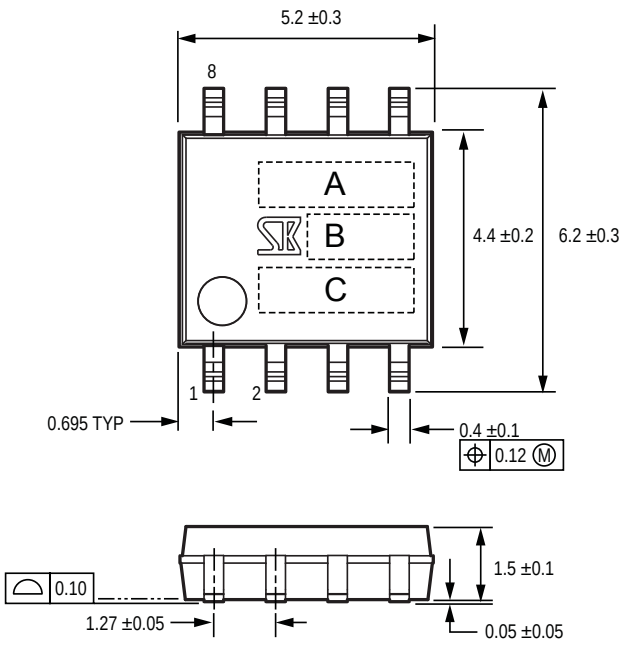
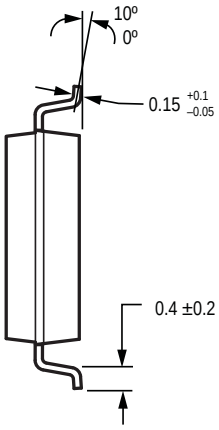


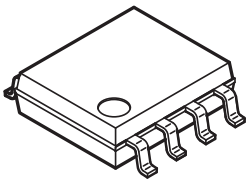
Figure 18. Typical application diagram

Package Outline Drawing





Dimensions in mm



Branding:

A. Type number (abbreviation): SC21xx

B. Lot number

1st letter: Last digit of year

2nd letter: Month

1 to 9 for January to September
O for October
N for November
D for December

3rd letter: Week

1 for dates 1 through 10
2 for dates 11 through 20
3 for dates 21 through 31

C. Sanken tracking number

Handling and Use Cautions and Warnings

Because reliability can be affected adversely by improper storage environments and handling methods during characteristic tests, please observe the following cautions.

Cautions for Storage

- Ensure that storage conditions comply with standard temperature (5°C to 35°C) and standard relative humidity (around 40% to 75%) and avoid storage locations that experience extreme changes in temperature or humidity.
- Avoid locations where dust or harmful gases are present, and avoid direct sunlight.
- Reinspect for rust on leads and solderability of devices which have been stored for a long time.

Cautions for Characteristic Tests and Handling

- When characteristic tests are carried out during inspection testing and other standard test periods, protect the devices from power surges from the test equipment, and from shorts between the devices and the heatsink.

Recommended Operating Temperature

- Internal leadframe temperature in operation: T_F = 115°C (max). Note: Measure at pin 5, close the case molding.

Soldering

- When soldering the devices, please be sure to minimize the working time, and stay within the following conditions:
  - 260 (+0 / –10) °C for 10 s (during reflow)
  - 350 ±5 °C for 3 s (using a soldering iron)

Considerations to protect the Products from Electrostatic Discharge

- When handling the devices, the operator must be grounded. Grounded wrist straps should be worn, and have at least 1 MΩ of resistance from operators to ground to prevent shock hazard.
- Workbenches where the devices are handled should be grounded and be provided with conductive table and floor mats.
- When using measuring equipment such as a curve tracer, the equipment also should be grounded.
- When soldering the devices, the head of the soldering iron or the solder bath must be grounded in order to prevent leakage voltage generated by them from being applied to the devices.
- The devices should always be stored and transported in Sanken shipping containers or conductive containers, or be wrapped up in aluminum foil.

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