DALLAS SEMICONDUCTOR

DS1501/DS1511
Y2KC Watchdog Real Time Clock

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FEATURES

- BCD coded century, year, month, date, day, hours, minutes, and seconds with automatic leap year compensation valid up to the year 2100
- Programmable watchdog timer and RTC alarm
- Century register; Y2K-compliant RTC
- +3.3 or +5-volt operation
- Precision power-on reset
- Power control circuitry supports system power-on from date/day/time alarm or key closure/modem detect signal
- 256 bytes user NV SRAM
- Burst mode for reading/writing successive addresses in NV SRAM
- Auxiliary battery input
- Accuracy of DS1511 is better than ± 1 min./month @ 25°C
- Day of week/date alarm register
- Crystal select bit allows RTC to operate with 6 pF or 12.5 pF crystal
- Battery voltage level indicator flags
- Available as chip (DS1501) or standalone module with embedded battery and crystal (DS1511)
- Optional industrial temperature range -40°C to +85°C (DS1501 only)

ORDERING INFORMATION

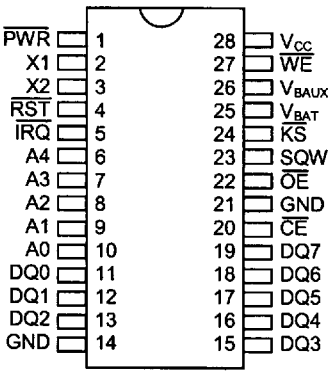
DS1501XXX

blank	commercial temp range
N	industrial temp range
Blank	28-pin DIP
E	28-pin TSOP
S	28-pin SOIC
Y	5 Volt operation
W	3.3 Volt operation

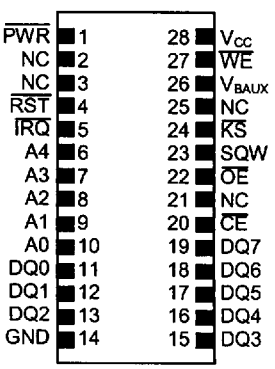
DS1511X Dip Module

Y	5 Volt operation
W	3.3 Volt operation

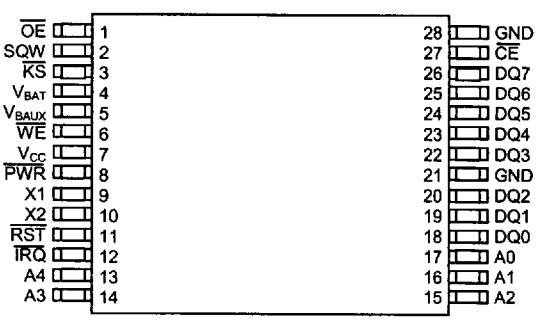
PIN ASSIGNMENT



28-Pin DIP, 28-Pin SOIC



28-Pin ENCAPSULATED PACKAGE
(720-mil FLUSH)



28-Pin TSOP

111699

DESCRIPTION

The DS1501/DS1511 is a full function, year 2000-compliant (Y2KC), real-time clock/calendar (RTC) with a RTC alarm, watchdog timer, power-on reset, battery monitors, and 256 bytes nonvolatile static RAM in a monolithic chip. User access to all registers within the DS1501 is accomplished with a bytewide interface as shown in Figure 1. The RTC registers contain century, year, month, date, day, hours, minutes, and seconds data in 24-hour BCD format. Corrections for day of month and leap year are made automatically.

SIGNAL DESCRIPTION

V_{CC} - Supply Voltage
A0-A4 - Address Inputs
DQ0-DQ8 - Data I/O
$\overline{CE}$ - Chip Enable Input
$\overline{OE}$ - Output Enable Input
$\overline{WE}$ - Write Enable Input
$\overline{IRQ}$ - Interrupt Output (Open Drain)
$\overline{PWR}$ - Power-On Output (Open Drain)
$\overline{RST}$ - Reset Output (Open Drain)
$\overline{KS}$ - Kickstart Input
SQW - Square Wave Output
V_{BAT} - Backup Battery Supply
V_{BAUX} - Auxiliary Battery Supply
X1 - Oscillator Input
X2 - Oscillator Output
GND - Ground
NC - No Connection

The RTC registers are double-buffered into an internal and external set. The user has direct access to the external set. Clock/calendar updates to the external set of registers can be disabled and enabled to allow the user to access static data. Assuming the internal oscillator is turned on, the internal set of registers are continuously updated; this occurs regardless of external registers settings to guarantee that accurate RTC information is always maintained.

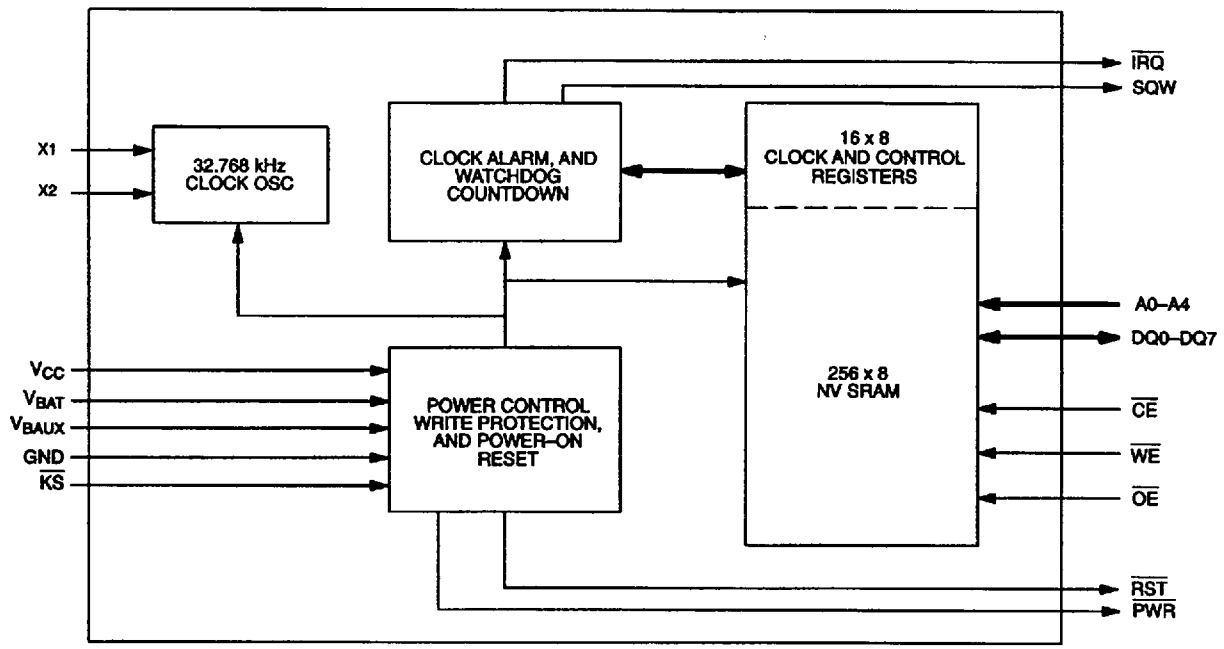
The DS1501/DS1511 contains its own power-fail circuitry which automatically deselects the device when the V_{CC} supply enters an out-of-tolerance condition. This feature provides a high degree of data security during unpredictable system operation brought on by low V_{CC} levels.

The DS1501/DS1511 has interrupt ($\overline{IRQ}$), wakeup ($\overline{PWR}$), and reset ($\overline{RST}$) outputs which can be used to control CPU activity. The $\overline{IRQ}$ interrupt output can be used to generate an external interrupt under several conditions. A Wakeup interrupt will be generated when the RTC register values match user programmed alarm values and Time of day/date Power Enable bit (TPE) (Bit 4), in register 0Fh is set to a logic 1. A Kickstart interrupt will be generated when a high to low transition occurs on the Kickstart ($\overline{KS}$) pin while the Kickstart Interrupt Enable bit (KIE) (Bit 2), in register 0Fh is set to a logic 1. The interrupt is always available while the device is powered from the system supply. The $\overline{PWR}$ output can be programmed to occur when in the battery backed state to serve as a system wake-up. The $\overline{PWR}$ pin is under software control, so that when a task is complete, the system power can then be shut down. Either the $\overline{IRQ}$ or $\overline{RST}$ outputs can also be used as a CPU watchdog timer, CPU activity is monitored and an

interrupt or reset output will be activated if the correct activity is not detected within programmed limits. The DS1501/DS1511 power-on reset can be used to detect a system power down or failure and hold the CPU in a safe reset state until normal power returns and stabilizes; the $\overline{RST}$ output is used for this function.

The DS1501/DS1511 also incorporates a 32.768kHz output for sustaining power management activities.

DS1501/DS1511 BLOCK DIAGRAM Figure 1



DS1501/DS1511 OPERATING MODES Table 1

V_{CC}	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ0-DQ7	A0-A4	MODE	POWER
IN TOLERANCE	V_{IH}	X	X	HIGH-Z	X	DESELECT	STANDBY
	V_{IL}	X	V_{IL}	D_{IN}	A_{IN}	WRITE	ACTIVE
	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}	READ	ACTIVE
	V_{IL}	V_{IH}	V_{IH}	HIGH-Z	A_{IN}	READ	ACTIVE
$V_{BAT} < V_{CC} <$ TOLERANCE	X	X	X	HIGH-Z	X	DESELECT	CMOS STANDBY
$V_{CC} < V_{BAT}$	X	X	X	HIGH-Z	X	DATA RETENTION	BATTERY CURRENT

DATA READ MODE

The DS1501/DS1511 is in the read mode whenever $\overline{CE}$ (chip enable) is low and $\overline{WE}$ (write enable) is high. The device architecture allows ripple-through access to any valid address location. Valid data will be available at the DQ pins within t_{AA} (address access) after the last address input is stable, providing that $\overline{CE}$ and $\overline{OE}$ access times are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, valid data will be available at the latter of chip enable access (t_{CEA}) or at output enable access time (t_{OEA}). The state of the data input/output pins (DQ) is controlled by $\overline{CE}$ and $\overline{OE}$. If the outputs are activated before t_{AA}, the data lines are driven to an intermediate state until t_{AA}. If the address inputs are changed while $\overline{CE}$ and $\overline{OE}$ remain valid, output data will remain valid for output data hold time (t_{OH}) but will then go indeterminate until the next address access. (See Table 1.)

DATA WRITE MODE

The DS1501/DS1511 is in the write mode whenever $\overline{WE}$ and $\overline{CE}$ are in their active state. The start of a write is referenced to the latter occurring transition of $\overline{WE}$ or $\overline{CE}$. The addresses must be held valid throughout the cycle. $\overline{CE}$ and $\overline{WE}$ must return inactive for a minimum of t_{WR} prior to the initiation of a subsequent read or write cycle. Data in must be valid t_{DS} (data setup) prior to the end of the write and remain valid for t_{DH} (data hold) afterward. In a typical application, the $\overline{OE}$ signal will be high during a write cycle. However, $\overline{OE}$ can be active provided that care is taken with the data bus to avoid bus contention. If $\overline{OE}$ is low prior to a high to low transition on $\overline{WE}$, the data bus can become active with read data defined by the address inputs. A low transition on $\overline{WE}$ will then disable the outputs t_{WEZ} ($\overline{WE}$ data off time) after $\overline{WE}$ goes active. (See Table 1.)

DATA RETENTION MODE

The 5-volt device is fully accessible and data can be written and read only when V_{CC} is greater than V_{PF}. However, when V_{CC} falls below the power-fail point V_{PF} (point at which write protection occurs) the internal clock registers and SRAM are blocked from any access. While in the data retention mode, all inputs are don't cares and outputs go to a high-Z state. When V_{CC} falls below the greater of V_{BAT} and V_{BAUX}, device power is switched from the V_{CC} pin to either the V_{BAT} or V_{BAUX} pin. RTC operation and SRAM data are maintained from the battery until V_{CC} is returned to nominal levels.

The 3.3-volt device is fully accessible and data can be written and read only when V_{CC} is greater than V_{PF}. However, when V_{CC} falls below V_{PF}, access to the device is inhibited. If V_{PF} is less than V_{BAT} and V_{BAUX}, the device power is switched from V_{CC} to the greater of V_{BAT} and V_{BAUX} when V_{CC} drops below V_{PF}. If V_{PF} is greater than V_{BAT} and V_{BAUX}, the device power is switched from V_{CC} to the larger of V_{BAT} and V_{BAUX} when V_{CC} drops below the larger of V_{BAT} and V_{BAUX}. RTC operation and SRAM data are maintained from the battery until V_{CC} is returned to nominal levels. (See Table 1.)

All control, data, and address signals must be powered down when V_{CC} is absent.

AUXILIARY BATTERY

The V_{BAUX} input is provided to supply power from an auxiliary battery for the DS1501/DS1511 kickstart and SQW output features in the absence of V_{CC}. This power source must be available in order to use these auxiliary features when V_{CC} is not applied to the device.

This auxiliary battery may be used as the primary backup power source for maintaining the clock/calendar and extended user RAM. This occurs if the V_{BAT} pin is at a lower voltage than V_{BAUX}. If the DS1501/DS1511 is to be backed-up using a single battery with the auxiliary features enabled, then V_{BAUX} should be used and V_{BAT} should be grounded. If V_{BAUX} is not to be used, it should be grounded.

POWER-ON RESET

A temperature compensated comparator circuit monitors the level of V_{CC}. When V_{CC} falls to the write protection voltage, the $\overline{RST}$ signal (open drain) is pulled low. When V_{CC} returns to nominal levels, the $\overline{RST}$ signal continues to be pulled low for a period of 40 ms to 200 ms. The power-on reset function is independent of the RST oscillator and thus is operational whether or not the oscillator is enabled.

DS1501/DS1511 REGISTER MAP Table 2

	DATA									BCD
Address	B7	B6	B5	B4	B3	B2	B1	B0	FUNCTION	RANGE
00H	0	10 SECONDS			SECONDS				SECONDS	00-59
01H	0	10 MINUTES			MINUTES				MINUTES	00-59
02H	0	0	10 HOURS		HOUR				HOURS	00-23
03H	0	0	0	0	0	DAY			DAY	1-7
04H	0	0	10 DATE		DATE				DATE	00-31
05H	$\overline{\text{EOSC}}$	$\overline{\text{E32K}}$	$\overline{\text{BB32}}$	10 MO	MONTH				MONTH	01-12
06H	10 YEAR				YEAR				YEAR	00-99
07H	0	0	10 CENTURY		CENTURY				CENTURY	00-39
08H	AM1	10 SECONDS			SECONDS				ALARM SECONDS	00-59
09H	AM2	10 MINUTES			MINUTES				ALARM MINUTES	00-59
0AH	AM3	0	10 HOURS		HOUR				ALARM HOURS	00-23
0BH	AM4	DY/DT	10 DAY/DATE		DAY/DATE				ALARM DAY/ DATE	1-7/01-31
0CH	0.1 SECOND				0.01 SECOND				WATCHDOG	00-99
0DH	10 SECOND				SECOND				WATCHDOG	00-99
0EH	VRT1	VRT2	PRS	PAB	TDF	KSF	WDF	IRQF	CONTROL A	
0FH	TE	CS	BME	TPE	TIE	KIE	WDE	WDS	CONTROL B	
10H	EXTENDED RAM ADDRESS								RAM ADDR LSB	00-FF
11H	RESERVED									
12H	RESERVED									
13H	EXTENDED RAM DATA								RAM DATA	00-FF
14H	RESERVED									
15H	RESERVED									
16H	RESERVED									
17H	RESERVED									
18H	RESERVED									
19H	RESERVED									
1AH	RESERVED									
1BH	RESERVED									
1CH	RESERVED									
1DH	RESERVED									
1EH	RESERVED									
1FH	RESERVED									

TABLE 2 LEGEND (DS1501/DS1511 REGISTER MAP):

0="0" and is Read Only
PRS=PAB Reset Select Bit
BME=Burst Mode Enable Bit
$\overline{\text{EOSC}}$ =Oscillator Start/Stop Bit
PAB=Power Active Bar Control Bit
TPE=Time of Day/Date Alarm Power Enable Bit
$\overline{\text{E32K}}$ =Enable 32.768 kHz Output Bit
TDF=Time of Day/Date Alarm Flag
TIE=Time of Day/Date Alarm Interrupt Enable Bit
BB32=Battery Backup 32 kHz Enable Bit
KSF=Kickstart Flag
AM1-AM4=Alarm Mask Bits
WDF=Watchdog Flag
KIE=Kickstart Interrupt Enable Bit
DY/DT=Day/Date Bit
IRQF=Interrupt Request Flag
WDE=Watchdog Enable Bit
VRT1=Valid RAM and Time Bit
TE=Transfer Enable Bit
WDS=Watchdog Steering Bit
VRT2=Auxiliary Battery Low Bit
CS=Crystal Select Bit

NOTE: Unless otherwise specified, the state of the control/RTC/SRAM bits in the DS1501/DS1511 is not defined upon initial power application; the DS1501/DS1511 should be properly configured/defined during initial configuration.

CLOCK OSCILLATOR CONTROL

The Clock oscillator may be stopped at any time. To increase the shelf life of a backup lithium battery source, the oscillator can be turned off to minimize current drain from the battery. The $\overline{EOSC}$ bit is the MSB of the month register (B7 of 05h). Setting it to a 1 stops the oscillator, setting to a 0 starts the oscillator.

READING THE CLOCK

When reading the RTC data, it is recommended to halt updates to the external set of double-buffered RTC registers. This puts the external registers into a static state allowing data to be read without register values changing during the read process. Normal updates to the internal registers continue while in this state. External updates are halted when a 0 is written into the read (TE) bit, B7, of Control register B (0Fh). As long as a 0 remains in the Control register B (TE) bit, updating is halted. After a halt is issued, the registers reflect the RTC count (day, date, and time) that was current at the moment the halt command was issued. Normal updates to the external set of registers will resume within 1 second after the (TE) bit is set to a 1.

SETTING THE CLOCK

It is also recommended to halt updates to the external set of double-buffered RTC registers when writing to the clock. The (TE) bit should be used as described above before loading the RTC registers with the desired RTC count (day, date, and time) in 24-hour BCD format. Setting the (TE) bit to a 1 then transfers the values written to the internal RTC registers and allows normal operation to resume.

CLOCK ACCURACY

A standard 32.768 kHz quartz crystal should be directly connected to the DS1501 X1 and X2 oscillator pins. The crystal selected for use should have a specified load capacitance (CL) of either 6 pF or 12.5 pF depending on crystal capacitance setting selected with the Crystal Select (CS) bit. For more information on crystal selection and crystal layout considerations, please consult Application Note 58, "Crystal Considerations with Dallas Real Time Clocks." The DS1501 can also be driven by an external 32.768 kHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated. Accuracy of DS1511 is better than ±1 min./month @ 25°C.

USING THE CLOCK ALARM

The alarm settings and control for the DS1501/DS1511 reside within registers 08h - 0Bh. Bit 7 of registers 08h to 0Bh contains an alarm mask bit: AM1 through AM4. The TIE (Time of Day/Date alarm Interrupt Enable bit, B3 of 0Fh) and Alarm Mask bits AM1-AM4 must be set as described below for the $\overline{IRQ}$ output to be activated for a matched alarm condition.

The alarm can be programmed to activate on a specific day of the month, day of the week, or repeat every day, hour, minute, or second. It can also be programmed to go off while the DS1501/DS1511 is in the battery backed state of operation to serve as a system wake-up. Alarm Mask bits AM1-AM4 control the alarm mode. Table 3 shows the possible settings. Configurations not listed in the table default to the once per second mode to notify the user of an incorrect alarm setting. When the RTC register values match alarm register settings, the Time of Day/Date Alarm Flag 'TDF' bit is set to logic 1. If TIE is also set to logic 1, the alarm condition activates the $\overline{IRQ}$.

NOTE: Please refer to Table 2 as required for the following functional descriptions.

ALARM MASK BITS Table 3

DY/DT	AM4	AM3	AM2	AM1	ALARM RATE
X	1	1	1	1	ONCE PER SECOND
X	1	1	1	0	WHEN SECONDS MATCH
X	1	1	0	0	WHEN MINUTES AND SECONDS MATCH
X	1	0	0	0	WHEN HOURS, MINUTES, AND SECONDS MATCH
0	0	0	0	0	WHEN DATE, HOURS, MINUTES, AND SECONDS MATCH
1	0	0	0	0	WHEN DAY, HOURS, MINUTES, AND SECONDS MATCH

USING THE WATCHDOG TIMER

The watchdog timer can be used to detect an out-of-control processor. The user programs the watchdog timer by setting the desired amount of time-out into the two BCD Watchdog Registers (Address 0Ch and 0Dh). (For example: writing 60h in the watchdog register 0Ch and 00h to watchdog register 0Dh will set the watchdog time-out to 60 milliseconds.) If the processor does not access the timer, with a read or write, within the specified period, the Watchdog Flag 'WDF' will be set. The Interrupt Request Flag 'IRQF' will be set and either $\overline{IRQ}$ or $\overline{RST}$ will go active at this time if the Watchdog Enable bit 'WDE' is set to logic 1 (enabled). The Watchdog Steering Bit 'WDS' determines which of the outputs, $\overline{IRQ}$ or $\overline{RST}$, will go active when 'WDE' is enabled and the watchdog times out. The watchdog will be reloaded and restarted whenever the watchdog times out.

Bit 0 of register 0Fh is the Watchdog Steering Bit 'WDS'. When set to a 0 and 'WDE' is set to logic 1, the watchdog will activate the $\overline{IRQ}$ output and the 'IRQF' flag will be set when the watchdog times out. The WDF bit will be set to a logic 1 regardless of the state of 'WDE' to serve as an indication to the processor that a watchdog time-out has occurred.

When WDS is set to a 1 and 'WDE' is set to logic 1, the watchdog will output a negative pulse on the $\overline{RST}$ output for a duration of 40 ms to 200 ms and the 'IRQF' flag will be set when the watchdog times out. The WDE bit will reset to a logic 0 immediately after $\overline{RST}$ goes active. The WDF bit will be set to a logic 1 regardless of the state of 'WDE' to serve as an indication to the processor that a watchdog time out has occurred.

The watchdog timer is reloaded when the processor performs a read or write of the Watchdog register. The time-out period then starts over. The watchdog timer is disabled by writing a value of 00h to both watchdog registers. The watchdog function is automatically disabled upon power-up.

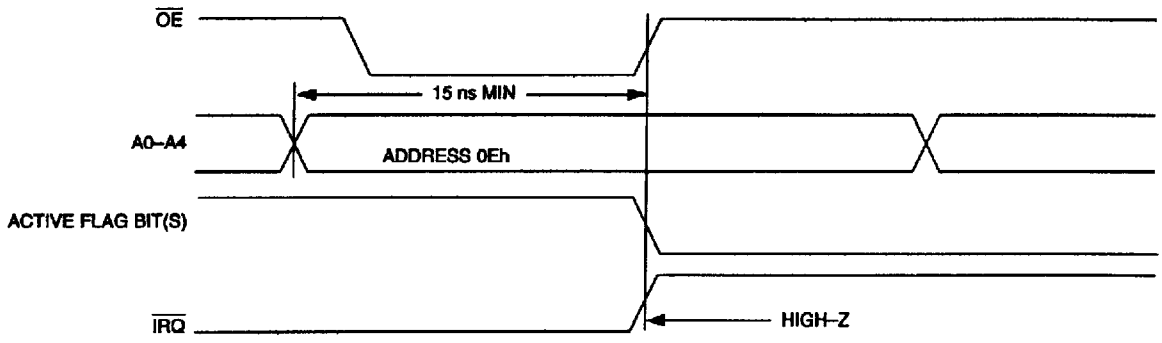
The following summarizes the configurations in which the watchdog can be used.

1. 'WDE'=0 and 'WDS'=0: 'WDF' will be set.
2. 'WDE'=0 and 'WDS'=1: 'WDF' will be set.
3. 'WDE'=1 and 'WDS'=0: 'WDF' and 'IRQF' will be set, and the $\overline{IRQ}$ pin will be pulled low.
4. 'WDE'=1 and 'WDS'=1: 'WDF' will be set, the $\overline{RST}$ pin will be pulled low for a duration of 40 ms to 200 ms, and 'WDE' will be reset to '0'.

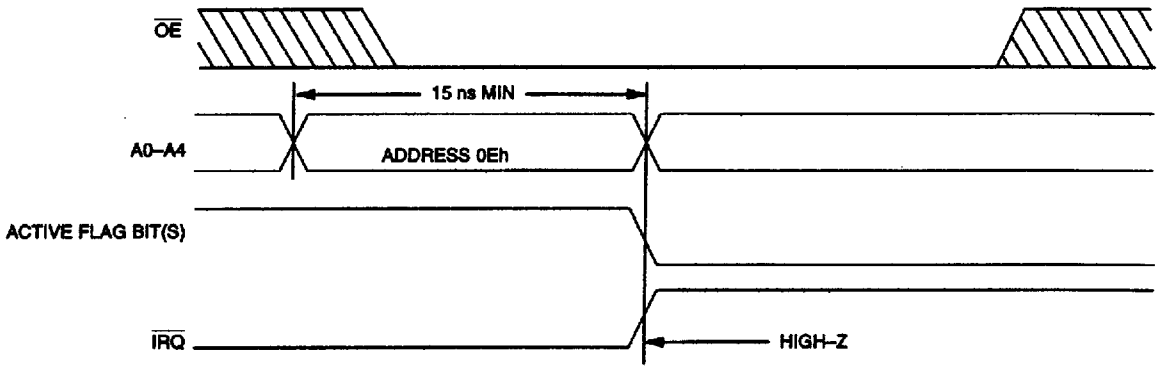
CLEARING IRQ AND FLAGS

The alarm flag(s), watchdog flag, interrupt request flag, and the $\overline{IRQ}$ output are cleared by reading the Flags register (0Eh) or writing "0" to the corresponding Flag as shown in Figures 2a and 2b.

IRQ AND FLAG WAVEFORMS Figure 2a



IRQ AND FLAG WAVEFORMS Figure 2b



WAKE-UP/KICKSTART

The DS1501/DS1511 incorporates a wake-up feature which can power-on at a predetermined date through activation of the $\overline{PWR}$ output pin. In addition, the kickstart feature can allow the system to be powered up in response to a low going transition on the $\overline{KS}$ pin, without operating voltage applied to the V_{CC} pin. As a result, system power may be applied upon such events as key closure, or modem ring-detect signal. In order to use either the wake-up or the kickstart features, the DS1501/DS1511 must have a battery connected to the V_{BAUX} pin and the oscillator must be running.

The wake-up feature is controlled through the Time of Day/Date Alarm Power Enable bit 'TPE' in Control B register (B4 of 0Fh). Setting TPE to 1 enables the wake-up feature, clearing TPE to 0 disables it. Similarly, the kickstart feature is controlled through the Kickstart Interrupt Enable bit 'KIE' in Control B register (B2 of 0Fh).

A wake-up sequence will occur as follows: When wake-up is enabled via TPE = 1 while the system is powered down (no V_{CC} voltage), the clock/calendar will monitor the current day or date for a match condition with Day/Date Alarm register (0Bh). In conjunction with the Day/Date Alarm register, the hours, minutes, and seconds alarm bytes in the clock calendar register map (02h, 01h, and 00h) are also monitored. As a result, a wake-up will occur at the day or date and time specified by the day/date, hours, minutes, and seconds alarm register values. This additional alarm will occur regardless of the programming of the TIE bit (Time of Day/Date Alarm Interrupt Enable bit) (B3 of 0Fh). When the match

condition occurs, the $\overline{PWR}$ pin will automatically be driven low. This output can be used to turn on the main system power supply which provides V_{CC} voltage to the DS1501/DS1511 as well as the other major components in the system. Also, at this time, the Time of Day/Date Alarm Flag will be set, indicating that a wake-up condition has occurred.

While the system is powered down and V_{BAUX} is present, the $\overline{KS}$ input pin will be monitored for a low-going transition of minimum pulse width t_{KSPW}. When such a transition is detected, the $\overline{PWR}$ line will be pulled low, as it is for a wake-up condition. Also at this time, the Kickstart Flag (KSF, register 0Eh) will be set, indicating that a kickstart condition has occurred. The $\overline{KS}$ input pin is always enabled and must not be allowed to float.

The timing associated with both the wake-up and kickstarting sequences is illustrated in the Wake-Up/Kickstart Timing Diagram, Figure 9, in the Electrical Specifications section of this datasheet. The timing associated with these functions is divided into 5 intervals, labeled 1-5 on the diagram.

The occurrence of either a kickstart or wake-up condition will cause the $\overline{PWR}$ pin to be driven low, as described above. During interval 1, if the supply voltage on the DS1501/DS1511 V_{CC} pin rises above the battery switch voltage (V_{SW}) before the power-on timeout period (t_{POTO}) expires, then $\overline{PWR}$ will remain at the active low level. If V_{CC} does not rise above the battery switch voltage (V_{SW}) in time, then the $\overline{PWR}$ output pin will be turned off and will return to its high-impedance level. In this event, the $\overline{IRQ}$ pin will also remain tri-stated. The interrupt flag bit (either TDF or KSF) associated with the attempted power-on sequence will remain set until cleared by software during a subsequent system power-on.

If V_{CC} is applied within the time-out period, then the system power-on sequence will continue as shown in intervals 2-5 in the timing diagram. During interval 2, $\overline{PWR}$ will remain active and $\overline{IRQ}$ will be driven to its active low level, indicating that either TDF or KSF was set in initiating the power-on. In the diagram $\overline{KS}$ is assumed to be pulled up to the V_{BAUX} supply (logic high). Also at this time, the PAB bit will be automatically cleared to 0 in response to a successful power-on. The $\overline{PWR}$ line will remain active as long as the PAB remains cleared to 0.

At the beginning of interval 3, the system processor has begun code execution and clears the interrupt condition of TDF and/or KSF by writing zeroes to both of these control bits. As long as no other interrupt within the DS1501 is pending, the $\overline{IRQ}$ line will be taken inactive once these bits are reset, and execution of the application software may proceed. During this time, both the wakeup and kickstart functions may be used to generate status and interrupts. TDF will be set in response to a day/date, hours, minutes, and seconds match condition. KSF will be set in response to a low going transition on $\overline{KS}$. If the associated interrupt enable bit is set (TDE and/or KIE) then the $\overline{IRQ}$ line will be driven low in response to enabled event. In addition, the other possible interrupt sources within the DS1501/DS1511 may cause $\overline{IRQ}$ to be driven low. While system power is applied, the on chip logic will always attempt to drive the $\overline{PWR}$ pin active in response to the enabled kickstart or wake-up condition. This is true even if $\overline{PWR}$ was previously inactive as the result of power being applied by some means other than wake-up or kickstart.

The system may be powered down under software control by setting the PAB bit to a 1. This causes the open-drain $\overline{PWR}$ pin to be placed in a high-impedance state, as shown at the beginning of interval 4 in the timing diagram. As V_{CC} voltage decays, the $\overline{IRQ}$ output pin will be placed in a high-impedance state when V_{CC} goes below V_{PF}. If the system is to be again powered on in response to a wake-up or kickstart,

then both the TDF and KSF flags should be cleared and TPE and/or KIE should be enabled prior to setting the PAB bit.

During interval 5, the system is fully powered down. Battery backup of the clock calendar and nonvolatile RAM is in effect and $\overline{IRQ}$ is tri-stated, and monitoring of wake-up and kickstart takes place. If PRS=1, $\overline{PWR}$ stays active; otherwise if PRS=0, $\overline{PWR}$ is tri-stated.

SQUARE WAVE OUTPUT

The square wave output is enabled and disabled via the 'E32K' bit in the month register (B6 of 05h). If the square wave is enabled ($\overline{E32K}$ = '0') and the oscillator is enabled, then a 32.768 kHz square wave will be output on the SQW pin. If $\overline{E32K}$ = '0' and the Battery Backup 32 kHz enable bit 'BB32' is enabled (B5 of 05h) and volt-age is applied to V_{BAUX}, then the 32 kHz square wave signal will be output on the SQW pin in the absence of V_{CC}.

BATTERY MONITOR

Upon power-up, the DS1501/DS1511 checks the battery voltage of the back-up battery sources (V_{BAT} and V_{BAUX}). The Battery Low Flag 'VRT1' and 'VRT2' bits of control A register (B7 and B6 of 0Eh) will be set to a logic 1 at power-up if the battery voltage on V_{BAT} and V_{BAUX} are less than 2.5V (typical), otherwise VRT1 and VRT2 bits will be logic 0. VRT1 monitors V_{BAT} with VRT2 monitoring V_{BAUX}.

POWER-UP DEFAULT STATES

These bits are set upon power-up: $\overline{EOSC}$=0, $\overline{E32K}$=0, TIE=0, KIE=0, WDE=0, and WDS=0.

256 X 8 EXTENDED RAM

The DS1501/DS1511 provides 256 x 8 of on-chip SRAM which is controlled as nonvolatile data storage sustained from a lithium battery. On power-up, the RAM is taken out of write protect status by an internal signal.

Access to the SRAM is controlled by two on-chip latch registers. One register is used to hold the SRAM address, and the other is used to hold read/write data. The SRAM address space is from 00h to FFh. The 8-bit address of the RAM location to be accessed must be loaded into the extended RAM address register located at 10h. Data in the addressed location may be read by performing a read operation from location 13h, or written to by performing a write operation to location 13h. Data in any addressed location may be read or written repeatedly without changing the address in location 10h.

To read or write consecutive extended RAM locations, a burst mode feature can be enabled to increment the extended RAM address. To enable the burst mode feature, set the BME bit (B4 of control B register) to a logic 1. With burst mode enabled, write the extended RAM starting address location to register 10h. Then read or write the extended RAM data from/to register 13h. The extended RAM address locations are automatically incremented on the rising edge of $\overline{OE}$, $\overline{WE}$, or $\overline{CE}$ only when register 13h is being accessed. Refer to the Burst Mode Timing Waveform (Figure 6).

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.5V to +6.0V
Operating Temperature, Commercial Range	0°C to 70°C
Operating Temperature, Industrial Range	-40°C to +85°C
Storage Temperature, DS1501	-55°C to +125°C
Storage Temperature, DS1511	-40°C to +70°C
Soldering Temperature	260°C for 10 seconds (See Note 8)

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1 Voltage All Inputs						
V_{CC} = 5V ±10%	V_{IH}	2.2		V_{CC} +0.3	V	1
V_{CC} = 3.3V ±10%	V_{IH}	2.0		V_{CC} +0.3	V	1
Logic 0 Voltage All Inputs						
V_{CC} = 5V ±10%	V_{IL}	-0.3		0.8	V	1
V_{CC} = 3.3V ±10%	V_{IL}	-0.3		0.6	V	1
Battery Voltage	V_{BAT}	2.5		3.7	V	1
Auxiliary Battery Voltage	V_{BAUX}	2.5		3.7	V	1

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = 5.0V ±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	I_{CC}		X	15	mA	2
TTL Standby Current($\overline{CE}$ = V_{IH})	I_{CC1}		X	3	mA	2
CMOS Standby Current ($\overline{CE} \geq V_{CC}$ -0.2V)	I_{CC2}		X	3	mA	2
Battery Current, Oscillator On	I_{BAT1}			1.0	µA	
Battery Current, Oscillator Off	I_{BAT2}			0.1	µA	
Input Leakage Current (any input)	I_{IL}	-1		+1	µA	
Output Leakage Current (any output)	I_{OL}	-1		+1	µA	
Output Logic 1 Voltage (I_{OUT} = -1.0 mA)	V_{OH}	2.4			V	1
Output Logic 0 Voltage						
I_{OUT} = 2.1 mA, DQ0-7 Outputs	V_{OL1}			0.4	V	1
I_{OUT} = 10.0 mA, $\overline{IRQ}$, $\overline{PWR}$, and $\overline{RST}$ Outputs	V_{OL2}			0.4	V	1, 3
Power-fail Voltage	V_{PF}	4.25	4.37	4.50	V	1
Battery Switch-over Voltage	V_{SO}		V_{BAT}, V_{BAUX}		V	1, 4

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = 3.3V ±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	I_{CC}		X	10	mA	2
TTL Standby Current($\overline{CE}$ = V_{IH})	I_{CC1}		X	2	mA	2
CMOS Standby Current ($\overline{CE} \geq V_{CC}$ -0.2V)	I_{CC2}		X	2	mA	2
Battery Current, Oscillator On	I_{BAT1}			1.0	µA	
Battery Current, Oscillator Off	I_{BAT2}			0.1	µA	
Input Leakage Current (any input)	I_{IL}	-1		+1	µA	
Output Leakage Current (any output)	I_{OL}	-1		+1	µA	
Output Logic 1 Voltage (I_{OUT} = -1.0 mA)	V_{OH}	2.4			V	1
Output Logic 0 Voltage I_{OUT} = -2.1 mA, DQ0-7 Outputs	V_{OL1}			0.4	V	1
I_{OUT} = 10.0 mA, $\overline{IRQ}$, $\overline{PWR}$, and $\overline{RST}$ Outputs	V_{OL2}			0.4	V	1, 3
Power-fail Voltage	V_{PF}	2.80	2.88	2.97	V	1
Battery Switch-over Voltage	V_{SO}		V_{BAT}, V_{BAUX}, or V_{PF}		V	1, 7

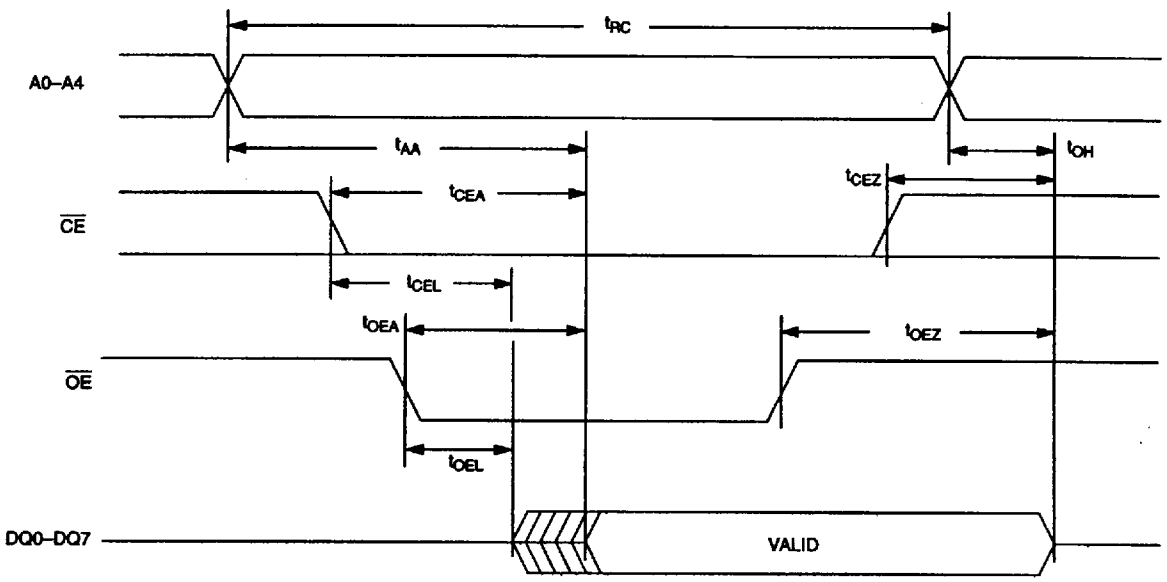
READ CYCLE, AC CHARACTERISTICS (0°C to 70°C; V_{CC} = 5.0V ±10%)

PARAMETER	SYMBOL	MIN	TYPE	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	70			ns	
Address Access Time	t_{AA}			70	ns	
$\overline{CE}$ to DQ Low-Z	t_{CEL}	5			ns	
$\overline{CE}$ Access Time	t_{CEA}			70	ns	
$\overline{CE}$ Data Off Time	t_{CEZ}			25	ns	
$\overline{OE}$ to DQ Low-Z	t_{OEL}	5			ns	
$\overline{OE}$ Access Time	t_{OEA}			35	ns	
$\overline{OE}$ Data Off Time	t_{OEZ}			25	ns	
Output Hold from Address	t_{OH}	5			ns	

READ CYCLE, AC CHARACTERISTICS (0°C to 70°C; V_{CC} = 3.3V ±10%)

PARAMETER	SYMBOL	MIN	TYPE	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	120			ns	
Address Access Time	t_{AA}			120	ns	
$\overline{CE}$ to DQ Low-Z	t_{CEL}	5			ns	
$\overline{CE}$ Access Time	t_{CEA}			120	ns	
$\overline{CE}$ Data Off Time	t_{CEZ}			40	ns	
$\overline{OE}$ to DQ Low-Z	t_{OEL}	5			ns	
$\overline{OE}$ Access Time	t_{OEA}			100	ns	
$\overline{OE}$ Data Off Time	t_{OEZ}			35	ns	
Output Hold from Address	t_{OH}	5			ns	

READ CYCLE TIMING Figure 3



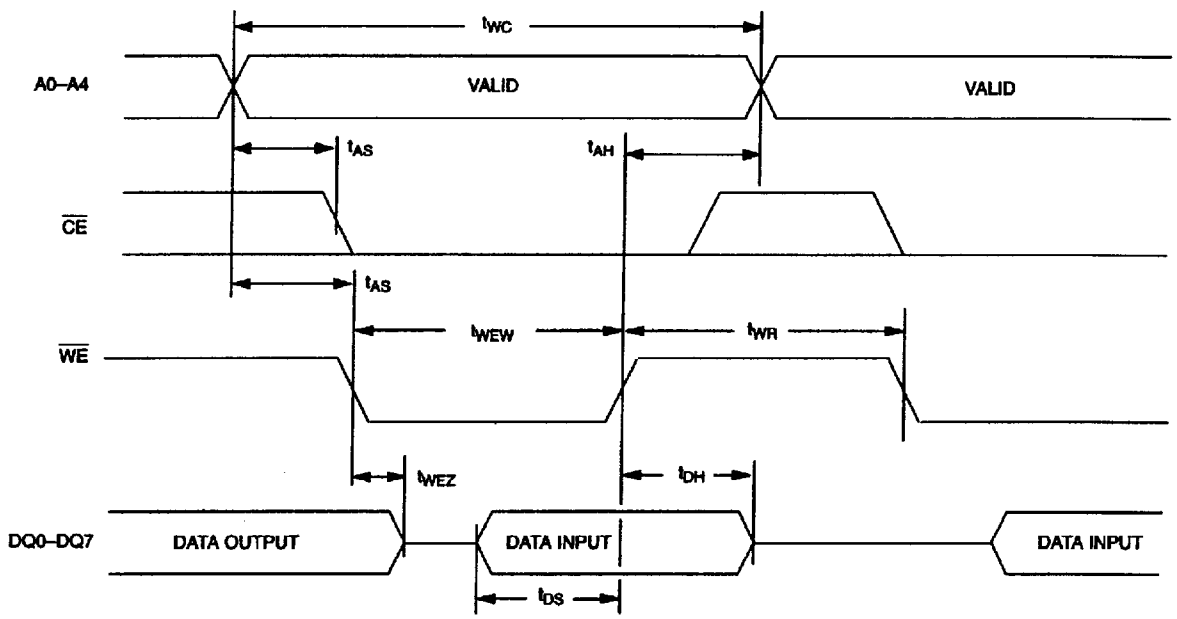
WRITE CYCLE, AC CHARACTERISTICS (0°C to 70°C; V_{CC}= 5.0V ±10%)

PARAMETER	SYMBOL	MIN	TYPE	MAX	UNITS	NOTES
Write Cycle Time	t_{WC}	70			ns	
Address Step-up Time	t_{AS}	0			ns	
$\overline{WE}$ Pulse Width	t_{WEW}	50			ns	
$\overline{CE}$ Pulse Width	t_{CEW}	55			ns	
Data Setup Time	t_{DS}	30			ns	
Data Hold Time	t_{DH}	0			ns	
Address Hold Time	t_{AH}	0			ns	
$\overline{WE}$ Data Off Time	t_{WEZ}			25	ns	
Write Recovery Time	t_{WR}	5			ns	

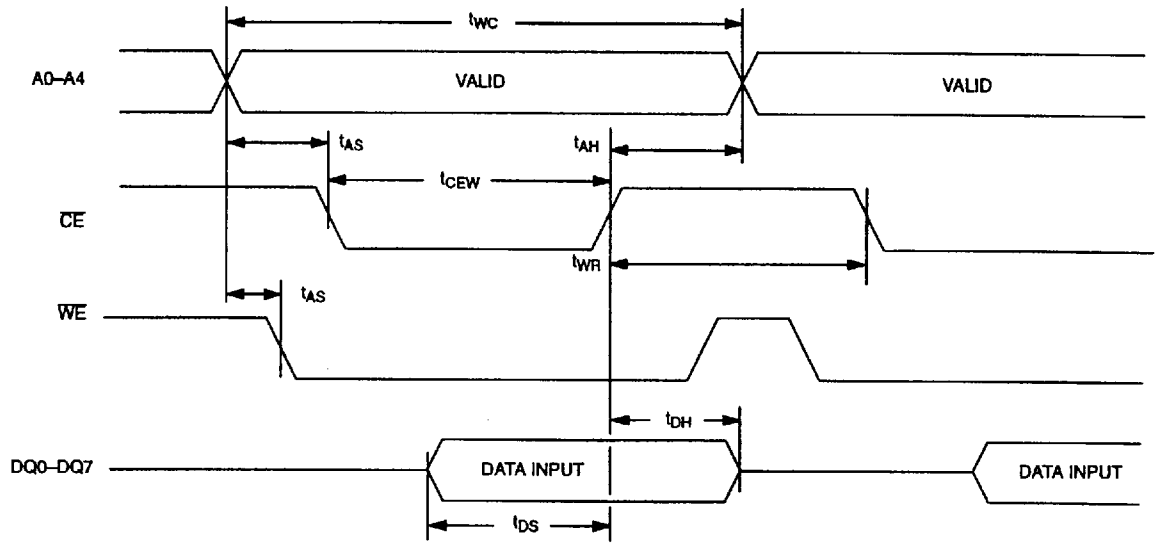
WRITE CYCLE, AC CHARACTERISTICS (0°C to 70°C; V_{CC}= 3.3V ±10%)

PARAMETER	SYMBOL	MIN	TYPE	MAX	UNITS	NOTES
Write Cycle Time	t_{WC}	120			ns	
Address Step-up Time	t_{AS}	0			ns	
$\overline{WE}$ Pulse Width	t_{WEW}	100			ns	
$\overline{CE}$ Pulse Width	t_{CEW}	110			ns	
Data Setup Time	t_{DS}	80			ns	
Data Hold Time	t_{DH}	0			ns	
Address Hold Time	t_{AH}	0			ns	
$\overline{WE}$ Data Off Time	t_{WEZ}			40	ns	
Write Recovery Time	t_{WR}	10			ns	

WRITE CYCLE TIMING, WRITE ENABLE CONTROLLED Figure 4



WRITE CYCLE TIMING, CHIP ENABLE CONTROLLED Figure 5



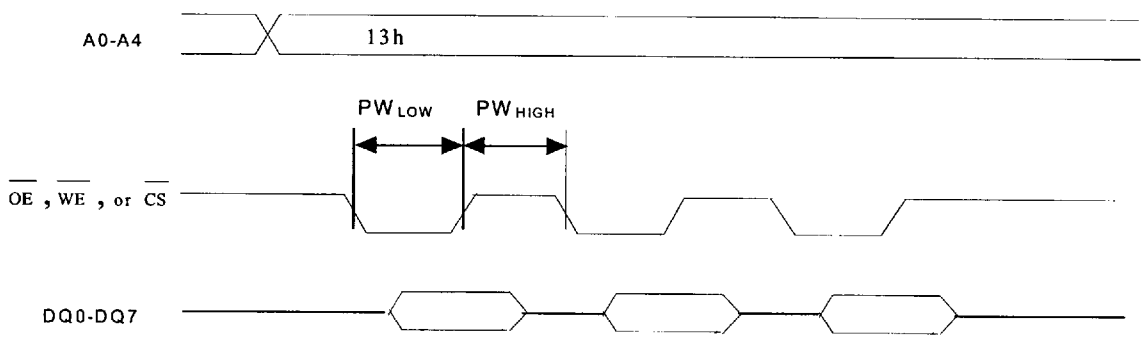
BURST MODE TIMING CHARACTERISTICS (0°C to 70°C; V_{CCI}=5.0V±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pulse Width $\overline{OE}$, $\overline{WE}$, or $\overline{CE}$ High	PW_{HIGH}	x			nS	
Pulse Width $\overline{OE}$, $\overline{WE}$, or $\overline{CE}$ Low	PW_{LOW}	x			nS	

BURST MODE TIMING CHARACTERISTICS (0°C to 70°C; V_{CCI}=3.3V±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pulse Width $\overline{OE}$, $\overline{WE}$, or $\overline{CE}$ High	PW_{HIGH}	x			nS	
Pulse Width $\overline{OE}$, $\overline{WE}$, or $\overline{CE}$ Low	PW_{LOW}	x			nS	

BURST MODE TIMING WAVEFORM Figure 6



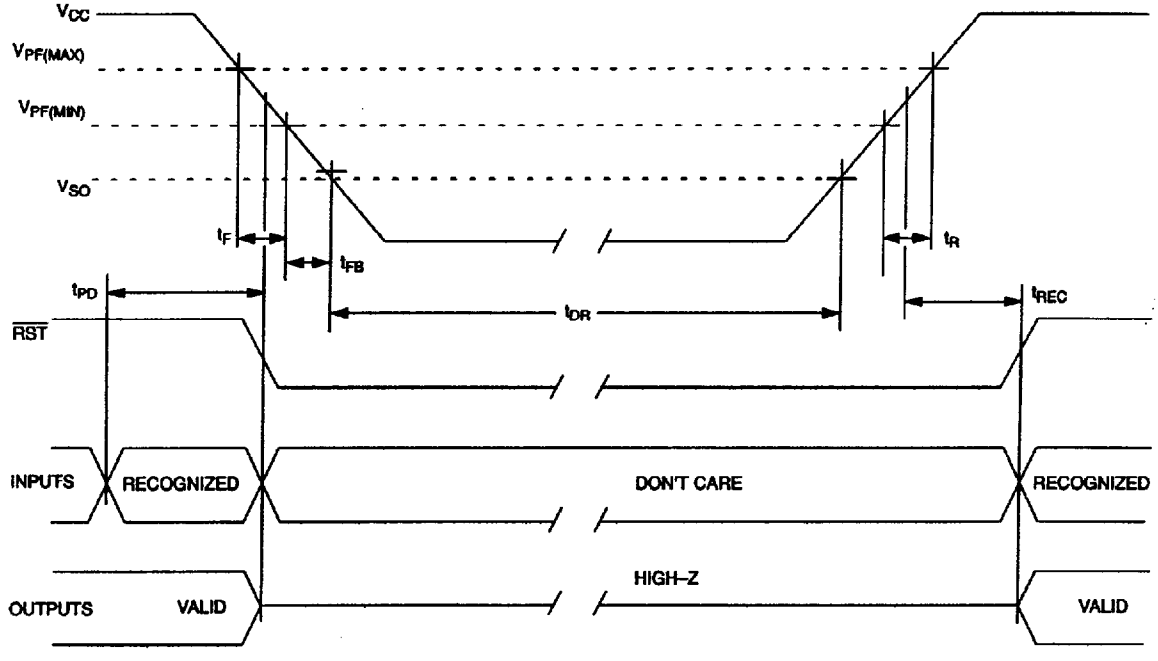
POWER UP/DOWN CHARACTERISTICS (0°C to 70°C; V_{CC}= 5.0V ±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ or $\overline{WE}$ at V_{IH} Before Power-Down	t_{PD}	0			µs	
V_{CC} Fall Time: $V_{PF(max)}$ to $V_{PF(min)}$	t_F	300			µs	
V_{CC} Fall Time: $V_{PF(min)}$ to V_{SO}	t_{FB}	10			µs	
V_{CC} Rise Time: $V_{PF(min)}$ to $V_{PF(max)}$	t_R	0			µs	
V_{PF} to $\overline{RST}$ High	t_{REC}	40		200	ms	

(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time(Oscillator On)	t_{DR}	10			years	6

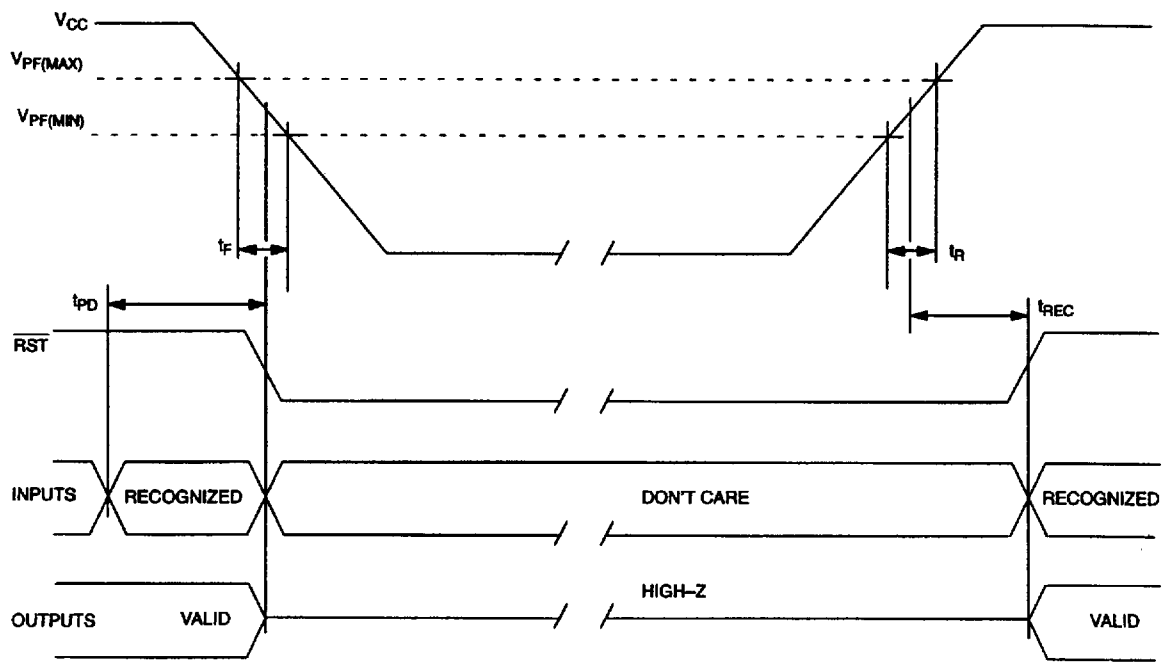
POWER-UP/DOWN WAVEFORM TIMING 5-VOLT DEVICE Figure 7



POWER UP/DOWN CHARACTERISTICS (0°C to 70°C; V_{CC}= 3.3V ±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ or $\overline{WE}$ at V_{IH} Before Power-Down	t_{PD}	0			µs	
V_{CC} Fall Time: $V_{PF(max)}$ to $V_{PF(min)}$	t_F	300			µs	
V_{CC} Rise Time: $V_{PF(min)}$ to $V_{PF(max)}$	t_R	0			µs	
V_{PF} to $\overline{RST}$ High	t_{REC}	40		200	ms	

POWER-UP/DOWN WAVEFORM TIMING 3.3-VOLT DEVICE Figure 8



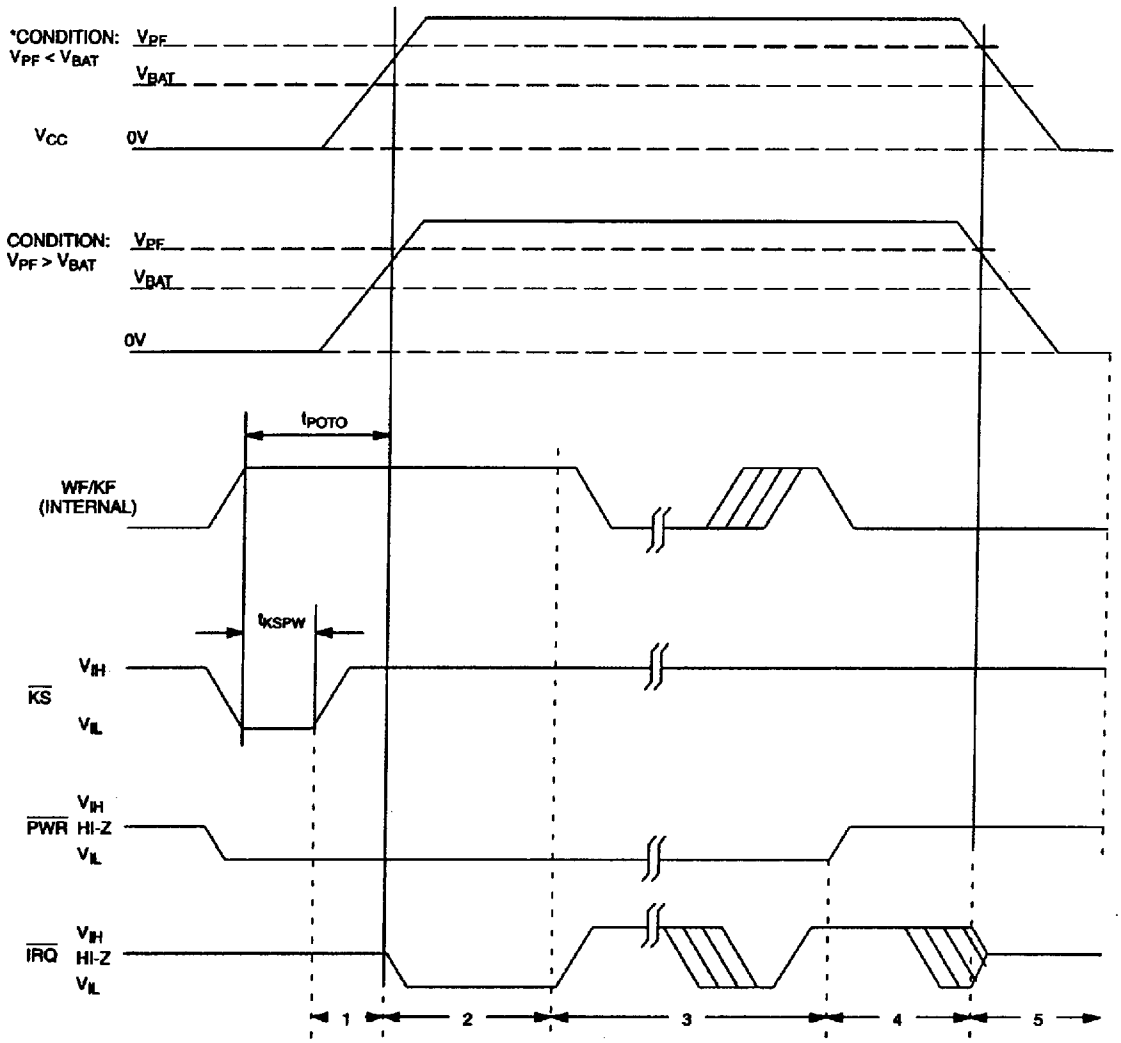
CAPACITANCE (T_A= 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance on all input pins	C_{IN}			10	pF	
Capacitance on $\overline{IRQ}$, $\overline{PWR}$, $\overline{RST}$, and DQ pins	C_{IO}			10	pF	

AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0.0 to 3.0 Volts
Timing Measurement Reference Levels:
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

WAKE-UP/KICKSTART TIMING Figure 9



NOTE:

Time intervals shown above are referenced in Wake-up/Kickstart section.
*This condition can occur with the 3.3V device.

WAKE-UP/KICKSTART TIMING

(T_A= 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Kickstart Input Pulse Width	t_{KSPW}	2			µs	
Wake-up/Kickstart Power-on Timeout	t_{POTO}	2			seconds	5

NOTE

1. Voltage referenced to ground.

2. Outputs are open.

3. The $\overline{IRQ}$, $\overline{PWR}$, and $\overline{RST}$ outputs are open drain.

4. Battery switch-over occurs at the battery terminal voltage level.

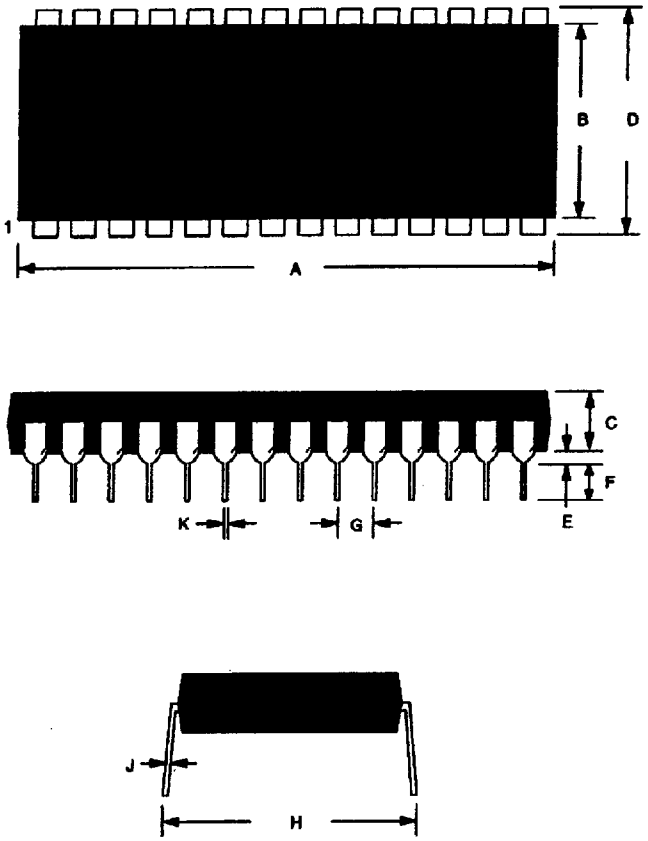
5. Wakeup kickstart timeout generated only when the oscillator is enabled and the countdown chain is not reset.

6. t_{DR} is the amount of time that the internal battery can power the internal oscillator and internal registers of the DS1511.

7. If V_{PF} is less than V_{BAT} and V_{BAUX}, the device power is switched from V_{CC} to the greater of V_{BAT} and V_{BAUX} when V_{CC} drops below V_{PF}. If V_{PF} is greater than V_{BAT} and V_{BAUX}, the device power is switched from V_{CC} to the larger of V_{BAT} and V_{BAUX} when V_{CC} drops below the larger of V_{BAT} and V_{BAUX}.

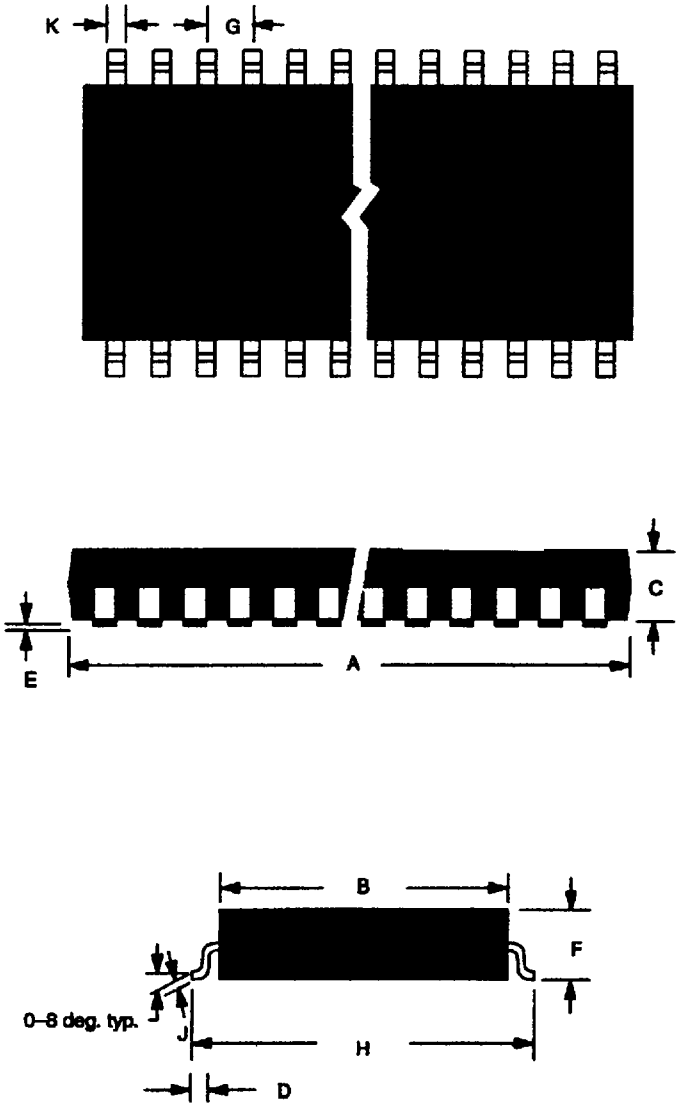
8. Real-Time Clock Modules can be successfully processed through conventional wave-soldering techniques as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. Post-solder cleaning with water washing techniques is acceptable, provided that ultrasonic vibration is not used.

DS1501 28-PIN DIP



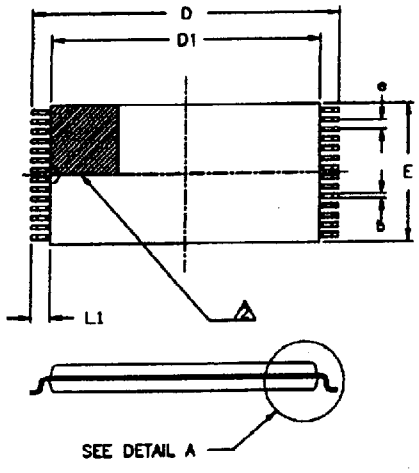
PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN.	1.445	1.470
MM	36.70	37.34
B IN.	0.530	0.550
MM	13.46	13.97
C IN.	0.140	0.160
MM	3.56	4.06
D IN.	0.600	0.625
MM	15.24	15.88
E IN.	0.015	0.040
MM	0.38	1.02
F IN.	0.120	0.145
MM	3.05	3.68
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.625	0.675
MM	15.88	17.15
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.022
MM	0.38	0.56

DS1501S 28-PIN SOIC



PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN.	0.697	0.728
MM	17.70	18.50
B IN.	0.324	0.350
MM	8.23	8.90
C IN.	0.087	0.118
MM	2.20	3.00
D IN.	0.016	0.050
MM	0.40	1.27
E IN.	0.002	0.014
MM	0.05	0.35
F IN.	0.100	0.120
MM	2.55	3.05
G IN.	0.050	BSC
MM	1.27	
H IN.	0.453	0.500
MM	11.50	12.70
J IN.	0.006	0.013
MM	0.14	0.32
K IN.	0.014	0.020
MM	0.35	0.50

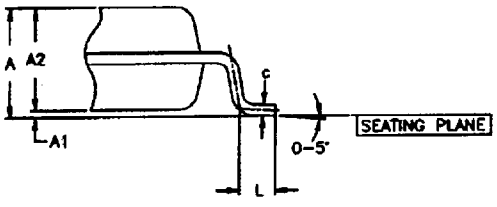
DS1501E 28-PIN TSOP



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS

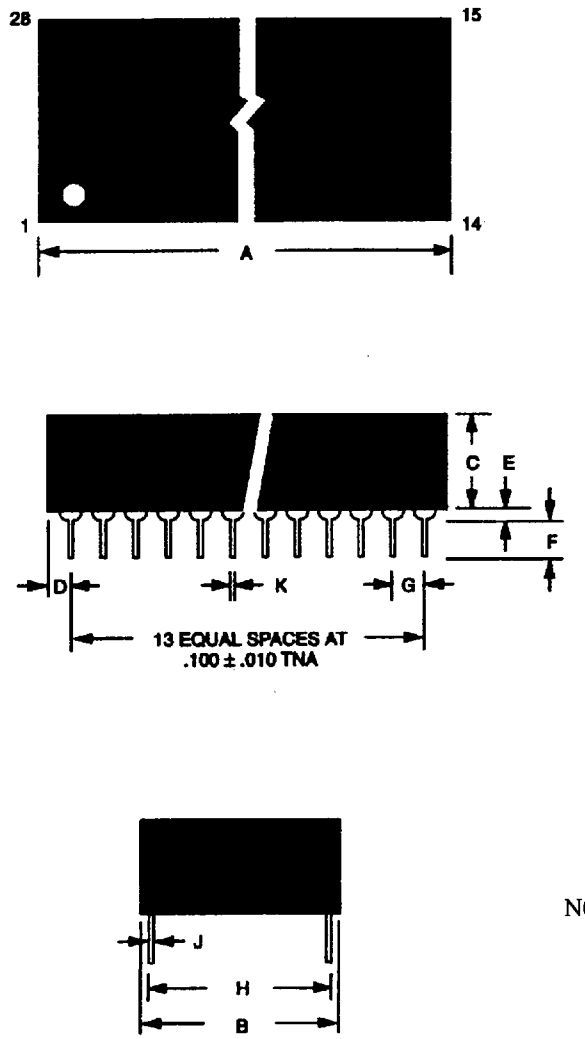
2. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT ONE HALF OF ITS AREA MUST BE LOCATED WITHIN THE ZONE INDICATED



DETAIL A

PKG	28-PIN	
DIM	MIN	MAX
A	-	1.20
A1	0.05	-
A2	0.91	1.02
b	0.18	0.27
c	0.15	0.20
D	13.20	13.60
D1	11.70	11.90
E	7.90	8.10
e	0.55 BSC	
L	0.30	0.70
l	0.80 BSC	

DS1511



PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN.	1.520	1.540
MM	38.61	39.12
B IN.	0.695	0.720
MM	17.65	18.29
C IN.	0.350	0.375
MM	8.89	9.52
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.015	0.030
MM	0.38	0.76
F IN.	0.110	0.140
MM	2.79	3.56
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

NOTE: PINS 2, 3, 21, AND 25 ARE MISSING BY DESIGN.