



TDA7463A

LOW VOLTAGE TONE CONTROL DIGITALLY CONTROLLED AUDIO PROCESSOR

1 FEATURES

- 2 STEREO INPUT
- 1 STEREO OUTPUT
- TREBLE BOOST
- BASS CONTROL
- BASS AUTOMATIC LEVEL CONTROL
- VOLUME CONTROL IN 1dB STEPS
- MUTE
- STAND-BY FUNCTION SOFTWARE CONTROLLED
- ALL FUNCTION ARE PROGRAMMABLE VIA SERIAL BUS

2 DESCRIPTION

The TDA7463A is a volume tone (bass and treble) processor for quality audio applications in Low voltage supply portable systems.

Bass ALC (Automatic Level Control) function can

Figure 1. Package

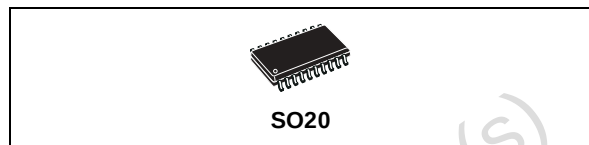


Table 1. Order Codes

Part Number	Package
TDA7463A	SO20

be adjusted by a dedicated pin. The control of all the functions is accomplished by serial bus.

The AC signal setting is obtained by resistor networks and switches combined with operational amplifiers.

Thanks to the used BIPOLAR/CMOS Technology, Low Distortion, Low Noise and DC stepping are obtained.

Figure 2. Application & Test Circuit

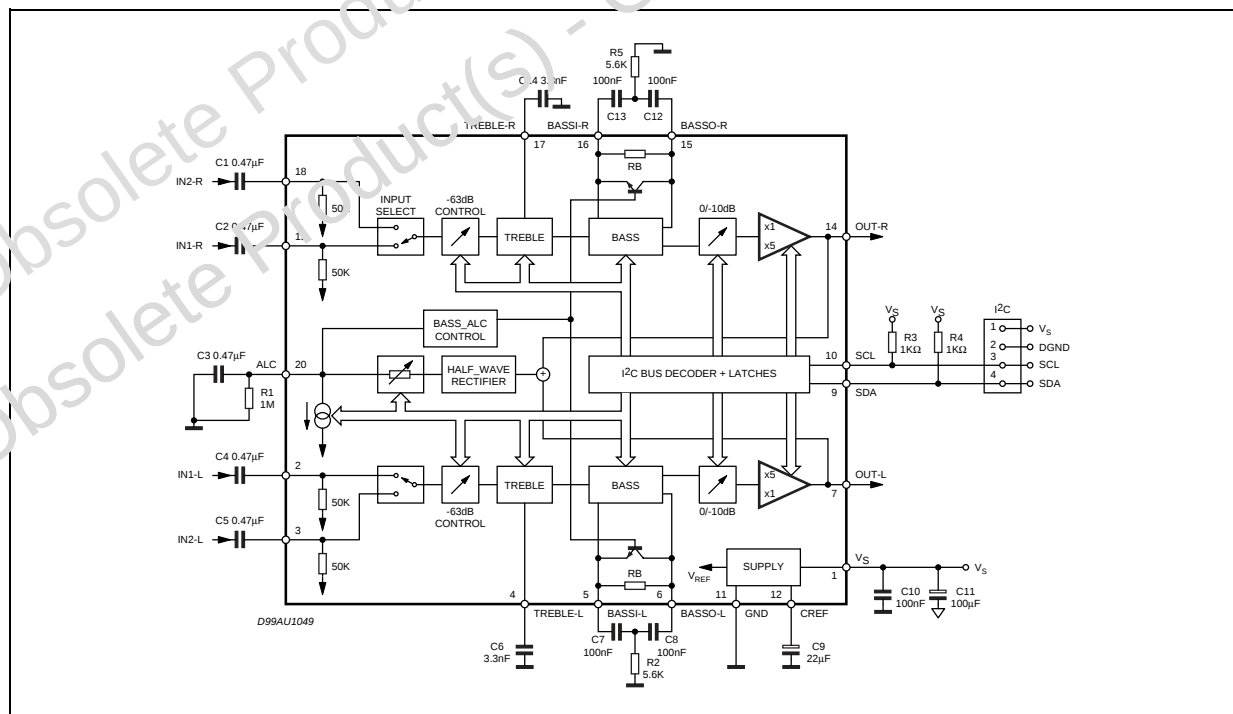


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_S	Operating Supply Voltage	5	V
T_{amb}	Operating Ambient Temperature	0 to 70	°C
T_{stg}	Storage Temperature Range	-55 to 150	°C

Figure 3. Pin Connection

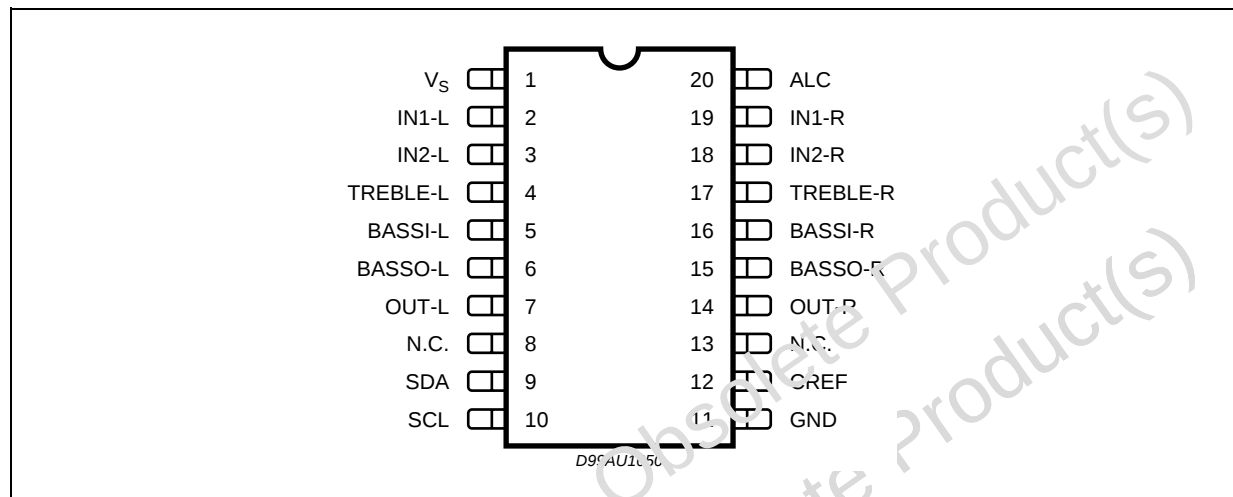


Table 3. Thermal Data

Symbol	Parameter	Value	Unit
$R_{th j-pin}$	Thermal Resistance Junction-pins	85	°C/W

Table 4. Quick Reference Data

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply voltage		1.8	2.4	3	V
V_{CL}	Max. input signal handling		0.2			V _{rms}
THD	Total Harmonic Distortion	$V = 0.1V_{rms}$; $f = 1KHz$			0.1	%
S/N	Signal to Noise Ratio	$V_{out} = 0.1V_{rms}$ (mode = OFF)		80		dB
Sc	Channel Separation	$f = 1KHz$		80		dB
	Volume control	(1dB step)	-63		0	dB
		-10dB damping	-10		0	dB
		-14dB	0		14	dB
		Treble Control	0		8	dB
		Bass Control	0		14	dB
		mute attenuation		100	8	dB

Table 5. Electrical Characteristics (refer to the test circuit $T_{amb} = 25^{\circ}\text{C}$, $V_S = 2.4\text{V}$, $R_L = 10\text{K}\Omega$, $R_G = 600\Omega$, all controls flat, unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY						
V_S	Supply Voltage		1.8	2.4	3	V
I_S	Supply Current			4		mA
I_{ST-BY}	Stand-By Current			50		μA
SVR	Ripple Rejection			70		dB
INPUT STAGE						
R_{IN}	Input Resistance		35	50	65	$\text{K}\Omega$
V_{CL}	Clipping Level	THD = 0.3%	0.2			V _{rms}
VOLUME CONTROL						
C_{RANGE}	Control Range			13		dB
AV_{MIN}	Min Attenuation		-1	0	1	dB
AV_{MAX}	Max. Attenuation		62	63	64	dB
A_{STEP}	Step Resolution			1		dB
A_{mute}	Mute Attenuation		80	100		dB
A_{-10dB}	-10dB damping			10		dB
G_{14dB}	14dB gain			14		dB
BASS CONTROL (1)						
G_b	Control Range	Max. Boost/on		14		dB
R_B	Internal Feedback Resistance		33.75	45	56.25	$\text{K}\Omega$
TREBLE CONTROL (1)						
G_t	Control Range	Max. Boost on		8		dB
AUDIO OUTPUTS						
V_{CLIP}	Clipping Level	d = 0.3%	0.2			V _{RMS}
R_L	Output Load Resistance		10			$\text{K}\Omega$
V_{DC}	DC voltage Level			0.8		V
GENERAL						
E_{NO}	Output Noise	Output Muted All gains = 0dB; BW = 20Hz to 20KHz flat		5 8		μV μV
E_t	Total Tracking Error			0	1	dB
S/N	Signal to Noise Ratio	All gains 0dB; $V_O = 0.1\text{V}_{RMS}$;		80		dB
SC	Channel Separation Left/Right			80		dB
d	Distortion	$A_V = 0$; $V_I = 0.1\text{V}_{RMS}$;			0.1	%
BUS INPUT						
V_{IL}	Input Low Voltage				0.5	V
V_{IH}	Input High Voltage		1.9			V
I_{IN}	Input Current	$V_{IN} = 0.4\text{V}$	-5		5	μA
V_O	Output Voltage SDA Acknowledge	$I_O = 1.6\text{mA}$			0.4	V

Note: 1. BASS and TREBLE response: The center frequency and the response quality can be chosen by the external circuitry.

3 DATA BYTES

Address = (HEX) 10001000

Table 6. FUNCTION SELECTION:

The first byte (subaddress)58

MSB							LSB	SUBADDRESS
D7	D6	D5	D4	D3	D2	D1	D0	
	X	X	B	0	0	0	0	STAND-BY & TREBLE & OTHERS
	X	X	B	0	0	0	1	BASS
	X	X	B	0	0	1	0	VOLUME

B = 1 incremental bus; active

B = 0 no incremental bus;

X = indifferent 0,1

Table 7. STAND_BY & TREBLE & OTHERS

MSB							LSB	
D7	D6	D5	D4	D3	D2	D1	D0	
								STAND-BY
							1	ALL CIRCUITS STOP
								TREBLE
						1		STAND-BY (Treble block stops)
					1	0		BOOST OFF
					0	0		BOOST ON
				1	0	0		High Boost (+8dB)
				0	0	0		Low Boost (+4dB)
								MUTE
			1					Input Mute ON
			0					Input Mute OFF
		1						Output Mute ON
		0						Output Mute OFF
								BASS
	1							Release Current Circuit ON
	0							Release Current Circuit OFF
								INPUT Select
1								INPUT 1
0								INPUT 2

Table 8. BASS

MSB							LSB	BASS
D7	D6	D5	D4	D3	D2	D1	D0	
							1	STAND-BY (Bass block stops)
						1		BASS (boost OFF)
						0		BASS (boost ON)
					1	0		High boost (Ex. + 14dB)
					0	0		Low boost (Ex. + 6dB)
				1				ALC mode OFF (ALC block stops)
				0				ALC mode ON
		0	0					Attack time resistor (12.5K Ω) Release current (0.4 μ A)
		0	1					Attack time resistor (25K Ω) Release current (0.2 μ A)
		1	0					Attack time resistor (50K Ω) Release current (0.1 μ A)
		1	1					Attack time resistor (100K Ω) Release current (0.05 μ A)
0	0							Threshold1 (0.2Vrms)
0	1							Threshold2 (0.14Vrms)
1	0							Threshold3 (0.1Vrms)
1	1							Threshold4 (0.07Vrms)

Table 9. VOLUME

MSB							LSB	VOLUME
D7	D6	D5	D4	D3	D2	D1	D0	1 dB STEPS
					0	0	0	0
					0	0	1	-1
					0	1	0	-2
					0	1	1	-3
					1	0	0	-4
					1	0	1	-5
					1	1	0	-6
					1	1	1	-7
								8 dB STEPS
		0	0	0				0
		0	0	1				-8
		0	1	0				-16
		0	1	1				-24
		1	0	0				-32
		1	0	1				-40
		1	1	0				-48
		1	1	1				-56
								OUTPUT GAIN
	1							0dB
	0							+14dB
								OUTPUT ATTENUATION
1								0dB
0								-10dB

VOLUME : 0 ~ -63dB

3.1 ALC IN general:

Table 10. VOLUME setting with ALC

Target Volume [dB]	Volume [dB]	Output Gain 0/+14dB0/-10dB [dB]	Output Attenuation 0/-10dB [dB]
0	-14	+14	0
-1	-15		
-2	-16		
-3	-17		
-4	-18		
-5	-19		
-6	-20		
-7	-21		
-8	-22		
-9	-23		
-10	-24		
-11	-25		
-12	-26		
-13	-27		
-14	-14	0	0
-15	-15		
-16	-16		
-17	-17		
-18	-18		
-19	-19		
-20	-20		
-21	-21		
-22	-22		
-23	-23		
-24	-14	0	-10
-25	-15		
-26	-16		
-27	-17		
:	:		
:	:		
-70	-60		
-71	-61		
-72	-62		
-73	-63		

Figure 4. PIN: IN-L, IN-R

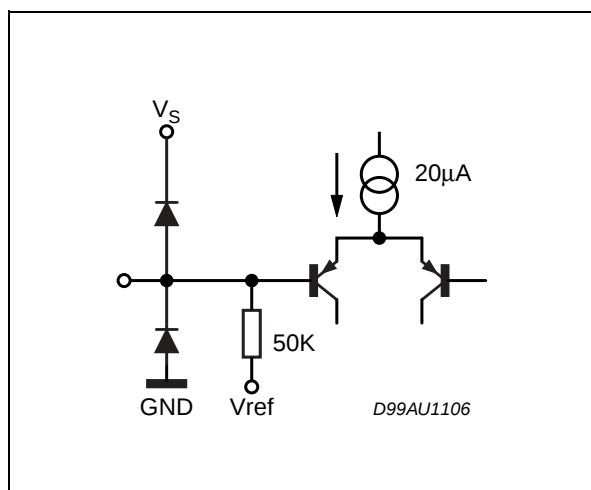


Figure 7. OUT-L, OUT-R

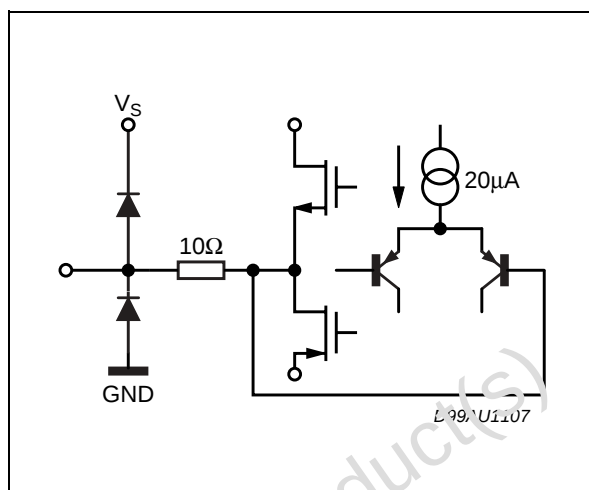


Figure 5. PIN: TREBLE-L, TREBLE-R

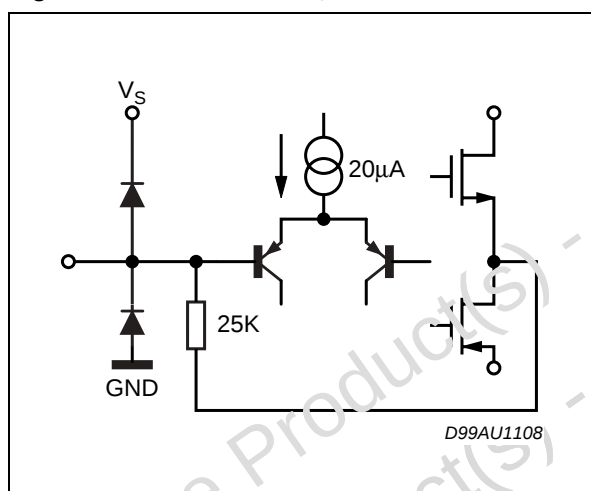


Figure 8. SCL, SDA

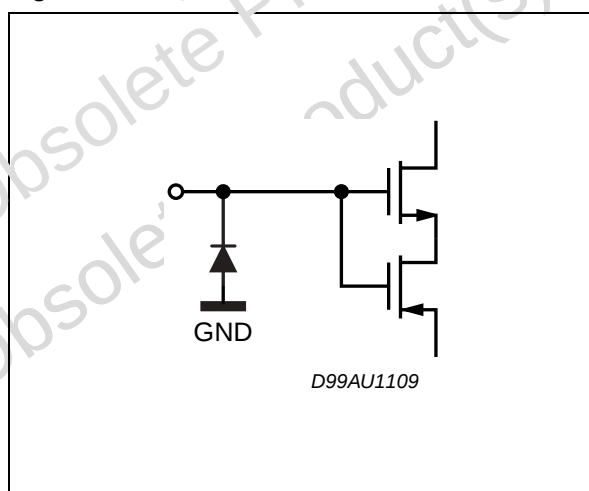


Figure 6. PIN: BASSI-L, BASSI-R

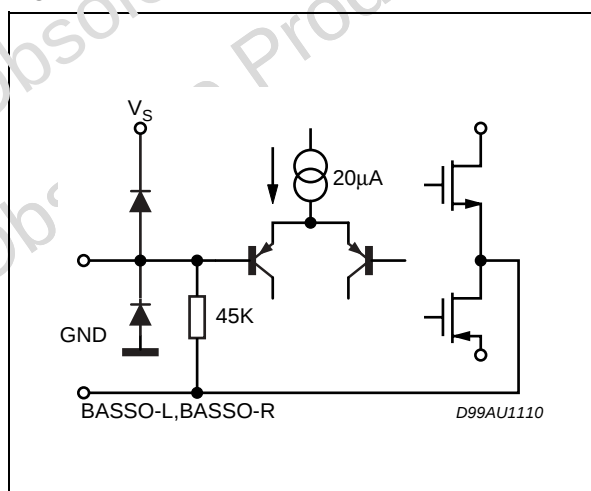


Figure 9. BASSO-L, BASSO-R

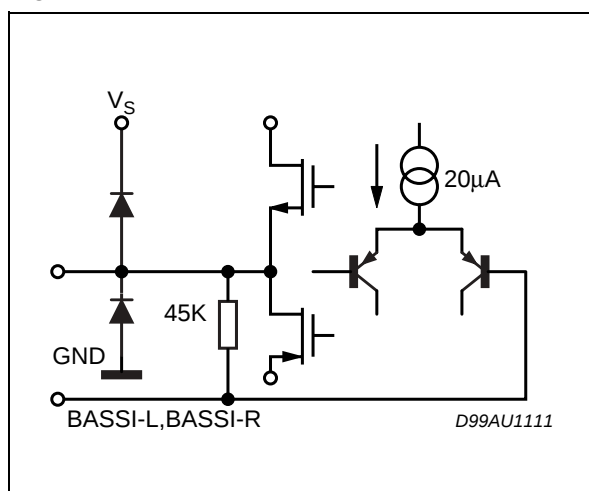


Figure 10. PIN: ALC

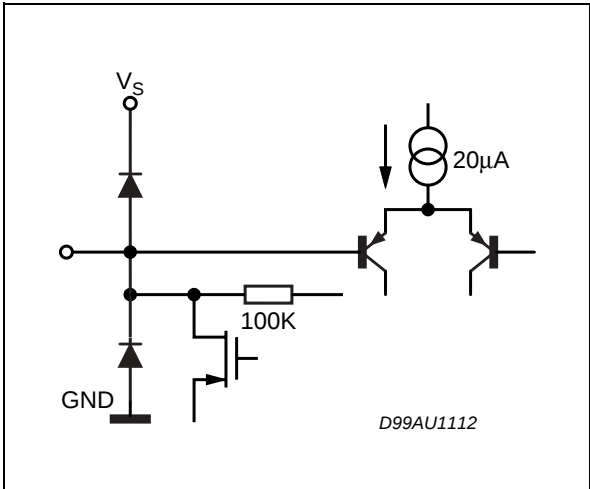


Figure 11. PIN CREF

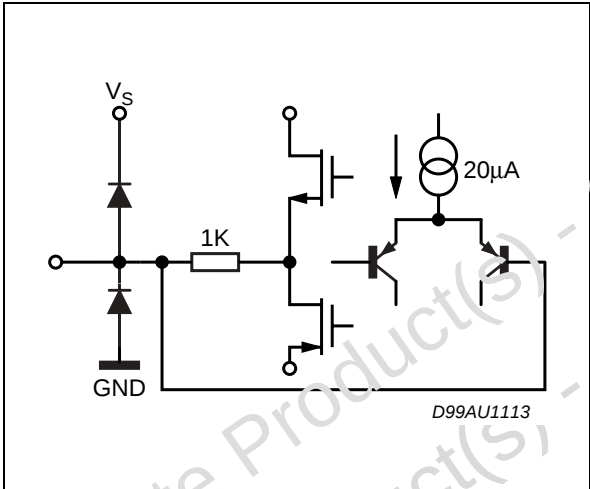


Figure 12. BASS ALC: Threshold curve

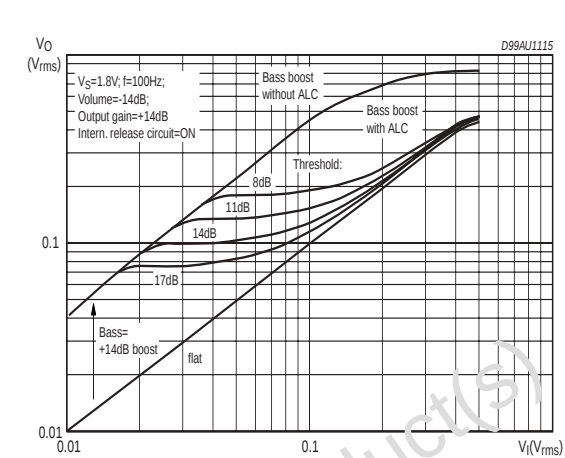


Figure 13. BASS ALC: THD

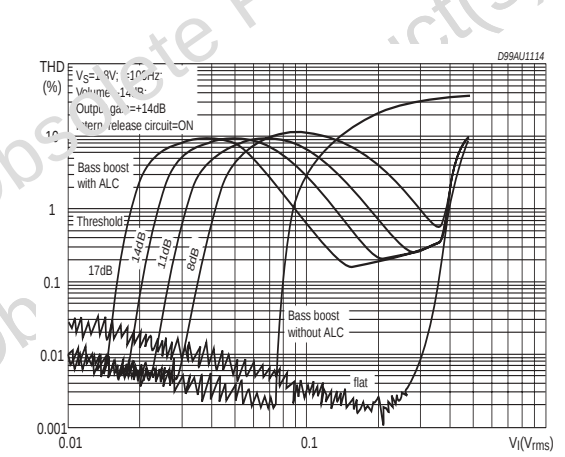
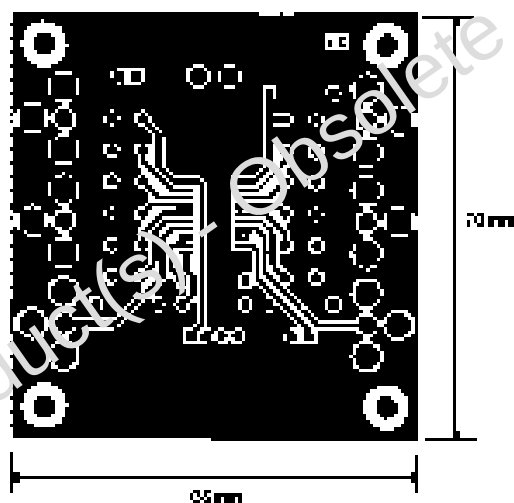
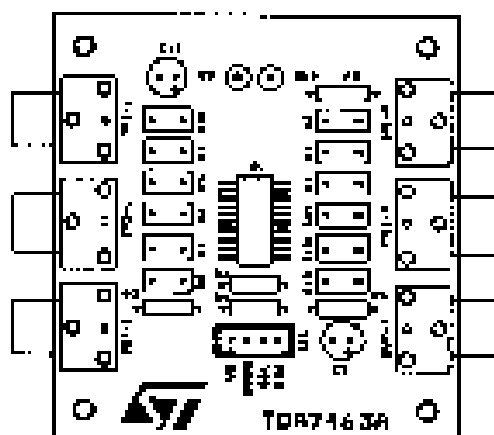
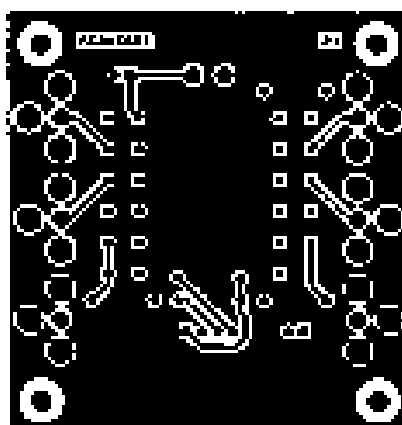


Figure 14. board and Components Layout of the Application & Test Circuit.



Component
layer

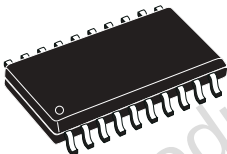


Solder
layer

Figure 15. SO20 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.200
C	0.23		0.32	0.009		0.013
D ⁽¹⁾	12.60		13.00	0.496		0.512
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004
(1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.						

OUTLINE AND MECHANICAL DATA



SO20

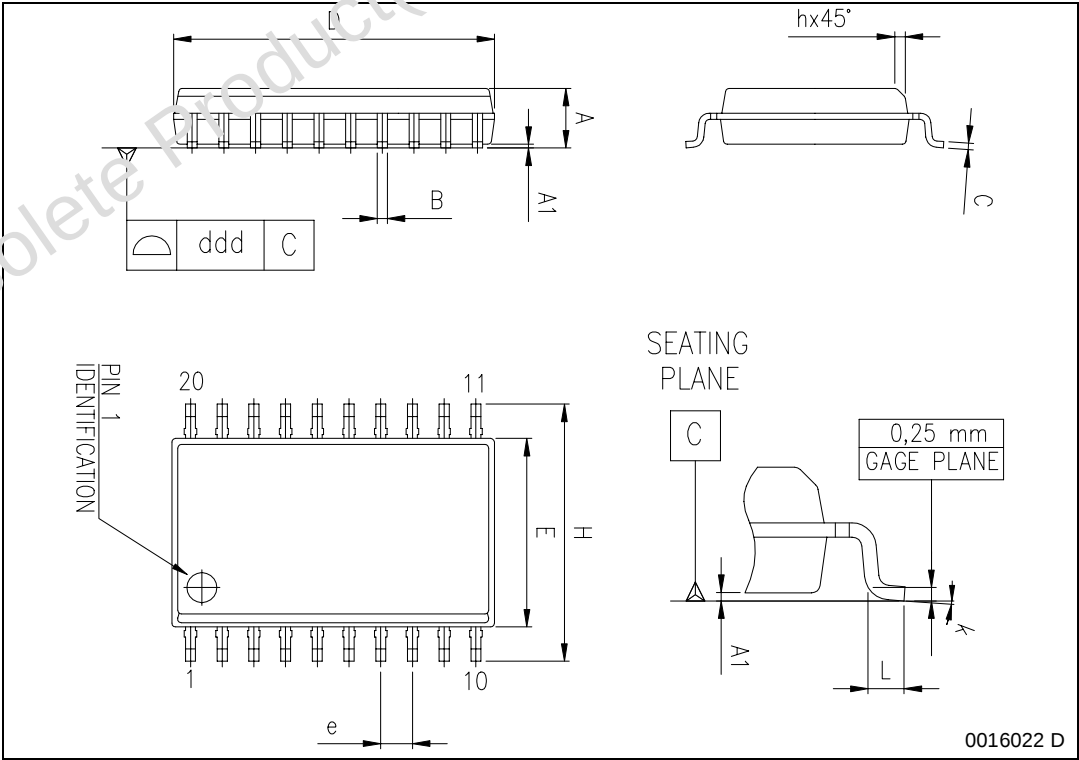


Table 11. Revision History

Date	Revision	Description of Changes
January 2003	3	Third issue
June 2004	3	Changed the Style-sheet in compliance to the new "Corporate Technical Publications Design Guide"

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