

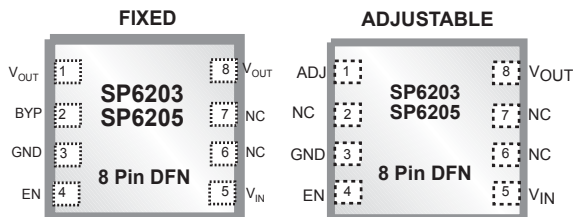


# SP6203/6205

## Low Noise, 300mA and 500mA CMOS LDO Regulators

### FEATURES

- Very Low Dropout Voltage:  $0.6\Omega$  PMOS Pass Device
- Accurate Output Voltage: 2% over Temperature
- Guaranteed 500mA Output Current: SP6205
- Ultra Low Noise Output:  $12\mu V_{RMS}$  with 10nF Bypass
- Unconditionally Stable with  $2.2\mu F$  Ceramic
- Low Quiescent Current:  $45\mu A$
- Very Low Ground Current:  $350\mu A$  at 500 mA
- Power-Saving Shutdown Mode:  $< 1\mu A$
- Fast Turn-On and Turn-Off:  $60\mu S$
- Fast Transient Response
- Current Limit and Thermal Shutdown Protection
- Very Good Load/Line Regulation:  $0.07/0.04\%$
- Excellent PSRR:  $67dB < 1kHz$
- Industry Standard SOT-23-5 and Small 8 pin 2X3 DFN Package
- Fixed Output Voltages: 2.5V, 2.7V, 2.8V, 2.85V, 3.0V and 3.3V
- Adjustable Output Available



*Now Available in Lead Free Packaging*

### APPLICATIONS

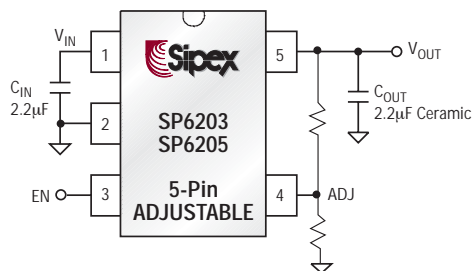
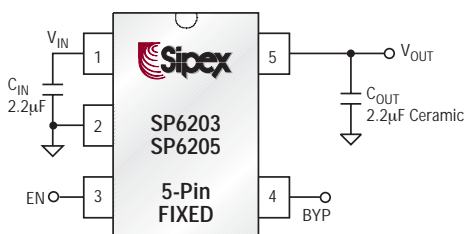
- Cellular / GSM Phones
- Laptop / Palmtop Computers
- Battery-Powered Systems
- Pagers
- Medical Devices
- MP3/CD Players
- Digital Still Cameras

### DESCRIPTION

The SP6203/6205 are ultra low noise CMOS LDOs with very low dropout and ground current. The noise performance is achieved by means of an external bypass capacitor without sacrificing turn-on and turn-off speed critical to portable applications. Extremely stable and easy to use, these devices offer excellent PSRR and Line/Load regulation. Target applications include battery-powered equipment such as portable and wireless products. Regulators' ground current increases only slightly in dropout. Fast turn-on/turn-off enable control and an internal  $30\Omega$  pull down on output allows quick discharge of output even under no load conditions. Both LDOs are protected with current limit and thermal shutdown.

Both LDOs are available in fixed & adjustable output voltage versions and come in an industry standard SOT-23 5-pin and small 2X3 8pin DFN packages. For SC-70 100mA CMOS LDO, SP6213 is available.

### TYPICAL APPLICATION CIRCUIT



## ABSOLUTE MAXIMUM RATINGS

Supply Input Voltage ( $V_{IN}$ ).....-2V to 6V  
 Output Voltage ( $V_{OUT}$ ).....-0.6V to  $V_{IN} + 1V$   
 Enable Input Voltage ( $V_{EN}$ ).....-2V to 6V  
 Power Dissipation ( $P_D$ ).....Internally Limited, Note 1  
 Lead Temperature (soldering 5s).....+260°C  
 Storage Temperature.....-65°C to +150°C  
 Junction Temperature.....+150°C

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

## OPERATING RATINGS

Input Voltage ( $V_{IN}$ ).....+2.7V to +5.5V  
 Enable Input Voltage ( $V_{EN}$ ).....0 to 5.5V  
 Junction Temperature ( $T_J$ ).....-40°C to +125°C  
 Thermal Resistance, SOT-23-5 ( $\theta_{JA}$ ).....Note 1  
 Thermal Resistance, SOT-23-6 ( $\theta_{JA}$ ).....Note 1

Remark: The device is not guaranteed to function outside its operating rating.

## ELECTRICAL SPECIFICATIONS

Unless otherwise specified:  $V_{IN} = V_{OUT} + 0.5V$  to 6V,  $C_{OUT} = 2.2\mu F$  ceramic,  $C_{IN} = 2.2\mu F$ ,  $I_{OUT} = 100\mu A$ , -40°C <  $T < 125^\circ C$ . The ♦ denotes the specifications which apply over full operating temperature range -40°C to +125°C, unless otherwise specified.

PARAMETER	MIN	TYP	MAX	UNITS	♦	CONDITIONS
Input Voltage			6	V	♦	
Output Voltage Accuracy	-2		+2	%	♦	Variation from specified $V_{OUT}$
Output Voltage Temperature Coefficient, Note2		50		ppm/°C		$\Delta V_{OUT}/\Delta T$
Reference Voltage	1.225	1.25	1.275	V	♦	Adjustable version only
Line Regulation		0.04	0.3	%/V		$\Delta V_{OUT}$ ( $V_{IN}$ below 6V)
Load Regulation, Note 3		0.07 0.13	0.3 0.5	%		$I_{OUT} = 0.1mA$ to 300mA (SP6203) $I_{OUT} = 0.1mA$ to 500mA (SP6205)
Dropout Voltage for $V_{OUT} \geq 3.0V$ , Note 4		0.06 60 120 180 300	300 500	mV	♦ ♦	$I_{OUT} = 0.1mA$ $I_{OUT} = 100mA$ $I_{OUT} = 200mA$ $I_{OUT} = 300mA$ (SP6203) $I_{OUT} = 500mA$ (SP6205)
Ground Pin Current, Note 5		45 110 175 235 350	100 330 490	$\mu A$	♦ ♦ ♦	$I_{OUT} = 0.1mA$ (IQUIESCENT) $I_{OUT} = 100mA$ $I_{OUT} = 200mA$ $I_{OUT} = 300mA$ (SP6203) $I_{OUT} = 500mA$ (SP6205)
Shutdown Supply Current		0.01	1	$\mu A$	♦	$V_{EN} < 0.4V$ (shutdown)
Current Limit	0.33 0.55	0.50 0.85	0.8 1.4	A		$V_{OUT} = ZeroV$ (SP6203) $V_{OUT} = ZeroV$ (SP6205)
Thermal Shutdown Junction Temperature		170		°C		Regulator Turns off
Thermal Shutdown Hysteresis		12		°C		Regulator turns on again at 158°C
Power Supply Rejection Ratio		67		dB		$f \leq 1kHz$
Output Noise Voltage, Note 6		150 630 12 50	75	$\mu V_{RMS}$		$C_{BYP} = 0nF$ , $I_{OUT} = 0.1mA$ $C_{BYP} = 0nF$ , $I_{OUT} = 300mA$ $C_{BYP} = 10nF$ , $I_{OUT} = 0.1mA$ $C_{BYP} = 10nF$ , $I_{OUT} = 300mA$
Thermal Regulation, Note 7		0.05		%/W		$\Delta V_{OUT}/\Delta P_D$
Wake-Up Time ( $T_{WU}$ ), Note 8 (from shutdown mode)		25	50	$\mu s$		$V_{IN} \geq 4V$ , Note 10 $I_{OUT} = 30mA$
Turn-On Time ( $T_{ON}$ ), Note 9 (from shutdown mode)		60	120	$\mu s$		$V_{IN} \geq 4V$ , Note 10 $I_{OUT} = 30mA$
Turn-Off Time ( $T_{OFF}$ ),		100 15	250 25	$\mu s$		$I_{OUT} = 0.1mA$ , $V_{IN} \geq 4V$ , Note 10 $I_{OUT} = 300mA$ , $V_{IN} \geq 4V$ , Note 10
Output Discharge Resistance		30		$\Omega$		No Load
Enable Input Logic Low Voltage			0.4	V	♦	Regulator Shutdown
Enable Input Logic High Voltage	1.6			V	♦	Regulator Enabled

## ELECTRICAL SPECIFICATIONS NOTES

**Note 1:** Maximum power dissipation can be calculated using the formula:  $P_D = (T_{J(max)} - T_A) / \theta_{JA}$ , where  $T_{J(max)}$  is the junction temperature,  $T_A$  is the ambient temperature and  $\theta_{JA}$  is the junction-to-ambient thermal resistance.  $\theta_{JC}$  is  $6^\circ\text{C/W}$  for this package. Exceeding the maximum allowable power dissipation will result in excessive die temperature and the regulator will go into thermal shutdown mode.  $\theta_{JA}$  is  $191^\circ\text{C/W}$  for SOT-23-5, and is  $59^\circ\text{C/W}$  for the 8-pin DFN. A part mounted on a PC board will deliver improved thermal performance based upon copper surface area.

**Note 2:** Output voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

**Note 3:** Regulation is measured at constant junction temperature using low duty cycle pulse testing. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

**Note 4:** Dropout-voltage is defined as the input to output differential at which the output voltage drops 2% below its nominal value measured at 1V differential.

**Note 5:** Ground pin current is the regulator quiescent current. The total current drawn from the supply is the sum of the load current plus the ground pin current.

**Note 6:** Output noise voltage is defined within a certain bandwidth, namely  $10\text{Hz} < \text{BW} < 100\text{kHz}$ . An external bypass cap (10nF) from reference output (BYP pin) to ground significantly reduces noise at output.

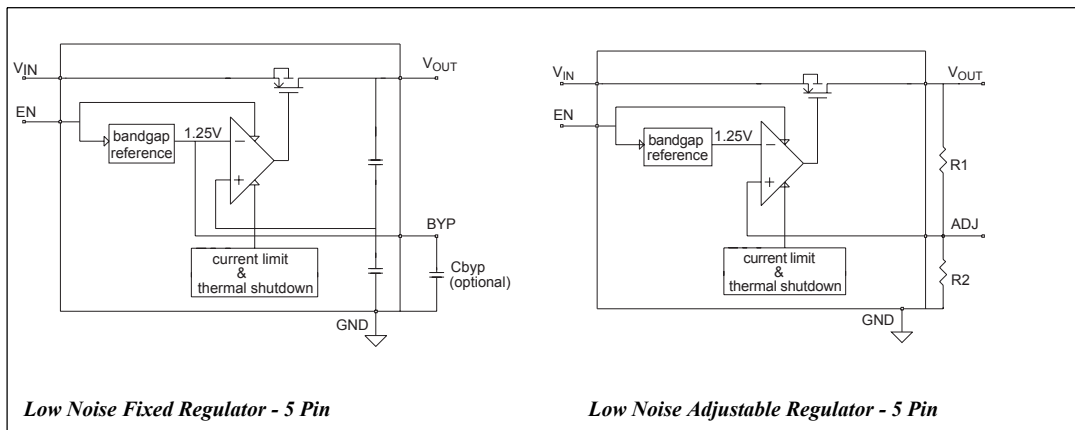
**Note 7:** Thermal regulation is defined as the change in output voltage at a time "t" after a change in power dissipation is applied, excluding load and line regulation effects. Specifications are for a 300mA load pulse at  $V_{IN} = 6\text{V}$  for  $t = 1\text{ms}$ .

**Note 8:** The wake-up time ( $T_{WU}$ ) is defined as the time it takes for the output to start rising after enable is brought high.

**Note 9:** The total turn-on time is called the settling time ( $T_S$ ), which is defined as the condition when both the output and the bypass node are within 2% of their fully enabled values when released from shutdown.

**Note 10:** For output voltage versions requiring  $V_{IN}$  to be lower than 4V, timing ( $T_{ON}$  &  $T_{OFF}$ ) increases slightly.

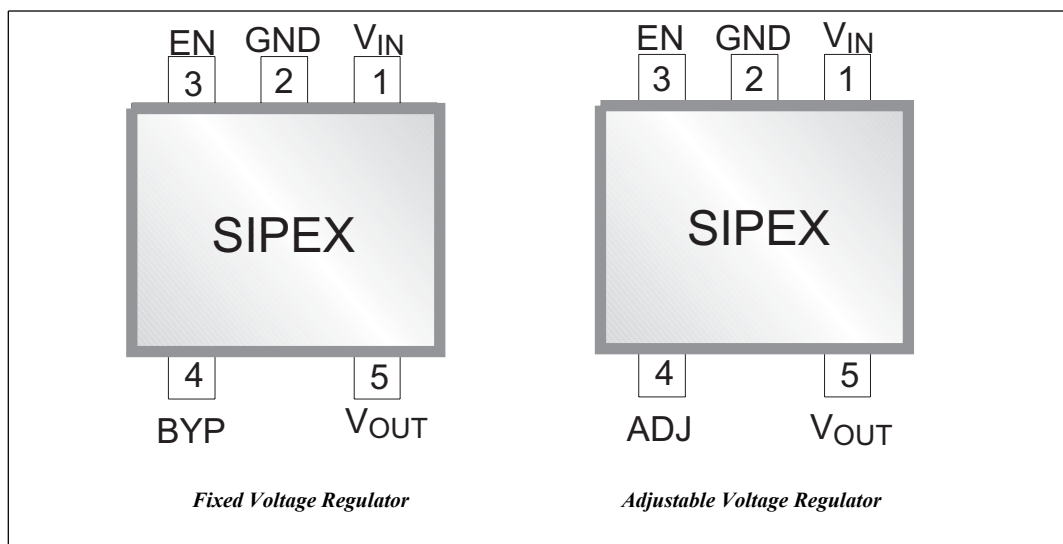
## FUNCTIONAL DIAGRAM



**5 PIN OPTION**

PIN NUMBER	NAME	FUNCTION
1	$V_{IN}$	Power Supply Input
2	GND	Ground Terminal
3	EN	Enable/Shutdown (Logic high = enable, logic low = shutdown)
4 (Fixed)	BYP	Reference bypass input for ultra-quiet operation. Connecting a 10nF cap on this pin reduces output noise.
4 (adj.)	ADJ	Adjustable (Input): Adjustable regulator feedback input. Connect to a resistive voltage-divider network.
5	$V_{OUT}$	Regulator Output Voltage

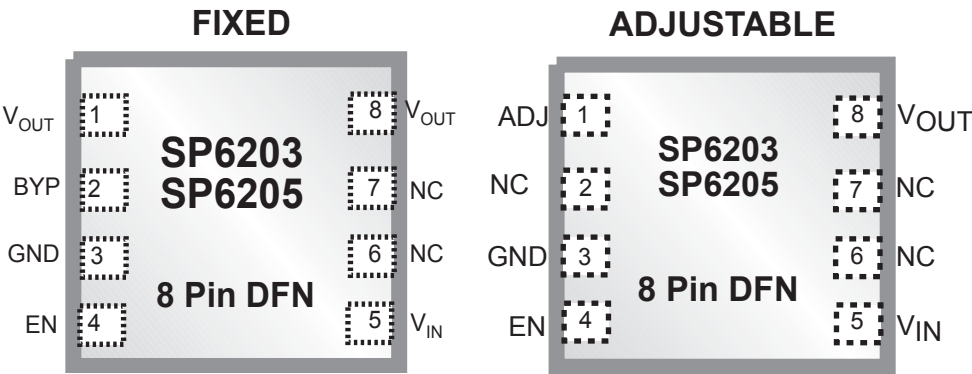
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**PINOUT 5 PIN SOT-23**


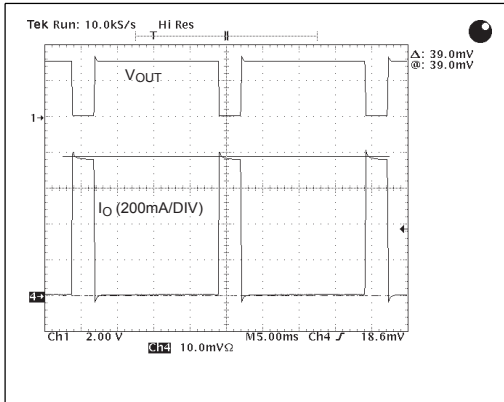
8 PIN OPTION

8 PIN DFN		PIN CONFIGURATION
PIN NUMBER	NAME	FUNCTION
1(fixed)	V <sub>OUT</sub>	Regulator Output Voltage. Connect to Pin 8 V <sub>OUT</sub> .
1(Adj)	ADJ	Adjustable (Input): Adjustable regulator feed-back input. Connect to a resistive voltage-divider network.
2(fixed)	BYP	Reference bypass input for ultra-quiet operation. Connecting a 10nF cap on this pin reduces output noise.
2(Adj)	NC	No Connect
3	GND	Ground
4	EN	Enable/Shutdown (Logic high = enable, logic low = shutdown)
5	V <sub>IN</sub>	Power Supply Input
6	NC	No Connect
7	NC	No Connect
8	V <sub>OUT</sub>	Regulator Output VoltageA

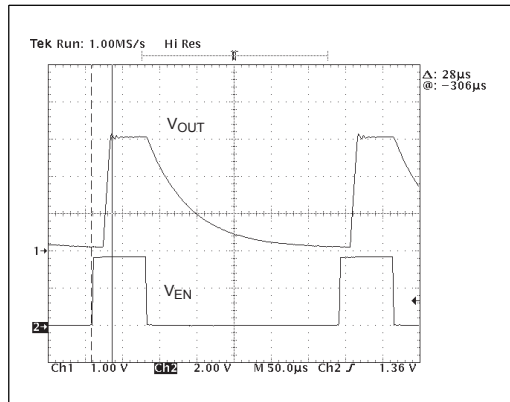
PINOUT 8 PIN DFN



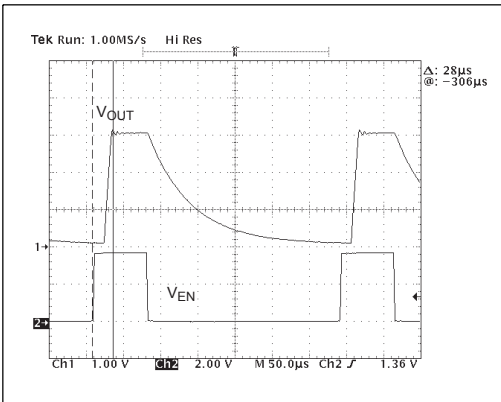
# TYPICAL PERFORMANCE CHARACTERISTICS



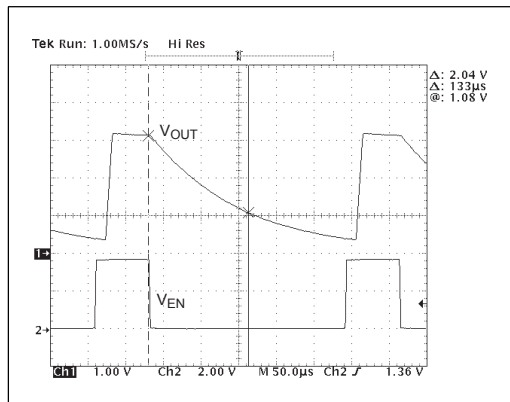
**Current Limit**



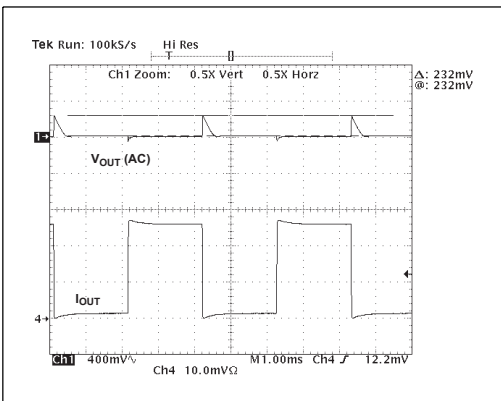
**Turn on Time,  $R_{LOAD} = 50\Omega$  (60mA)**



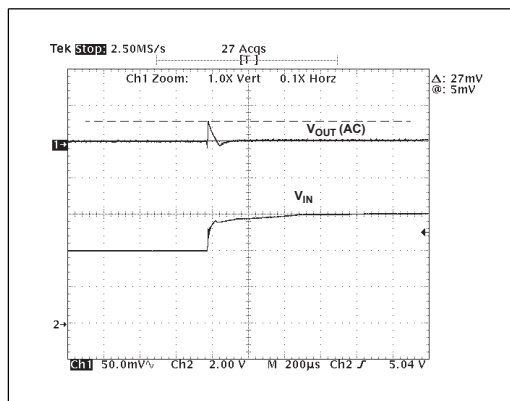
**Turn off Time,  $R_{LOAD} = 6\Omega$  (500mA)**



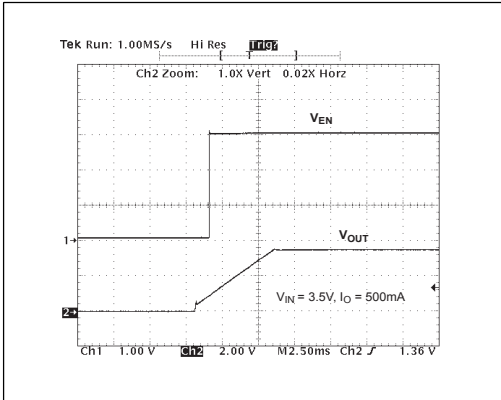
**Turn off Time,  $R_{LOAD} = 30K$  (0.1mA)**



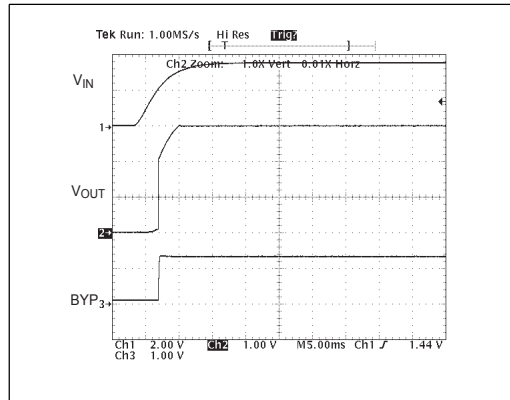
**Load Regulation,  $I_o = 100\mu A \sim 500mA$**



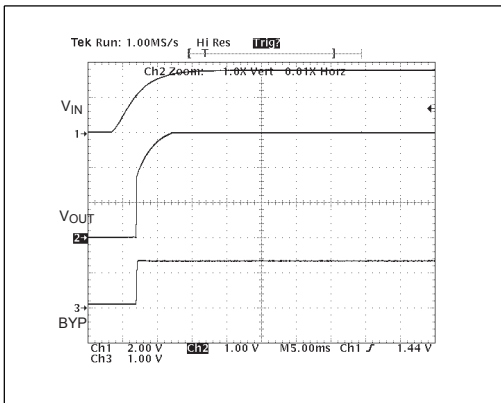
**Line Regulation, Line Step from 4V to 6V,  $I_o = 1mA$**



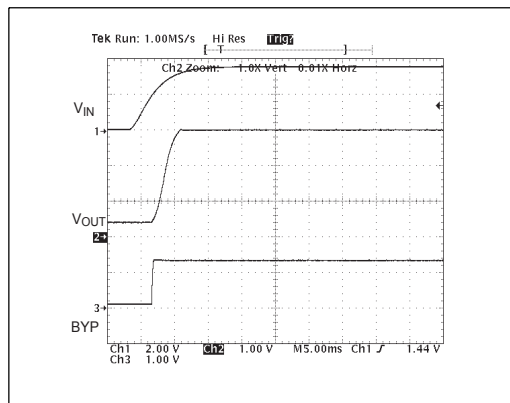
Start Up Waveform,  $V_{IN} = 3.5V$ ,  $I_O = 500mA$



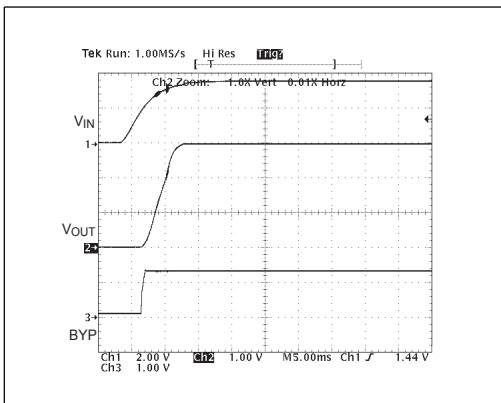
Start Up Waveform, Slow  $V_{IN}$ , No Load



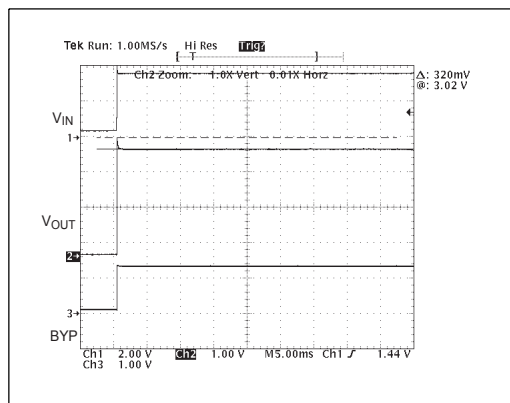
Start Up Waveform, Slow  $V_{IN}$ , 500mA Output Load



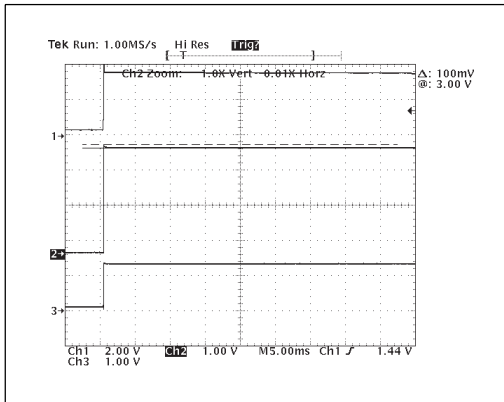
Start Up Waveform, Slow  $V_{IN}$ ,  $C_{OUT}=1000\mu F$ ,  $I_O=0mA$



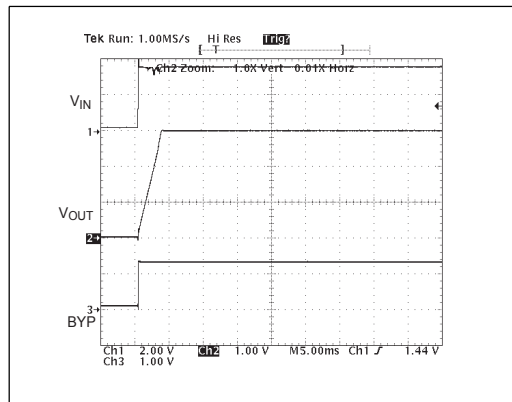
Start Up Waveform, Slow  $V_{IN}$ ,  $C_{OUT}=1000\mu F$ ,  $I_O=500mA$



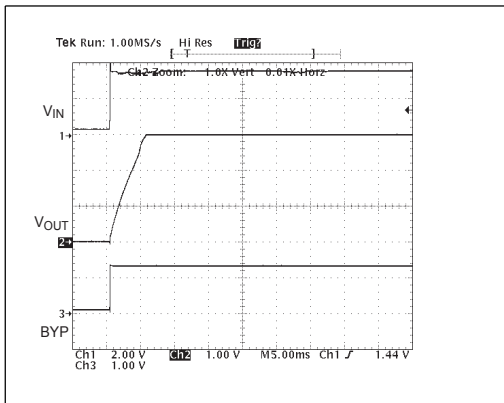
Fast  $V_{IN}$ , No Load



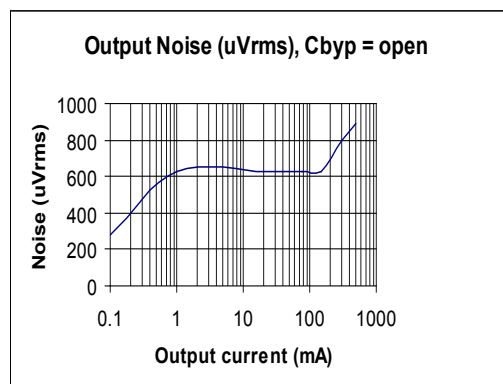
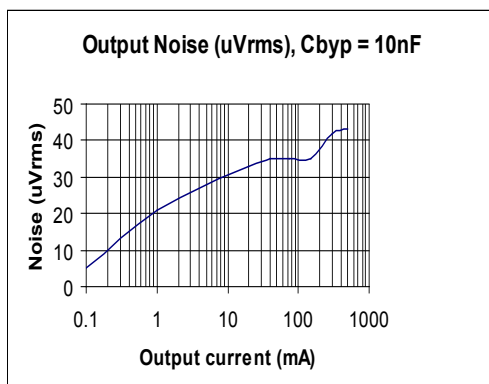
**Fast  $V_{IN}$ , 500mA Output Load**



**Fast  $V_{IN}$ , 1000μF Output Load**



**Fast  $V_{IN}$ ,  $C_{OUT}=1000\mu F$ ,  $I_O=500mA$**





## General Overview

The SP6203/6205 is intended for applications where very low dropout voltage, low supply current and low output noise are critical, even with high load conditions (500mA maximum). Unlike bipolar regulators, the SP6203/6205 (CMOS LDO) supply current increases only slightly with load current.

The SP6203/6205 contains an internal bandgap reference which is fed into the inverting input of the LDO-amplifier. The output voltage is then set by means of a resistor divider and compared to the bandgap reference voltage. The error LDO-amplifier drives the gate of a P-channel MOSFET pass device that has a  $R_{DS(ON)}$  of  $0.6\Omega$  at 500mA producing a 300mV drop at the output.

Furthermore, the SP6203/6205 has its own current limit circuitry (500mA/850mA) to ensure that the output current will not damage the device during output short, overload or start-up.

Also, the SP6203/6205 includes thermal shutdown circuitry to turn off the device when the junction temperature exceeds  $170^{\circ}\text{C}$  and it remains off until the temperature drops by  $12^{\circ}\text{C}$ .

## Enable/Shutdown Operation

The SP6203/6205 is turned off by pulling the  $V_{EN}$  pin below 0.4V and turned on by pulling it above 1.6V.

If this enable/shutdown feature is not required, it should be tied directly to the input supply voltage to keep the regulator output on at all time.

While in shutdown,  $V_{OUT}$  quickly falls to zero (turn-off time is dependent on load conditions and output capacitance on  $V_{OUT}$ ) and power consumption drops nearly to zero.

## Input Capacitor

A small capacitor of  $2.2\mu\text{F}$  is required from  $V_{IN}$  to GND if a battery is used as the power source. Any good quality electrolytic, ceramic or tantalum capacitor may be used at the input.

## Output Capacitor

An output capacitor is required between  $V_{OUT}$  and GND to prevent oscillation. A  $2.2\mu\text{F}$  output capacitor is recommended.

Larger values make the chip more stable which means an improvement of the regulator's transient response. Also, when operating from other sources than batteries, supply-noise rejection can be improved by increasing the value of the input and output capacitors and using passive filtering techniques.

For a lower output current, a smaller output capacitance can be chosen.

Finally, the output capacitor should have an effective series resistance (ESR) of  $0.5\Omega$  or less.

Therefore, the use of good quality ceramic or tantalum capacitors is advised.

## Bypass Capacitor

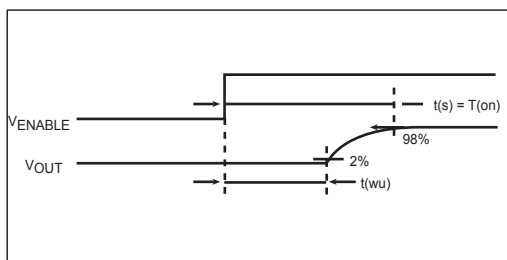
A bypass pin (BYP) is provided to decouple the bandgap reference. A  $10\text{nF}$  external capacitor connected from BYP to GND reduces noise present on the internal reference, which in turn significantly reduces output noise and also improves power supply rejection. Note that the minimum value of  $C_{OUT}$  must be increased to maintain stability when the bypass capacitor is used because  $C_{BYP}$  reduces the regulator phase margin. If output noise is not a concern, this input may be left unconnected. Larger capacitor values may be used to further improve power supply rejection, but result in a longer time period (slower turn on) to settle output voltage when power is initially applied.

## No Load Stability

The SP6203/6205 will remain stable and in regulation with no external load (other than the internal voltage driver) unlike many other voltage regulators. This is especially important in CMOS RAM battery back-up applications.

## Turn On Time

The turn on response is split up in two separate response categories: the wake up time ( $T_{WU}$ ) and the settling time ( $T_S$ ). The wake up time is defined as the time it takes for the output to rise to 2% of its total value after being released from shutdown ( $E_N > 0.4V$ ). The settling time is defined as the condition where the output reaches 98% of its total value after being released from shutdown. The latter is also called the turn on time and is dependent on the output capacitor, a little bit on load and, if present, on a bypass capacitor.



## Turn Off Time

The turn off time is defined as the condition where the output voltage drops about 66% ( $\theta$ ) of its total value.  $5\theta$  to  $7\theta$  is the constant where the output voltage drops nearly to zero. There will always be a small voltage drop in shutdown because of the switch unless we short-circuit it. The turn off time of the output voltage is dependent on load conditions, output capacitance on  $V_{OUT}$  (time constant  $\tau = R_L C_L$ ) and also on the difference in voltage between input and output.

## Thermal Considerations

The SP6203/6205 is designed to provide 300/500 mA of continuous current in a tiny package. Maximum power dissipation can be calculated based on the output current and the voltage drop across the part. To determine the maximum power dissipation of the package, use the junction-to-ambient thermal resistance of the device and the following basic equation:

$$P_D = (T_{J(max)} - T_A) / \theta_{JA}$$

$T_{J(max)}$  is the maximum junction temperature of the die and is 125°C.  $T_A$  is the ambient temperature.  $\theta_{JA}$  is the junction-to-ambient thermal resistance for the regulator and is layout dependent. The SOT-23-5 package has a  $\theta_{JA}$  of approximately 256°C/W for minimum PCB copper footprint area.

This results in a maximum power dissipation of:

$$P_{D(max)} = [(125^\circ\text{C} - 25^\circ\text{C}) / (191^\circ\text{C/W})] = 523\text{mW}$$

The actual power dissipation of the regulator circuit can be determined using one simple equation:

$$P_D = (V_{IN} - V_{OUT}) * I_{OUT} + V_{IN} * I_{GND}$$

To prevent the device from entering thermal shutdown, maximum power dissipation can not be exceeded.

Substituting  $P_{D(max)}$  for  $P_D$  and solving for the operating conditions that are critical to the application will give the maximum operating conditions for the regulator circuit. For example, if we are operating the SP6203 3.0V at room temperature, with a minimum footprint layout and an output current of 300mA, the maximum input voltage can be determined, based on the equation below. Ground pin current can be taken from the electrical specifications table (0.23mA at 300mA).

$$390\text{mW} = (V_{IN} - 3.0V) * 300\text{mA} + V_{IN} * 0.23\text{mA}$$

After calculations, we find that the maximum input voltage of a 3.0V application at 300mA of output current in a SOT-23-5 package is 4.7V.

So if the intent is to operate a 5V output version from a 6V supply at 300mA load and at a 25°C ambient temperature, then the actual total power dissipation will be:

$$P_D = [(6V - 5V) * [300\text{mA}]] + (6V * 0.23\text{mA}) = 301.4\text{mW}$$

This is well below the 523mW package maximum. Therefore, the regulator can be used.

Note that the regulator cannot always be used at its maximum current rating. For example, in a 5V input to 3.0V output application at an ambient temperature of 25°C and operating at the full 500mA ( $I_{GND} = 0.355\text{mA}$ ) load, the regulator is limited to a much lower load current, determined by the following equation:

$$523\text{mW} = ([5\text{V}-3\text{V}] * [I_{\text{load(max)}}]) + (5\text{V} * 0.350\text{mA})$$

After calculation, we find that in such an application (SP6205) the regulator is limited to 260.6mA. Doing the same calculations for the 300mA LDO (SP6203) will limit the regulator's output current to 260.9mA.

Also, taking advantage of the very low dropout voltage characteristics of the SP6203/6205, power dissipation can be reduced by using the lowest possible input voltage to minimize the input-to-output drop.

### **Adjustable Regulator Applications**

The SP6203/6205 can be adjusted to a specific output voltage by using two external resistors (see functional diagram). The resistors set the output voltage based on the following equation:

$$V_{\text{OUT}} = V_{\text{REF}} * (R1/R2 + 1)$$

Resistor values are not critical because ADJ (adjust) has a high input impedance, but for best performance use resistors of 470K $\Omega$  or less. A bypass capacitor from ADJ to  $V_{\text{OUT}}$  provides improved noise performance.

### **Dual-Supply Operation**

When used in dual supply systems where the regulator load is returned to a negative supply, the output voltage must be diode clamped to ground.

### **Layout Considerations**

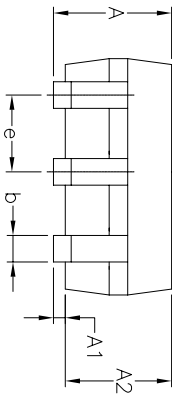
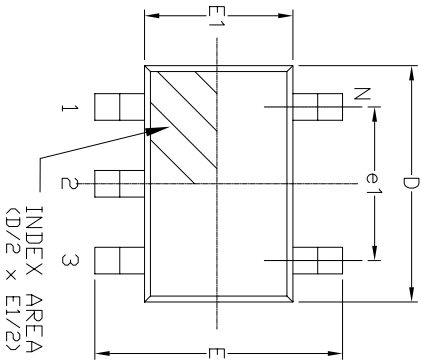
The primary path of heat conduction out of the package is via the package leads. Therefore, careful considerations have to be taken into account:

- 1) Attaching the part to a larger copper footprint will enable better heat transfer from the device, especially on PCB's where there are internal ground and power planes.
- 2) Place the input, output and bypass capacitors close to the device for optimal transient response and device behavior.
- 3) Connect all ground connections directly to the ground plane. In case there's no ground plane, connect to a common local ground point before connecting to board ground.

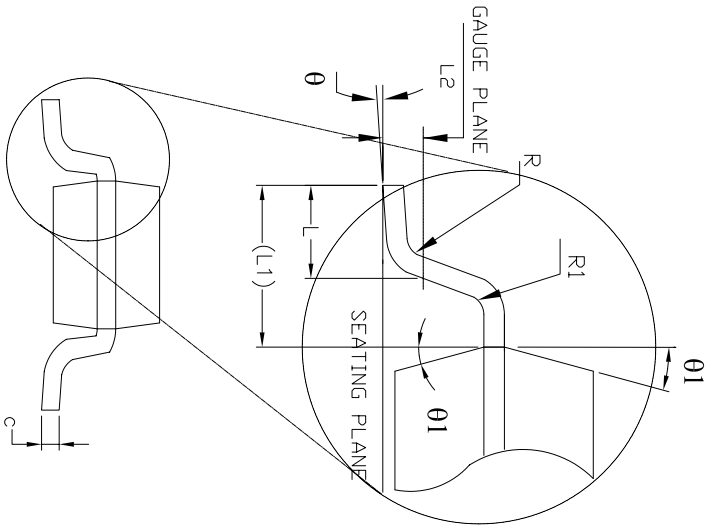
Such layouts will provide a much better thermal conductivity (lower  $\theta_{JA}$ ) for, a higher maximum allowable power dissipation limit.

REVISION HISTORY				
REV.	DESCRIPTION	DATE	APP'D	
A	DRAWING ORIGINATION	10/3/05	JL	
B	DRAWING FORMAT MODIFICATION	07/25/06	JL	

Top View



Side View



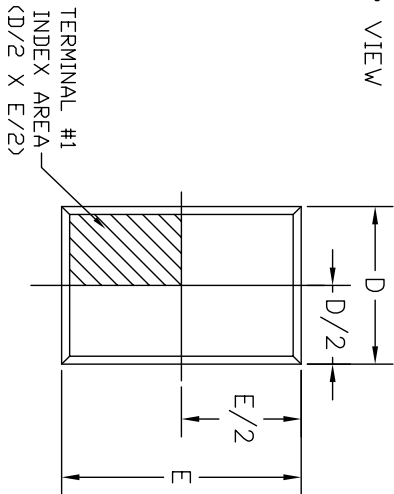
Front View

5 Pin SOT-23 JEDEC MO-178 Variation AA									
SYMBOLS	DIMENSIONS IN MM (Control Unit)				DIMENSIONS IN INCH (Reference Unit)				
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.45	—	—	0.057	—	—	—
A1	0.00	—	0.15	0.000	—	0.006	—	—	—
A2	0.90	1.15	1.30	0.036	0.045	0.051	—	—	—
b	0.30	—	0.50	0.012	—	0.020	—	—	—
c	0.08	—	0.22	0.003	—	0.009	—	—	—
D	2.90 BSC				0.115 BSC				—
E	2.80 BSC				0.111 BSC				—
E1	1.60 BSC				0.063 BSC				—
e	0.95 BSC				0.038 BSC				—
e1	1.90 BSC				0.075 BSC				—
L	0.30	0.45	0.60	0.012	0.018	0.024	—	—	—
L1	0.60 REF				0.024 REF				—
L2	0.25 BSC				0.010 BSC				—
R	0.10	—	—	0.004	—	—	—	—	—
R1	0.10	—	0.25	0.004	—	0.010	—	—	—
theta	0°	4°	8°	0°	4°	8°	—	—	—
theta1	5°	10°	15°	5°	10°	15°	—	—	—
N	5				5				—

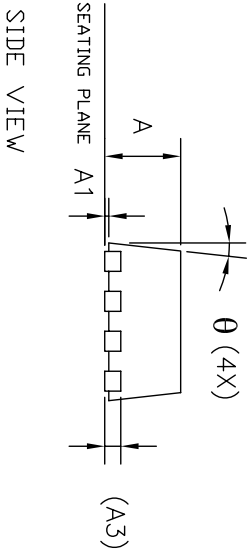
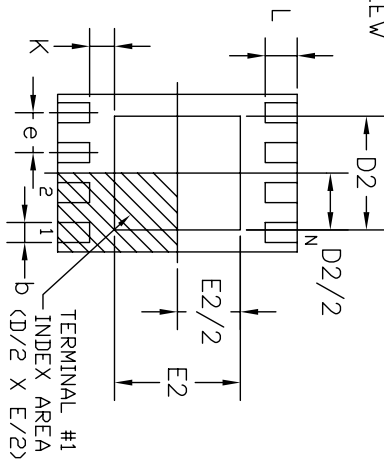
SIPLEX CORPORATION				
		5 PIN SOT-23 PACKAGE OUTLINE		
Packaging Approval:	Drawing No:	5-PIN SOT-23		
By: JL	Date: 07/25/06	Revision: B	Sheet: 1	OF 1

REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	08/18/05	JL
B	MODIFY DRAWING FORMAT	07/17/06	JL

TOP VIEW



BOTTOM VIEW



8LD 2x3 DFN JEDEC MO-229 Variation VCE0-2									
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)					
	MIN	NOM	MAX	MIN	NOM	MAX			
A	0.80	0.90	1.00	0.032	0.036	0.039			
A1	0.00	0.02	0.05	0.000	0.001	0.002			
A3	0.20 REF			0.008 REF					
b	0.18	0.25	0.30	0.007	0.010	0.012			
D	2.00 BSC			0.079 BSC					
D2	1.50	—	1.75	0.059	—	0.069			
E	3.00 BSC			0.118 BSC					
E2	1.60	—	1.90	0.063	—	0.075			
e	0.50 BSC			0.020 BSC					
L	0.30	0.40	0.50	0.012	0.016	0.020			
K	0.20	—	—	0.008	—	—			
theta	0°	—	14°	0°	—	14°			
N	8			8					
ND	4			4					



**SIPEX CORPORATION**

8 PIN 2x3 DFN PACKAGE OUTLINE

Packaging Approval:

Drawing No: 8-PIN 2x3 DFN

By: JL Date: 07/17/06

Revision: B

Sheet: 1 OF 1

Part Number	Top Marking	Temperature Range	Voltage Option	Package Type
SP6203EM5-1-8	N2WW	-40°C to +125°C	2.5V	5 Pin SOT-23
SP6203EM5-1-8/TR	N2WW	-40°C to +125°C	2.5V	5 Pin SOT-23
SP6203EM5-2-5	L2WW	-40°C to +125°C	2.5V	5 Pin SOT-23
SP6203EM5-2-5/TR	L2WW	-40°C to +125°C	2.5V	5 Pin SOT-23
SP6203EM5-2-7	G2WW	-40°C to +125°C	2.7V	5 Pin SOT-23
SP6203EM5-2-7/TR	G2WW	-40°C to +125°C	2.7V	5 Pin SOT-23
SP6203EM5-2-8	Q3WW	-40°C to +125°C	2.8V	5 Pin SOT-23
SP6203EM5-2-8/TR	Q3WW	-40°C to +125°C	2.8V	5 Pin SOT-23
SP6203EM5-2-85	H2WW	-40°C to +125°C	2.85V	5 Pin SOT-23
SP6203EM5-2-85/TR	H2WW	-40°C to +125°C	2.85V	5 Pin SOT-23
SP6203EM5-3-0	M2WW	-40°C to +125°C	3.0V	5 Pin SOT-23
SP6203EM5-3-0/TR	M2WW	-40°C to +125°C	3.0V	5 Pin SOT-23
SP6203EM5-3-3	J2WW	-40°C to +125°C	3.3V	5 Pin SOT-23
SP6203EM5-3-3/TR	J2WW	-40°C to +125°C	3.3V	5 Pin SOT-23
SP6203EM5	Q2WW	-40°C to +125°C	ADJ	5 Pin SOT-23
SP6203EM5 /TR	Q2WW	-40°C to +125°C	ADJ	5 Pin SOT-23
SP6203ER-1-8	620318YWW	-40°C to +125°C	2.5V	8 Pin DFN
SP6203ER-1-8/TR	620318YWW	-40°C to +125°C	2.5V	8 Pin DFN
SP6203ER-2-5	620325YWW	-40°C to +125°C	2.5V	8 Pin DFN
SP6203ER-2-5/TR	620325YWW	-40°C to +125°C	2.5V	8 Pin DFN
SP6203ER-2-7	620327YWW	-40°C to +125°C	2.7V	8 Pin DFN
SP6203ER-2-7/TR	620327YWW	-40°C to +125°C	2.7V	8 Pin DFN
SP6203ER-2-8	620328YWW	-40°C to +125°C	2.8V	8 Pin DFN
SP6203ER-2-8/TR	620328YWW	-40°C to +125°C	2.8V	8 Pin DFN
SP6203ER-2-85	620385YWW	-40°C to +125°C	2.85V	8 Pin DFN
SP6203ER-2-85/TR	620385YWW	-40°C to +125°C	2.85V	8 Pin DFN
SP6203ER-3-0	620330YWW	-40°C to +125°C	3.0V	8 Pin DFN
SP6203ER-3-0/TR	620330YWW	-40°C to +125°C	3.0V	8 Pin DFN
SP6203ER-3-3	620333YWW	-40°C to +125°C	3.3V	8 Pin DFN
SP6203ER-3-3/TR	620333YWW	-40°C to +125°C	3.3V	8 Pin DFN
SP6203ER	6203ERYWW	-40°C to +125°C	ADJ	8 Pin DFN
SP6203ER /TR	6203ERYWW	-40°C to +125°C	ADJ	8 Pin DFN

Available in lead free packaging. To order add "-L" suffix to part number.  
Example: SP6203ER-ADJ/TR = standard; SP6203ER-L-ADJ/TR = lead free.

/TR = Tape and Reel.

Pack quantity is 2,500 for SOT-23 and 3,000 for DFN.

TOP MARKING note: "WW" for SOT-23 package is datecode Work Week. "YWW" for DFN package is datecode Year & Work Week. Lead Free SOT-23 packages can be identified by a Bar "|" to the left of the standard Top Marking. Lead Free DFN packages can be identified by a Bar "—" under the standard Top Marking.

Part Number	Top Marking	Temperature Range	Voltage Option	Package Type
SP6205EM5-1-8	X2WW	-40°C to +125°C	2.5V	5 Pin SOT-23
SP6205EM5-1-8/TR	X2WW	-40°C to +125°C	2.5V	5 Pin SOT-23
SP6205EM5-2-5	V2WW	-40°C to +125°C	2.5V	5 Pin SOT-23
SP6205EM5-2-5/TR	V2WW	-40°C to +125°C	2.5V	5 Pin SOT-23
SP6205EM5-2-7	R2WW	-40°C to +125°C	2.7V	5 Pin SOT-23
SP6205EM5-2-7/TR	R2WW	-40°C to +125°C	2.7V	5 Pin SOT-23
SP6205EM5-2-8	E3WW	-40°C to +125°C	2.8V	5 Pin SOT-23
SP6205EM5-2-8/TR	E3WW	-40°C to +125°C	2.8V	5 Pin SOT-23
SP6205EM5-2-85	S2WW	-40°C to +125°C	2.85V	5 Pin SOT-23
SP6205EM5-2-85/TR	S2WW	-40°C to +125°C	2.85V	5 Pin SOT-23
SP6205EM5-3-0	W2WW	-40°C to +125°C	3.0V	5 Pin SOT-23
SP6205EM5-3-0/TR	W2WW	-40°C to +125°C	3.0V	5 Pin SOT-23
SP6205EM5-3-3	T2WW	-40°C to +125°C	3.3V	5 Pin SOT-23
SP6205EM5-3-3/TR	T2WW	-40°C to +125°C	3.3V	5 Pin SOT-23
SP6205EM5	A3WW	-40°C to +125°C	ADJ	5 Pin SOT-23
SP6205EM5 /TR	A3WW	-40°C to +125°C	ADJ	5 Pin SOT-23

SP6205ER-1-8	520518YWW	-40°C to +125°C	2.5V	8 Pin DFN
SP6205ER-1-8/TR	520518YWW	-40°C to +125°C	2.5V	8 Pin DFN
SP6205ER-2-5	520525YWW	-40°C to +125°C	2.5V	8 Pin DFN
SP6205ER-2-5/TR	520525YWW	-40°C to +125°C	2.5V	8 Pin DFN
SP6205ER-2-7	520527YWW	-40°C to +125°C	2.7V	8 Pin DFN
SP6205ER-2-7/TR	520527YWW	-40°C to +125°C	2.7V	8 Pin DFN
SP6205ER-2-8	520528YWW	-40°C to +125°C	2.8V	8 Pin DFN
SP6205ER-2-8/TR	520528YWW	-40°C to +125°C	2.8V	8 Pin DFN
SP6205ER-2-85	520585YWW	-40°C to +125°C	2.85V	8 Pin DFN
SP6205ER-2-85/TR	520585YWW	-40°C to +125°C	2.85V	8 Pin DFN
SP6205ER-3-0	520530YWW	-40°C to +125°C	3.0V	8 Pin DFN
SP6205ER-3-0/TR	520530YWW	-40°C to +125°C	3.0V	8 Pin DFN
SP6205ER-3-3	520533YWW	-40°C to +125°C	3.3V	8 Pin DFN
SP6205ER-3-3/TR	520533YWW	-40°C to +125°C	3.3V	8 Pin DFN
SP6205ER	5205ERYWW	-40°C to +125°C	ADJ	8 Pin DFN
SP6205ER /TR	5205ERYWW	-40°C to +125°C	ADJ	8 Pin DFN

Available in lead free packaging. To order add "-L" suffix to part number.  
Example: SP6205ER-ADJ/TR = standard; SP6205ER-L-ADJ/TR = lead free.

/TR = Tape and Reel.

Pack quantity is 2,500 for SOT-23 and 3,000 for DFN.

TOP MARKING note: "WW" for SOT-23 package is datecode Work Week. "YWW for DFN package is datecode Year & Work Week. Lead Free SOT-23 packages can be identified by a Bar "|" to the left of the standard Top Marking. Lead Free DFN packages can be identified by a Bar "-" under the standard Top Marking.



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