

FEATURES

- Single 18-bit DAC, ± 0.5 LSB INL
- 7.5 nV/ $\sqrt{\text{Hz}}$ noise spectral density
- 0.05 LSB long-term linearity stability
- <0.05 ppm/ $^{\circ}\text{C}$ temperature drift
- 1 μs settling time
- 1.4 nV-sec glitch impulse
- 20-lead TSSOP package
- Wide power supply range of up to ± 16.5 V
- 35 MHz Schmitt triggered digital interface
- 1.8 V compatible digital interface
- Extended automotive operating temperature range -55°C to $+125^{\circ}\text{C}$

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range (-55°C to $+125^{\circ}\text{C}$)
- Controlled manufacturing baseline
- One assembly/test site
- One fabrication site
- Enhanced product change notification
- Qualification data available on request

APPLICATIONS

- Medical instrumentation
- Test and measurement
- Industrial control
- Scientific and aerospace instrumentation
- Data acquisition systems
- Digital gain and offset adjustment
- Power supply control

GENERAL DESCRIPTION

The **AD5781-EP**¹ is a single 18-bit, unbuffered voltage output DAC that operates from a bipolar supply of up to 33 V. The **AD5781-EP** accepts a positive reference input range of 5 V to $V_{DD} - 2.5$ V and a negative reference input range of $V_{SS} + 2.5$ V to 0 V. The **AD5781-EP** offers a relative accuracy specification of ± 0.5 LSB maximum, and operation is guaranteed monotonic with a ± 0.5 LSB DNL maximum specification.

The part uses a versatile 3-wire serial interface that operates at clock rates of up to 35 MHz and is compatible with standard SPI, QSPI™, MICROWIRE™, and DSP interface standards. The part incorporates a power-on reset circuit that ensures that the DAC output powers up to 0 V and in a known output impedance

¹ Protected by U.S. Patent No. 8,089,380, and other patents are pending.

Rev. A

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FUNCTIONAL BLOCK DIAGRAM

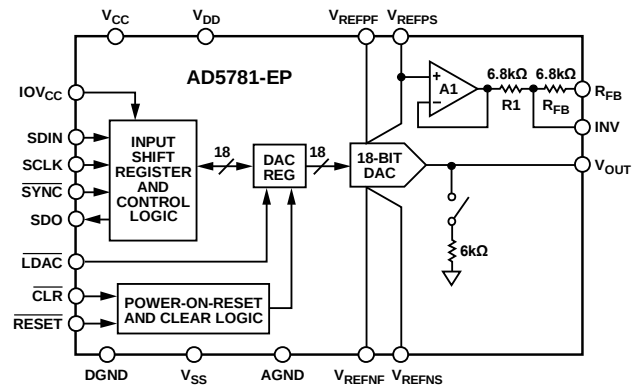


Figure 1.

COMPANION PRODUCTS

Ultra precision op amps: **AD8675**, **AD8676**

High voltage op amp: **ADA4898-1**

Additional companion products on the [AD5781 product page](#)

Table 1. Related Devices

Part No.	Description
AD5791	20-bit, 1 ppm accurate DAC
AD5541A/AD5542A	16-bit, 1 LSB accurate 5 V DAC

state and remains in this state until a valid write to the device takes place.

The part provides an output clamp feature that places the output in a defined load state.

The **AD5781-EP** is available in a compact, 20-lead TSSOP package and operates at the extended automotive temperature range of -55°C to $+125^{\circ}\text{C}$. Additional application and technical information can be found in the **AD5781** data sheet.

PRODUCT HIGHLIGHTS

- True 18-Bit Accuracy.
- Wide Power Supply Range of Up to ± 16.5 V.
- -55°C to $+125^{\circ}\text{C}$ Operating Temperature Range.
- Low 7.5 nV/ $\sqrt{\text{Hz}}$ Noise.
- Low 0.05 ppm/ $^{\circ}\text{C}$ Temperature Drift.

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REVISION HISTORY

7/13—Rev. 0 to Rev. A	
Changes to t ₁ Test Conditions/Comments and Endnote 2	5
Deleted Figure 4.....	7
2/12—Revision 0: Initial Version	

SPECIFICATIONS

$V_{DD} = +12.5\text{ V to }+16.5\text{ V}$, $V_{SS} = -16.5\text{ V to }-12.5\text{ V}$, $V_{REFP} = +10\text{ V}$, $V_{REFN} = -10\text{ V}$, $V_{CC} = +2.7\text{ V to }+5.5\text{ V}$, $IOV_{CC} = +1.71\text{ V to }+5.5\text{ V}$, $R_L = \text{unloaded}$, $C_L = \text{unloaded}$, T_{MIN} to T_{MAX} , unless otherwise noted.

Table 2.

Parameter ¹	Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE ²					
Resolution	18			Bits	
Integral Nonlinearity Error (Relative Accuracy)	-0.5	±0.25	+0.5	LSB	$V_{REFP} = +10\text{ V}$, $V_{REFN} = -10\text{ V}$
Differential Nonlinearity Error	-0.5	±0.25	+0.5	LSB	$V_{REFP} = +10\text{ V}$, $V_{REFN} = 0\text{ V}^3$
	-1	±0.5	+1	LSB	$V_{REFP} = +5\text{ V}$, $V_{REFN} = 0\text{ V}^3$
	-0.5	±0.25	+0.5	LSB	$V_{REFP} = +10\text{ V}$, $V_{REFN} = -10\text{ V}$
	-0.5	±0.25	+0.5	LSB	$V_{REFP} = +10\text{ V}$, $V_{REFN} = 0\text{ V}$
Linearity Error Long-Term Stability ⁴	-1	±0.5	+1	LSB	$V_{REFP} = +5\text{ V}$, $V_{REFN} = 0\text{ V}$
		0.04		LSB	After 500 hours at $T_A = 125^\circ\text{C}$
		0.05		LSB	After 1000 hours at $T_A = 125^\circ\text{C}$
		0.03		LSB	After 1000 hours at $T_A = 100^\circ\text{C}$
Full-Scale Error	-1.75	±0.25	+1.75	LSB	$V_{REFP} = +10\text{ V}$, $V_{REFN} = -10\text{ V}^3$
	-2.75	±0.062	+2.75	LSB	$V_{REFP} = +10\text{ V}$, $V_{REFN} = 0\text{ V}^3$
	-5.25	±0.2	+5.25	LSB	$V_{REFP} = +5\text{ V}$, $V_{REFN} = 0\text{ V}^3$
	-1	±0.25	+1	LSB	$V_{REFP} = +10\text{ V}$, $V_{REFN} = -10\text{ V}^3$, $T_A = 0^\circ\text{C to }105^\circ\text{C}$
Full-Scale Error Temperature Coefficient	-1	±0.062	+1	LSB	$V_{REFP} = 10\text{ V}$, $V_{REFN} = 0\text{ V}^3$, $T_A = 0^\circ\text{C to }105^\circ\text{C}$
	-1.5	±0.2	+1.5	LSB	$V_{REFP} = 5\text{ V}$, $V_{REFN} = 0\text{ V}^3$, $T_A = 0^\circ\text{C to }105^\circ\text{C}$
		±0.02		ppm FSR/ $^\circ\text{C}$	
				LSB	$V_{REFP} = +10\text{ V}$, $V_{REFN} = -10\text{ V}^3$
Zero-Scale Error	-1.75	±0.025	+1.75	LSB	$V_{REFP} = +10\text{ V}$, $V_{REFN} = 0\text{ V}^3$
	-2.5	±0.38	+2.5	LSB	$V_{REFP} = +5\text{ V}$, $V_{REFN} = 0\text{ V}^3$
	-5.25	±0.19	+5.25	LSB	$V_{REFP} = +10\text{ V}$, $V_{REFN} = -10\text{ V}^3$, $T_A = 0^\circ\text{C to }105^\circ\text{C}$
	-1	±0.025	+1	LSB	$V_{REFP} = 10\text{ V}$, $V_{REFN} = 0\text{ V}^3$, $T_A = 0^\circ\text{C to }105^\circ\text{C}$
Zero-Scale Error Temperature Coefficient ³	-1	±0.38	+1	LSB	$V_{REFP} = 10\text{ V}$, $V_{REFN} = 0\text{ V}^3$, $T_A = 0^\circ\text{C to }105^\circ\text{C}$
	-1.5	±0.19	+1.5	LSB	$V_{REFP} = 5\text{ V}$, $V_{REFN} = 0\text{ V}^3$, $T_A = 0^\circ\text{C to }105^\circ\text{C}$
		±0.04		ppm FSR/ $^\circ\text{C}$	
				ppm FSR	$V_{REFP} = +10\text{ V}$, $V_{REFN} = -10\text{ V}^3$
Gain Error	-6	±0.3	+6	ppm FSR	$V_{REFP} = +10\text{ V}$, $V_{REFN} = 0\text{ V}^3$
	-10	±0.4	+10	ppm FSR	$V_{REFP} = +5\text{ V}$, $V_{REFN} = 0\text{ V}^3$
	-20	±0.4	+20	ppm FSR	$V_{REFP} = +10\text{ V}$, $V_{REFN} = -10\text{ V}^3$, $T_A = 0^\circ\text{C to }105^\circ\text{C}$
Gain Error Temperature Coefficient ³		±0.04		ppm FSR/ $^\circ\text{C}$	
R_1 , R_{FB} Matching		0.01		%	
OUTPUT CHARACTERISTICS ³					
Output Voltage Range	V_{REFN}		V_{REFP}	V	
Output Slew Rate		50		V/ μs	Unbuffered output, $10\text{ M}\Omega 20\text{ pF}$ load
Output Voltage Settling Time		1		μs	10 V step to 0.02%, using AD845 buffer in unity-gain mode
Output Noise Spectral Density		1		μs	125 code step to $\pm 1\text{ LSB}^5$
		7.5		nV/ $\sqrt{\text{Hz}}$	At 1 kHz, DAC code = midscale
		7.5		nV/ $\sqrt{\text{Hz}}$	At 10 kHz, DAC code = midscale
		7.5		nV/ $\sqrt{\text{Hz}}$	At 100 kHz, DAC code = midscale
Output Voltage Noise		1.1		$\mu\text{V p-p}$	DAC code = midscale, 0.1 Hz to 10 Hz bandwidth ⁶

Parameter ¹	Min	Typ	Max	Unit	Test Conditions/Comments
Midscale Glitch Impulse ⁷		3.1		nV-sec	$V_{REFP} = +10\text{ V}$, $V_{REFN} = -10\text{ V}$
		1.7		nV-sec	$V_{REFP} = +10\text{ V}$, $V_{REFN} = 0\text{ V}$
		1.4		nV-sec	$V_{REFP} = +5\text{ V}$, $V_{REFN} = 0\text{ V}$
MSB Segment Glitch Impulse ⁷		9.1		nV-sec	$V_{REFP} = +10\text{ V}$, $V_{REFN} = -10\text{ V}$, see Figure 42
		3.6		nV-sec	$V_{REFP} = 10\text{ V}$, $V_{REFN} = 0\text{ V}$, see Figure 43
		1.9		nV-sec	$V_{REFP} = 5\text{ V}$, $V_{REFN} = 0\text{ V}$, see Figure 44
Output Enabled Glitch Impulse		45		nV-sec	On removal of output ground clamp
Digital Feedthrough		0.4		nV-sec	
DC Output Impedance (Normal Mode)		3.4		k Ω	
DC Output Impedance (Output Clamped to Ground)		6		k Ω	
Spurious Free Dynamic Range		100		dB	1 kHz tone, 10 kHz sample rate
Total Harmonic Distortion		97		dB	1 kHz tone, 10 kHz sample rate
REFERENCE INPUTS ³					
V_{REFP} Input Range	5		$V_{DD} - 2.5\text{ V}$	V	
V_{REFN} Input Range	$V_{SS} + 2.5\text{ V}$		0	V	
DC Input Impedance	5	6.6		k Ω	V_{REFP} , V_{REFN} , code dependent, typical at mid-scale code
Input Capacitance		15		pF	V_{REFP} , V_{REFN}
LOGIC INPUTS ³					
Input Current ⁸	-1		+1	μA	
Input Low Voltage, V_{IL}			$0.3 \times IOV_{CC}$	V	$IOV_{CC} = 1.71\text{ V}$ to 5.5 V
Input High Voltage, V_{IH}	$0.7 \times IOV_{CC}$			V	$IOV_{CC} = 1.71\text{ V}$ to 5.5 V
Pin Capacitance		5		pF	
LOGIC OUTPUT (SDO) ³					
Output Low Voltage, V_{OL}			0.4	V	$IOV_{CC} = 1.71\text{ V}$ to 5.5 V , sinking 1 mA
Output High Voltage, V_{OH}	$IOV_{CC} - 0.5\text{ V}$			V	$IOV_{CC} = 1.71\text{ V}$ to 5.5 V , sourcing 1 mA
High Impedance Leakage Current			± 1	μA	
High Impedance Output Capacitance		3		pF	
POWER REQUIREMENTS					
V_{DD}	7.5		$V_{SS} + 33$	V	All digital inputs at DGND or IOV_{CC}
V_{SS}	$V_{DD} - 33$		-2.5	V	
V_{CC}	2.7		5.5	V	
IOV_{CC}	1.71		5.5	V	$IOV_{CC} \leq V_{CC}$
I_{DD}		4.2	5.2	mA	
I_{SS}		4	4.9	mA	
I_{CC}		600	900	μA	
IOI_{CC}		52	140	μA	SDO disabled
DC Power Supply Rejection Ratio ^{3, 9}		± 0.6		$\mu\text{V/V}$	$V_{DD} \pm 10\%$, $V_{SS} = 15\text{ V}$
		± 0.6		$\mu\text{V/V}$	$V_{SS} \pm 10\%$, $V_{DD} = 15\text{ V}$
AC Power Supply Rejection Ratio ³		95		dB	$V_{DD} \pm 200\text{ mV}$, 50 Hz/60 Hz, $V_{SS} = -15\text{ V}$
		95		dB	$V_{SS} \pm 200\text{ mV}$, 50 Hz/60 Hz, $V_{DD} = 15\text{ V}$

¹ Temperature range: -55°C to +125°C, typical conditions: $T_A = 25^\circ\text{C}$, $V_{DD} = +15\text{ V}$, $V_{SS} = -15\text{ V}$, $V_{REFP} = +10\text{ V}$, $V_{REFN} = -10\text{ V}$.

² Performance characterized with [AD8676BRZ](#) voltage reference buffers and [AD8675ARZ](#) output buffer.

³ Guaranteed by design and characterization; not production tested.

⁴ Linearity error refers to both INL error and DNL error; either parameter can be expected to drift by the amount specified after the length of time specified.

⁵ [AD5791-EP](#) configured in $\times 2$ gain mode, 25 pF compensation capacitor on [AD797](#).

⁶ Includes noise contribution from [AD8676BRZ](#) voltage reference buffers.

⁷ The [AD5781-EP](#) is configured in the bias compensation mode with a low-pass RC filter on the output. $R = 300\ \Omega$, $C = 143\text{ pF}$ (total capacitance seen by the output buffer, lead capacitance, and so forth).

⁸ Current flowing in an individual logic pin.

⁹ Includes PSRR of [AD8676BRZ](#) voltage reference buffers.

TIMING CHARACTERISTICS

$V_{CC} = 2.7\text{ V to }5.5\text{ V}$; all specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 3.

Parameter	Limit ¹		Unit	Test Conditions/Comments
	$IOV_{CC} = 1.71\text{ V to }3.3\text{ V}$	$IOV_{CC} = 3.3\text{ V to }5.5\text{ V}$		
t_1^2	40	28	ns min	SCLK cycle time
	92	60	ns min	SCLK cycle time (readback mode)
t_2	15	10	ns min	SCLK high time
t_3	9	5	ns min	SCLK low time
t_4	5	5	ns min	$\overline{SYNC}$ to SCLK falling edge setup time
t_5	2	2	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge hold time
t_6	48	40	ns min	Minimum $\overline{SYNC}$ high time
t_7	8	6	ns min	$\overline{SYNC}$ rising edge to next SCLK falling edge ignore
t_8	9	7	ns min	Data setup time
t_9	12	7	ns min	Data hold time
t_{10}	13	10	ns min	$\overline{LDAC}$ falling edge to $\overline{SYNC}$ falling edge
t_{11}	20	16	ns min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge
t_{12}	14	11	ns min	$\overline{LDAC}$ pulse width low
t_{13}	130	130	ns typ	$\overline{LDAC}$ falling edge to output response time
t_{14}	130	130	ns typ	$\overline{SYNC}$ rising edge to output response time ($\overline{LDAC}$ tied low)
t_{15}	50	50	ns min	$\overline{CLR}$ pulse width low
t_{16}	140	140	ns typ	$\overline{CLR}$ pulse activation time
t_{17}	0	0	ns min	$\overline{SYNC}$ falling edge to first SCLK rising edge
t_{18}	65	60	ns max	$\overline{SYNC}$ rising edge to SDO tristate ($C_L = 50\text{ pF}$)
t_{19}	62	45	ns max	SCLK rising edge to SDO valid ($C_L = 50\text{ pF}$)
t_{20}	0	0	ns min	$\overline{SYNC}$ rising edge to SCLK rising edge ignore
t_{21}	35	35	ns typ	$\overline{RESET}$ pulse width low
t_{22}	150	150	ns typ	$\overline{RESET}$ pulse activation time

¹ All input signals are specified with $t_R = t_F = 1\text{ ns/V}$ (10% to 90% of IOV_{CC}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

² Maximum SCLK frequency is 35 MHz for write mode and 16 MHz for readback mode.

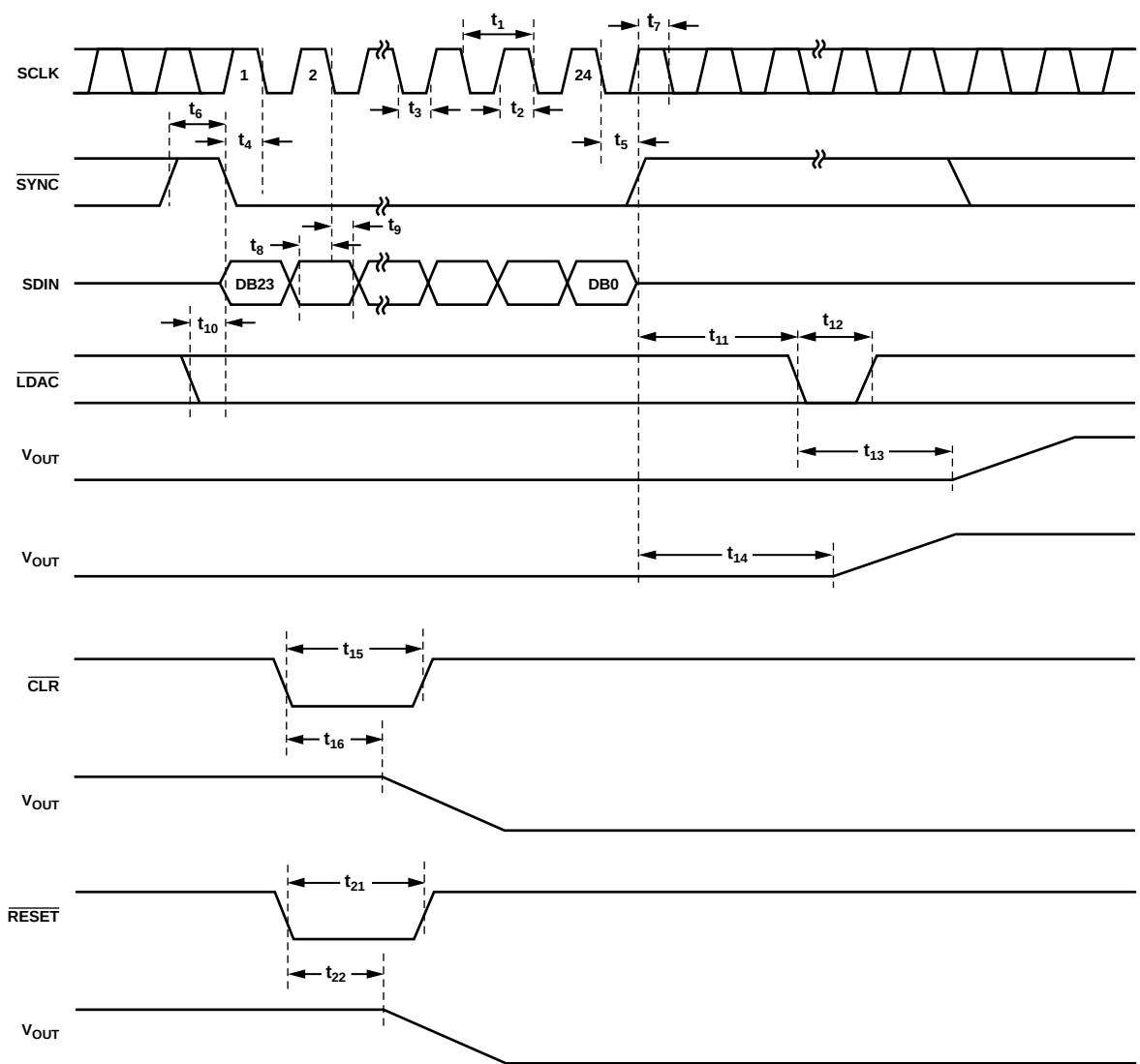


Figure 2. Write Mode Timing Diagram

10454-002

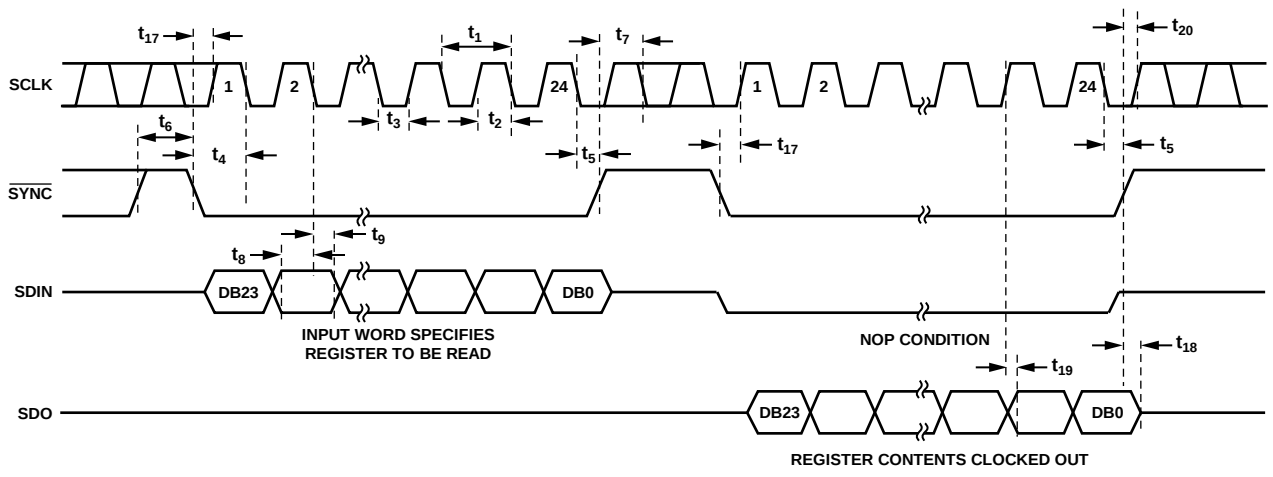


Figure 3. Readback Mode Timing Diagram

10454-003

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted. Transient currents of up to 100 mA do not cause SCR latch-up.

Table 4.

Parameter	Rating
V_{DD} to AGND	$-0.3\text{ V to }+34\text{ V}$
V_{SS} to AGND	$-34\text{ V to }+0.3\text{ V}$
V_{DD} to V_{SS}	$-0.3\text{ V to }+34\text{ V}$
V_{CC} to DGND	$-0.3\text{ V to }+7\text{ V}$
IOV_{CC} to DGND	$-0.3\text{ V to }V_{CC} + 3\text{ V or }+7\text{ V}$ (whichever is less)
Digital Inputs to DGND	$-0.3\text{ V to }IOV_{CC} + 0.3\text{ V or }+7\text{ V}$ (whichever is less)
V_{OUT} to AGND	$-0.3\text{ V to }V_{DD} + 0.3\text{ V}$
V_{REFPF} to AGND	$-0.3\text{ V to }V_{DD} + 0.3\text{ V}$
V_{REFPS} to AGND	$-0.3\text{ V to }V_{DD} + 0.3\text{ V}$
V_{REFNF} to AGND	$V_{SS} - 0.3\text{ V to }+0.3\text{ V}$
V_{REFNS} to AGND	$V_{SS} - 0.3\text{ V to }+0.3\text{ V}$
DGND to AGND	$-0.3\text{ V to }+0.3\text{ V}$
Operating Temperature Range, T_A	
Industrial	$-55^\circ\text{C to }+125^\circ\text{C}$
Storage Temperature Range	$-65^\circ\text{C to }+150^\circ\text{C}$
Maximum Junction Temperature, $T_{J\text{ max}}$	150°C
Power Dissipation	$(T_{J\text{ max}} - T_A)/\theta_{JA}$
TSSOP Package	
θ_{JA} Thermal Impedance	143°C/W
θ_{JC} Thermal Impedance	45°C/W
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020
ESD (Human Body Model)	1.5 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance integrated circuit with an ESD rating of 1.5 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

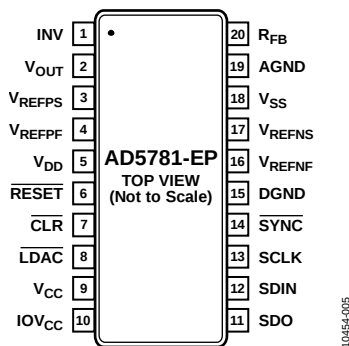


Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	INV	Connection to Inverting Input of External Amplifier.
2	V _{OUT}	Analog Output Voltage.
3	V _{REFPS}	Positive Reference Sense Voltage Input. A voltage range of 5 V to V _{DD} – 2.5 V can be connected. A unity gain amplifier must be connected at this pin, in conjunction with the V _{REFPF} pin.
4	V _{REFPF}	Positive Reference Force Voltage Input. A voltage range of 5 V to V _{DD} – 2.5 V can be connected. A unity gain amplifier must be connected at these pin, in conjunction with the V _{REFPS} pin.
5	V _{DD}	Positive Analog Supply Connection. A voltage range of 7.5 V to 16.5 V can be connected. V _{DD} should be decoupled to AGND.
6	RESET	Active Low Reset Logic Input Pin. Asserting this pin returns the AD5781-EP to its power-on status.
7	CLR	Active Low Clear Logic Input Pin. Asserting this pin sets the DAC register to a user defined value and updates the DAC output. The output value depends on the DAC register coding that is being used, either binary or twos complement.
8	LDAC	Active Low Load DAC Logic Input Pin. This is used to update the DAC register and, consequently, the analog output. When tied permanently low, the output is updated on the rising edge of SYNC. If LDAC is held high during the write cycle, the input register is updated, but the output update is held off until the falling edge of LDAC. The LDAC pin should not be left unconnected.
9	V _{CC}	Digital Supply Connection. A voltage in the range of 2.7 V to 5.5 V can be connected. V _{CC} should be decoupled to DGND.
10	IOV _{CC}	Digital Interface Supply Pin. Digital threshold levels are referenced to the voltage applied to this pin. A voltage range of 1.71 V to 5.5 V can be connected. IOV _{CC} should not be allowed to exceed V _{CC} .
11	SDO	Serial Data Output Pin. Data is clocked out on the rising edge of the serial clock input.
12	SDIN	Serial Data Input Pin. This device has a 24-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
13	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at clock rates of up to 35 MHz.
14	SYNC	Active Low Digital Interface Synchronization Input Pin. This is the frame synchronization signal for the input data. When SYNC is low, it enables the input shift register, and data is then transferred in on the falling edges of the following clocks. The input shift register is updated on the rising edge of SYNC.
15	DGND	Ground Reference Pin for Digital Circuitry.
16	V _{REFNF}	Negative Reference Force Voltage Input. A voltage range of V _{SS} + 2.5 V to 0 V can be connected. A unity gain amplifier must be connected at this pin, in conjunction with the V _{REFNS} pin.
17	V _{REFNS}	Negative Reference Sense Voltage Input. A voltage range of V _{SS} + 2.5 V to 0 V can be connected. A unity gain amplifier must be connected at these pin, in conjunction with the V _{REFNF} pin.
18	V _{SS}	Negative Analog Supply Connection. A voltage range of –16.5 V to –2.5 V can be connected. V _{SS} should be decoupled to AGND.
19	AGND	Ground Reference Pin for Analog Circuitry.
20	R _{FB}	Feedback Connection for External Amplifier.

TYPICAL PERFORMANCE CHARACTERISTICS

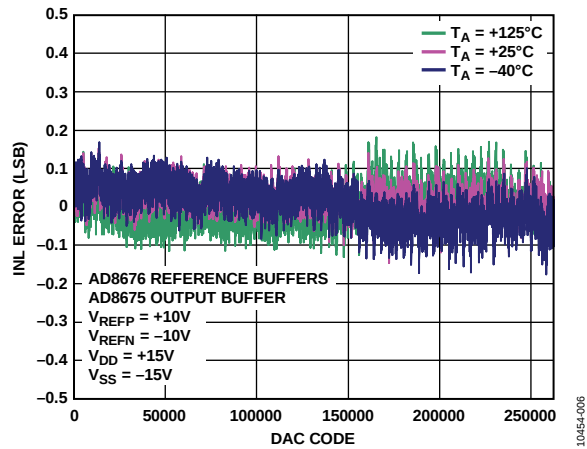
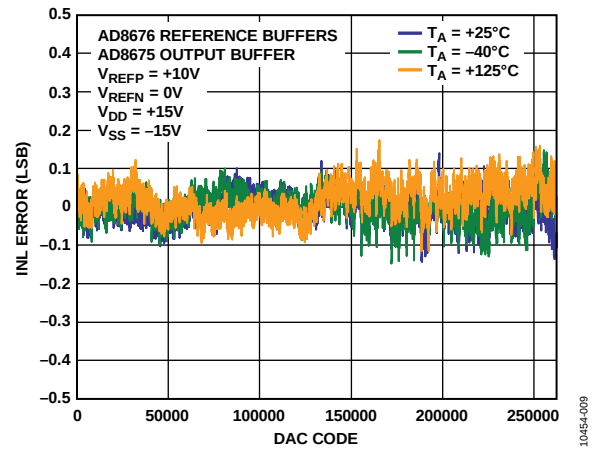
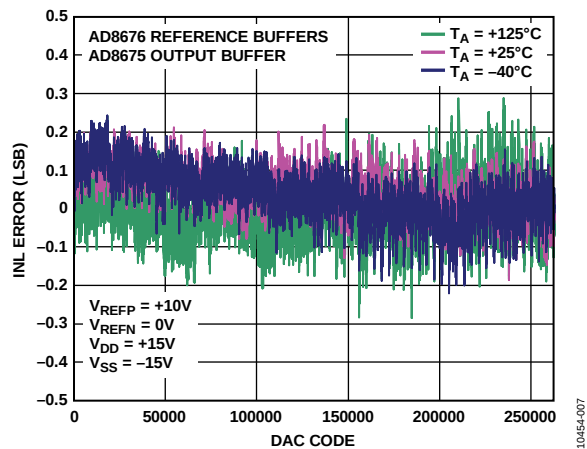
Figure 5. Integral Nonlinearity Error vs. DAC Code, ± 10 V SpanFigure 8. Integral Nonlinearity Error vs. DAC Code, ± 10 V Span, $\times 2$ Gain Mode

Figure 6. Integral Nonlinearity Error vs. DAC Code, +10 V Span

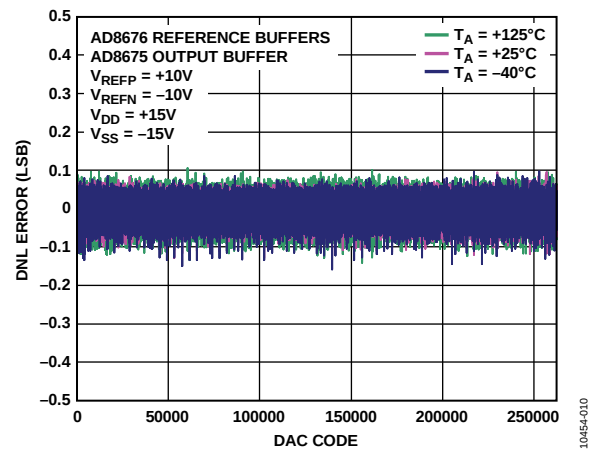
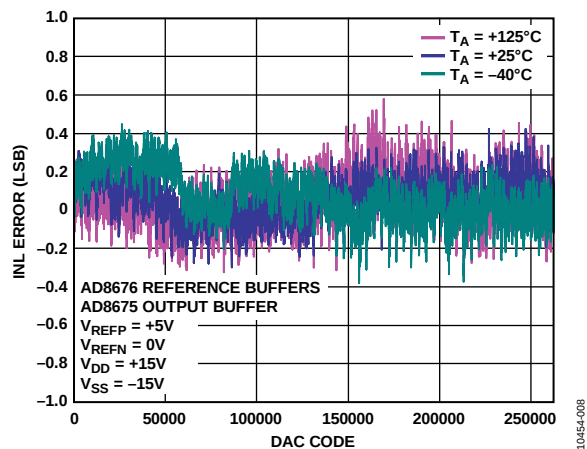
Figure 9. Differential Nonlinearity Error vs. DAC Code, ± 10 V Span

Figure 7. Integral Nonlinearity Error vs. DAC Code, +5 V Span

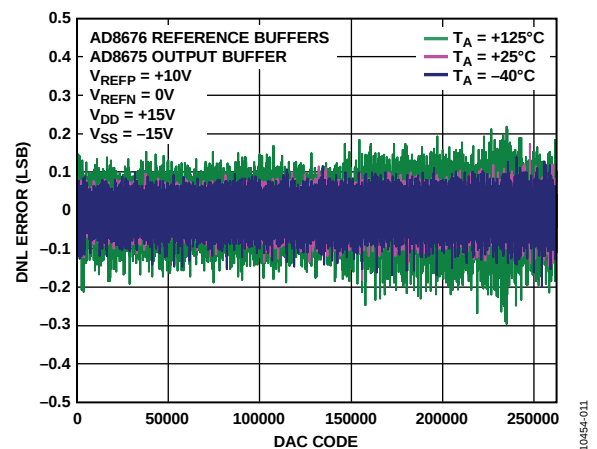


Figure 10. Differential Nonlinearity Error vs. DAC Code, +10 V Span

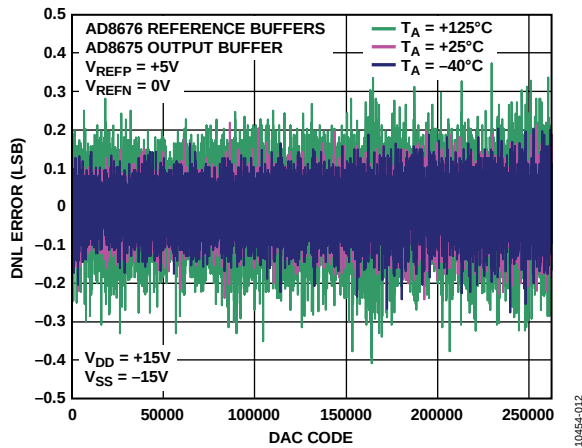


Figure 11. Differential Nonlinearity Error vs. DAC Code, +5 V Span

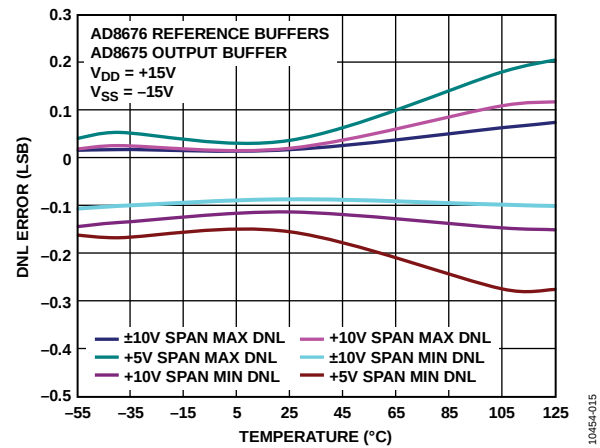


Figure 14. Differential Nonlinearity Error vs. Temperature

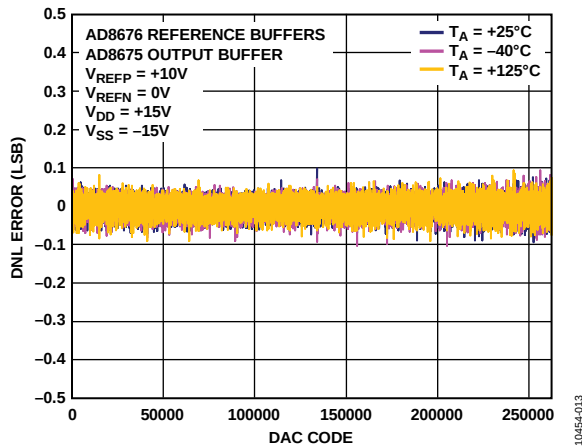


Figure 12. Differential Nonlinearity Error vs. DAC Code, ±10 V Span, ×2 Gain Mode

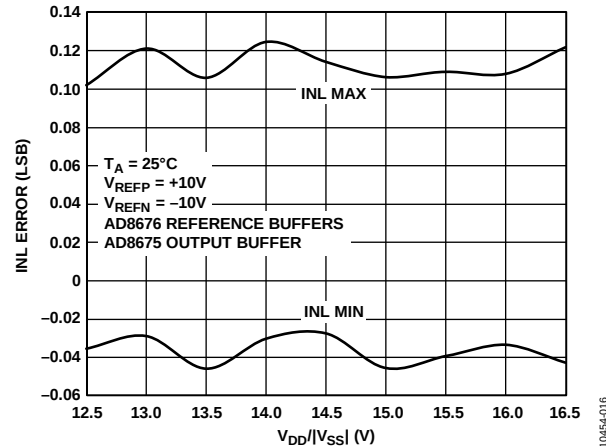


Figure 15. Integral Nonlinearity Error vs. Supply Voltage, ±10 V Span

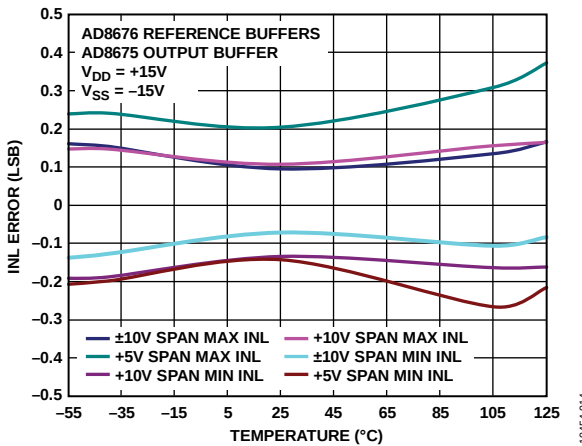


Figure 13. Integral Nonlinearity Error vs. Temperature

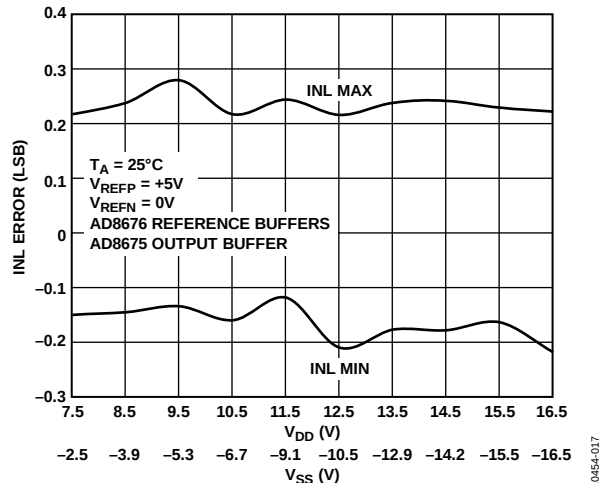


Figure 16. Integral Nonlinearity Error vs. Supply Voltage, +5 V Span

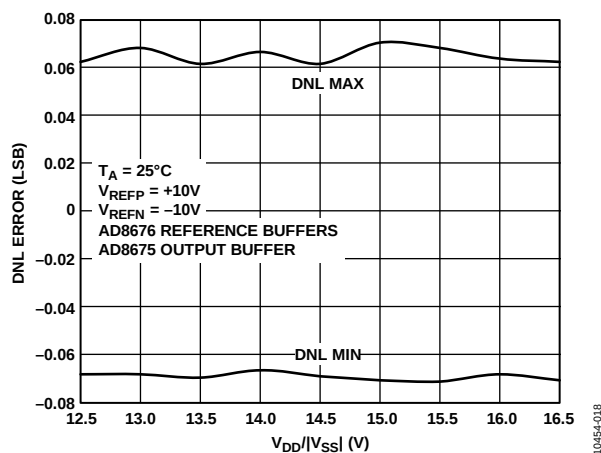
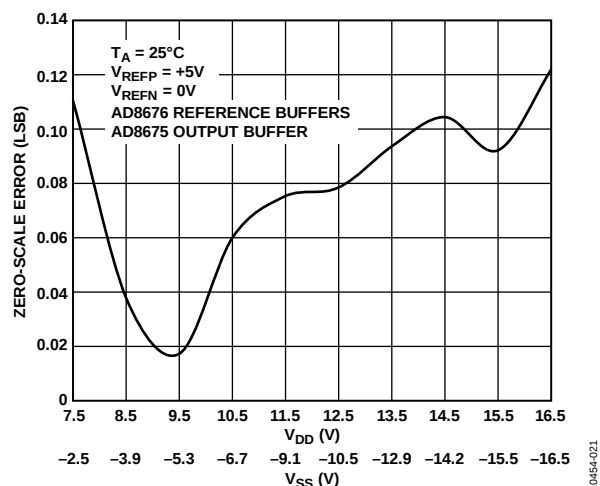
Figure 17. Differential Nonlinearity Error vs. Supply Voltage, ± 10 V Span

Figure 20. Zero-Scale Error vs. Supply Voltage, +5 V Span

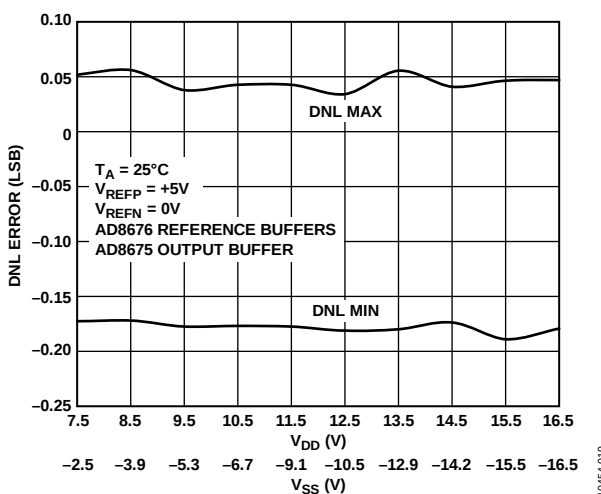


Figure 18. Differential Nonlinearity Error vs. Supply Voltage, +5 V Span

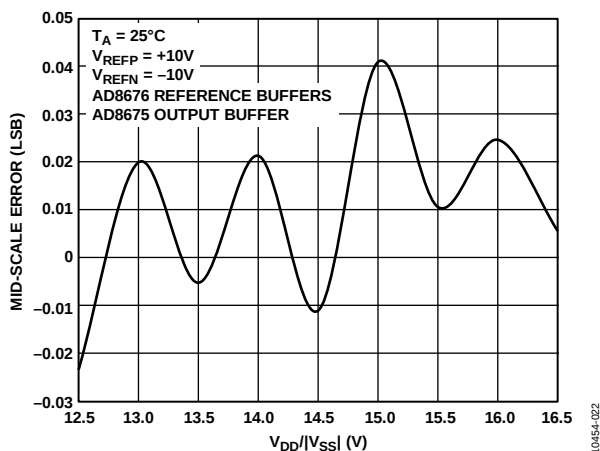
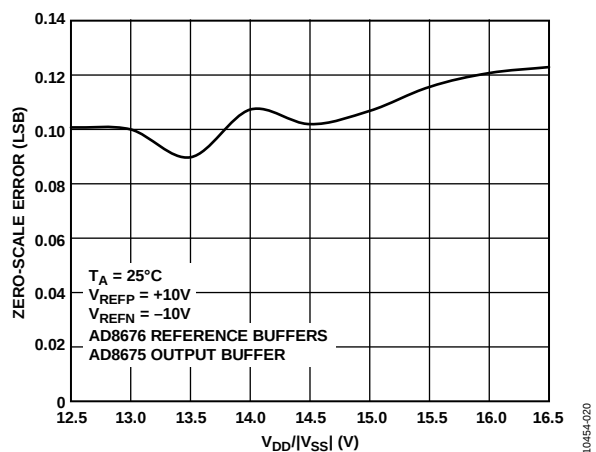
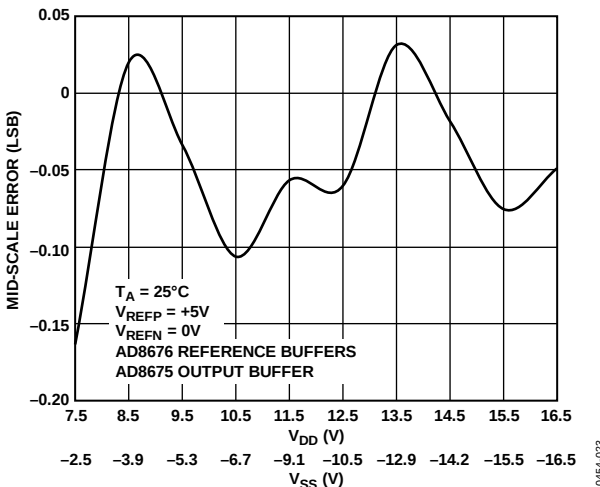
Figure 21. Midscale Error vs. Supply Voltage, ± 10 V SpanFigure 19. Zero-Scale Error vs. Supply Voltage, ± 10 V Span

Figure 22. Midscale Error vs. Supply Voltage, +5 V Span

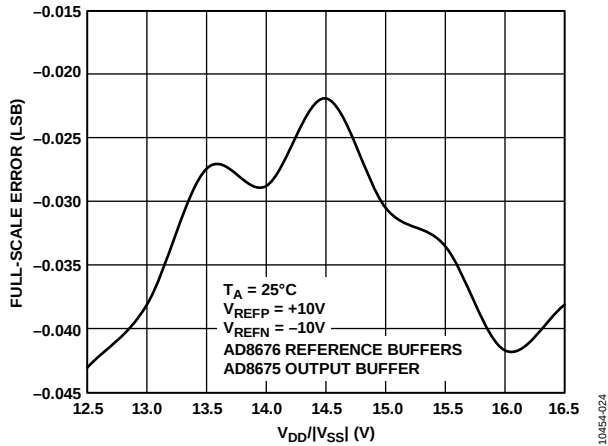
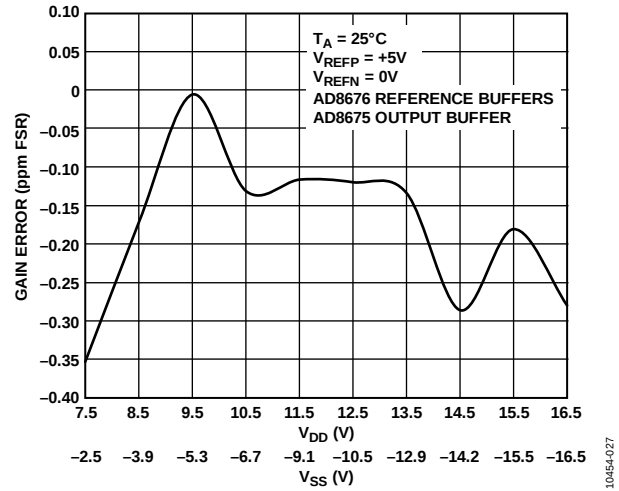
Figure 23. Full-Scale Error vs. Supply Voltage, ± 10 V Span

Figure 26. Gain Error vs. Supply Voltage, +5 V Span

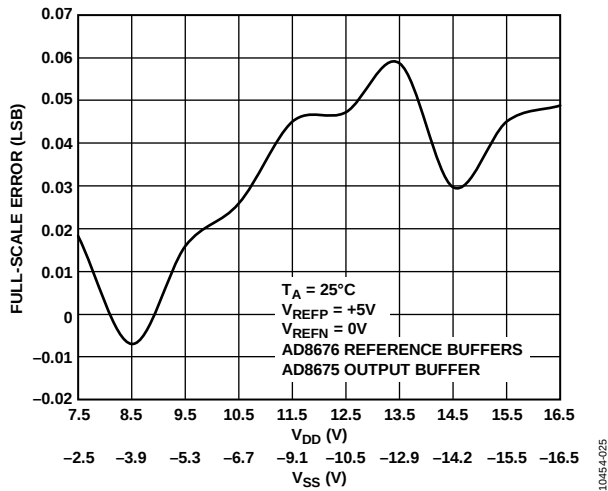


Figure 24. Full-Scale Error vs. Supply Voltage, +5 V Span

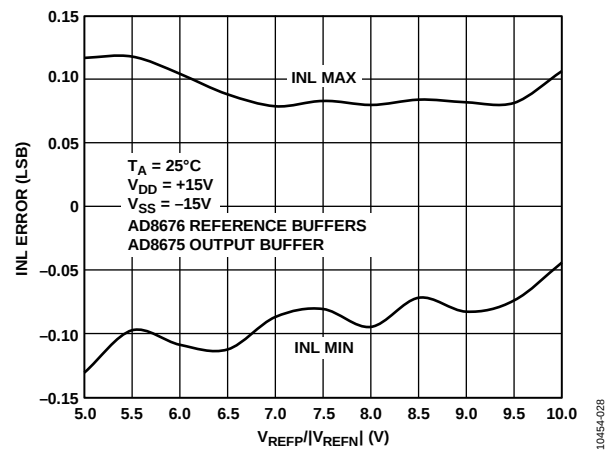


Figure 27. Integral Nonlinearity Error vs. Reference Voltage

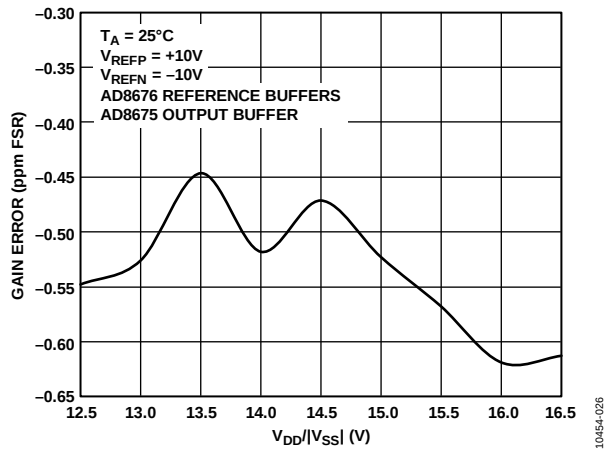
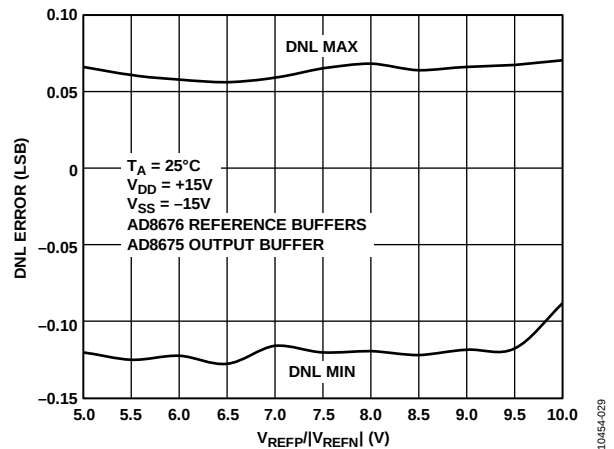
Figure 25. Gain Error vs. Supply Voltage, ± 10 V Span

Figure 28. Differential Nonlinearity Error vs. Reference Voltage

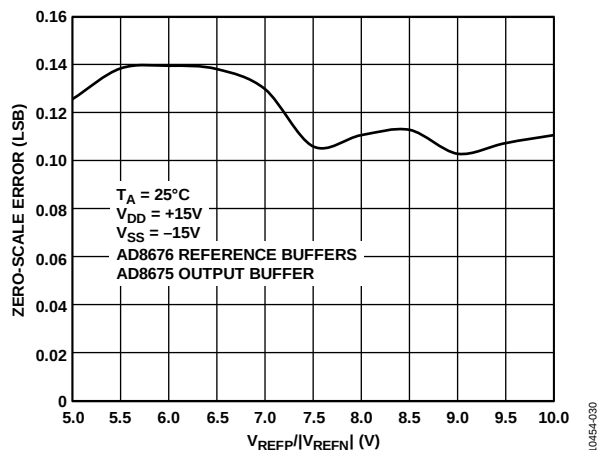


Figure 29. Zero-Scale Error vs. Reference Voltage

10454-030

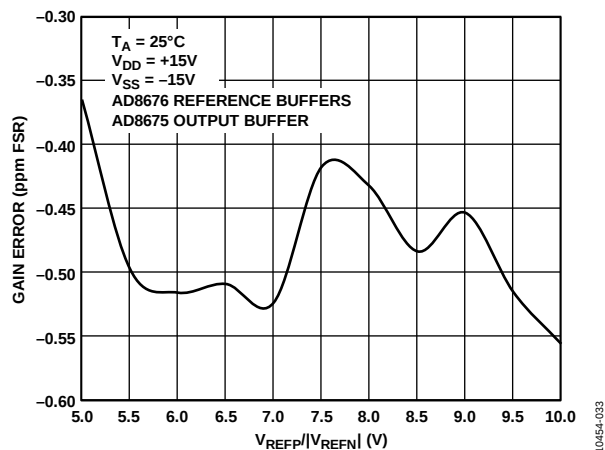


Figure 32. Gain Error vs. Reference Voltage

10454-033

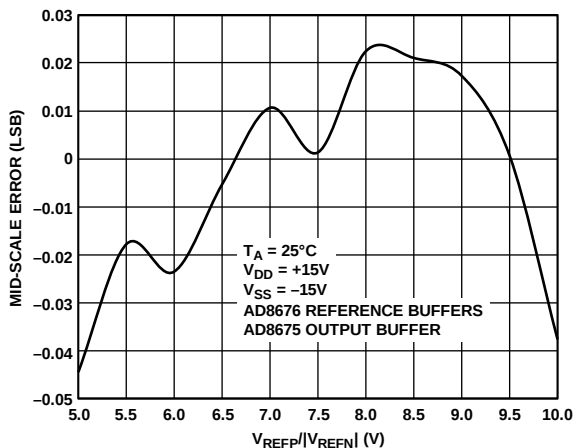


Figure 30. Mid-Scale Error vs. Reference Voltage

10454-031

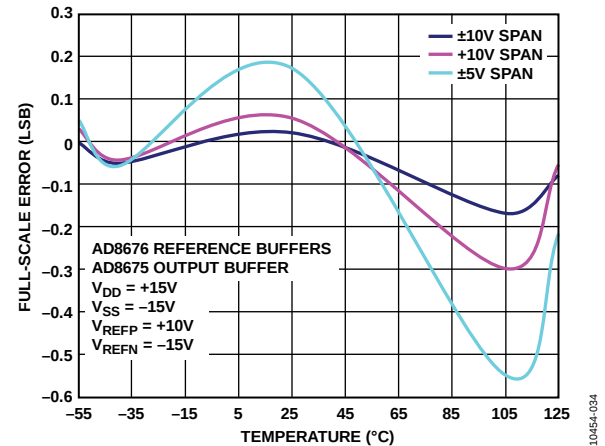


Figure 33. Full-Scale Error vs. Temperature

10454-034

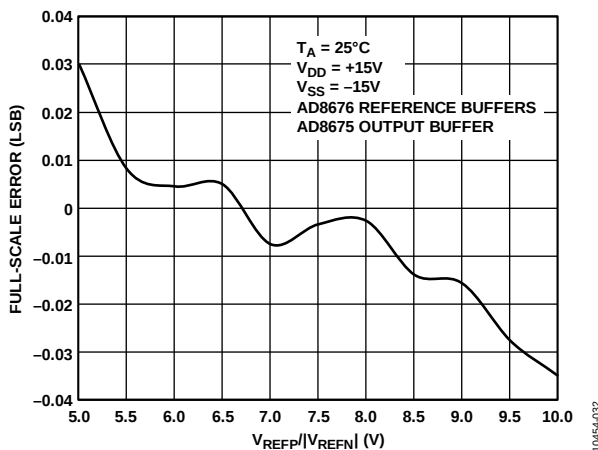


Figure 31. Full-Scale Error vs. Reference Voltage

10454-032

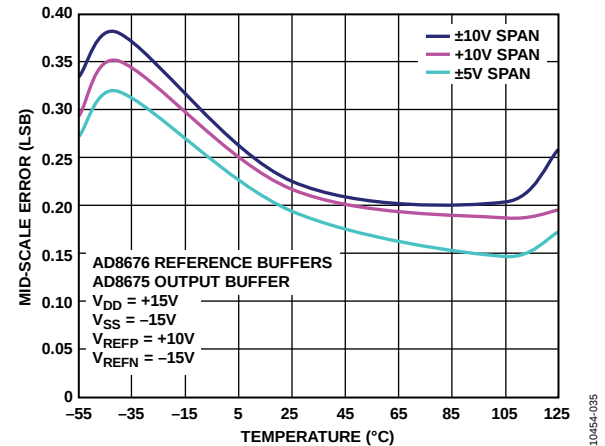


Figure 34. Mid-Scale Error vs. Temperature

10454-035

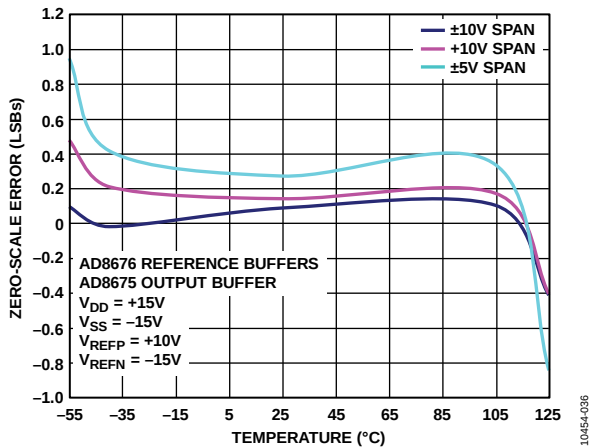


Figure 35. Zero-Scale Error vs. Temperature

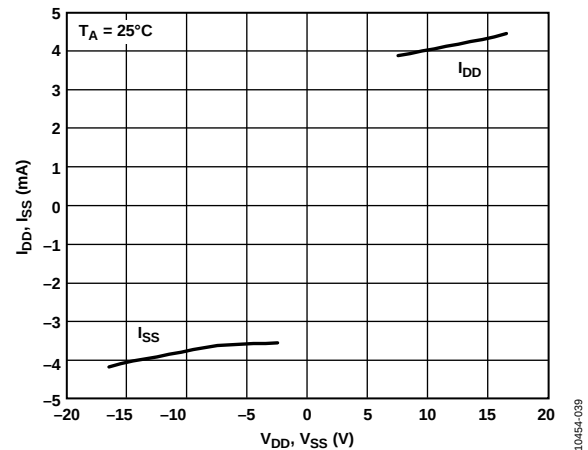


Figure 38. Power Supply Currents vs. Power Supply Voltages

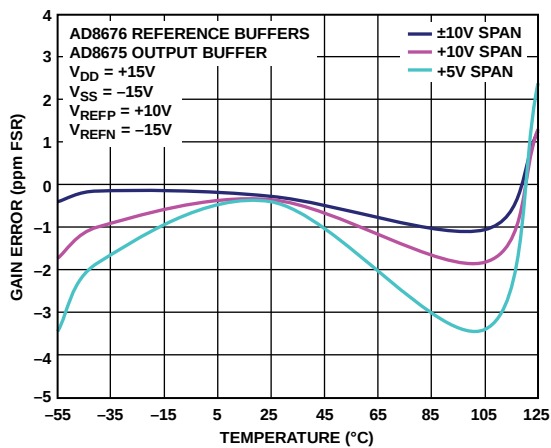


Figure 36. Gain Error vs. Temperature

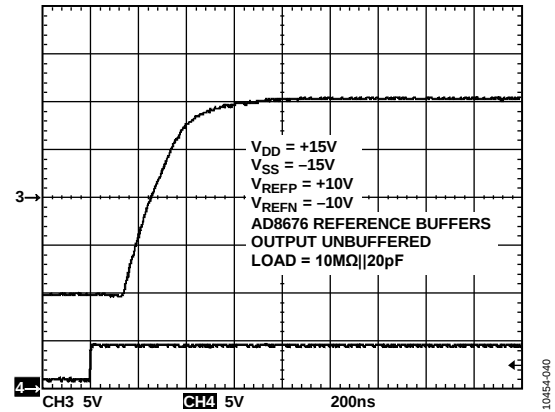


Figure 39. Rising Full-Scale Voltage Step

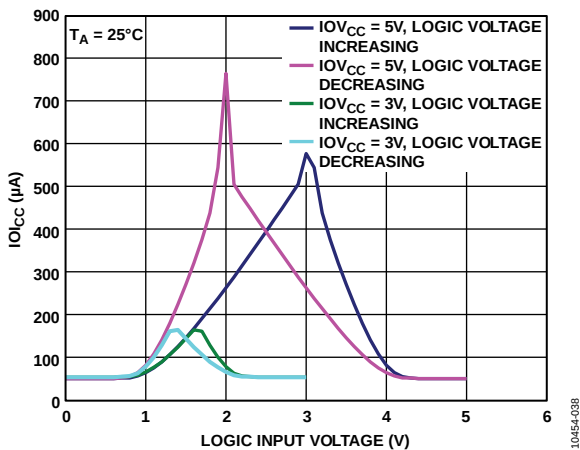


Figure 37. IOCC vs. Logic Input Voltage

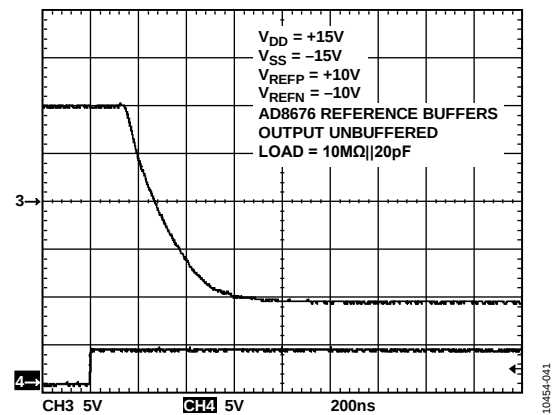


Figure 40. Falling Full-Scale Voltage Step

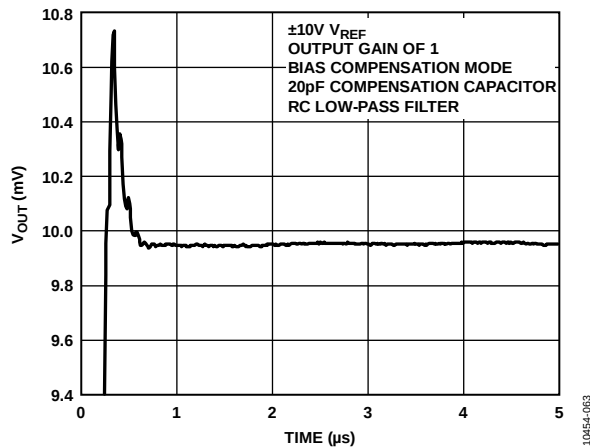


Figure 41. 125 Code Step Settling Time

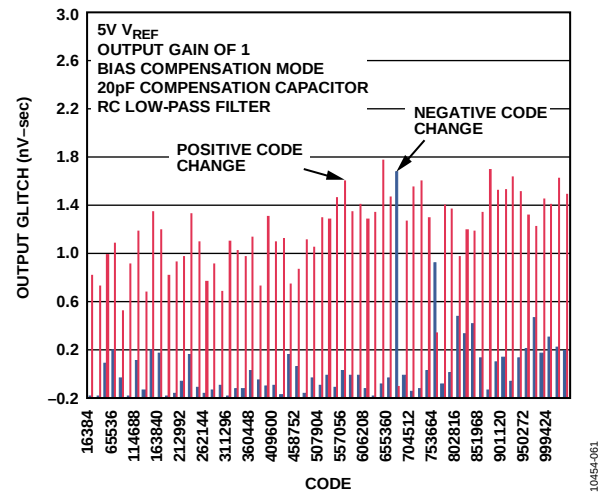
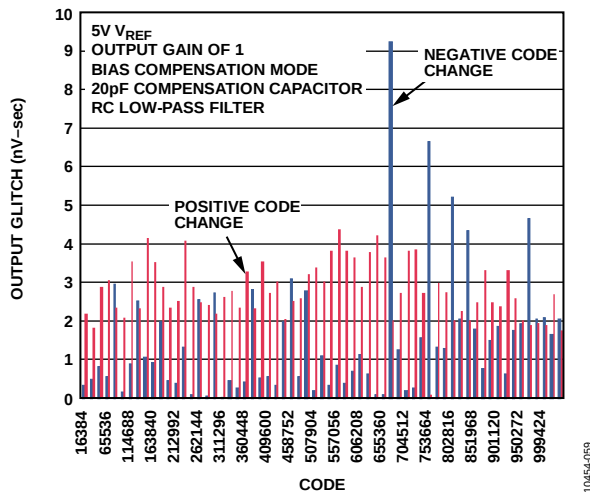
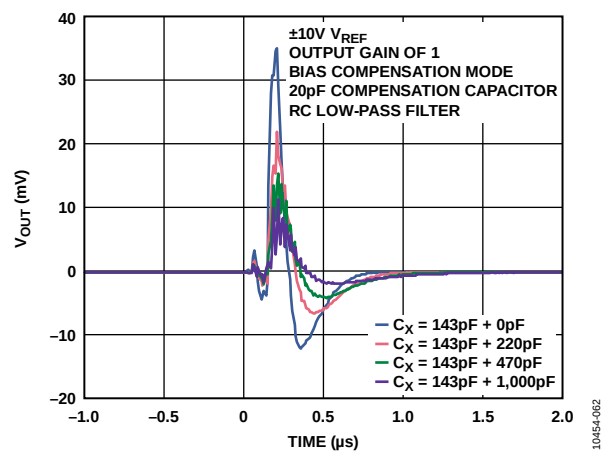
Figure 44. 6 MSB Segment Glitch Energy for 5V V_{REF} Figure 42. 6 MSB Segment Glitch Energy for ±10V V_{REF} 

Figure 45. Midscale Peak-to-Peak Glitch for ±10V

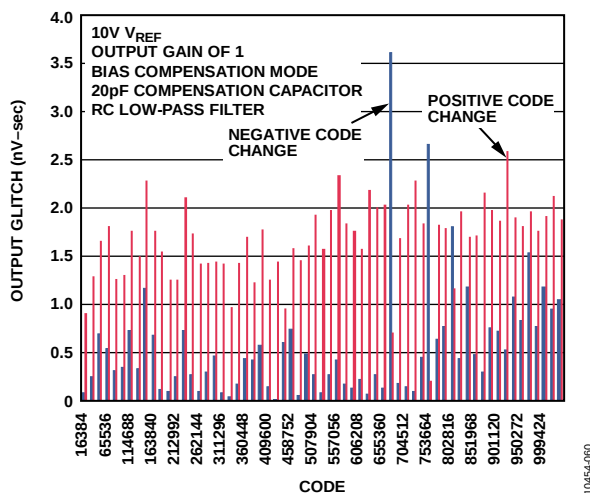
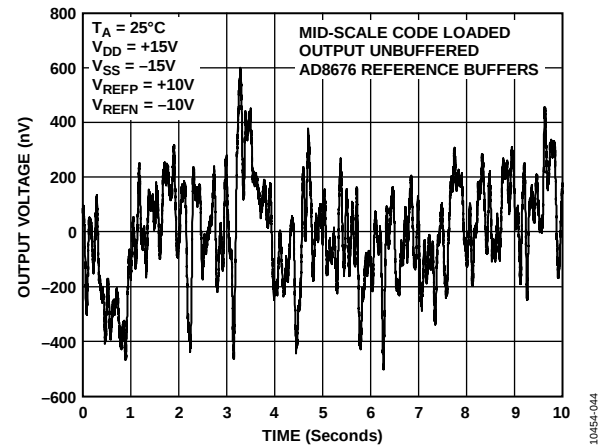
Figure 43. 6 MSB Segment Glitch Energy for 10V V_{REF} 

Figure 46. Voltage Output Noise, 0.1 Hz to 10 Hz Bandwidth

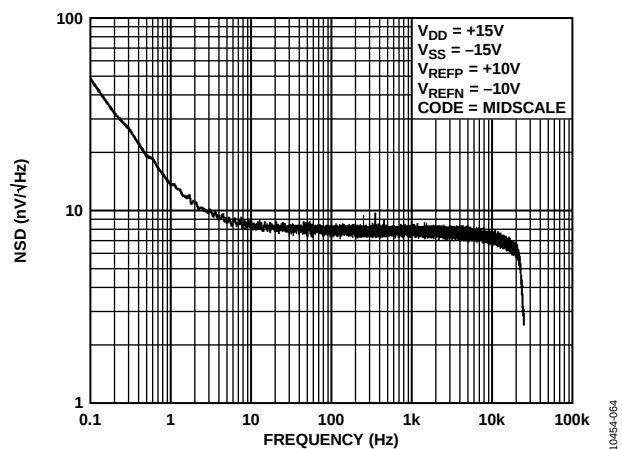


Figure 47. Noise Spectral Density vs. Frequency

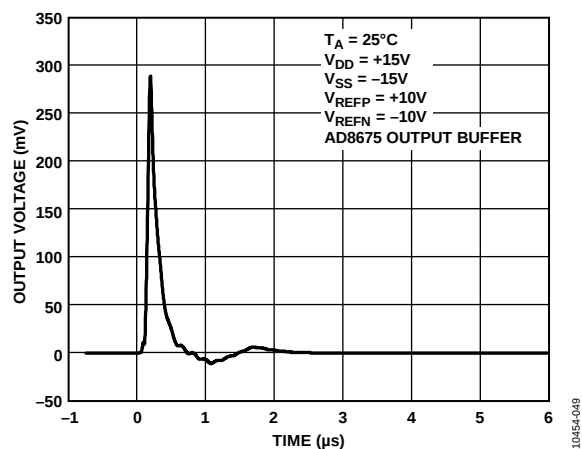


Figure 48. Glitch Impulse on Removal of Output Clamp

OUTLINE DIMENSIONS

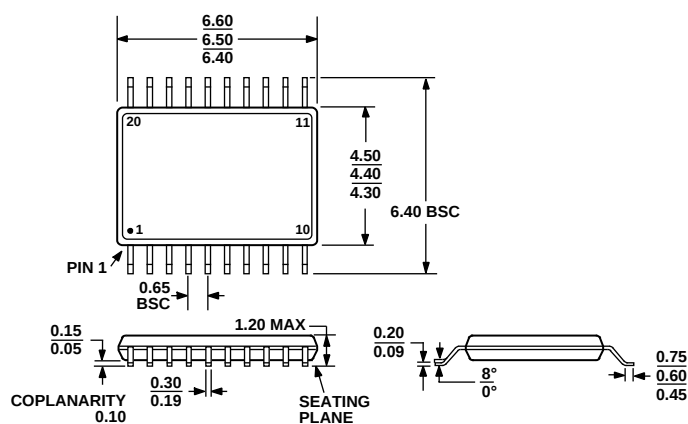


Figure 50. 20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)

Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	INL	Package Description	Package Option
AD5781SRU-EP	-55°C to +125°C	±0.5 LSB	20-Lead TSSOP	RU-20

NOTES

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