DISCRETE SEMICONDUCTORS

DATA SHEET

PDTA144T series PNP resistor-equipped transistors; R1 = 47 k Ω , R2 = open

Product specification Supersedes data of 2004 Apr 27 2004 Aug 05





PDTA144T series

FEATURES

- Built-in bias resistors
- · Simplified circuit design
- Reduction of component count
- Reduced pick and place costs.

APPLICATIONS

- · General purpose switching and amplification
- · Inverter and interface circuits
- · Circuit driver.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V _{CEO}	collector-emitter voltage	_	-50	V
I _O	output current (DC)	_	-100	mA
R1	bias resistor	47	_	kΩ
R2	open	_	_	_

DESCRIPTION

PNP resistor-equipped transistor (see "Simplified outline, symbol and pinning" for package details).

PRODUCT OVERVIEW

TYPE NUMBER	PAC	KAGE	MARKING CODE	NDN COMPLEMENT	
I TPE NUMBER	PHILIPS	EIAJ	WARKING CODE	NPN COMPLEMENT	
PDTA144TE	SOT416	SC-75	5B	PDTC144TE	
PDTA144TEF	SOT490	SC-89	2M	PDTC144TEF	
PDTA144TK	SOT346	SC-59	58	PDTC144TK	
PDTA144TM	SOT883	SC-101	F9	PDTC144TM	
PDTA144TS	SOT54 (TO-92)	SC-43	TA144T	PDTC144TS	
PDTA144TT	SOT23	_	*AF ⁽¹⁾	PDTC144TT	
PDTA144TU	SOT323	SC-70	*7A ⁽¹⁾	PDTC144TU	

Note

^{1. * =} p: Made in Hong Kong.

^{* =} t: Made in Malaysia.

^{* =} W: Made in China.

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PDTA144T series

SIMPLIFIED OUTLINE, SYMBOL AND PINNING

TYPE NUMBER	CIMPLIFIED OUTLINE AND CYMPOL		PINNING
TYPE NUMBER	SIMPLIFIED OUTLINE AND SYMBOL	PIN	DESCRIPTION
PDTA144TS	1 R1 R1 3 MAM352	1 2 3	base collector emitter
PDTA144TE PDTA144TEF PDTA144TK PDTA144TT PDTA144TU	3 1 R1 2 Top view MDB272	1 2 3	base emitter collector
PDTA144TM	2 R1 3 1 Bottom view MDB268	1 2 3	base emitter collector

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PDTA144T series

ORDERING INFORMATION

TYPE NUMBER		PACKAGE	
I TPE NUMBER	NAME	DESCRIPTION	VERSION
PDTA144TE	_	plastic surface mounted package; 3 leads	SOT416
PDTA144TEF	_	plastic surface mounted package; 3 leads	SOT490
PDTA144TK	_	plastic surface mounted package; 3 leads	
PDTA144TM	_	leadless ultra small plastic package; 3 solder lands; body 1.0 \times 0.6 \times 0.5 mm	SOT883
PDTA144TS	_	plastic single-ended leaded (through hole) package; 3 leads	SOT54
PDTA144TT	_	 plastic surface mounted package; 3 leads 	
PDTA144TU	_	plastic surface mounted package; 3 leads	SOT323

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CBO}	collector-base voltage	open emitter	_	-50	V
V _{CEO}	collector-emitter voltage	open base	_	-50	V
V _{EBO}	emitter-base voltage	open collector	_	- 5	V
Io	output current (DC)		_	-100	mA
I _{CM}	peak collector current		_	-100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C			
	SOT23	note 1	_	250	mW
	SOT54	note 1	_	500	mW
	SOT323	note 1	_	200	mW
	SOT346	note 1	_	250	mW
	SOT416	note 1	_	150	mW
	SOT490	notes 1 and 2	_	250	mW
	SOT883	notes 2 and 3	_	250	mW
T _{stg}	storage temperature		-65	+150	°C
Tj	junction temperature		_	150	°C
T _{amb}	operating ambient temperature		-65	+150	°C

Notes

- 1. Refer to standard mounting conditions.
- 2. Reflow soldering is the only recommended soldering method.
- 3. Refer to SOT883 standard mounting conditions; FR4 with 60 μm copper strip line.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th(j-a)}	thermal resistance from junction to ambient	in free air		
	SOT23	note 1	500	K/W
	SOT54	note 1	250	K/W
	SOT323	note 1	625	K/W
	SOT346	note 1	500	K/W
	SOT416	note 1	833	K/W
	SOT490	notes 1 and 2	500	K/W
	SOT883	notes 2 and 3	500	K/W

Notes

- 1. Refer to standard mounting conditions.
- 2. Reflow soldering is the only recommended soldering method.
- 3. Refer to SOT883 standard mounting conditions; FR4 with 60 μm copper strip line.

CHARACTERISTICS

 T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I _{CBO}	collector-base cut-off current	$V_{CB} = -50 \text{ V}; I_E = 0 \text{ A}$	_	_	-100	nA
I _{CEO}	collector-emitter cut-off current	$V_{CE} = -30 \text{ V}; I_B = 0 \text{ A}$	_	_	-1	μΑ
		$V_{CE} = -30 \text{ V}; I_B = 0; T_j = 150 ^{\circ}\text{C}$	_	_	-50	μΑ
I _{EBO}	emitter-base cut-off current	$V_{EB} = -5 \text{ V}; I_{C} = 0 \text{ A}$	_	_	-100	nA
h _{FE}	DC current gain	$V_{CE} = -5 \text{ V}; I_{C} = -1 \text{ mA}$	100	_	_	
V _{CEsat}	collector-emitter saturation voltage	$I_C = -10 \text{ mA}; I_B = -0.5 \text{ mA}$	_	_	-150	mV
R1	input resistor		33	47	61	kΩ
C _c	collector capacitance	$I_E = I_e = 0$; $V_{CB} = -10 \text{ V}$; $f = 1 \text{ MHz}$	_	_	3	pF

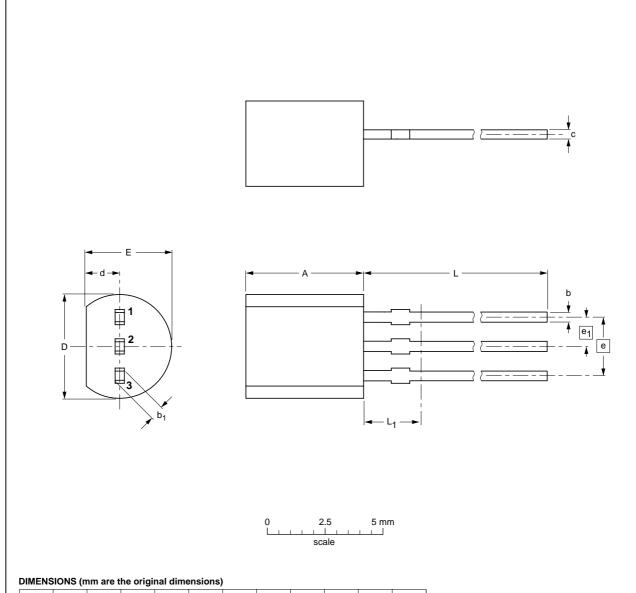
PNP resistor-equipped transistors; R1 = 47 k Ω , R2 = open

PDTA144T series

PACKAGE OUTLINES

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



UNIT	A	b	b ₁	С	D	d	E	е	e ₁	L	L ₁ ⁽¹⁾ max.	
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5	

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

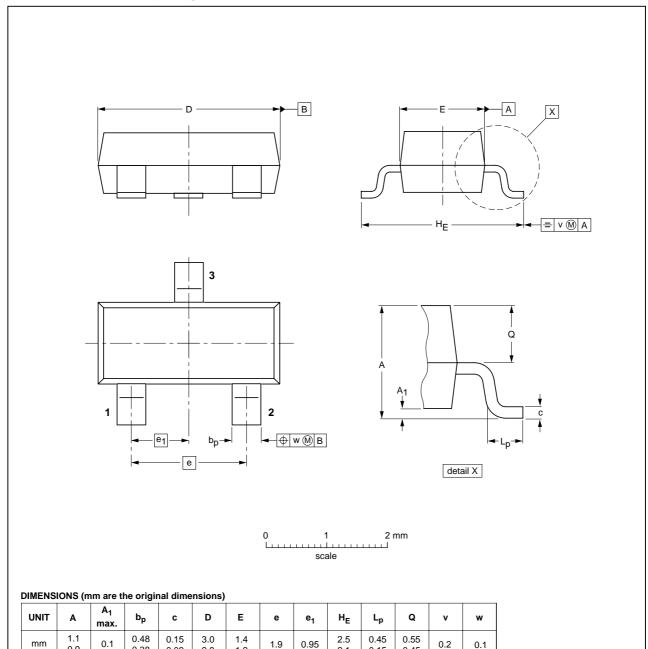
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VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT54		TO-92	SC-43A			97-02-28 04-06-28	

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Plastic surface mounted package; 3 leads

SOT23



OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	EIAJ	PROJECTION	ISSUE DATE	
SOT23		TO-236AB			-97-02-28- 99-09-13	

2004 Aug 05 7

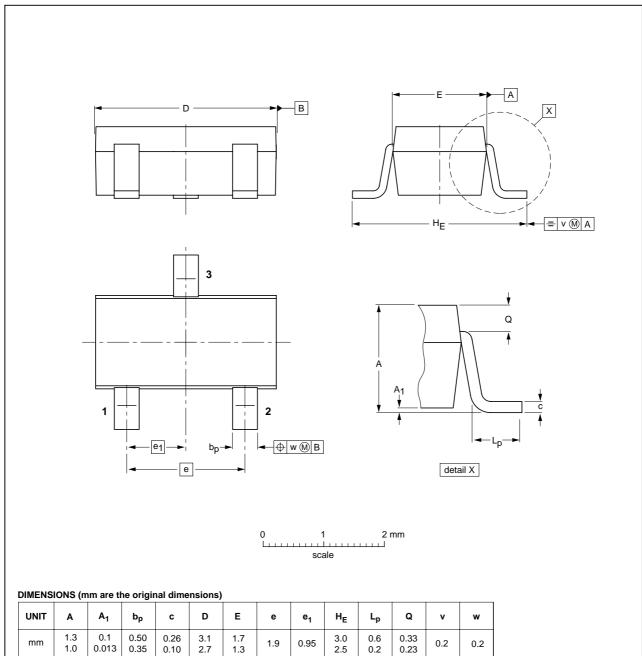
0.38

0.9

PDTA144T series

Plastic surface mounted package; 3 leads

SOT346



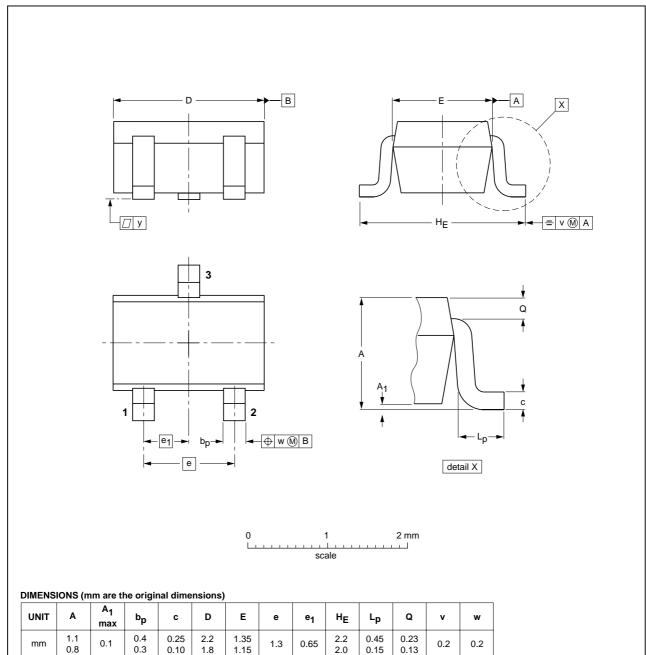
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IEC	JEDEC	EIAJ	PROJECTION	ISSUE DATE	
	TO-236	SC-59		98-07-17	
-	IEC	IEC JEDEC	IEC JEDEC EIAJ	IEC JEDEC EIAJ PROJECTION	

PNP resistor-equipped transistors; R1 = 47 k Ω , R2 = open

PDTA144T series

Plastic surface mounted package; 3 leads

SOT323

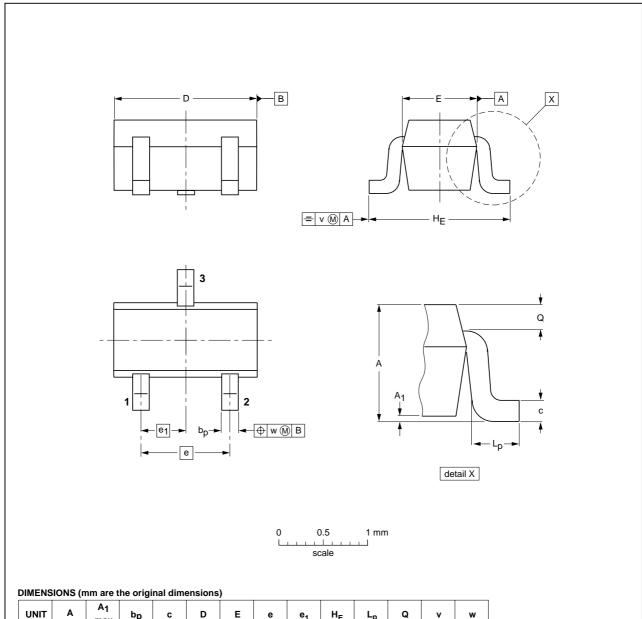


OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	EIAJ	PROJECTION	ISSUE DATE	
SOT323			SC-70		97-02-28	

PDTA144T series

Plastic surface mounted package; 3 leads

SOT416



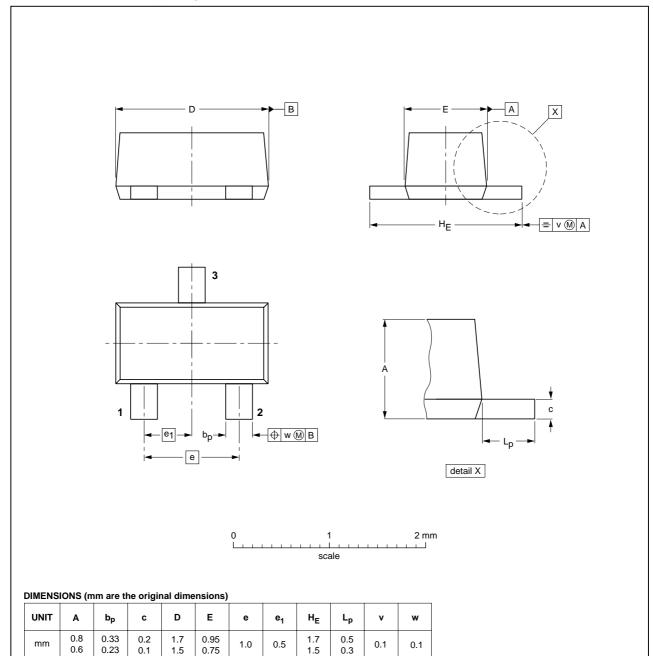
UNIT	А	max	bp	С	D	E	е	e ₁	HE	L _p	Q	V	W
mm	0.95 0.60	0.1	0.30 0.15	0.25 0.10	1.8 1.4	0.9 0.7	1	0.5	1.75 1.45	0.45 0.15	0.23 0.13	0.2	0.2

OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	EIAJ	PROJECTION	ISSUE DATE
SOT416			SC-75		97-02-28

PDTA144T series

Plastic surface mounted package; 3 leads

SOT490



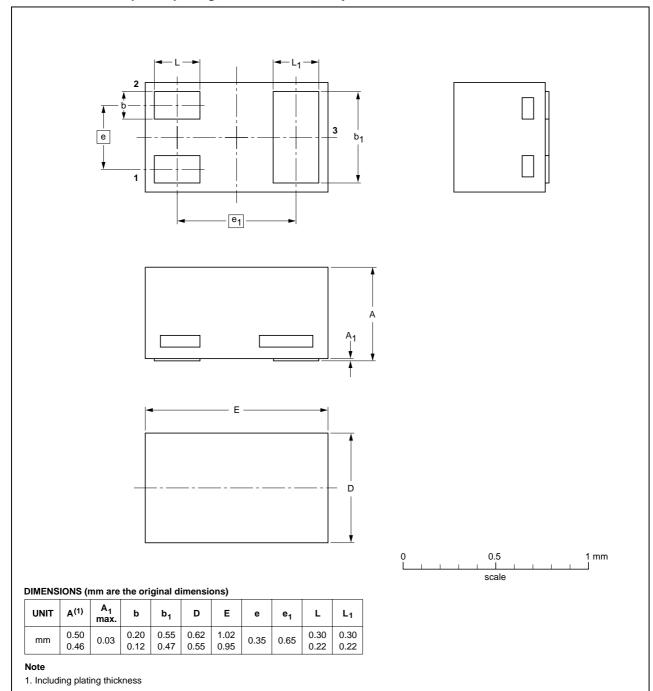
VERSION IEC JEDEC EIAJ PROJECTION	OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE
	VERSION	IEC	JEDEC	EIAJ	PROJECTION	ISSUE DATE
	SOT490			SC-89		98-10-23

PNP resistor-equipped transistors; R1 = 47 k Ω , R2 = open

PDTA144T series

Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.5 mm

SOT883



OUTLINE		REFER	RENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT883			SC-101		03-02-05 03-04-03

PNP resistor-equipped transistors; R1 = 47 k Ω , R2 = open

PDTA144T series

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS(2)(3)	DEFINITION
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Notes

- 1. Please consult the most recently issued data sheet before initiating or completing a design.
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- 3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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