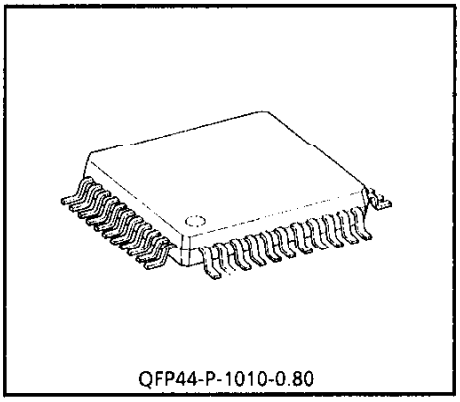
TENTATIVE TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9287AF

2 CHANNEL 1BIT AD / DA CONVERTER FOR AUDIO

TC9287AF is 2'nd order Σ-Δ modulation 1bit AD / DA converter for Digital Audio. This IC built-in 2 channel AD / DA converter and digital, analog filter, so construct hi-performance and low cost AD / DA converter system.



QFP44-P-1010-0.80

Weight : 0.5g (Typ.)

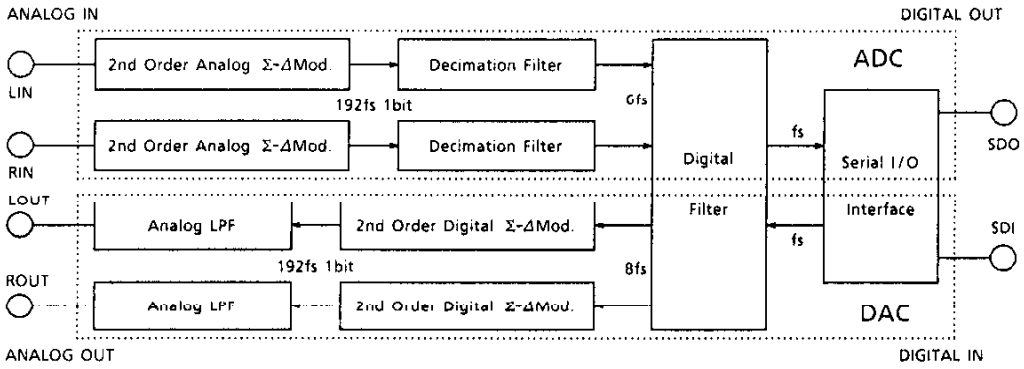
FEATURES

- Built in input and output digital analog filter circuit, so external filter is CR filter.
- Operating voltage is 5.0V.
- Power dissipation is 250mW (V_{DD} = 5V)
  [At ADOFF mode, 190mW (V_{DD} = 5V)]
- Package is QFP44-P-1010-0.80.

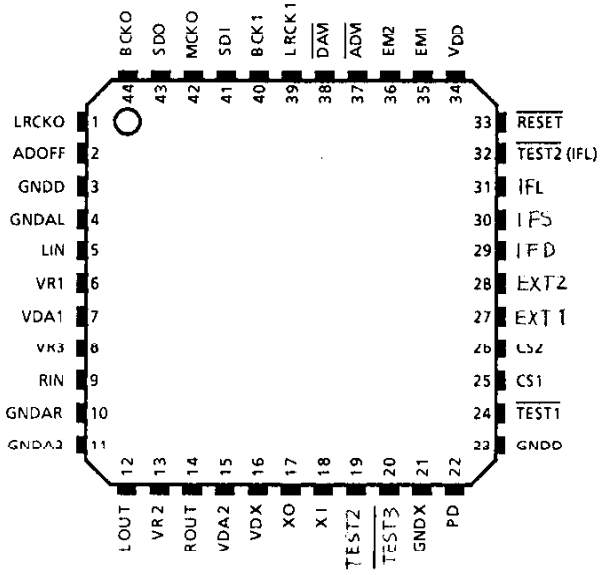
AD / DA AC characteristics is as follows.

	S / N RATIO (A-Weight)	THD + N	Units
AD converter	92 (Typ.)	−82 (Typ.)	dB
DA converter	95 (Typ.)	−87 (Typ.)	dB

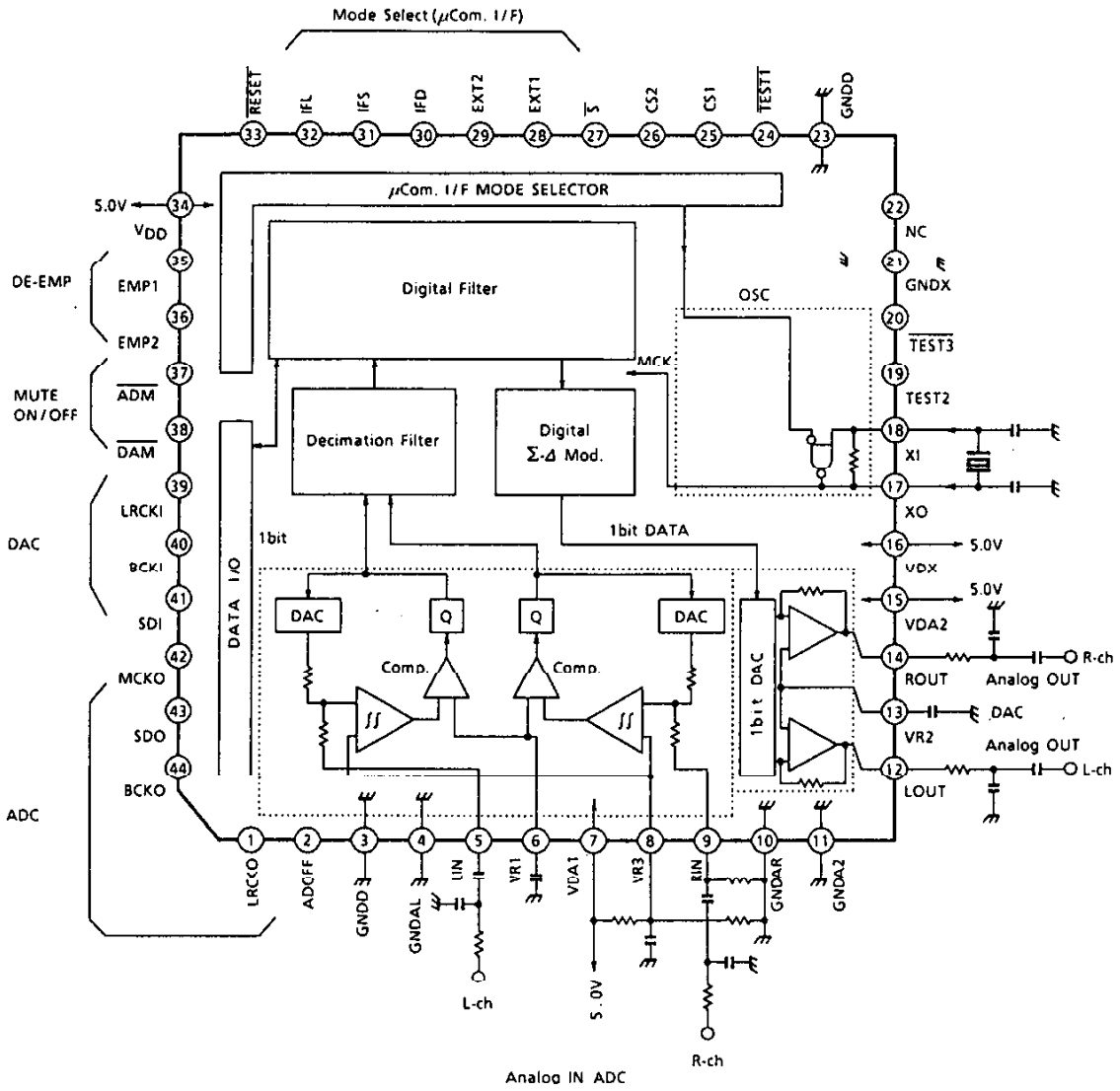
SYSTEM BLOCK



TERMINAL LAYOUT



BLOCK DIAGRAM

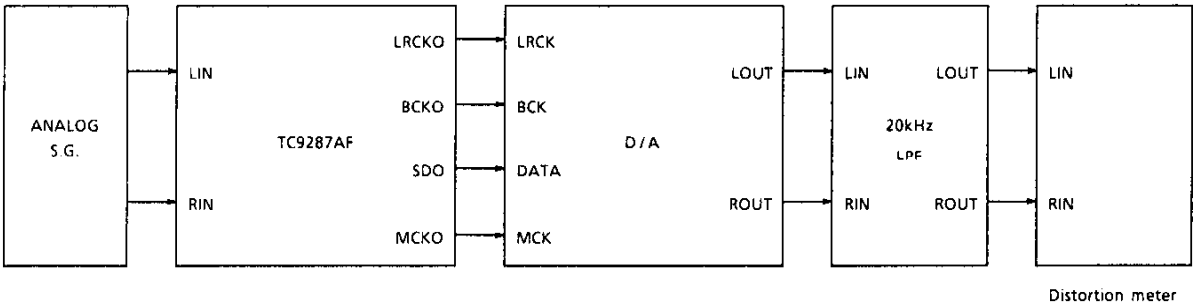


TERMINAL DESCRIPTION

NO.	TERMINAL	I/O	FUNCTION	REMARK
1	LRCKO	—	Channel clock (LRCK) output terminal	
2	ADOFF	I	AD converter off setting terminal. At "H" level, decimation filter OFF.	Pull-down
3	GNDD	—	Digital GND terminal.	0V
4	GNDAL	—	Analog GND terminal for AD converter L channel.	0V
5	LIN	I	AD converter L-ch signal input terminal.	2.5V ± α
6	VR1	I	Reference voltage terminal for AD converter comparator.	2.5V
7	VDA1	—	Voltage supply terminal for AD converter.	5.0V
8	VR3	I	Reference voltage terminal for AD converter.	2.5V
9	RIN	I	A/D converter R-ch signal input terminal.	2.5V ± α
10	GNDAR	—	Analog GND terminal for AD converter R-ch channel.	0V
11	GNDA2	—	Analog GND terminal for DA converter.	0V
12	LOUT	O	DA converter L channel signal output terminal.	2.5V − α
13	VR2	I	Reference voltage terminal for DA converter.	2.5V
14	ROUT	I	DA converter R channel signal output terminal.	2.5V − α
15	VDA2	—	Voltage supply terminal for DA converter.	5.0V
16	VDX	—	Voltage supply terminal for Oscillator.	5.0V
17	XO	O	Crystal oscillator connection terminal.	
18	XI	I	Crystal oscillator connection terminal.	
19	$\overline{\text{TEST2}}$	O	Test terminal 2.	
20	$\overline{\text{TEST3}}$	I	Test terminal 3.	
21	GNDX	—	GND terminal for Oscillator.	0V
22	NC	O	Non-connecting terminal.	
23	GNDD	—	Digital GND terminal.	0V
24	$\overline{\text{TEST1}}$	I	Test terminal 1. Usually use at "H" level.	Pull-up
25	CS1	I	Master mode setting terminal 1.	Pull-up
26	CS2	I	Master mode setting terminal 2.	Pull-up
27	$\overline{S}$	I	Serial mode switching terminal. (fixed "L")	Pull-up
28	EXT1	O	External output terminal 1.	Serial mode
29	EXT2	O	External output terminal 2.	Serial mode
30	IFD	I	MCU interface data input terminal.	Pull-up Serial mode
31	IFS	I	MCU interface shift clock input terminal.	Pull-up Serial mode
32	IFL	I	MCU interface latch pulse input terminal.	Serial mode

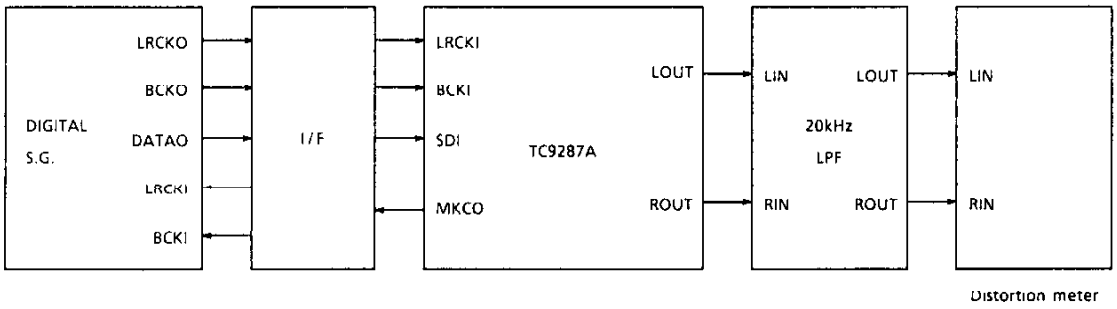
NO.	TERMINAL	I/O	FUNCTION	REMARK
33	$\overline{\text{RESET}}$	I	Reset terminal.	Pull-up
34	V_{DD}	—	Digital voltage supply terminal.	5.0V
35	EM1	I	De-emphasis Coefficient select terminal 1.	Pull-down
36	EM2	I	De-emphasis Coefficient select terminal 2.	Pull-down
37	ADM	I	AD converter output mute terminal. At "L" level, mute "ON".	Pull-up
38	$\overline{\text{DAM}}$	I	AD converter output mute terminal. At "L" level, mute "ON".	Pull-up
39	LRCKI	I	External channel clock (LRCK) input terminal.	
40	BCKI	I	External bit clock (BCK) input terminal.	
41	SDI	I	Digital data input terminal. (DA converter serial data input)	
42	MCKO	O	384fs clock output terminal. (system clock)	
43	SDO	O	Digital data output terminal. (AD converter serial data output)	
44	BCKO	O	Bit clock (BCK) output terminal.	

TEST CIRCUIT 1 : A/D converter evaluation system



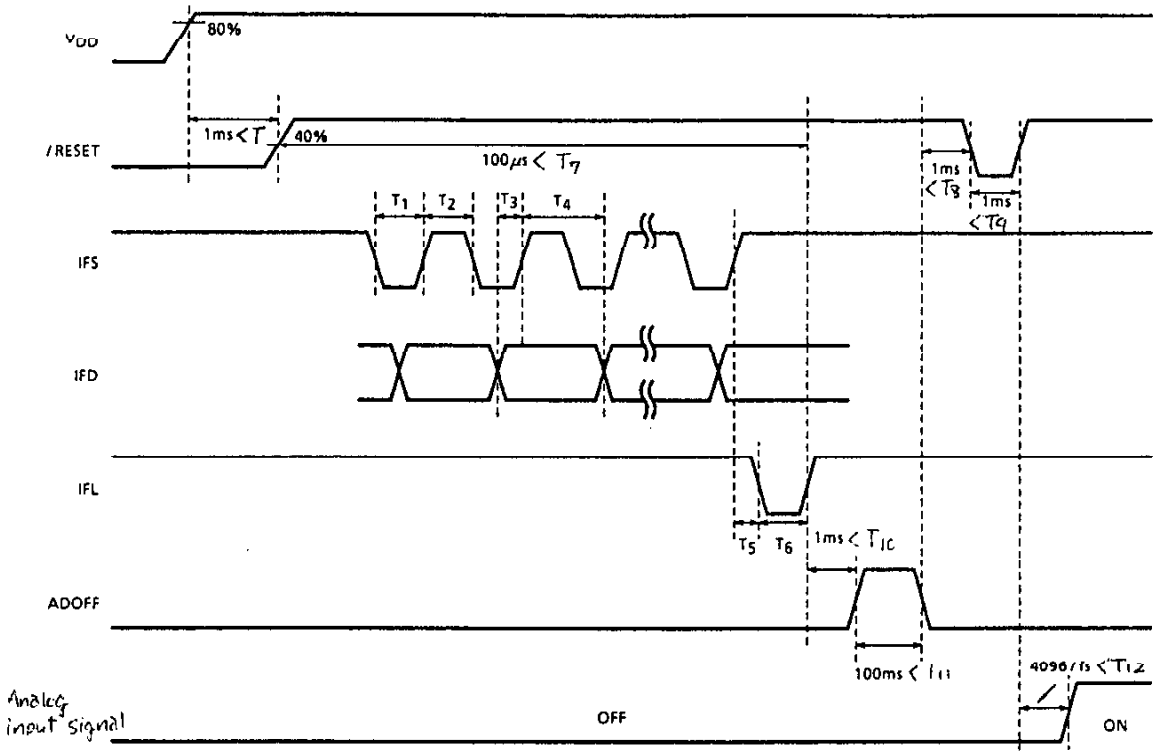
ANALOG S.G. : SHIBASOKU, AM51A
20kHz LPF : SHIBASOKU, AM51A FILTER
Distortion meter : SHIBASOKU, AM51A

TEST CIRCUIT 2 : D/A converter evaluation system



DIGITAL S.G. : ANRITSU, MG-22A
20kHz LPF : SHIBASOKU, 725C FILTER
Distortion meter : SHIBASOKU, 725C

7.



T1, T2, T6	: Clock puls width	$>1\mu s$
T3	: Setup time	$>1\mu s$
T4	: Hold time	$>1\mu s$
T5	: Hold time	$>1\mu s$

Fig. Timing

MAXIMUM RATINGS (Ta=25℃)

CHARACTERISTIC	記 号	定 格	単 位
Supply Voltage	V_{DD}	-0.3 ~ 6.0	V
	V_{DX}	-0.3 ~ 6.0	
	V_{DA1}	-0.3 ~ 6.0	
	V_{DA2}	-0.3 ~ 6.0	
Input Voltage	V_{in}	-0.3 ~ V_{DD} + 0.6	V
Power Dissipation	P_D	250	mW
Operating Temperature	Topr	-30 ~ 85	℃
Storage Temperature	Tstg	-55 ~ 150	℃

ELECTRICAL CHARACTERISTIC (Unless otherwise specified, Ta=25℃, V_{DD}=V_{DX}=V_{DA1}=V_{DA2}=5.0V)

DC item

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage		V_{DD}	—	Ta=−35~85 ℃	4.5	5.0	5.5	V
		V_{DX}						
		V_{DA1}						
		V_{DA2}						
Power Dissipation		I_{DD}	—	XI=16.9344MHz ADOFF="L"	—	50	90	mA
Power Dissipation (at ADOFF=OFF)				XI=16.9344MHz ADOFF="H"	—	35	63	
Input Voltage	"H" Level	V_{IH}	—		3.5	—	—	V
	"L" Level	V_{IL}			—	—	1.5	
Output Current	"H" Level	I_{OH}	—	42pin V_{OH}=0.4V	−9.4	—	−3.6	mA
				1, 28, 29, 43 and 44pin V_{OH}=0.4V	−5.0	—	−2.1	
	"L" Level	I_{OL}		42pin V_{OL}=4.6V	8.0	—	22.0	
				1, 28, 29, 43 and 44pin V_{OL}=4.6V	3.5	—	14.0	
Input Current		I_{IN}	—		−10.0	—	10.0	μA
Pull Up / Down Resister		$R_{U/D}$	—		60	—	150	kΩ

AC Item

A / D converter

CHARACTERISTIC	SYMBOL	TEST CIR -CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Maximum Input Voltage	V_{IM}	1	Input Voltage= Output level of A/D converter is full scale	0.9	1.0	1.1	Vrms
Input Impedance	Z_{IN}	1		—	25.0	—	kΩ
S / N ratio	S / N_A	1	At A-Weight filter ON	88	92	—	dB
Total Harmonic Distortion + Noise	THD_A	1		—	-62	-77	dB
Cross-talk	CT_A	1	At A-Weight filter ON	—	−90	−85	dB
Output Offset	OFST	1	Input AC is short circuit	−100	0	+100	LSB

D / A converter

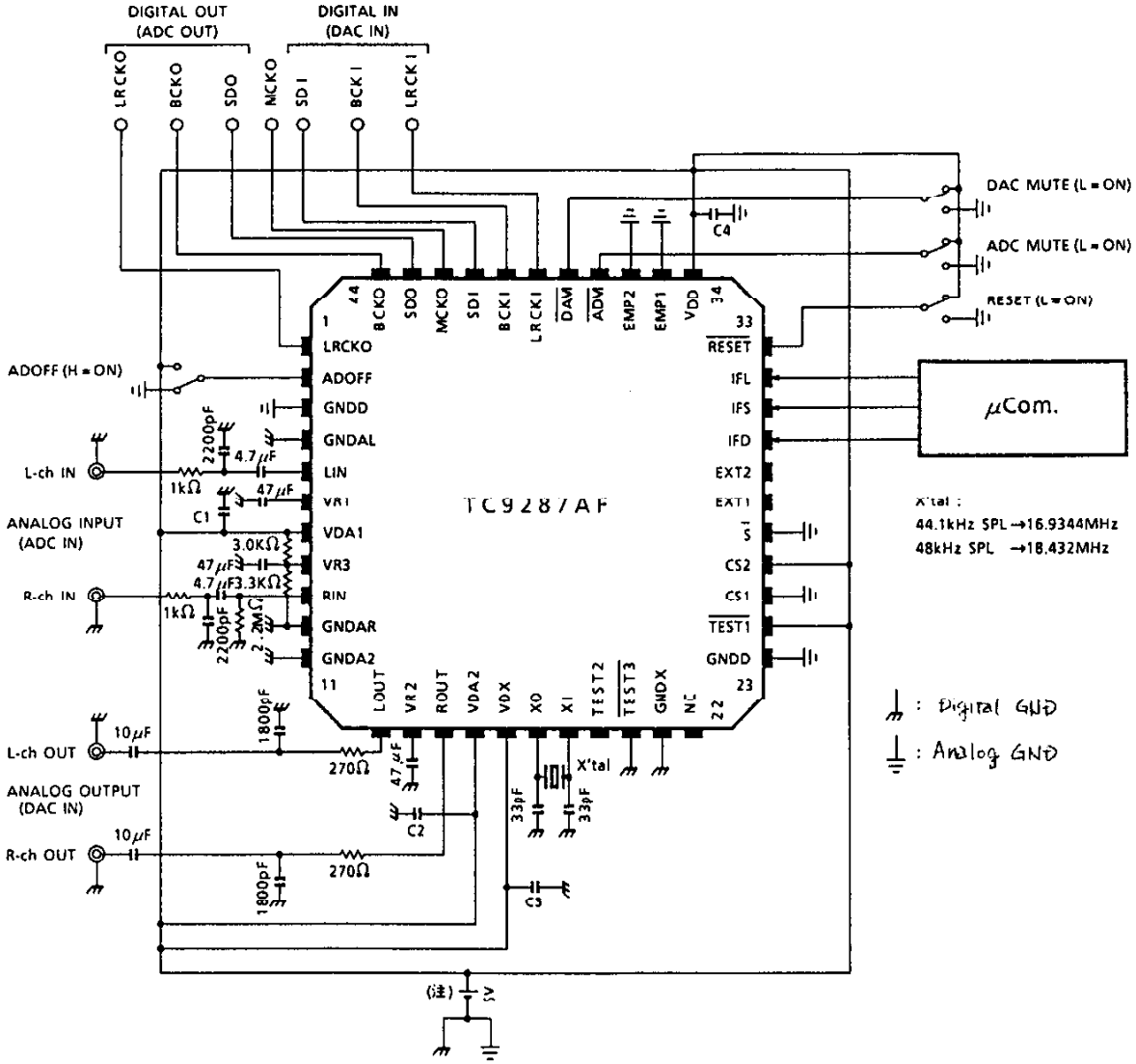
CHARACTERISTIC	SYMBOL	TEST CIR -CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Maximum output Voltage	V_{OM}	2	Output Voltage at full scale level input	—	1.25	—	Vrms
S / N ratio	S / N_D	2	At A-Weight filter ON	88	95	—	dB
Total Harmonic Distortion + Noise	THD_D	2		—	-87	-80	dB
Dynamic Range	DR_D	2	At A-Weight filter ON	85	92	—	dB
Cross-talk	CT_D	2	At A-Weight filter ON	—	−90	−85	dB

Common item

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating frequency		f_{opr}	—	$V_{DD}=V_{DA}=V_{DD} \geq 4.5V$	10	16.9344	19.2	MHz
Input frequency		f_{LRCKI}	—		30	44.1	100	kHz
		f_{BCKI}			1	1.41	6.2	
Rise Time of input signal		t_{ri}	—	LRCKI, BCKI terminal (10~90 %)	—	—	15	ns
Fall Time of input signal		t_{fi}	—		—	—	15	
Delay Time of input signal		t_{di}	—	The falling edge of BCKI → LRCKI, SDI	—	—	40	
MCU I / F	Rise Time of input signal	t_{riM}	—	IFL, IFS terminal (10~90 %)	—	—	15	
	Fall Time of input signal	t_{fiM}	—		—	—	15	
	Delay Time of input signal	t_{diM}	—	The falling edge of IFS → IFL, IFD	—	—	40	
Rise Time of output signal		t_{ro}	—	LRCKO, BCKO terminal (10~90 %)	—	—	15	
Fall Time of output signal		t_{fo}	—		—	—	15	
Delay Time of Output signal		t_{do}	—	The falling edge of BCKO → LRCKO, SDO	—	—	40	

APPLICATION CIRCUIT

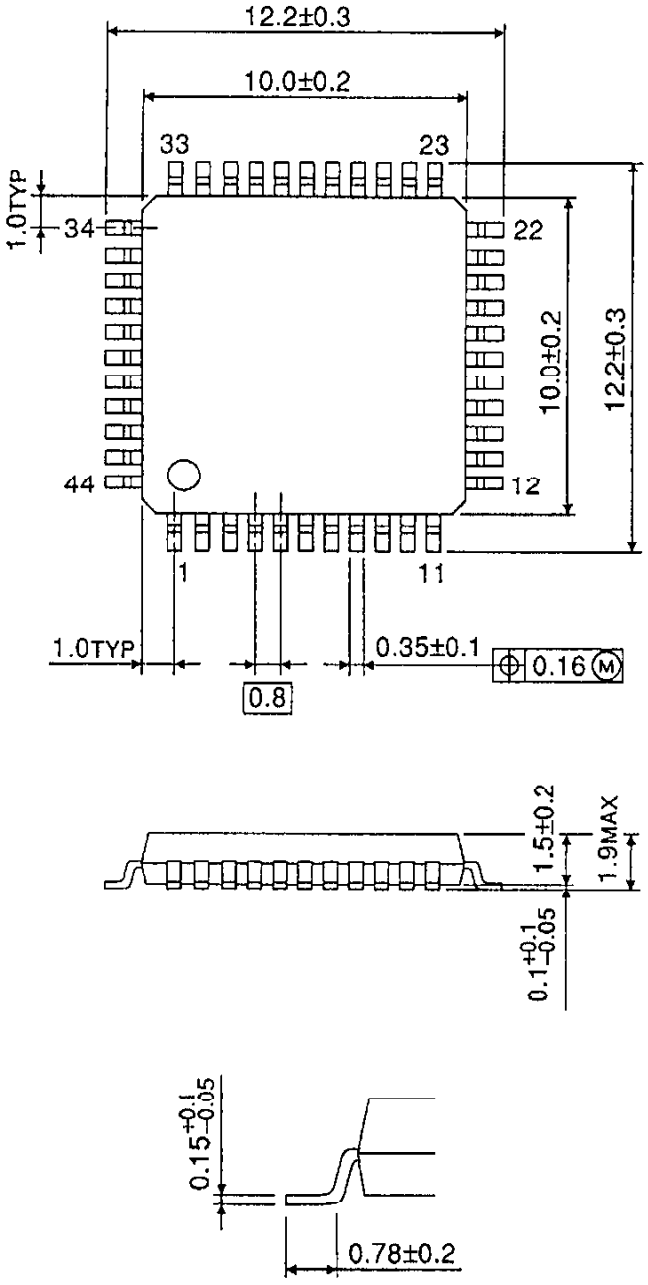
(use Crystal Oscillator)



OUTLINE DRAWING

QFP44-P-1010-0.80

Unit : mm



Weight : 0.5g (Typ.)