

FEATURES

Low supply current: 250 μ A max
Very low input bias current: 1 pA max
Low offset voltage: 750 μ V max
Single-supply operation: 5 V to 26 V
Dual-supply operation: ± 2.5 V to ± 13 V
Rail-to-rail output
Unity-gain stable
No phase reversal
SC70 package

APPLICATIONS

Line-/battery-powered instruments
Photodiode amplifiers
Precision current sensing
Medical instrumentation
Industrial controls
Precision filters
Portable audio
ATE

GENERAL DESCRIPTION

The AD8641/AD8642/AD8643 are low power, precision JFET input amplifiers featuring extremely low input bias current and rail-to-rail output. The ability to swing nearly rail-to-rail at the input and rail-to-rail at the output enables designers to buffer CMOS DACs, ASICs, and other wide output swing devices in single-supply systems. The outputs remain stable with capacitive loads of more than 500 pF.

The AD8641/AD8642/AD8643 are suitable for applications utilizing multichannel boards that require low power to manage heat. Other applications include photodiodes, ATE reference level drivers, battery management, and industrial controls.

The AD8641/AD8642/AD8643 are fully specified over the extended industrial temperature range of -40°C to $+125^{\circ}\text{C}$. The AD8641 is available in 5-lead SC70 and 8-lead SOIC lead-free packages. The AD8642 is available in 8-lead MSOP and 8-lead SOIC lead-free packages. The AD8643 is available in 14-lead SOIC and 16-lead, $3\text{ mm} \times 3\text{ mm}$, LFCSP lead-free packages.

PIN CONFIGURATIONS

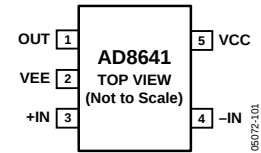


Figure 1. 5-Lead SC70 (KS-5)

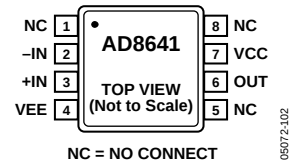


Figure 2. 8-Lead SOIC (R-8)

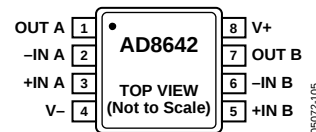


Figure 3. 8-Lead SOIC (R-8)

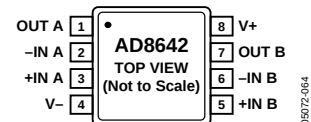


Figure 4. 8-Lead MSOP (RM-8)

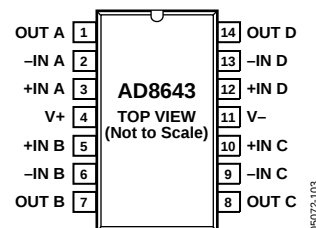


Figure 5. 14-Lead SOIC (R-14)

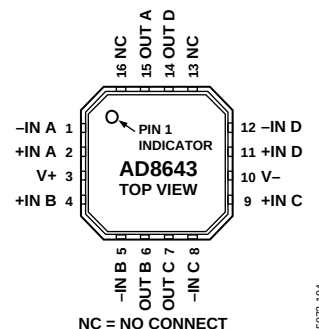


Figure 6. 16-Lead LFCSP (CP-16) (Not Drawn to Scale)

Rev. B

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REVISION HISTORY

4/05—Rev. A to Rev. B

Added AD8643 Universal

Added 14-Lead SOIC Universal

Added 16-Lead LFCSP..... Universal

Updated Outline Dimensions 13

Changes to Ordering Guide 14

10/04—Initial Version: Revision 0

3/05—Rev. 0 to Rev. A

Added AD8642 Universal

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Added Figure 3 and Figure 4..... 1

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

@ $V_S = 5.0\text{ V}$, $V_{CM} = 2.5\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	AD8643 LFCSP only $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $+85^\circ\text{C} < T_A < +125^\circ\text{C}$, $V_{CM} = 1.5\text{ V}$		50	750	μV
					1	mV
					1.5	mV
					1.6	mV
Input Bias Current	I_B	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.25	1	pA
Input Offset Current	I_{OS}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			180	pA
					0.5	pA
					60	pA
Input Voltage Range			0		3	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to } 2.5\text{ V}$	74	93		dB
Large Signal Voltage Gain	A_{VO}	$R_L = 10\text{ k}\Omega$, $V_O = 0.5\text{ to } 4.5\text{ V}$	80	140		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		2.5		$\mu\text{V}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$I_L = 1\text{ mA}$, $-40^\circ\text{C to } +125^\circ\text{C}$	4.95			V
			4.94			V
Output Voltage Low	V_{OL}	$I_L = 1\text{ mA}$, $-40^\circ\text{C to } +125^\circ\text{C}$			0.05	V
				0.01	0.05	V
Output Current	I_{OUT}			± 6		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = 5\text{ V to } 26\text{ V}$	90	107		dB
Supply Current/Amplifier	I_{SY}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		195	250	μA
					270	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	AD8641, AD8642 AD8643		2		V/ μs
Gain Bandwidth Product	GBP			3		MHz
				2.5		MHz
Phase Margin	ϕ_m			50		Degrees
NOISE PERFORMANCE						
Voltage Noise	$e_N\text{ p-p}$	$f = 0.1\text{ Hz to } 10\text{ Hz}$		4.0		$\mu\text{V p-p}$
Voltage Noise Density	e_N	$f = 1\text{ kHz}$		28.5		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	i_N	$f = 1\text{ kHz}$		0.5		fA/ $\sqrt{\text{Hz}}$

AD8641/AD8642/AD8643

@ $V_S = \pm 13$ V, $V_{CM} = 0$ V, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	AD8643 LFCSP only $-40^\circ < T_A < +125^\circ\text{C}$		70	750	μV
					1	mV
Input Bias Current	I_B	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.25	1.5	mV
					1	pA
Input Offset Current	I_{OS}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			260	pA
					0.5	pA
Input Voltage Range		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			65	pA
					+10	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -13$ V to $+10$ V	-13	90	107	dB
Large Signal Voltage Gain	A_{VO}	$R_L = 10$ k Ω , $V_O = -11$ V to $+11$ V	215	290		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		2.5		$\mu\text{V}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$I_L = 1$ mA, -40°C to $+125^\circ\text{C}$	+12.95			V
			+12.94			V
Output Voltage Low	V_{OL}	$I_L = 1$ mA, -40°C to $+125^\circ\text{C}$			-12.95	V
					-12.94	V
Output Current	I_{OUT}			± 12		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5$ V to ± 13 V	90	107		dB
Supply Current/Amplifier	I_{SY}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		200	290	μA
					330	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR			3		V/ μs
Gain Bandwidth Product	GBP			3.5		MHz
Phase Margin	ϕ_m			60		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_N p-p	$f = 0.1$ Hz to 10 Hz		4.2		μV p-p
Voltage Noise Density	e_N	$f = 1$ kHz		27.5		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	i_N	$f = 1$ kHz		0.5		fA/ $\sqrt{\text{Hz}}$

ABSOLUTE MAXIMUM RATINGS

Table 3.¹

Parameter	Rating
Supply Voltage	27.3 V
Input Voltage	VS– to VS+
Differential Input Voltage	±Supply Voltage
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
KS-5, R-8, RM-8, R-14, CP-16 Packages	–65°C to +150°C
Operating Temperature Range	–40°C to +125°C
Junction Temperature Range	
KS-5, R-8, RM-8, R-14, CP-16 Packages	–65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4.

Package Type	θ_{JA} ²	θ_{JC}	Unit
5-Lead SC70 (KS)	331.4	223.9	°C/W
8-Lead SOIC (R)	157	56	°C/W
8-Lead MSOP (RM)	206	44	°C/W
14-Lead SOIC (R)	120	36	°C/W
16-Lead LFCSP (CP)	44	31.5	°C/W

¹ Absolute maximum ratings apply at 25°C, unless otherwise noted.

² θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for devices soldered on circuit boards for surface-mounted packages.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



TYPICAL PERFORMANCE CHARACTERISTICS

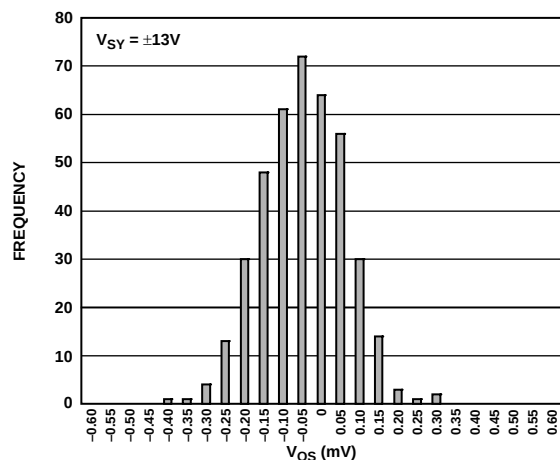


Figure 7. Input Offset Voltage

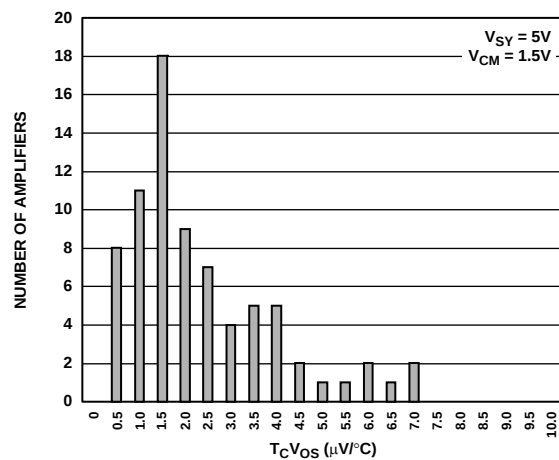


Figure 10. Offset Voltage Drift

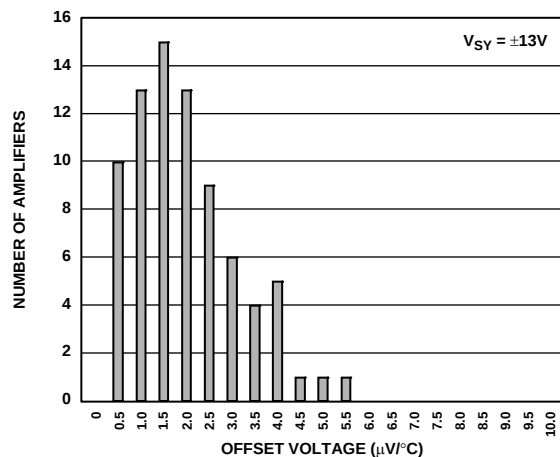


Figure 8. Offset Voltage Drift

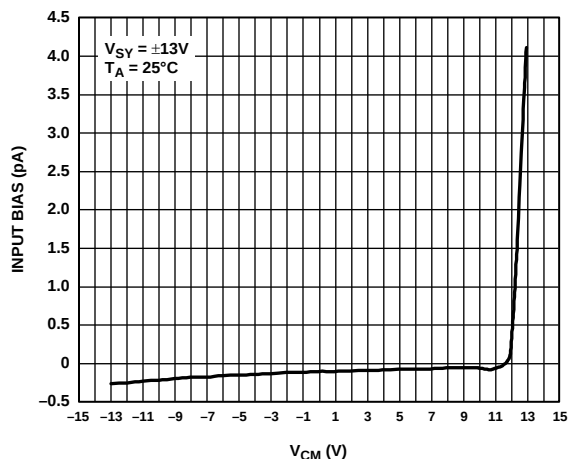
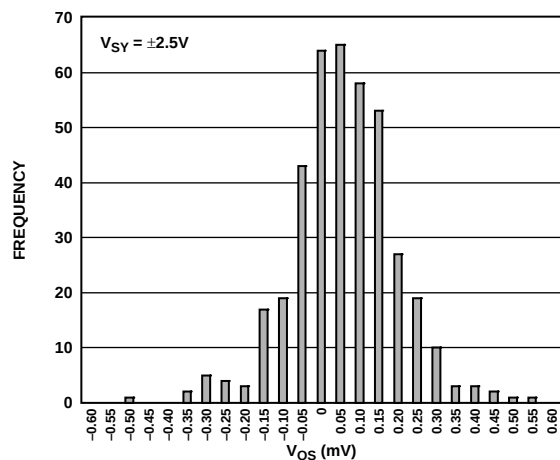
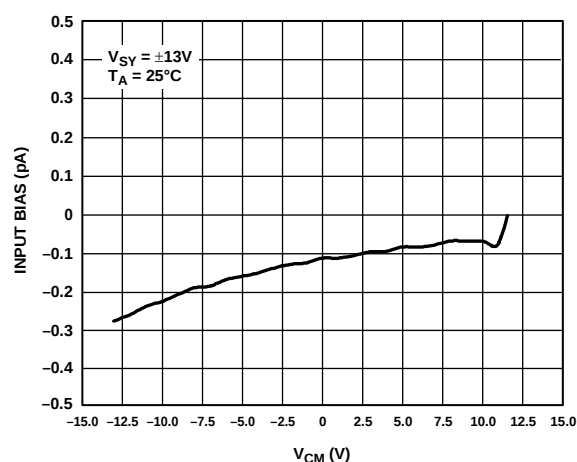
Figure 11. Input Bias Current vs. V_{CM} 

Figure 9. Input Offset Voltage

Figure 12. Input Bias Current vs. V_{CM}

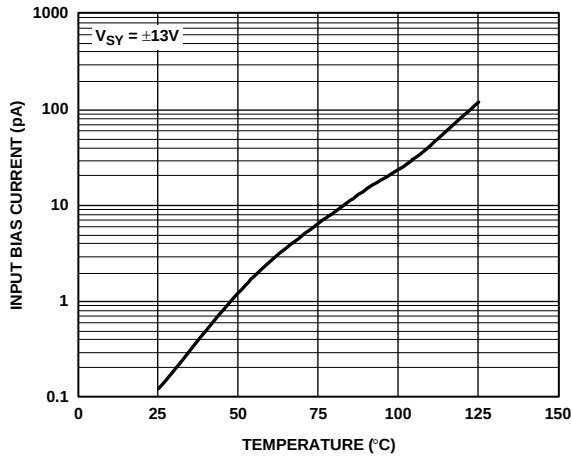


Figure 13. Input Bias Current vs. Temperature

05072-008

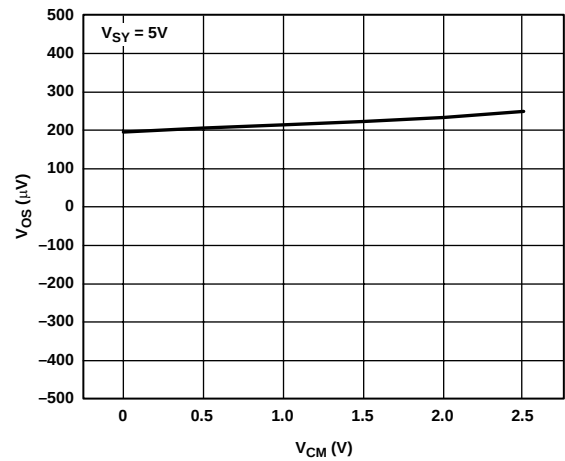


Figure 16. Input Offset Voltage vs. V_{CM}

05072-011

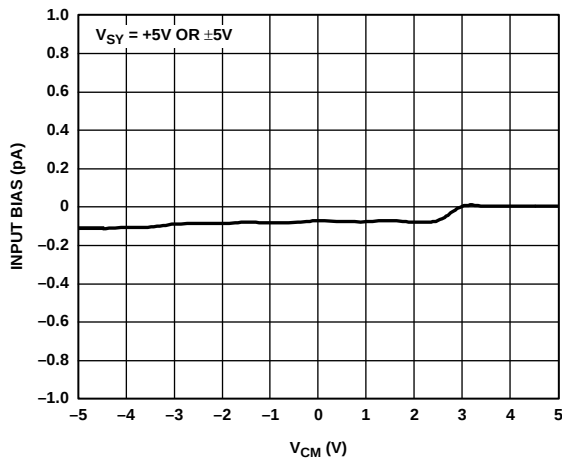


Figure 14. Input Bias Current vs. V_{CM}

05072-009

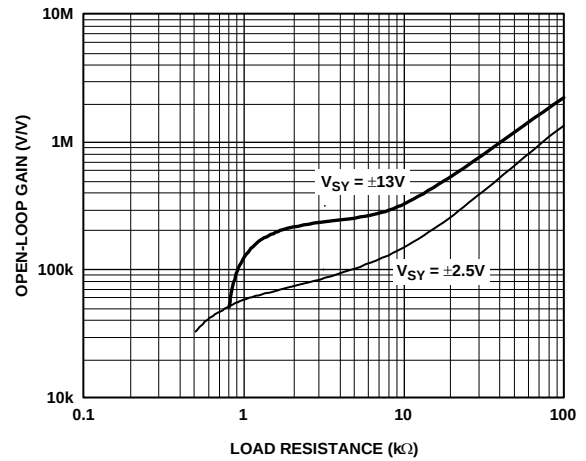


Figure 17. Open-Loop Gain vs. Load Resistance

05072-012

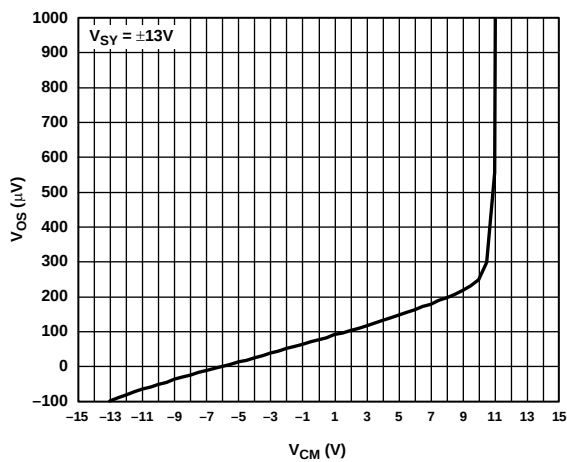


Figure 15. Input Offset Voltage vs. V_{CM}

05072-010

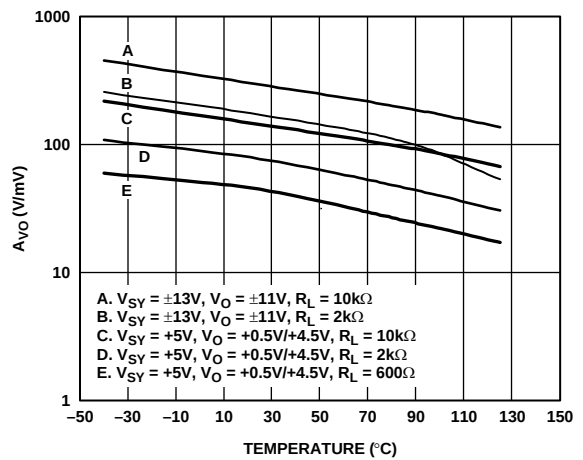


Figure 18. Open-Loop Gain vs. Temperature

05072-013

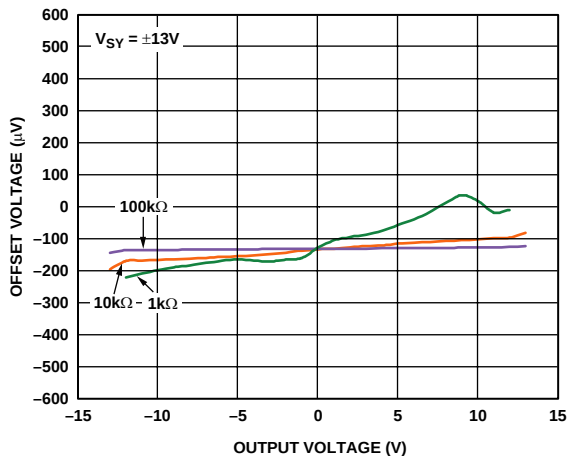


Figure 19. Input Error Voltage vs. Output Voltage for Resistive Loads

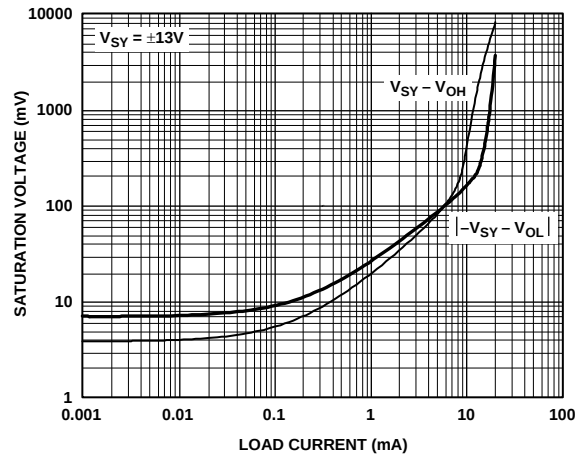


Figure 22. Output Saturation Voltage vs. Load Current

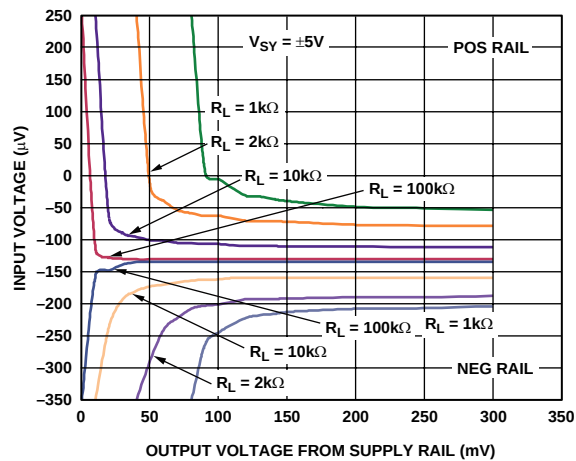


Figure 20. Input Error Voltage vs. Output Voltage Within 300 mV of Supply Rails

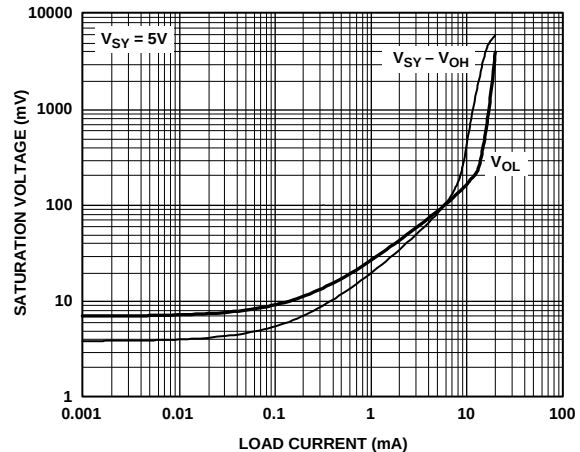


Figure 23. Output Saturation Voltage vs. Load Current

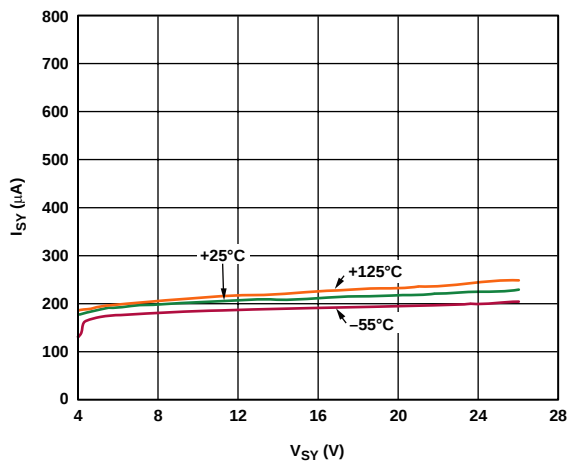


Figure 21. Quiescent Current vs. Supply Voltage at Different Temperatures

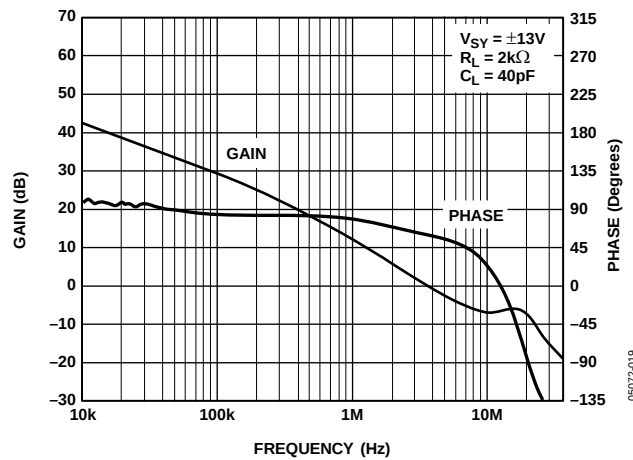


Figure 24. Open-Loop Gain and Phase Margin vs. Frequency

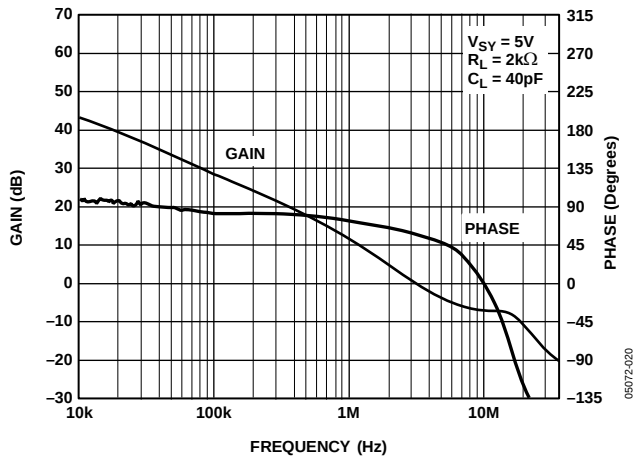


Figure 25. Open-Loop Gain and Phase Margin vs. Frequency

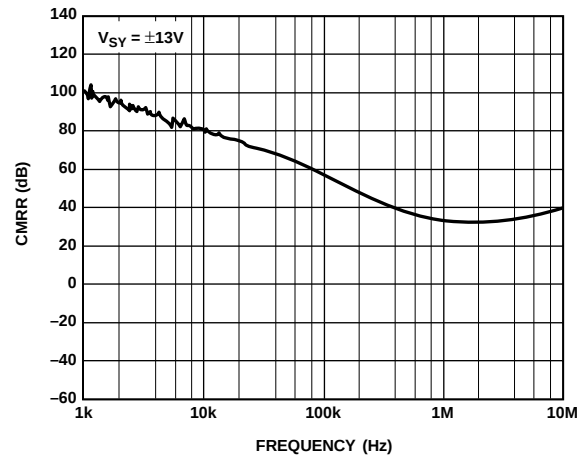


Figure 28. CMRR vs. Frequency

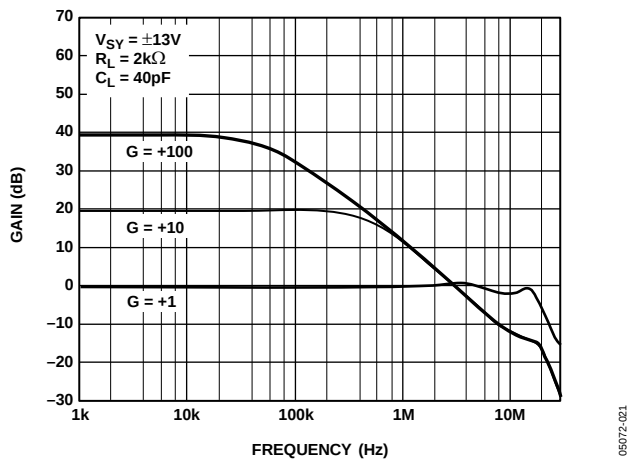


Figure 26. Closed-Loop Gain vs. Frequency

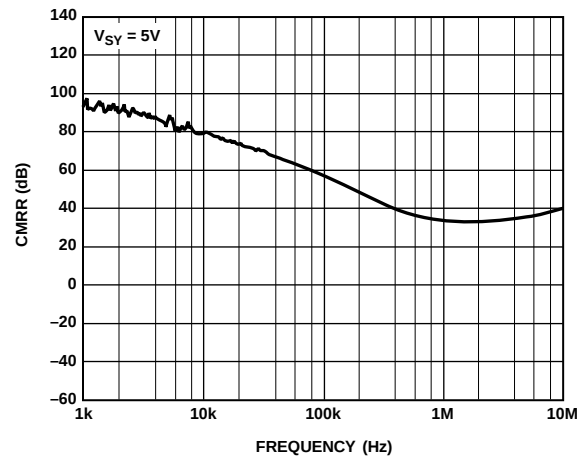


Figure 29. CMRR vs. Frequency

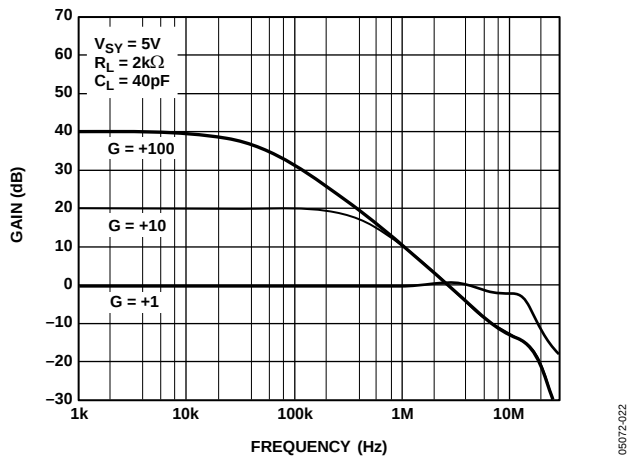


Figure 27. Closed-Loop Gain vs. Frequency

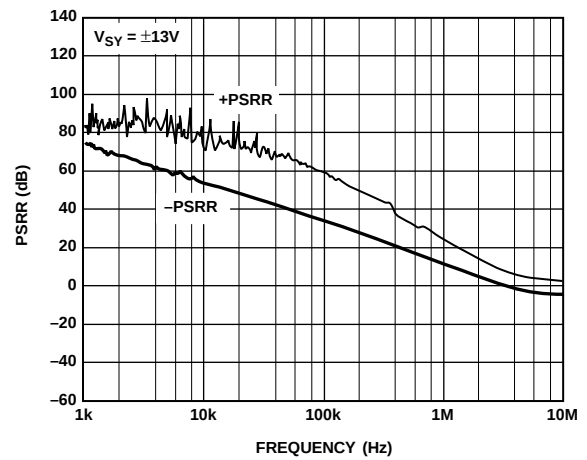


Figure 30. PSRR vs. Frequency

AD8641/AD8642/AD8643

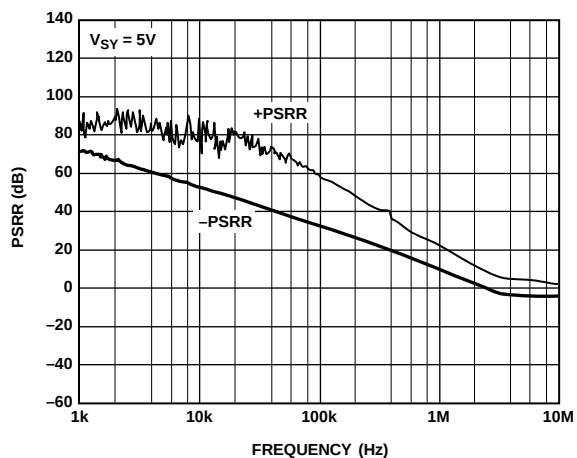


Figure 31. PSRR vs. Frequency

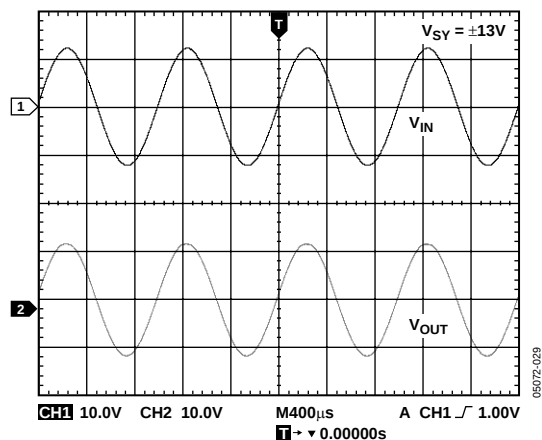


Figure 34. No Phase Reversal

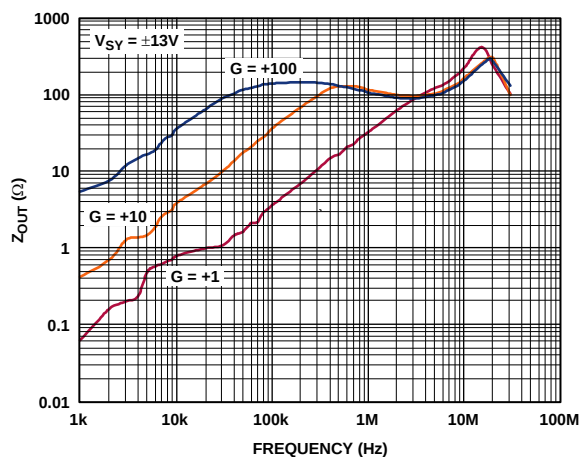


Figure 32. Output Impedance vs. Frequency

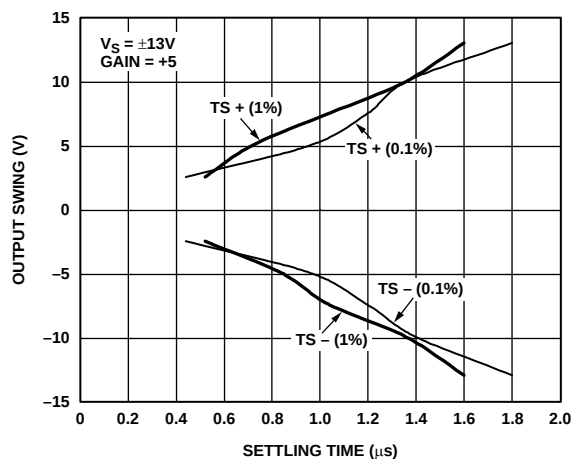


Figure 35. Output Swing and Error vs. Settling Time

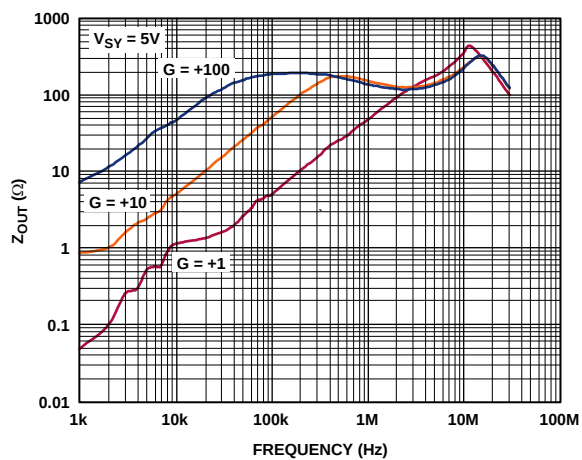


Figure 33. Output Impedance vs. Frequency

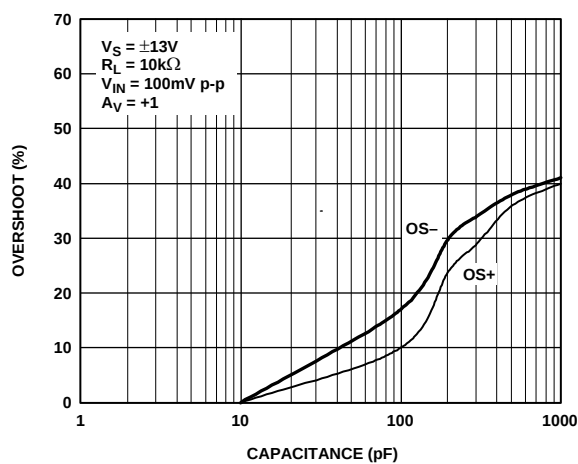


Figure 36. Small Signal Overshoot vs. Load Capacitance

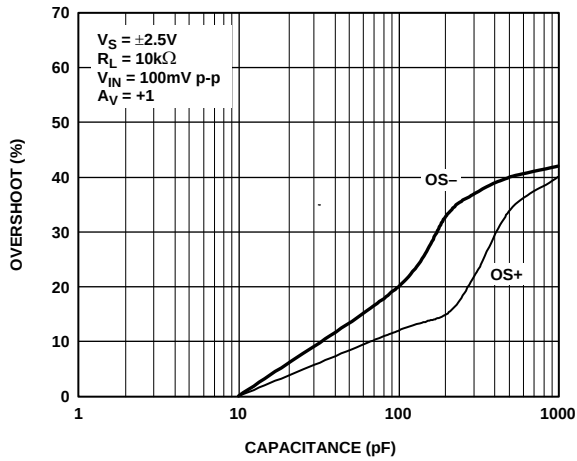


Figure 37. Small Signal Overshoot vs. Load Capacitance

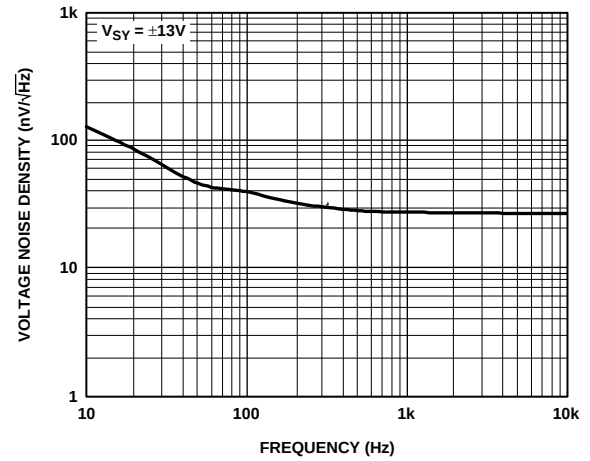


Figure 40. Voltage Noise Density

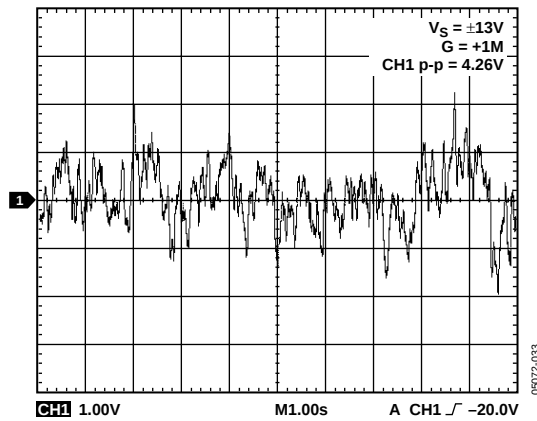


Figure 38. 0.1 Hz to 10 Hz Noise

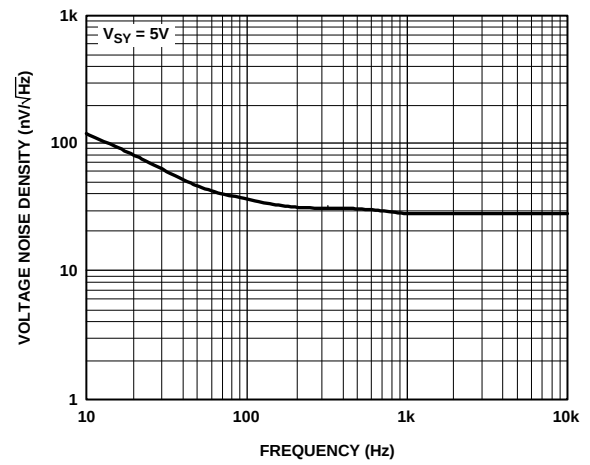


Figure 41. Voltage Noise Density

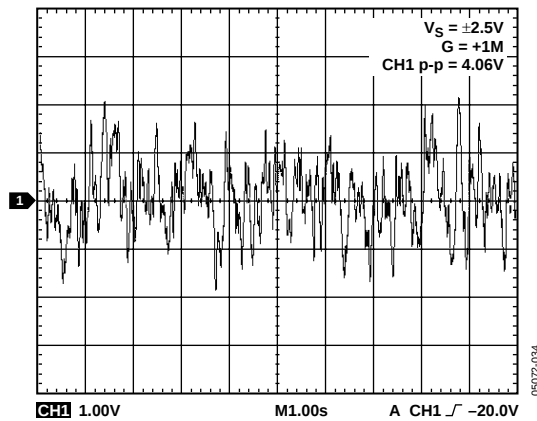


Figure 39. 0.1 Hz to 10 Hz Noise

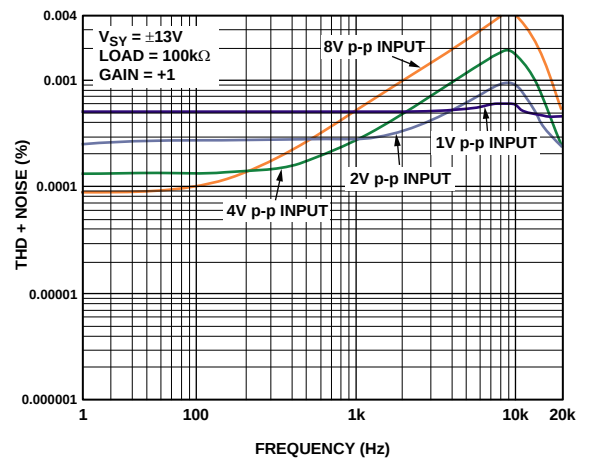


Figure 42. Total Harmonic Distortion + Noise vs. Frequency

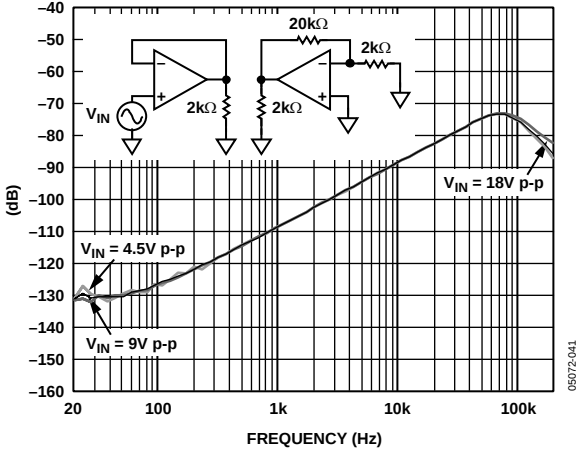


Figure 43. Channel Separation

OUTLINE DIMENSIONS

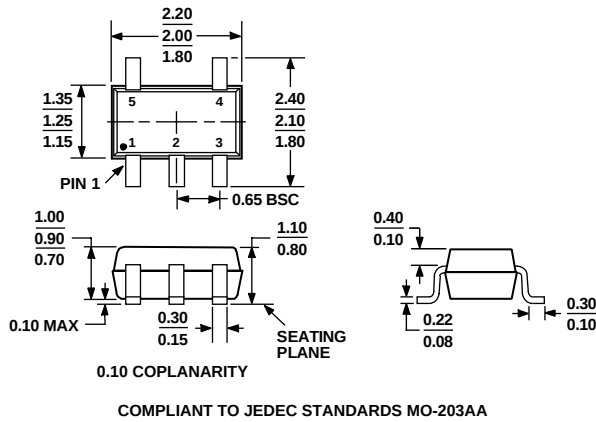


Figure 44. 5-Lead Thin Shrink Small Outline Transistor Package [SC70] (KS-5)
Dimensions shown in millimeters

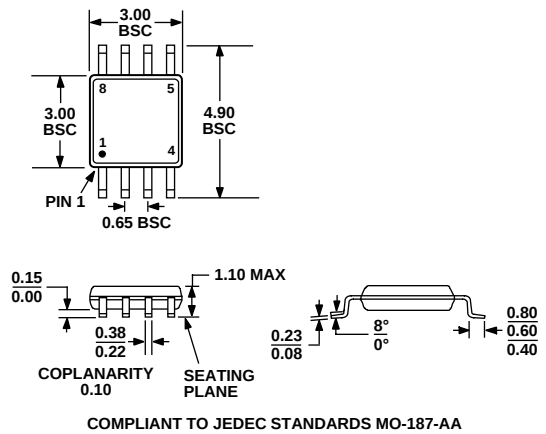
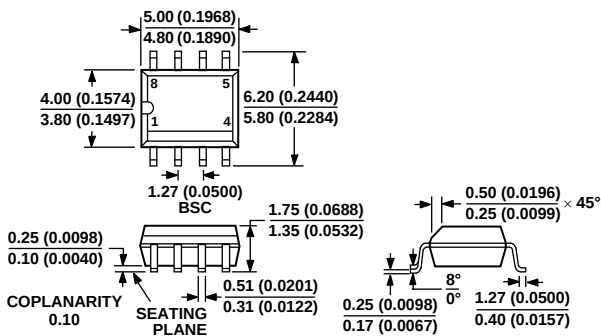
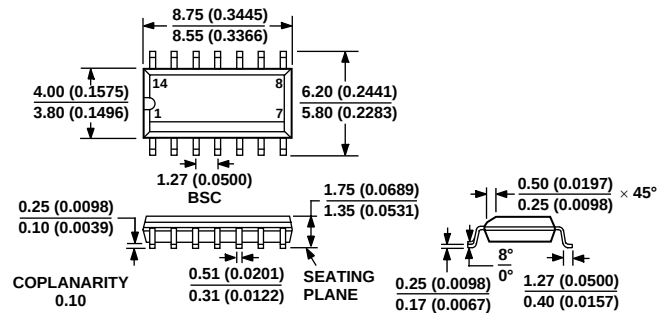


Figure 46. 8-Lead Mini Small Outline Package [MSOP] (RM-8)
Dimensions shown in millimeters



CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

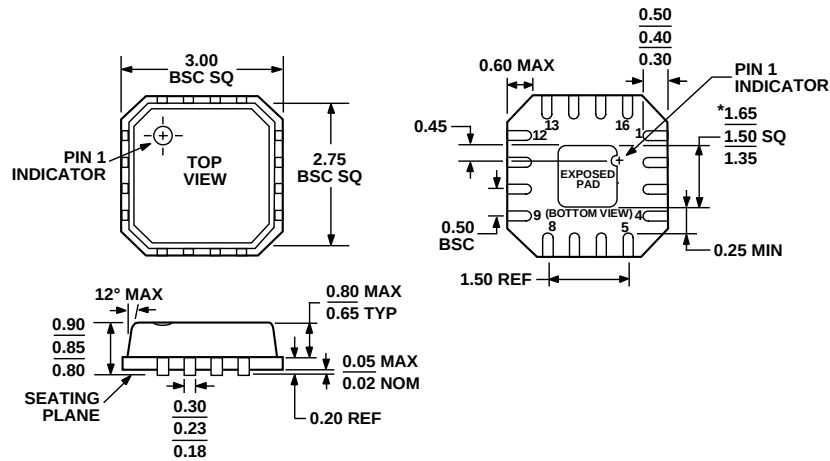
Figure 45. 8-Lead Standard Small Outline Package [SOIC_N] (R-8)
Dimensions shown in millimeters and (inches)



CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 47. 14-Lead Standard Small Outline Package [SOIC_N] (R-14)
Dimensions shown in millimeters and (inches)

AD8641/AD8642/AD8643



*COMPLIANT TO JEDEC STANDARDS MO-220-VEED-2
EXCEPT FOR EXPOSED PAD DIMENSION.

Figure 48. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
3 mm x 3 mm Body, Very Thin Quad (CP-16-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8641AKSZ-R2 ¹	-40°C to +125°C	5-Lead SC70	KS-5	A07
AD8641AKSZ-REEL7 ¹	-40°C to +125°C	5-Lead SC70	KS-5	A07
AD8641AKSZ-REEL ¹	-40°C to +125°C	5-Lead SC70	KS-5	A07
AD8641ARZ ¹	-40°C to +125°C	8-lead SOIC_N	R-8	
AD8641ARZ-REEL7 ¹	-40°C to +125°C	8-lead SOIC_N	R-8	
AD8641ARZ-REEL ¹	-40°C to +125°C	8-lead SOIC_N	R-8	
AD8642ARMZ-R2 ¹	-40°C to +125°C	8-lead MSOP	RM-8	A0A
AD8642ARMZ-REEL ¹	-40°C to +125°C	8-lead MSOP	RM-8	A0A
AD8642ARZ ¹	-40°C to +125°C	8-lead SOIC_N	R-8	
AD8642ARZ-REEL7 ¹	-40°C to +125°C	8-lead SOIC_N	R-8	
AD8642ARZ-REEL ¹	-40°C to +125°C	8-lead SOIC_N	R-8	
AD8643ARZ ¹	-40°C to +125°C	14-lead SOIC_N	R-14	
AD8643ARZ-REEL7 ¹	-40°C to +125°C	14-lead SOIC_N	R-14	
AD8643ARZ-REEL ¹	-40°C to +125°C	14-lead SOIC_N	R-14	
AD8643ACPZ-R2 ¹	-40°C to +125°C	16-Lead LFCSP_VQ	CP-16-3	AUA
AD8643ACPZ-REEL7 ¹	-40°C to +125°C	16-Lead LFCSP_VQ	CP-16-3	AUA
AD8643ACPZ-REEL ¹	-40°C to +125°C	16-Lead LFCSP_VQ	CP-16-3	AUA

¹ Z = Pb-free part.

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