

**MOS
LSI**

TMS 4062 JL, NL; TMS 4063 JL, NL **1024-WORD BY 1-BIT DYNAMIC RAM**

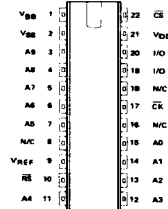
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- 1024 x 1 Organization
- Access Time . . . 130 ns Maximum
- Cycle Time . . . 200 ns Maximum
- Low Power Dissipation:
 Operating . . . 120 mW Typical
 Standby . . . 2 mW Typical
- Differential Output
- Wire-OR Capability
- Chip Select For Simplified Memory Expansion
- 22-Pin or 18-Pin Dual-In-Line Package

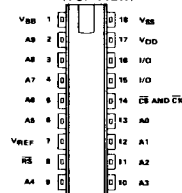
description and operation

The TMS 4062 JL, NL and TMS 4063 JL, NL are fabricated on a single monolithic chip with P-channel enhancement type MOS processing. The devices are designed for use in low-cost, high performance memory applications. Data is read or written through 2 input/output terminals. Clock and chip-select clock pulses allow the transfer of information to or from input/output lines. Refresh must occur at least once every 2 milliseconds.

TMS 4062 JL, NL
22-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



TMS 4063 JL, NL
18-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltages:

V _{DD} and V _{REF} , with respect to V _{SS}	-27 V to 0.5 V
V _{DD} and V _{REF} , with respect to V _{BB}	-30 V to 0.5 V
V _{BB} , with respect to V _{SS}	-0.5 V to 10 V
All input voltages, with respect to V _{SS}	-30 V to 0.5 V
Operating free-air temperature range	-0°C to 70°C
Storage temperature range	-55°C to 125°C

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V _{BB} -V _{SS} (see Notes 1 and 2)	2.3	2.5	2.7	V
Supply voltage, V _{DD}		0		V
Supply voltage, V _{SS}	19	20	21	V
Supply voltage, V _{REF}	6.6	7	7.4	V
High-level input voltage, all inputs, V _{IH}	V _{SS} - 2		V _{SS}	V
Low-level address input voltage, V _{IL(ad)} (see Note 3)	-2	0	1	V
Low-level input voltage at reset and both clocks, V _{IL(rs, ck)} (see Note 3)	-5	0	0.4	V
Low-level input voltage at I/O, V _{IL(I/O)}	V _{REF} - 1	V _{REF}	V _{REF} + 1	V
Refresh time, t _{refresh}			2	ms
Operating free-air temperature, T _A	0		70	°C

- NOTES: 1. Throughout this data sheet supply voltage values are with respect to V_{DD}, unless otherwise noted.
 2. V_{BB} must be applied prior to V_{SS}.
 3. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only.

100

PRELIMINARY DATA SHEET:
 Supplementary data will be
 published at a later date.

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