



**National
Semiconductor**

LF155/LF156/LF157 Series Monolithic JFET Input Operational Amplifiers

**LF155/LF155A/LF255/LF355/LF355A/
LF355B Low Supply Current
LF156/LF156A/LF256/LF356/LF356A/
LF356B Wide Band
LF157/LF157A/LF257/LF357/LF357A/
LF357B Wide Band Decompensated ($A_{V\text{MIN}} = 5$)**

General Description

These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (Bi-FET™ Technology). These amplifiers feature low input bias and offset currents/low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low $1/f$ noise corner.

Advantages

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance—very low $1/f$ corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (10,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

Applications

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers

- Photocell amplifiers
- Sample and Hold circuits

Common Features

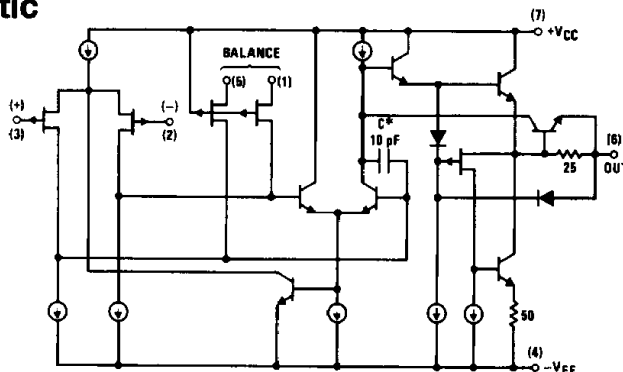
(LF155A, LF156A, LF157A)

- Low input bias current 30 pA
- Low Input Offset Current 3 pA
- High input impedance $10^{12}\Omega$
- Low input offset voltage 1 mV
- Low input offset voltage temp. drift $3 \mu\text{V}/^\circ\text{C}$
- Low input noise current $0.01 \text{ pA}/\sqrt{\text{Hz}}$
- High common-mode rejection ratio 100 dB
- Large dc voltage gain 106 dB

Uncommon Features

	LF155A	LF156A	LF157A ($A_V = 5$)	Units
■ Extremely fast settling time to 0.01%	4	1.5	1.5	μs
■ Fast slew rate	5	12	50	$\text{V}/\mu\text{s}$
■ Wide gain bandwidth	2.5	5	20	MHz
■ Low input noise voltage	20	12	12	$\text{nV}/\sqrt{\text{Hz}}$

Simplified Schematic



*3 pF in LF157 series.

TL/H/5846-1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 8)

	LF155A/6A/7A	LF155/6/7	LF355B/6B/7B LF255/6/7	LF355/6/7 LF355A/6A/7A
Supply Voltage	±22V	±22V	±22V	±18V
Differential Input Voltage	±40V	±40V	±40V	±30V
Input Voltage Range (Note 2)	±20V	±20V	±20V	±16V
Output Short Circuit Duration	Continuous	Continuous	Continuous	Continuous
T_{JMAX}				
H-Package	150°C	150°C	115°C	115°C
N-Package			100°C	100°C
J-Package		150°C	115°C	115°C
M-Package			100°C	100°C
Power Dissipation at $T_A = 25^\circ\text{C}$ (Notes 1 and 9)				
H-Package (Still Air)	560 mW	560 mW	400 mW	400 mW
H-Package (400 LF/Min Air Flow)	1200 mW	1200 mW	1000 mW	1000 mW
N-Package			670 mW	670 mW
J-Package		1260 mW	900 mW	900 mW
M-Package			380 mW	380 mW
Thermal Resistance (Typical) θ_{JA}				
H-Package (Still Air)	160°C/W	160°C/W	160°C/W	160°C/W
H-Package (400 LF/Min Air Flow)	65°C/W	65°C/W	65°C/W	65°C/W
N-Package			130°C/W	130°C/W
J-Package		100°C/W	100°C/W	100°C/W
M-Package			195°C/W	195°C/W
(Typical) θ_{JC}				
H-Package	23°C/W	23°C/W	23°C/W	23°C/W
Storage Temperature Range	-65°C to +150°C	-65°C to +150°C	-65°C to +150°C	-65°C to +150°C
Soldering Information (Lead Temp.)				
Metal Can Package				
Soldering (10 sec.)	300°C	300°C	300°C	300°C
Dual-In-Line Package				
Soldering (10 sec.)		260°C	260°C	260°C
Small Outline Package				
Vapor Phase (60 sec.)			215°C	215°C
Infrared (15 sec.)			220°C	220°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.				
ESD tolerance				
(100 pF discharged through 1.5 k Ω)	1200V	1200V	1200V	1200V

DC Electrical Characteristics (Note 3) $T_A = T_J = 25^\circ\text{C}$

Symbol	Parameter	Conditions	LF155A/6A/7A			LF355A/6A/7A			Units
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25^\circ\text{C}$ Over Temperature		1	2 2.5		1	2 2.3	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		3	5		3	5	$\mu\text{V}/^\circ\text{C}$
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5		$\mu\text{V}/^\circ\text{C}$ per mV
I_{OS}	Input Offset Current	$T_J = 25^\circ\text{C}$, (Notes 3, 5) $T_J \leq T_{HIGH}$		3	10 10		3	10 1	pA nA
I_B	Input Bias Current	$T_J = 25^\circ\text{C}$, (Notes 3, 5) $T_J \leq T_{HIGH}$		30	50 25		30	50 5	pA nA
R_{IN}	Input Resistance	$T_J = 25^\circ\text{C}$		10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15\text{V}$, $T_A = 25^\circ\text{C}$ $V_O = \pm 10\text{V}$, $R_L = 2\text{k}$ Over Temperature	50 25	200		50 25	200		V/mV V/mV
V_O	Output Voltage Swing	$V_S = \pm 15\text{V}$, $R_L = 10\text{k}$ $V_S = \pm 15\text{V}$, $R_L = 2\text{k}$	±12 ±10	±13 ±12		±12 ±10	±13 ±12		V V

DC Electrical Characteristics (Note 3) $T_A = T_J = 25^\circ\text{C}$ (Continued)

Symbol	Parameter	Conditions	LF155A/6A/7A			LF355A/6A/7A			Units
			Min	Typ	Max	Min	Typ	Max	
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15\text{V}$	± 11	+15.1 -12		± 11	+15.1 -12		V V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		dB

AC Electrical Characteristics $T_A = T_J = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$

Symbol	Parameter	Conditions	LF155A/355A			LF156A/356A			LF157A/357A			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SR	Slew Rate	LF155A/6A; $A_V = 1$, LF157A; $A_V = 5$	3	5		10	12		40	50		V/ μs V/ μs
GBW	Gain Bandwidth Product			2.5		4	4.5		15	20		MHz
t_s	Settling Time to 0.01%	(Note 7)		4			1.5			1.5		μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$ $f = 100\text{ Hz}$ $f = 1000\text{ Hz}$		25 25			15 12			15 12		nV/ $\sqrt{\text{Hz}}$ nV/ $\sqrt{\text{Hz}}$
i_n	Equivalent Input Noise Current	$f = 100\text{ Hz}$ $f = 1000\text{ Hz}$		0.01 0.01			0.01 0.01			0.01 0.01		pA/ $\sqrt{\text{Hz}}$ pA/ $\sqrt{\text{Hz}}$
C_{IN}	Input Capacitance			3			3			3		pF

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	LF155/6/7			LF255/6/7 LF355B/6B/7B			LF355/6/7			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25^\circ\text{C}$ Over Temperature		3	5 7		3	5 6.5		3	10 13	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		5			5			5		$\mu\text{V}/^\circ\text{C}$
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5			0.5		$\mu\text{V}/^\circ\text{C}$ per mV
I_{OS}	Input Offset Current	$T_J = 25^\circ\text{C}$, (Notes 3, 5) $T_J \leq T_{HIGH}$		3	20 20		3	20 1		3	50 2	pA nA
I_B	Input Bias Current	$T_J = 25^\circ\text{C}$, (Notes 3, 5) $T_J \leq T_{HIGH}$		30	100 50		30	100 5		30	200 8	pA nA
R_{IN}	Input Resistance	$T_J = 25^\circ\text{C}$		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15\text{V}$, $T_A = 25^\circ\text{C}$ $V_O = \pm 10\text{V}$, $R_L = 2\text{k}$ Over Temperature	50 25	200		50 25	200		25 15	200		V/mV V/mV
V_O	Output Voltage Swing	$V_S = \pm 15\text{V}$, $R_L = 10\text{k}$ $V_S = \pm 15\text{V}$, $R_L = 2\text{k}$	± 12 ± 10	± 13 ± 12		± 12 ± 10	± 13 ± 12		± 12 ± 10	± 13 ± 12		V V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15\text{V}$	± 11	+15.1 -12		± 11	+15.1 -12		+10	+15.1 -12		V V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		80	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		80	100		dB

DC Electrical Characteristics $T_A = T_j = 25^\circ\text{C}, V_S = \pm 15\text{V}$

Parameter	LF155A/155, LF255, LF355A/355B		LF355		LF156A/156, LF256/356B		LF356A/356		LF157A/157, LF257/357B		LF357A/357		Units
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Supply Current	2	4	2	4	5	7	5	10	5	7	5	10	mA

AC Electrical Characteristics $T_A = T_j = 25^\circ\text{C}, V_S = \pm 15\text{V}$

Symbol	Parameter	Conditions	LF155/255/355/355B	LF156/256, LF356B	LF156/256/356/356B	LF157/257, LF357B	LF157/257/357/357B	Units
			Typ	Min	Typ	Min	Typ	
SR	Slew Rate	LF155/6: $A_V = 1$, LF157: $A_V = 5$	5	7.5	12	30	50	V/ μs V/ μs
GBW	Gain Bandwidth Product		2.5		5		20	MHz
t_s	Settling Time to 0.01%	(Note 7)	4		1.5		1.5	μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$ $f = 100\text{ Hz}$ $f = 1000\text{ Hz}$	25 20		15 12		15 12	nV/ $\sqrt{\text{Hz}}$ nV/ $\sqrt{\text{Hz}}$
i_n	Equivalent Input Current Noise	$f = 100\text{ Hz}$ $f = 1000\text{ Hz}$	0.01 0.01		0.01 0.01		0.01 0.01	pA/ $\sqrt{\text{Hz}}$ pA/ $\sqrt{\text{Hz}}$
C_{IN}	Input Capacitance		3		3		3	pF

Notes for Electrical Characteristics

Note 1: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by $T_{j\text{MAX}}$, θ_{JA} , and the ambient temperature, T_A . The maximum available power dissipation at any temperature is $P_d = (T_{j\text{MAX}} - T_A) / \theta_{JA}$ or the $25^\circ\text{C } P_{d\text{MAX}}$, whichever is less.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: Unless otherwise stated, these test conditions apply:

	LF155A/6A/7A LF155//6/7	LF255//6/7	LF355A/6A/7A	LF355B/6B/7B	LF355//6/7
Supply Voltage, V_S	$\pm 15\text{V} \leq V_S \leq \pm 20\text{V}$	$\pm 15\text{V} \leq V_S \leq \pm 20\text{V}$	$\pm 15\text{V} \leq V_S \leq \pm 18\text{V}$	$\pm 15\text{V} \leq V_S \leq \pm 20\text{V}$	$V_S = \pm 15\text{V}$
T_A	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	$-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$	$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$	$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$
T_{HIGH}	$+125^\circ\text{C}$	$+85^\circ\text{C}$	$+70^\circ\text{C}$	$+70^\circ\text{C}$	$+70^\circ\text{C}$

and V_{OS} , I_B and I_{OS} are measured at $V_{CM} = 0$.

Note 4: The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5 $\mu\text{V}/^\circ\text{C}$ typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j . Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_d . $T_j = T_A + \theta_{JA} P_d$ where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 6: Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

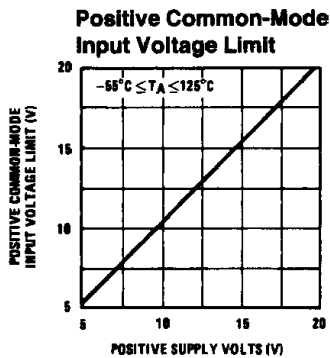
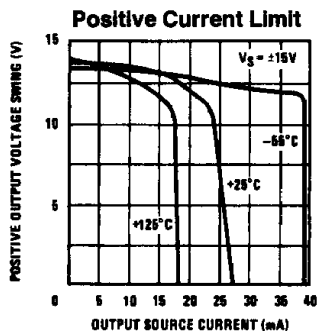
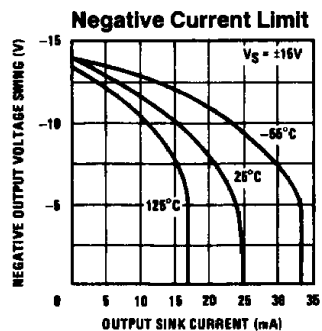
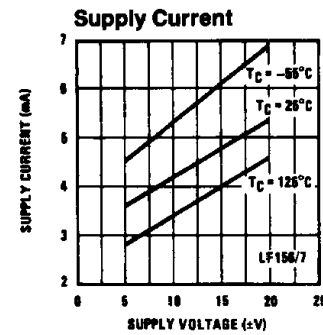
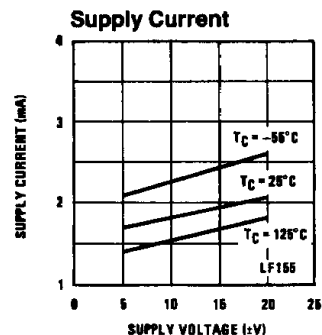
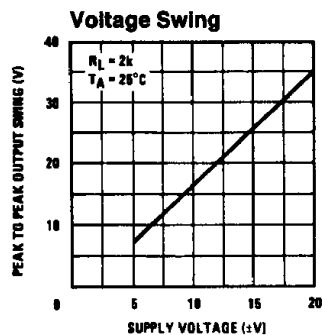
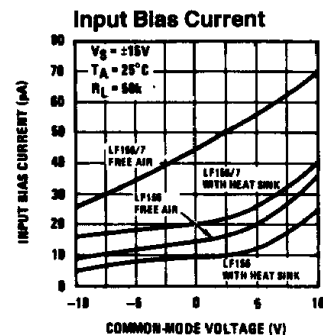
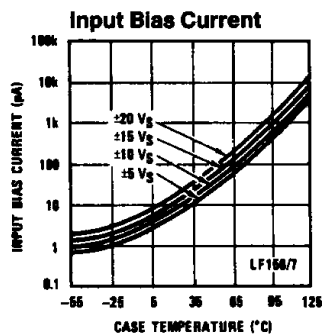
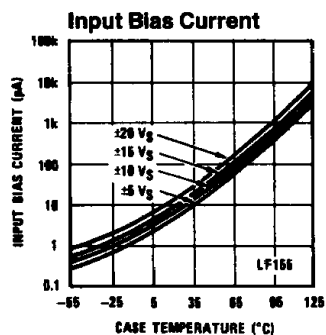
Note 7: Settling time is defined here, for a unity gain inverter connection using 2 k Ω resistors for the LF155/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF157, $A_V = -5$, the feedback resistor from output to input is 2 k Ω and the output step is 10V (See Settling Time Test Circuit).

Note 8: Refer to RETS155AX for LF155A, RETS155X for LF155, RETSF156AX for LF156A, RETS156X for LF156, RETS157A for LF157A and RETS157X for LF157 military specifications.

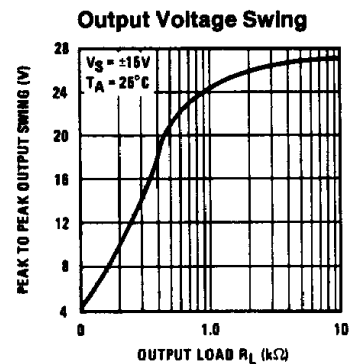
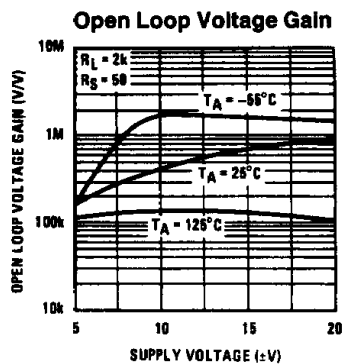
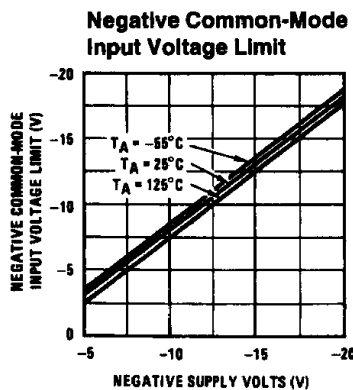
Note 9: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Typical DC Performance Characteristics

Curves are for LF155, LF156 and LF157 unless otherwise specified.



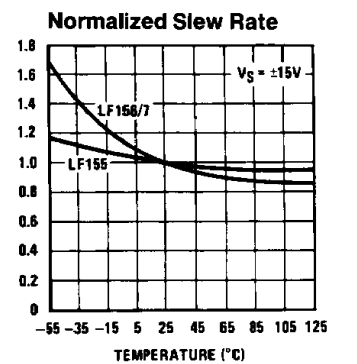
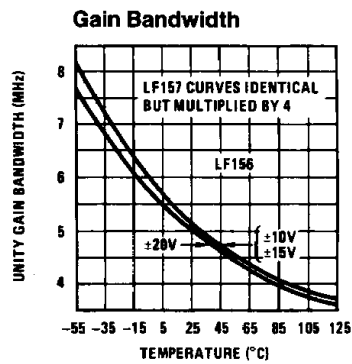
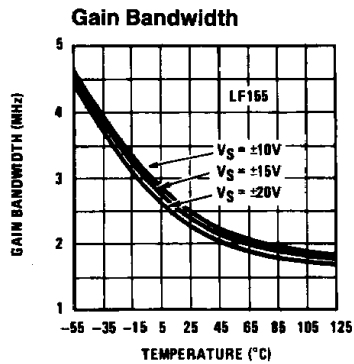
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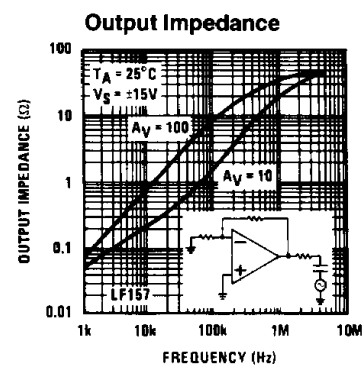
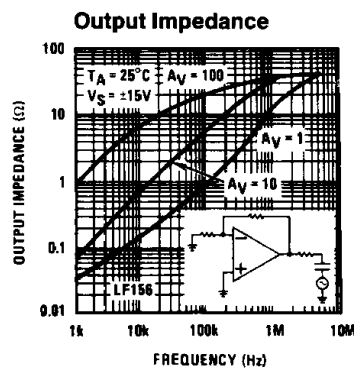
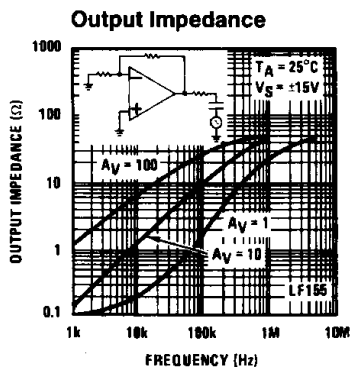
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Typical AC Performance Characteristics

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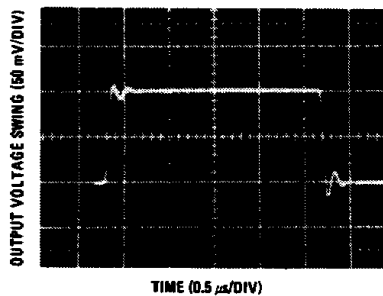


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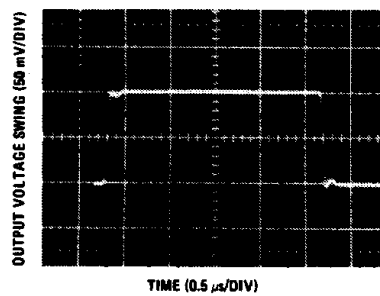
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LF155 Small Signal Pulse Response, $A_V = +1$



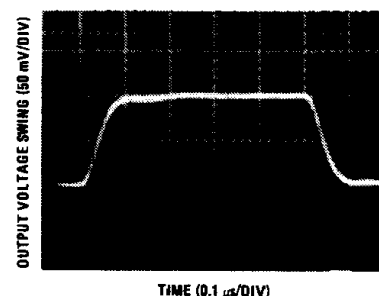
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LF156 Small Signal Pulse Response, $A_V = +1$



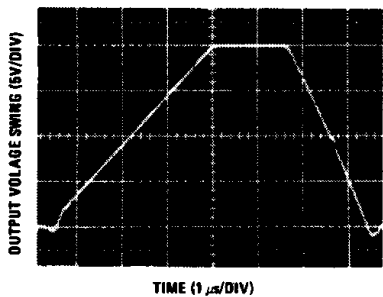
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Small Signal Pulse Response, $A_V = +5$



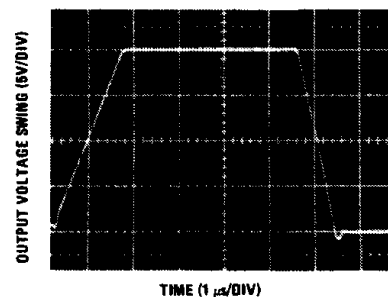
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LF155 Large Signal Pulse Response, $A_V = +1$



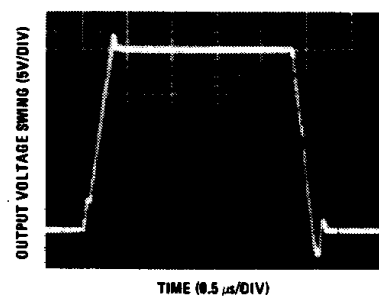
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LF156 Large Signal Pulse Response, $A_V = +1$



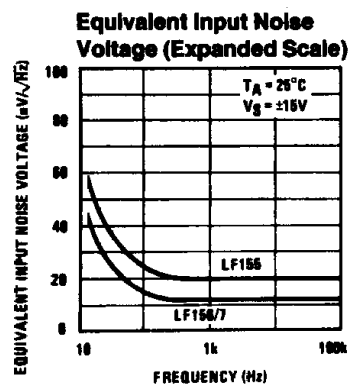
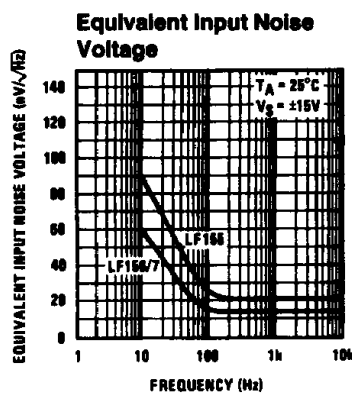
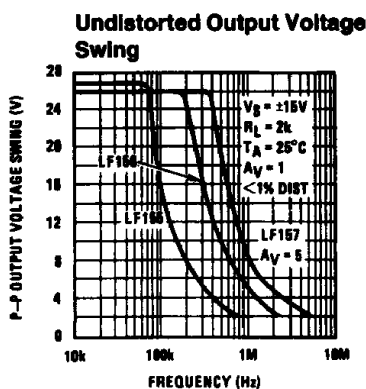
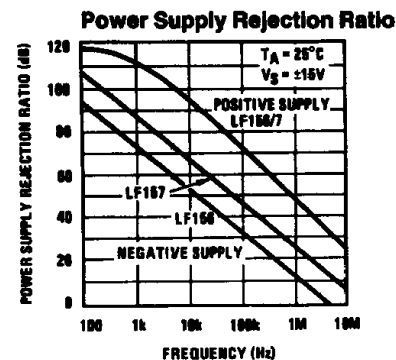
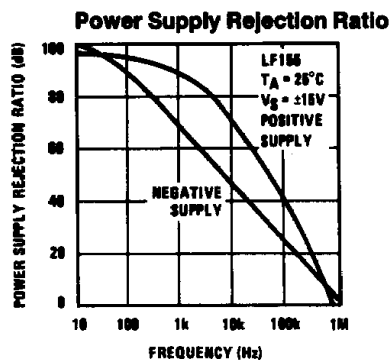
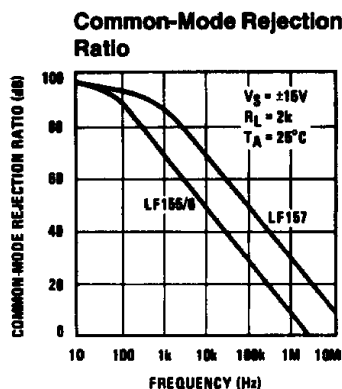
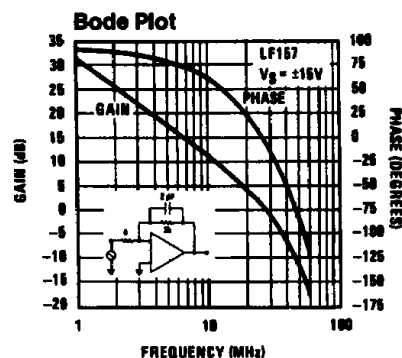
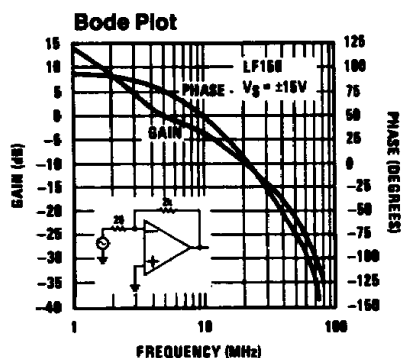
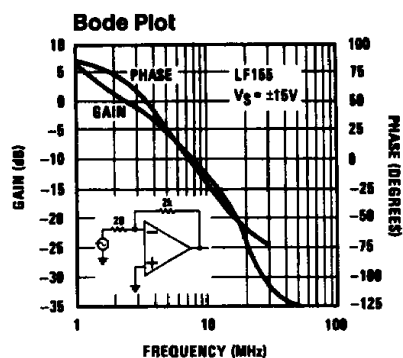
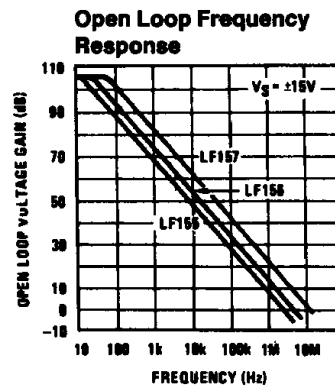
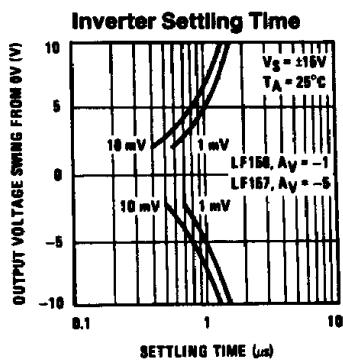
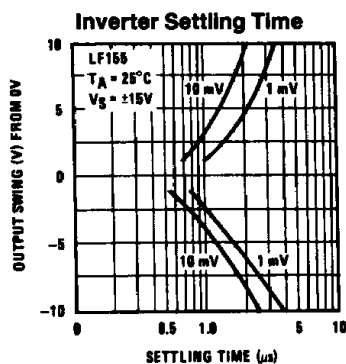
TL/H/5646-9

LF157 Large Signal Pulse Response, $A_V = +5$

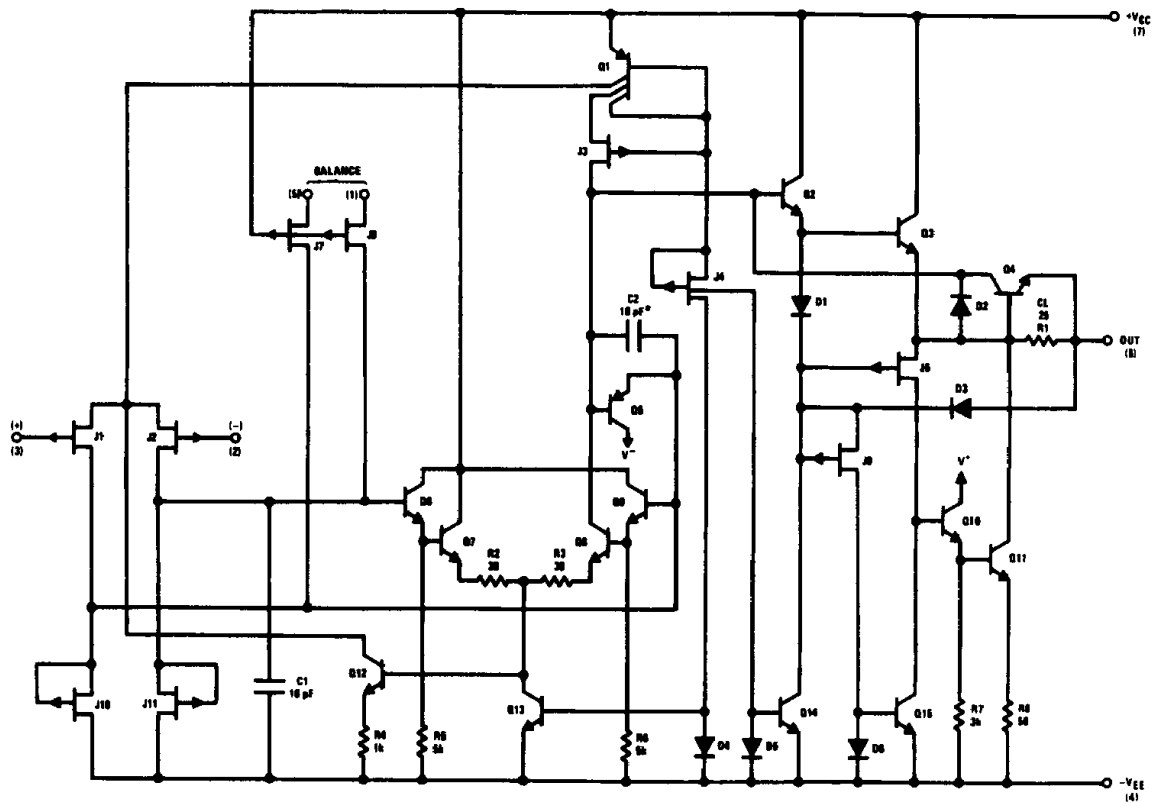


TL/H/5646-10

Typical AC Performance Characteristics (Continued)



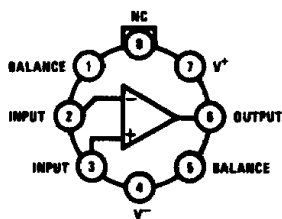
Detailed Schematic



TL/H/5646-13

Connection Diagrams (Top Views)

Metal Can Package (H)

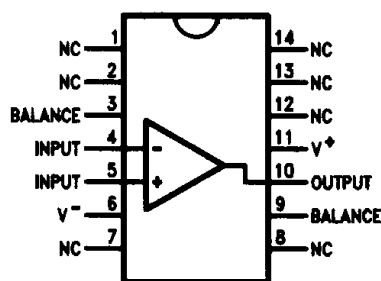


TL/H/5646-14

Order Number

LF155AH, LF156AH, LF157AH,
LF155H, LF156H, LF157H,
LF255H, LF256H, LF257H,
LF355AH, LF356AH, LF357AH,
LF355BH, LF356BH, LF357BH,
LF355H, LF356H or LF357H
See NS Package Number H08C

Dual-In-Line Package (J)

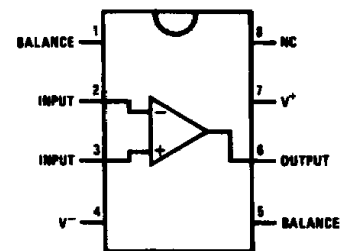


TL/H/5646-30

Order Number

LF155J, LF156J, LF157J,
LF355J, LF356J, LF357J,
LF355BJ, LF356BJ or LF357BJ
See NS Package Number J14A

Dual-In-Line Package (M and N)



TL/H/5646-29

Order Number

LF355M, LF356M, LF357M,
LF356BM, LF355BN, LF356BN,
LF357BN, LF355N, LF356N or
LF357N
See NS Package Number
M08A or N08E

Application Hints

The LF155/6/7 series are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in

polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

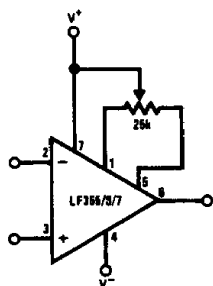
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

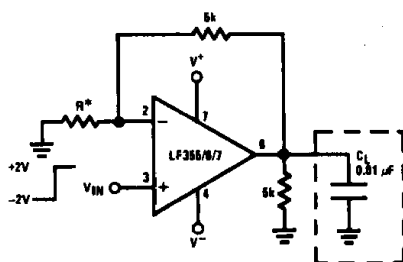
Typical Circuit Connections

V_{OS} Adjustment



- V_{OS} is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V⁺
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is $\approx 0.5 \mu\text{V}/^\circ\text{C}/\text{mV}$ of adjustment
- Typical overall drift: $5 \mu\text{V}/^\circ\text{C} \pm (0.5 \mu\text{V}/^\circ\text{C}/\text{mV of adj.})$

Driving Capacitive Loads



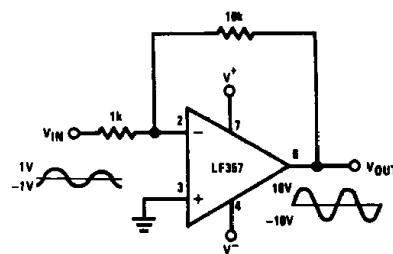
*LF155/6 R = 5k
LF157 R = 1.25k

Due to a unique output stage design, these amplifiers have the ability to drive large capacitive loads and still maintain stability. $C_{L(\text{MAX})} \approx 0.01 \mu\text{F}$.

Overshoot $\leq 20\%$

Settling time (t_s) $\approx 5 \mu\text{s}$

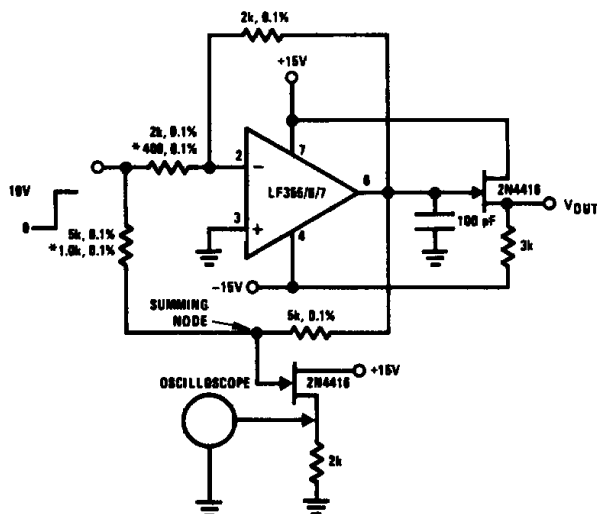
LF157. A Large Power BW Amplifier



TL/H/5846-15
For distortion $\leq 1\%$ and a 20 Vp-p V_{OUT} swing, power bandwidth is: 500 kHz.

Typical Applications

Settling Time Test Circuit

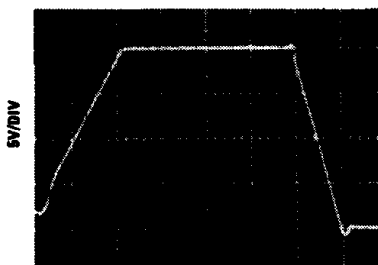


- Settling time is tested with the LF155/6 connected as unity gain inverter and LF157 connected for $A_V = -5$
- FET used to isolate the probe capacitance
- Output = 10V step
- $A_V = -5$ for LF157

TL/H/5646-16

Large Signal Inverter Output, V_{OUT} (from Settling Time Circuit)

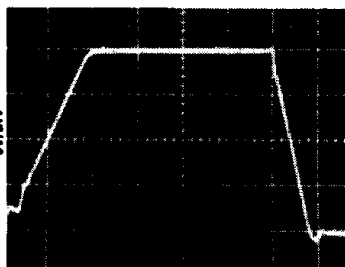
LF355



2 μs/DIV

TL/H/5646-17

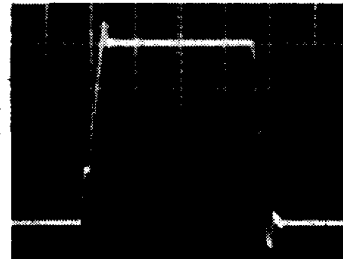
LF356



1 μs/DIV

TL/H/5646-18

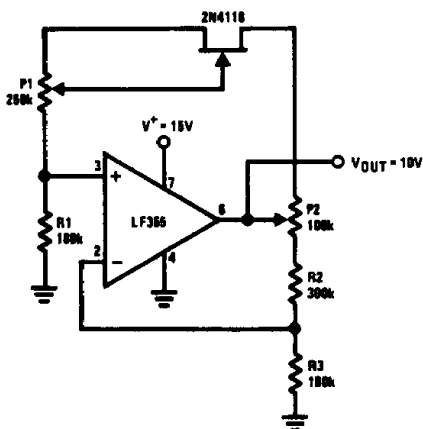
LF357



1 μs/DIV

TL/H/5646-19

Low Drift Adjustable Voltage Reference

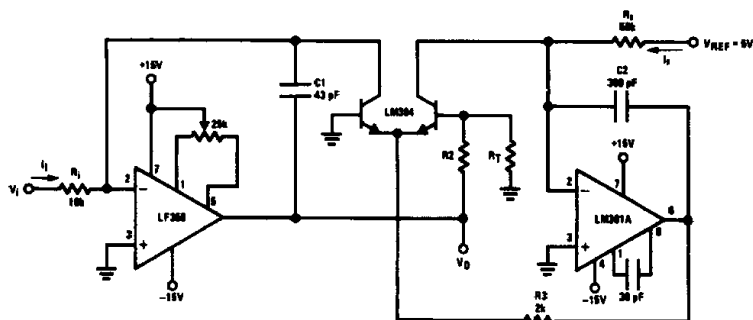


TL/H/5646-20

- $\Delta V_{OUT}/\Delta T = \pm 0.002\%/^{\circ}\text{C}$
- All resistors and potentiometers should be wire-wound
- P1: drift adjust
- P2: V_{OUT} adjust
- Use LF155 for
 - Low I_B
 - Low drift
 - Low supply current

Typical Applications (Continued)

Fast Logarithmic Converter

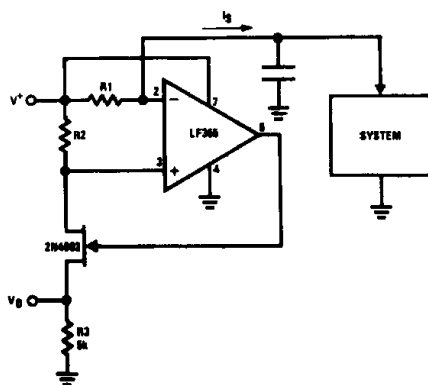


TL/H/5646-21

$$|V_{OUT}| = \left[1 + \frac{R_2}{R_T} \right] \frac{kT}{q} \ln V_i \left[\frac{R_T}{V_{REF} R_1} \right] = \log V_i \frac{1}{R_1 I_T} R_2 = 15.7k, R_T = 1k, 0.3\%/^{\circ}C \text{ (for temperature compensation)}$$

- Dynamic range: $100 \mu A \leq I_i \leq 1 \text{ mA}$ (5 decades), $|V_O| = 1V/\text{decade}$
- Transient response: $3 \mu s$ for $\Delta I_i = 1 \text{ decade}$
- C1, C2, R2, R3: added dynamic compensation
- V_{OS} adjust the LF156 to minimize quiescent error
- R_T : Tel Labs type Q81 $+ 0.3\%/^{\circ}C$

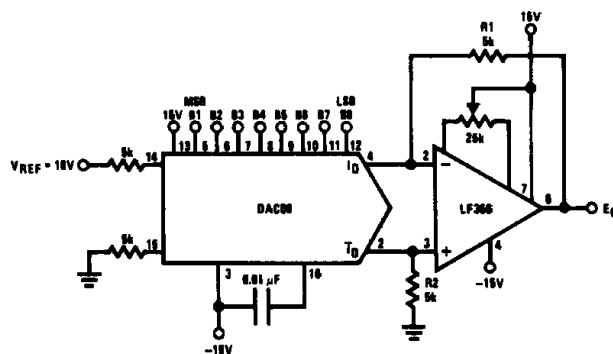
Precision Current Monitor



TL/H/5646-31

- $V_O = 5 R_1 / R_2$ (V/mA of I_S)
- R1, R2, R3: 0.1% resistors
- Use LF155 for
 - Common-mode range to supply range
 - Low I_S
 - Low V_{OS}
 - Low Supply Current

8-Bit D/A Converter with Symmetrical Offset Binary Operation



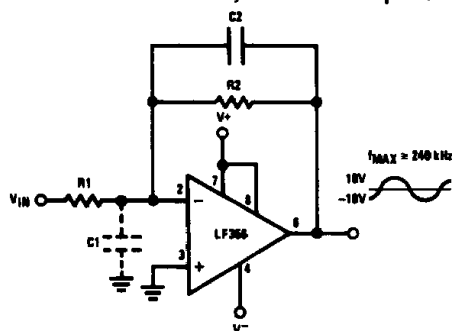
TL/H/5646-32

- R1, R2 should be matched within $\pm 0.05\%$
- Full-scale response time: $3 \mu s$

E _O	B1	B2	B3	B4	B5	B6	B7	B8	Comments
+9.920	1	1	1	1	1	1	1	1	Positive Full-Scale
+0.040	1	0	0	0	0	0	0	0	(+) Zero-Scale
-0.040	0	1	1	1	1	1	1	1	(-) Zero-Scale
-9.920	0	0	0	0	0	0	0	0	Negative Full-Scale

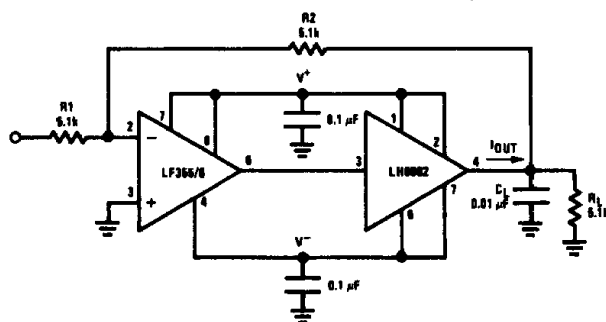
Typical Applications (Continued)

Wide BW Low Noise, Low Drift Amplifier



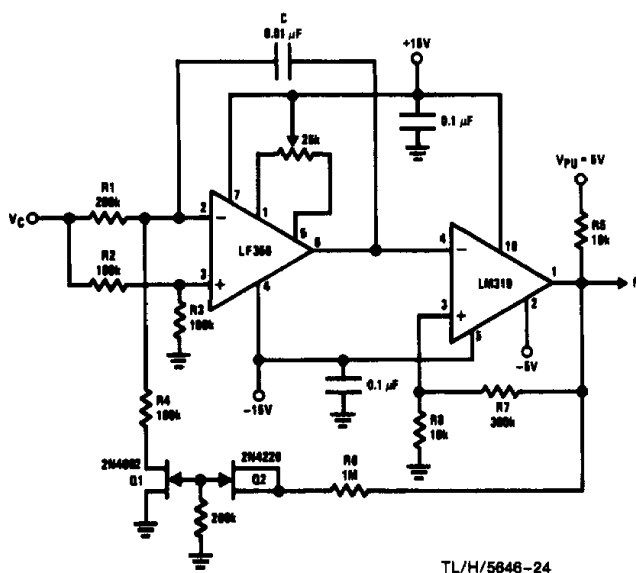
- Power BW: $f_{MAX} = \frac{S_F}{2\pi V_P} \approx 240 \text{ kHz}$
- Parasitic input capacitance $C_1 \approx (3 \text{ pF for LF155, LF156 and LF157 plus any additional layout capacitance})$ interacts with feedback elements and creates undesirable high frequency pole. To compensate add C_2 such that: $R_2 C_2 \approx R_1 C_1$.

Boosting the LF156 with a Current Amplifier



- $I_{OUT(MAX)} \approx 150 \text{ mA}$ (will drive $R_L \geq 100\Omega$)
- $\frac{\Delta V_{OUT}}{\Delta T} = \frac{0.15}{10^{-2}} \text{ V}/\mu\text{s}$ (with C_L shown)
- No additional phase shift added by the current amplifier

3 Decades VCO



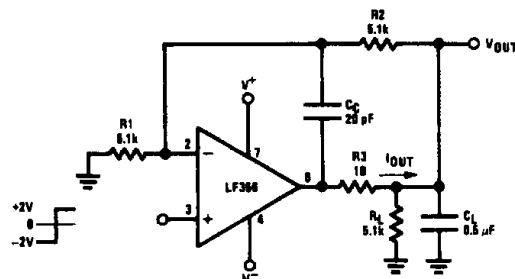
TL/H/5646-24

$$f = \frac{V_C (R_8 + R_7)}{(8 V_{PU} R_8 R_1) C}$$

$0 \leq V_C \leq 30\text{V}$, $10 \text{ Hz} \leq f \leq 10 \text{ kHz}$

R_1, R_4 matched. Linearity 0.1% over 2 decades.

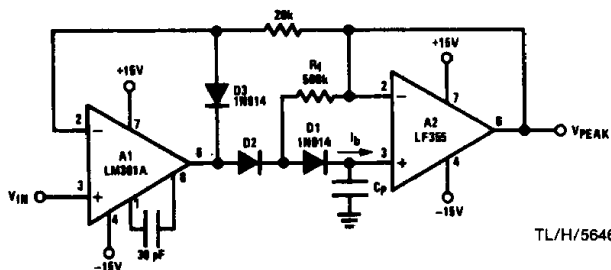
Isolating Large Capacitive Loads



- Overshoot 6%
- $t_s 10 \mu\text{s}$
- When driving large C_L , the V_{OUT} slew rate determined by C_L and $I_{OUT(MAX)}$:
 $\frac{\Delta V_{OUT}}{\Delta T} = \frac{I_{OUT}}{C_L} \approx \frac{0.02}{0.5} \text{ V}/\mu\text{s} = 0.04 \text{ V}/\mu\text{s}$ (with C_L shown)

TL/H/5646-22

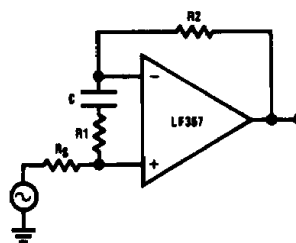
Low Drift Peak Detector



TL/H/5646

- By adding D_1 and R_1 , $V_{D1} = 0$ during hold mode. Leakage of D_2 provided by feedback path through R_1 .
- Leakage of circuit is essentially I_b (LF155, LF156) plus capacitor leakage of C_p .
- Diode D_3 clamps V_{OUT} (A1) to $V_{IN} - V_{D3}$ to improve speed and to limit reverse bias of D_2 .
- Maximum input frequency should be $<< \frac{1}{2\pi R_1 C_{D2}}$ where C_{D2} is the shunt capacitance of D_2 .

Non-Inverting Unity Gain Operation for LF157



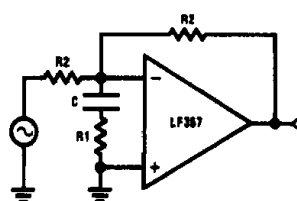
$$R_1 C \geq \frac{1}{(2\pi) (5 \text{ MHz})}$$

$$R_1 = \frac{R_2 + R_s}{4}$$

$$A_V(DC) = 1$$

$$f_{-3 \text{ dB}} \approx 5 \text{ MHz}$$

Inverting Unity Gain for LF157



$$R_1 C \geq \frac{1}{(2\pi) (5 \text{ MHz})}$$

$$R_1 = \frac{R_2}{4}$$

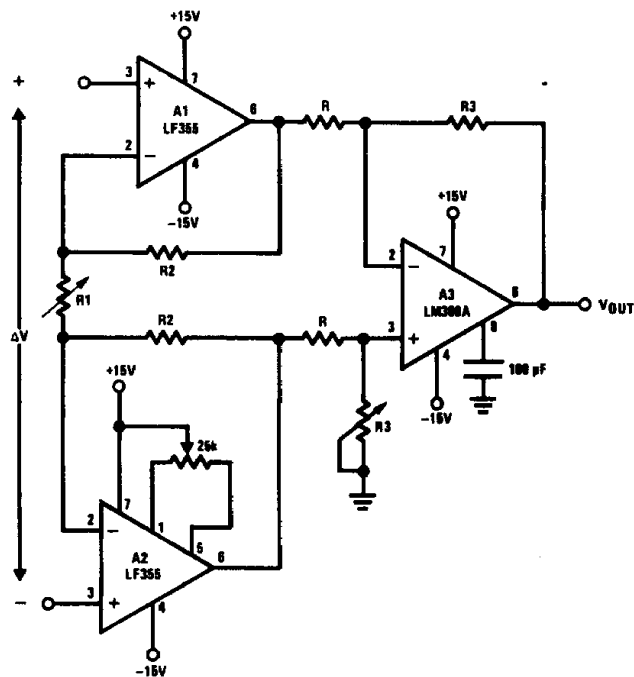
$$A_V(DC) = -1$$

$$f_{-3 \text{ dB}} \approx 5 \text{ MHz}$$

TL/H/5646-25

Typical Applications (Continued)

High Impedance, Low Drift Instrumentation Amplifier



TL/H/5646-26

- $V_{OUT} = \frac{R_3}{R} \left[\frac{2R_2}{R_1} + 1 \right] \Delta V$, $V^- + 2V \leq V_{IN \text{ common-mode}} \leq V^+$
- System V_{OS} adjusted via A2 V_{OS} adjust
- Trim R3 to boost up CMRR to 120 dB. Instrumentation amplifier resistor array recommended for best accuracy and lowest drift

LF155/155A/LF255/LF355/355A/355B/LF156/156A/LF256/LF356/LF356A/356B/LF157/157A/LF257/LF357/357A/357B

The circuit diagram illustrates a two-stage CMOS differential amplifier. The first stage is a differential pair using two NMOS transistors (A1 and A2) and two PMOS transistors (A3 and A4) as a current mirror load. The input signal V_{IN} is applied to the gates of A1 and A2. The gates of A3 and A4 are connected to a common-mode feedback network consisting of a 26k resistor and a 2pF capacitor. The output of the first stage is taken from the drains of A1 and A2, which are connected to a common-mode feedback network consisting of a 26k resistor and a 2pF capacitor. The second stage is a differential-to-single-ended converter, which uses a PMOS transistor (A5) and an NMOS transistor (A6) to convert the differential output of the first stage into a single-ended output V_{OUT} . The gates of A5 and A6 are connected to the outputs of the first stage. The gates of A3 and A4 are connected to a common-mode feedback network consisting of a 26k resistor and a 2pF capacitor. The gates of A5 and A6 are connected to a common-mode feedback network consisting of a 26k resistor and a 2pF capacitor. The output of the second stage is taken from the drain of A5, which is connected to a common-mode feedback network consisting of a 26k resistor and a 2pF capacitor.

- Both amplifiers (A1, A2) have feedback loops individually closed with stable responses (overshoot negligible)

$$T_A \approx \left[\frac{2R_{ON} V_{IN} C_h}{S_r} \right]^{1/2} \text{ provided that:}$$

$$V_{IN} < 2\pi S_r R_{ON} C_h \text{ and } T_A > \frac{V_{IN} C_h}{I_{OUT(MAX)}}, R_{ON} \text{ is of SW1}$$

If inequality not satisfied: $T_A \cong \frac{V_{IN} C_h}{20 \text{ mA}}$

- LF156 develops full S_T output capability for $V_{IN} \geq 1V$
- Addition of SW2 improves accuracy by putting the voltage drop across SW1 inside the feedback loop
- Overall accuracy of system determined by the accuracy of both amplifiers, A1 and A2

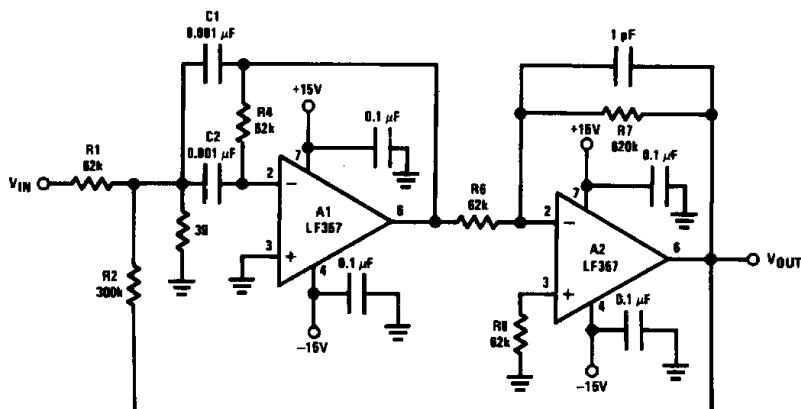
- By closing the loop through A2, the V_{OUT} accuracy will be determined uniquely by A1.

No V_{OS} adjust required for A2.

- T_A can be estimated by same considerations as previously but, because of the added propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold
- R_1 , C_C : additional compensation
- Use LF156 for
 - Fast settling time
 - Low V_{OS}

Typical Applications (Continued)

High Q Band Pass Filter



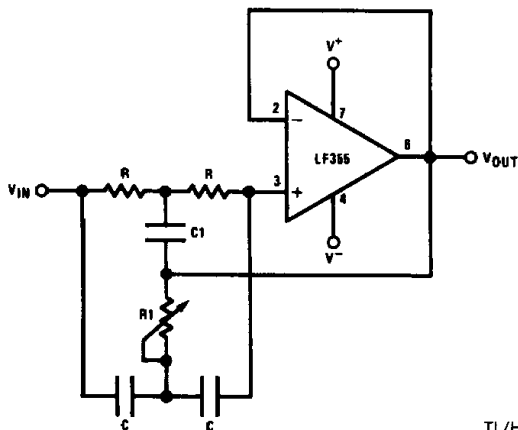
- By adding positive feedback (R2)
Q increases to 40
- $f_{BP} = 100 \text{ kHz}$

$$\frac{V_{OUT}}{V_{IN}} = 10\sqrt{Q}$$

- Clean layout recommended
- Response to a 1 Vp-p tone burst:
300 μs

TL/H/5646-28

High Q Notch Filter



- $2R1 = R = 10 \text{ M}\Omega$
- $2C = C1 = 300 \text{ pF}$
- Capacitors should be matched to obtain high Q
- $f_{NOTCH} = 120 \text{ Hz}$, notch = -55 dB, $Q > 100$
- Use LF155 for
 - Low I_B
 - Low supply current

TL/H/5646-34