Preliminary Product Information
December 1997 *(1 of 6)*

1.85 to 1.91 GHz 5V, 31 dBm, PCS/PCN Power Amplifier

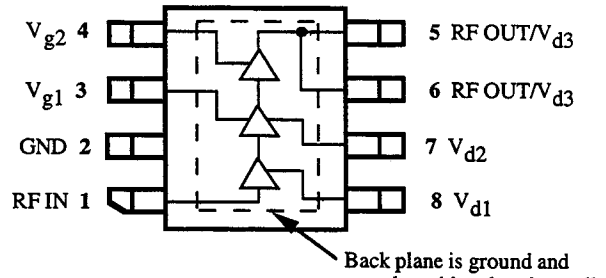
Features

- ❑ 35% Linear Power Added Efficiency
- ❑ 31 dBm Output Power (IS-136 TDMA)
- ❑ 29 dBm Output Power (J-STD-18 CDMA)
- ❑ 32 dB Gain
- ❑ Tested Under Digital Modulation
- ❑ Low Cost SO-8 Surface Mount Package

Applications

- ❑ PCS Handsets
- ❑ PCS Base Stations
- ❑ Wireless Local Loop Subscriber Units
- ❑ 1.6 GHz Satellite Subscriber Units

Functional Block Diagram



Back plane is ground and must be soldered to thermally conductive ground plane.

Description

The CMM1333 is a 5 V linear power amplifier intended for use in PCS handsets, wireless local loop subscriber units and PCS base stations. As a pin-compatible member of the new ***Triniti DX***™ amplifier family, the CMM1333 offers maximum performance and flexibility. The amplifier can be biased to support the requirements of PCS-1900, IS-136 (TDMA), J-STD-18 (CDMA) or DCS-1800 systems.

The CMM1333 is packaged in a low-cost, space efficient SO-8 power package that gives excellent electrical stability and thermal handling performance with a R_{Θ} of less than 18° C/W. The part is designed to require minimal external circuitry for bias and matching, simplifying design and keeping board space and cost to a minimum. Through matching adjustment, equivalent performance can also be achieved for the 1.93 to 1.99 GHz PCS bands as well as the 1.6 GHz satellite bands.

Absolute Maximum Ratings

Parameter	Rating	Parameter	Rating	Parameter	Rating
Drain Voltage (+V_d)	+8.0 V*	Power Dissipation	5 W	Operating Temperature	-40°C to +100°C
Drain Current (I_d)	1.8 A	Thermal Resistance	18°C/W	Channel Temperature	175°C
RF Input Power	+15 dBm*	Storage Temperature	-65°C to +150°C	Soldering Temperature	260°C for 5 Sec.
DC Gate Voltage (-V_g)	-4.0 V*				

* Max (+V_d) and (-V_g) under linear operation. Max potential difference across the device in RF compression ($2V_d$ + |-V_g|) not to exceed the minimum breakdown voltage (V_{br}) of +18V.

Recommended Operating Conditions

Parameter	Typ	Units	Parameter	Typ	Units
Drain Voltage (+V_d)	4.5 to 5.1	Volts	Operating Temperature (PC Board)	-30 to +80	°C

Electrical Characteristics

Unless otherwise specified, the following specifications are guaranteed at room temperature with drain voltage (+V_d) = 4.8 V in Celeritek test fixture.

Parameter	Condition	Min	Typ	Std Deviation	Max	Units
Frequency Range		1.85			1.91	GHz
Gain	@ Digital power output	29	32	0.95		dB
Power Output	Meets IS-136 TDMA mask Meets J-STD-18 CDMA mask	30 28.5	31 29	0.31		dBm dBm
Harmonics	2nd @ Digital power output 3rd @ Digital power output		-35 -40		-30 -35	dBc dBc
Noise Figure			4.5	0.2	5.0	dB
Return Loss			10			dB
Efficiency	Pout IS-136 TDMA Pout J-STD-18 CDMA	30 27	35 30	1.1		% %
Positive Supply Current (I_d)	Pout IS-136 TDMA Pout J-STD-18 CDMA		600 500	20 20		mA mA
Quiescent Current (I_q) †	No RF		350	20		mA
Negative Supply Current (-I_g)	Includes external resistor divider		1.1	0.2	2.0	mA
Negative Supply Voltage (-V_g)	Into external resistor divider	-1.3	-1.7	0.16	-2.2	V

† For dynamic bias applications see Typical Performance chart on page 4.

Small Signal S-Parameters (Deimbeded from external matching circuitry)

4.8 V, 500 mA [Output stage = 330 mA, Driver stages = 170 mA]

Frequency	S_{11}		S_{21}		S_{12}		S_{22}	
(GHz)	Mag	ANG	Mag	ANG	Mag	ANG	Mag	ANG
0.6	0.99	-42.2	0.53	12.1	0.001	167.0	0.56	-173.4
1.0	0.97	-75.7	0.57	30.3	0.002	-63.1	0.76	168.7
1.3	0.92	-101.8	13.34	-34.2	0.002	71.1	0.71	174.2
1.4	0.89	-111.9	26.51	-78.8	0.003	126.2	0.86	176.1
1.5	0.80	-126.0	39.98	-131.1	0.003	72.7	1.04	164.2
1.6	0.64	-141.7	45.29	179.6	0.002	65.0	1.03	148.4
1.7	0.42	-157.6	45.01	138.3	0.003	3.7	0.91	138.8
1.8	0.19	-171.5	42.38	101.8	0.001	-10.4	0.82	132.9
1.9	0.02	-90.9	37.99	69.4	0.002	14.8	0.78	130.0
2.0	0.14	-32.9	33.02	40.8	0.002	17.6	0.75	126.7
2.1	0.21	-36.5	28.20	15.5	0.002	85.2	0.72	123.0
2.2	0.25	-40.3	24.10	-6.8	0.001	-3.0	0.72	122.0
3.0	0.28	-69.0	7.29	-132.5	0.002	54.2	0.81	117.0
3.5	0.52	-111.5	3.69	173.2	0.004	105.5	0.82	121.7
4.0	0.73	-118.0	2.19	133.6	0.007	95.2	0.69	112.3

Small Signal S-Parameters (Deimbeded from external matching circuitry)

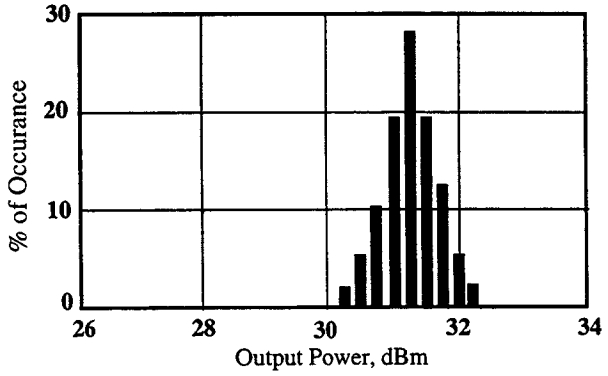
4.8 V, 300 mA [Output stage = 184 mA, Driver stages = 116 mA]

Frequency	S_{11}		S_{21}		S_{12}		S_{22}	
(GHz)	Mag	ANG	Mag	ANG	Mag	ANG	Mag	ANG
0.6	0.99	-42.5	0.46	9.0	0.001	65.1	0.55	-169.4
1.0	0.97	-75.4	0.53	33.2	0.001	129.2	0.73	170.3
1.3	0.92	-101.5	11.44	-32.2	0.002	118.7	0.69	177.3
1.4	0.88	-112.3	22.43	-76.1	0.002	112.4	0.84	179.2
1.5	0.80	-126.0	33.80	-127.3	0.004	100.9	1.02	167.1
1.6	0.64	-141.1	38.86	-175.6	0.003	75.7	1.02	152.0
1.7	0.42	-156.7	39.39	143.7	0.003	40.8	0.92	141.9
1.8	0.20	-169.7	37.60	107.4	0.001	-31.6	0.84	135.8
1.9	0.02	-115.9	34.50	74.9	0.002	-7.9	0.78	131.5
2.0	0.14	-30.1	30.55	45.8	0.001	-39.6	0.74	128.0
2.1	0.21	-38.3	26.51	20.1	0.002	2.9	0.73	123.7
2.2	0.25	-41.6	22.82	-2.8	0.001	-140.5	0.71	122.6
3.0	0.27	-64.9	6.91	-132.7	0.005	113.2	0.80	118.2
3.5	0.52	-110.1	3.46	171.9	0.001	56.3	0.82	122.4
4.0	0.73	-117.5	2.03	132.5	0.007	41.9	0.69	113.6

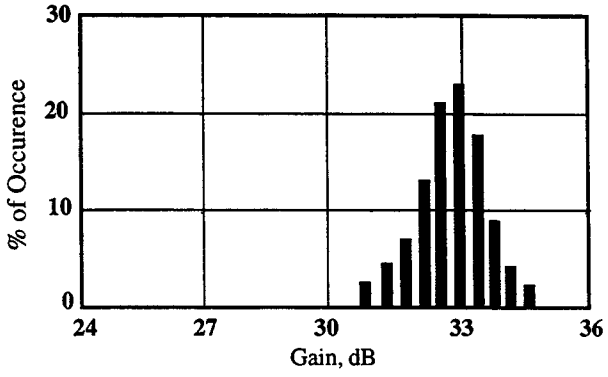
Note: Electronic copies of the S-Parameters above can be obtained by contacting the factory.

Typical Performance

Distribution of IS-136 TDMA Output Power
4.8V, 1.88 GHz



Distribution of Gain
4.8V, 1.88 GHz



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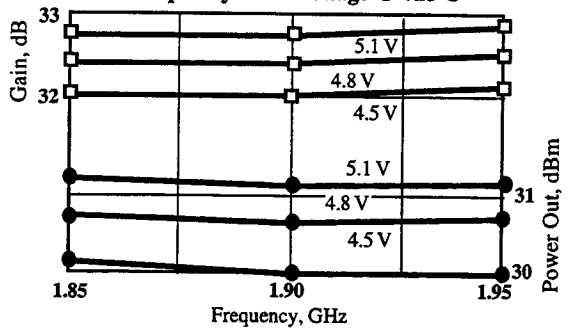
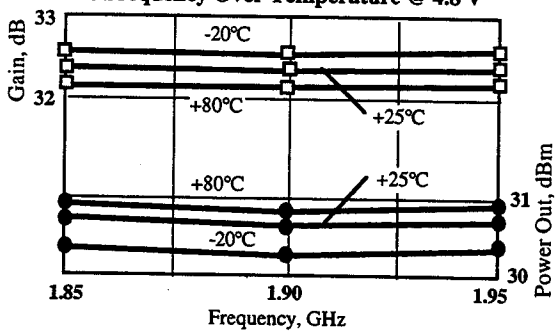
Typical Performance

Gain & IS-136 TDMA Output Power vs Frequency Over Voltage @ +25°C

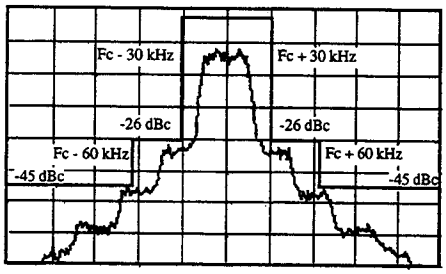


Gain & J-STD-18, IS-136 TDMA Output Power vs Frequency Over Temperature @ 4.8 V



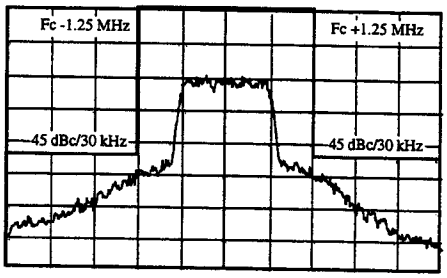
Note: As the device is temperature compensated, a design guideline of ±0.008 dB/°C is recommended.

IS-136 TDMA Spectral Mask



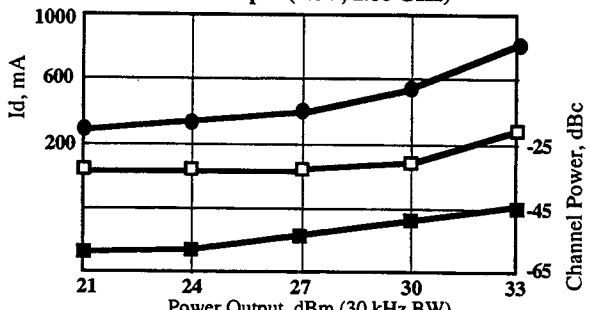
Span: 250 kHz, Frequency: 1880 MHz, RF Level: 31 dBm

J-STD-18 CDMA Spectral Mask



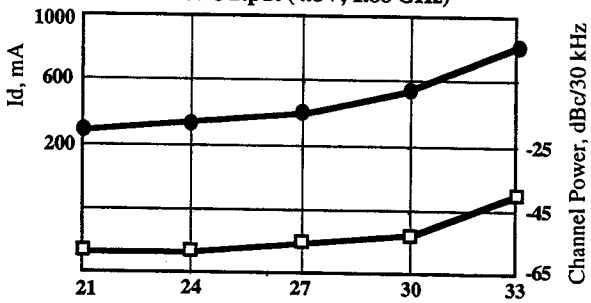
· Span: 6.2 MHz, Frequency: 1880 MHz, RF Level: 29 dBm

Id & IS-136 TDMA Channel Power vs Power Output (4.8V, 1.88 GHz)



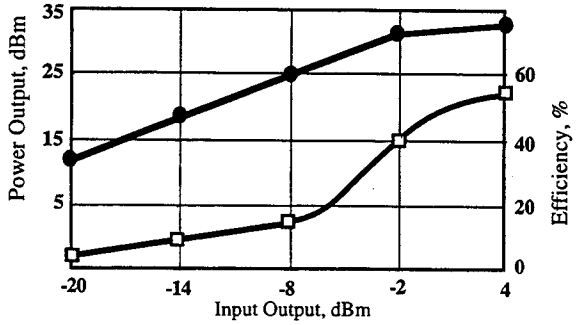
□ Adjacent channel power (worst case Fc ±30 kHz)
■ Alternate channel power (worst case Fc ±60 kHz)

Id & J-STD-18 CDMA Channel Power vs Power Output (4.8V, 1.88 GHz)

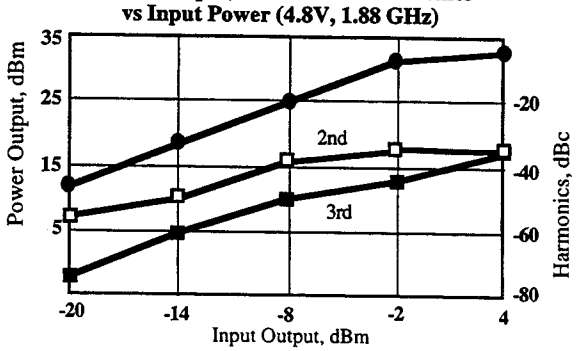


□ Adjacent channel power (worst case ±1.25 MHz)

Power Output and Efficiency vs Input Power (4.8V, 1.88 GHz)

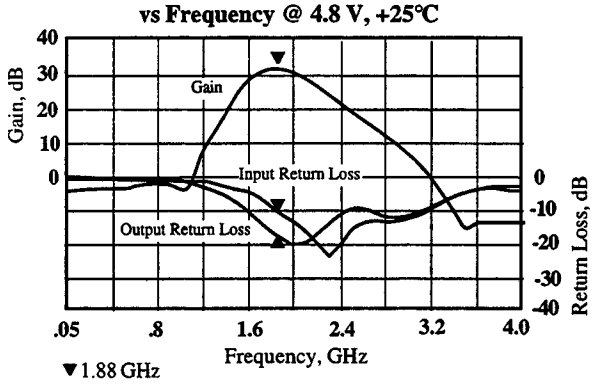


Power Output, 2nd and 3rd Harmonics vs Input Power (4.8V, 1.88 GHz)

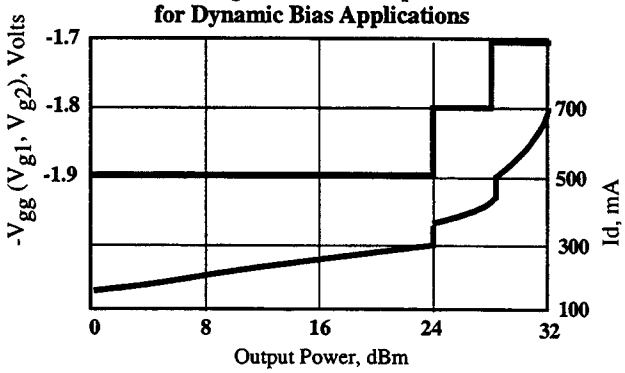


Typical Performance (Continued)

Wideband Gain & Return Loss vs Frequency @ 4.8 V, +25°C



Gate Voltage and Id vs Output Power for Dynamic Bias Applications



Application Information

The CMM1333 is a three stage amplifier that requires a positive and negative supply voltage for proper operation. It is essential when turning on the device that the negative supply be applied before the positive supply. When turning the device off, the positive supply should be removed before the negative supply is removed.

The CMM1333 can be operated over a range of supply voltages and bias points. It is important that the maximum power dissipation of the package be observed at all times and that the maximum voltage across the device, as specified, is not exceeded.

Design Considerations

Biasing A negative voltage is needed to bias the 3 stage GaAs FET power amplifier. The first stage bias is controlled internally via the gate bias to the second stage (Vg1). The output stage is controlled via Vg2.

The positive supply voltage is applied to pins 5, 6 and 7. The negative voltage supply should be adjusted to achieve the typical quiescent current specified prior to characterization. See performance curve above for use in dynamic bias applications.

Matching Circuits Input and output matching circuits are required. The CMM1333 S-Parameters are on page 2, and the evaluation board schematic and layout are on page 5. The test board is designed to be used at multiple frequencies. The matching elements for proper operation at 1.85– 1.91 GHz are described on page 5.

Two shunt capacitors (C7 & C15) are used to match the output.

Note: Circuit board 8217 is a multiple-use test board. The portions of the board that are used with the CMM1333 are shown as solid traces on the board layout drawing on Page 5. The interface/connection points to the evaluation board are shown. These connection points may not be labeled identically on Celeritek's PB-CMM1333 evaluation board. Contact the factory for support in translating the external match to a specific application.

Supply Ramping To obtain the necessary power ramp, supply side switching should be used. Drain voltages should be tied together and ramped to produce the required power vs. time response.

Modulation When biased as specified, the CMM1333 will achieve the required adjacent channel response for the digital PCS system specified. Celeritek tests each product under digital modulation to ensure correlation to customer applications.

S-Parameters The S-parameters shown in this data sheet are taken at a small signal bias. They do not apply at large signal conditions or when the device is biased for maximum efficiency. Electronic copies may be obtained by contacting the factory.

Thermal

1. The copper pad on the backside of the CMM1333 must be soldered to the ground plane.
2. All 8 leads of the package must be soldered to the appropriate electrical connection.
3. A large ground plane area with plated thru-holes as shown on the PCB layout should be used as a backside connection.

Contact the factory for a copy of a manufacturing application note containing more detailed information.

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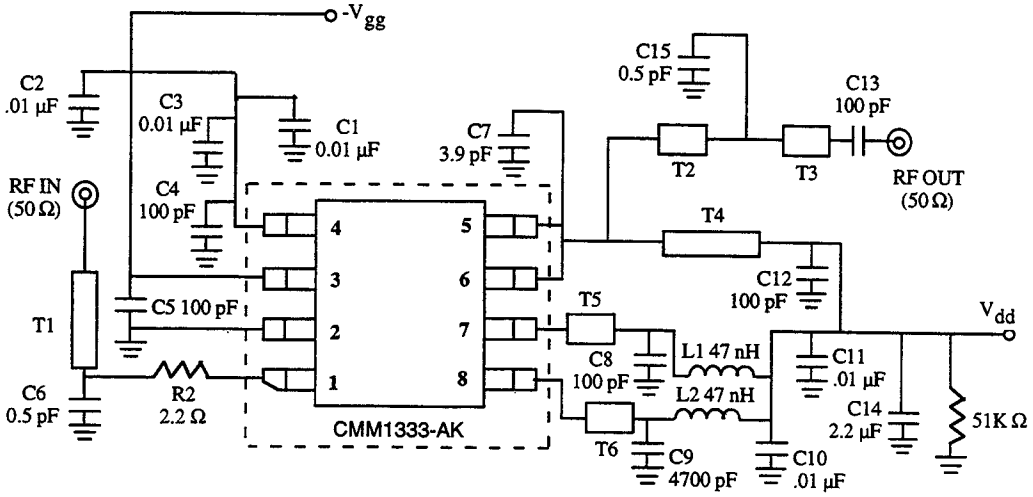
Test Circuits

Evaluation Board Schematic

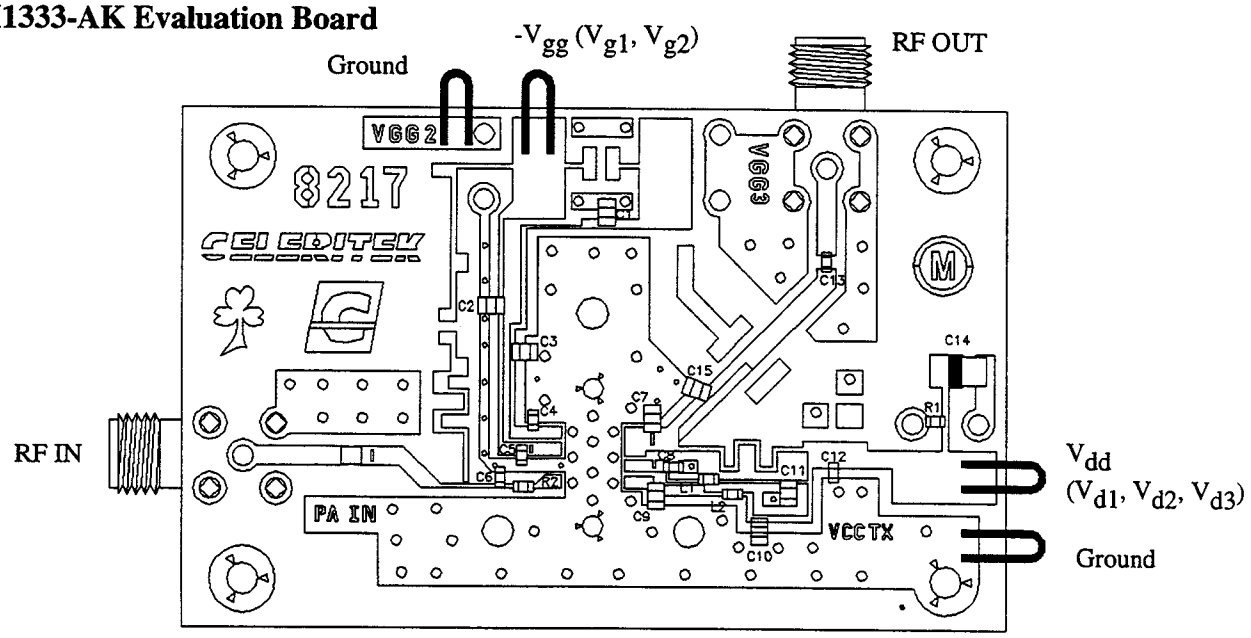
Board substrate:
ER = 4.60
Thickness = 0.031 in.

Transmission line electrical lengths at 1.88 GHz.
(Dimensions in inches)

Line	(W)	(L)	Z (Ø)	E (°)
T1	.010	.225	104	23
T2	.030	.100	69	10
T3	.030	.110	69	11
T4	.015	.666	91	68
T5	.036	.068	63	7
T6	.036	.025	63	3



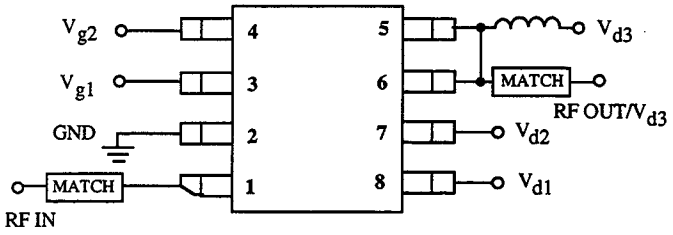
PB-CMM1333-AK Evaluation Board



Evaluation Board Parts List

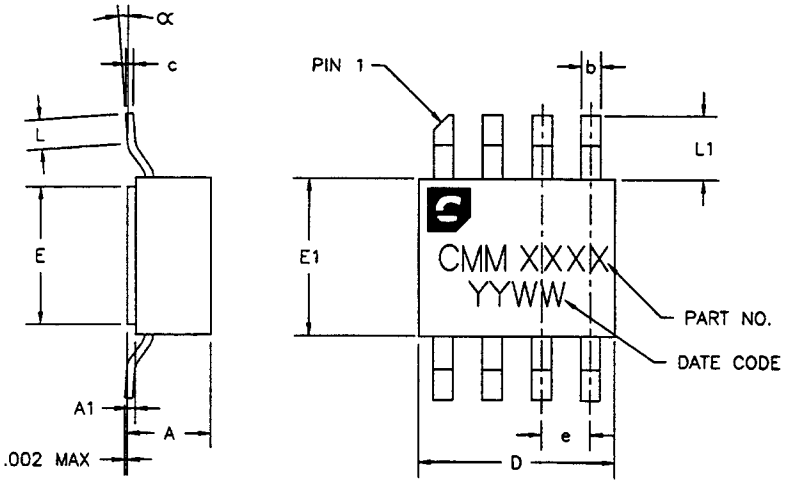
Part Type	Reference Designator	Description	Manufacturer	Part Number
Resistor	R2	2.2 Ω 0603	Rohm	MCR03J 2R2
Resistor	R1	51 K Ω 0603	Rohm	MCR03J 513
Capacitor	C14	2.2 µF Tantalum	Matsuo	267M2002225M
Capacitor	C1, C2, C3, C10, C11	0.01µF 0805 X7R	Rohm	MCH215 C103KK
Capacitor	C9	4700 pF 0805 X7R	Rohm	MCH215 C472KK
Capacitor	C15	0.5pF 0805 NPO	Rohm	MCH215 AOR5CK
Capacitor	C7	3.9pF 0805	ATC	ATC100A3R9CP150X
Capacitor	C6	0.5pF 0603 NPO	Rohm	MCH185A 0R5CK
Capacitor	C4, C5, C8, C12, C13	100pF 0603 NPO	Rohm	MCH185A 101JK
Inductor	L1, L2	47 nH 0603	Panasonic	ELJ-RC47NJF2

Connection Diagram and Pin Descriptions



Pin #	Name	Description
1	RF IN	RF input (internally DC blocked)
2	GND	Ground
3	V_{g1}	Input and intermediate stage gate bias
4	V_{g2}	Output stage gate bias
5	RF OUT/V_{d3}	RF output and V_{d3}. External matching circuit required
6	RF OUT/V_{d3}	RF output and V_{d3}. External matching circuit required
7	V_{d2}	Intermediate stage drain bias
8	V_{d1}	Input stage drain bias

Physical Dimensions



DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A		.086[2.184]	.100[2.540]
A1	.005[.1270]	.008[.2032]	.011[.2794]
b	.017[.4318]	.020[.5080]	.023[.5842]
c	.007[.1778]	.008[2032]	.009[.2286]
D	.195[4.953]	.200[5.080]	.205[5.207]
E	.135[3.429]	.140[3.556]	.145[3.683]
E1	.155[3.937]	.160[4.064]	.165[4.191]
e		.050[1.270]	
L	.020[.5080]		.040[1.016]
L1	.055[1.397]	.065[1.651]	.075[1.905]
α	0°		8°

DIMENSIONS IN INCHES [MILIMETERS]

Ordering Information

The CMM1333 is available in a surface mount SO-8 power package and devices are available in tape and reel.

Part Number for Ordering	Package
CMM1333-AK-00S0	**SO-8 surface mount power package for CDMA**
CMM1333-AK-00ST	**SO-8 surface mount power package in tape and reel for CDMA**
CMM1333-AK-00T0	**SO-8 surface mount power package for TDMA**
CMM1333-AK-00TT	**SO-8 surface mount power package in tape and reel for TDMA**
PB-CMM1333-AK	**Evaluation Board with SMA connectors**

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