

FEATURES

- Pin Compatible with LM111 Series Devices
- *Guaranteed* Max 0.5mV Input Offset Voltage
- *Guaranteed* Max 25nA Input Bias Current
- *Guaranteed* Max 3nA Input Offset Current
- *Guaranteed* Max 250ns Response Time
- *Guaranteed* Min 200,000 Voltage Gain
- 50mA Output Current Source or Sink
- $\pm 30\text{V}$ Differential Input Voltage
- Fully Specified for Single 5V Operation
- Available in 8-Lead PDIP and SO Packages

APPLICATIONS

- SAR A/D Converters
- Voltage-to-Frequency Converters
- Precision RC Oscillator
- Peak Detector
- Motor Speed Control
- Pulse Generator
- Relay/Lamp Driver

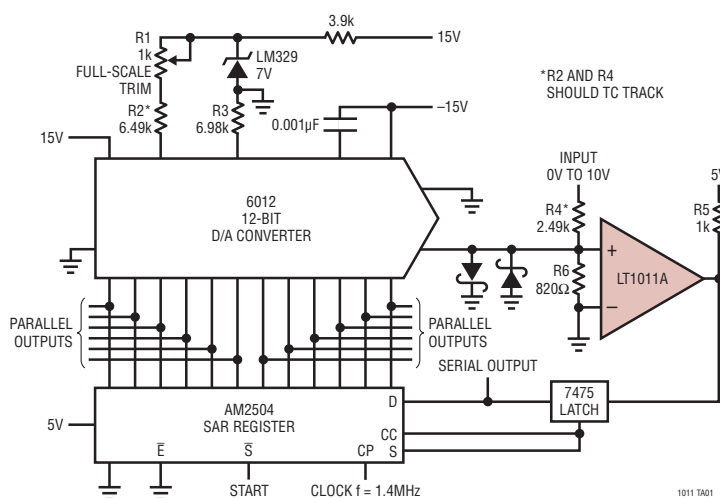
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DESCRIPTION

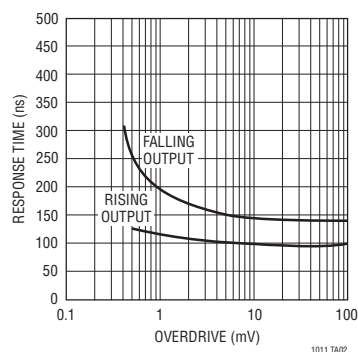
The LT®1011 is a general purpose comparator with significantly better input characteristics than the LM111. Although pin compatible with the LM111, it offers four times lower bias current, six times lower offset voltage and five times higher voltage gain. Offset voltage drift, a previously unspecified parameter, is guaranteed at $15\mu\text{V}/^\circ\text{C}$. Additionally, the supply current is lower by a factor of two with no loss in speed. The LT1011 is several times faster than the LM111 when subjected to large overdrive conditions. It is also fully specified for DC parameters and response time when operating on a single 5V supply. These parametric improvements allow the LT1011 to be used in high accuracy (≥ 12 -bit) systems without trimming. In a 12-bit A/D application, for instance, using a 2mA DAC, the offset error introduced by the LT1011 is less than 0.5LSB. The LT1011 retains all the versatile features of the LM111, including single 3V to $\pm 18\text{V}$ supply operation, and a floating transistor output with 50mA source/sink capability. It can drive loads referenced to ground, negative supply or positive supply, and is specified up to 50V between V^- and the collector output. A differential input voltage up to the full supply voltage is allowed, even with $\pm 18\text{V}$ supplies, enabling the inputs to be clamped to the supplies with simple diode clamps.

TYPICAL APPLICATION

10μs 12-Bit A/D Converter



Response Time vs Overdrive



LT1011/LT1011A

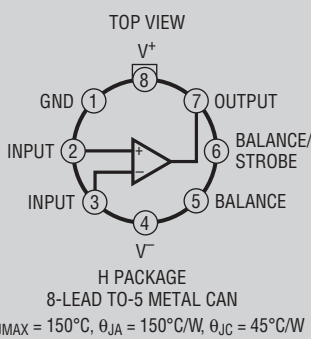
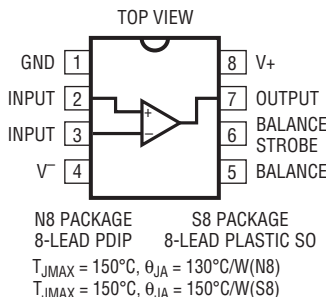
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (Pin 8 to Pin 4)	36V
Output to Negative Supply (Pin 7 to Pin 4)	
LT1011AC, LT1011C	40V
LT1011AI, LT1011I	40V
LT1011AM, LT1011M (OBSOLETE)	50V
Ground to Negative Supply (Pin 1 to Pin 4)	30V
Differential Input Voltage	±36V
Voltage at STROBE Pin (Pin 6 to Pin 8)	5V

Input Voltage (Note 2)	Equal to Supplies
Output Short-Circuit Duration	10 sec
Operating Temperature Range (Note 3)	
LT1011AC, LT1011C	0°C to 70°C
LT1011AI, LT1011I	–40°C to 85°C
LT1011AM, LT1011M (OBSOLETE)	–55°C to 125°C
Storage Temperature Range	–65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION

 TOP VIEW H PACKAGE 8-LEAD TO-5 METAL CAN $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 150^{\circ}\text{C/W}$, $\theta_{JC} = 45^{\circ}\text{C/W}$	ORDER PART NUMBER	 TOP VIEW N8 PACKAGE 8-LEAD PDIP $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 130^{\circ}\text{C/W (N8)}$ $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 150^{\circ}\text{C/W (S8)}$ S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 150^{\circ}\text{C/W (S8)}$ J8 PACKAGE 8-LEAD CERDIP $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 100^{\circ}\text{C/W (J8)}$	ORDER PART NUMBER
	LT1011ACH LT1011CH LT1011AMH LT1011MH		LT1011ACN8 LT1011CN8 LT1011CS8 LT1011AIS8 LT1011IS8
			S8 PART MARKING
			1011 1011AI 1011I
OBSOLETE PACKAGES Consider the N8 or S8 Packages for Alternate Source		ORDER PART NUMBER	
		LT1011ACJ8 LT1011CJ8	LT1011AMJ8 LT1011MJ8

Order Options Tape and Reel: Add #TR

Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF

Lead Free Part Marking: <http://www.linear.com/leadfree/>

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^{\circ}\text{C}$. $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$, $R_S = 0\Omega$, $V_{GND} = -15\text{V}$, output at pin 7 unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1011AC/AI/AM			LT1011C/I/M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 4)	●	0.3	0.5	0.6	1.5	3	mV
	*Input Offset Voltage	$R_S \leq 50\text{k}$ (Note 5)	●		0.75		2	3	mV

*Indicates parameters which are guaranteed for all supply voltages, including a single 5V supply. See Note 5.

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ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS	LT1011AC/AI/AM			LT1011C/I/M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{OS}	*Input Offset Current	(Note 5)	●	0.2	3 5		0.2	4 6	nA nA
I_B	Input Bias Current	(Note 4)		15	25		20	50	nA
	*Input Bias Current	(Note 5)	●	20	35 50		25	65 80	nA nA
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift (Note 6)	$T_{MIN} \leq T \leq T_{MAX}$	●	4	15		4	25	$\mu\text{V}/^\circ\text{C}$
A_{VOL}	*Large-Signal Voltage Gain	$R_L = 1\text{k}$ Connected to 15V, $-10\text{V} \leq V_{OUT} \leq 14.5\text{V}$		200	500		200	500	V/mV
		$R_L = 500\Omega$ Connected to 5V, $V_S = \text{Single } 5\text{V}$, $V_{GND} = 0\text{V}$, $0.5\text{V} \leq V_{OUT} \leq 4.5\text{V}$		50	300		50	300	V/mV
CMRR	Common Mode Rejection Ratio			94	115		90	115	dB
	*Input Voltage Range (Note 9)	$V_S = \pm 15\text{V}$ $V_S = \text{Single } 5\text{V}$	● ●	-14.5 0.5	13 3		-14.5 0.5	13 3	V V
t_D	*Response Time	(Note 7)		150	250		150	250	ns
V_{OL}	*Output Saturation Voltage, $V_{GND} = 0$	$V_{IN} = -5\text{mV}$, $I_{SINK} = 8\text{mA}$, $T_J \leq 100^\circ\text{C}$ $V_{IN} = -5\text{mV}$, $I_{SINK} = 8\text{mA}$ $V_{IN} = -5\text{mV}$, $I_{SINK} = 50\text{mA}$	● ●	0.25 0.25 0.7	0.4 0.45 1.5		0.25 0.25 0.7	0.4 0.45 1.5	V V V
	*Output Leakage Current	$V_{IN} = 5\text{mV}$, $V_{GND} = -15\text{V}$, $V_{OUT} = 20\text{V}$	●	0.2	10 500		0.2	10 500	nA nA
	*Positive Supply Current	$V_{GND} = 0$		3.2	4		3.2	4	mA
	*Negative Supply Current	$V_{GND} = 0$		1.7	2.5		1.7	2.5	mA
	*Strobe Current (Note 8)	Minimum to Ensure Output Transistor is Off, $V_{GND} = 0$		500			500		μA
	Input Capacitance			6			6		pF

* Indicates parameters which are guaranteed for all supply voltages, including a single 5V supply. See Note 5.

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Inputs may be clamped to supplies with diodes so that maximum input voltage actually exceeds supply voltage by one diode drop. See Input Protection in the Applications Information section.

Note 3: $T_{JMAX} = 150^\circ\text{C}$.

Note 4: Output is sinking 1.5mA with $V_{OUT} = 0\text{V}$.

Note 5: These specifications apply for all supply voltages from a single 5V to $\pm 15\text{V}$, the entire input voltage range, and for both high and low output states. The high state is $I_{SINK} = 100\mu\text{A}$, $V_{OUT} = (V^+ - 1\text{V})$ and the low state is $I_{SINK} = 8\text{mA}$, $V_{OUT} = 0.8\text{V}$. Therefore, this specification

defines a worst-case error band that includes effects due to common mode signals, voltage gain and output load.

Note 6: Drift is calculated by dividing the offset voltage difference measured at min and max temperatures by the temperature difference.

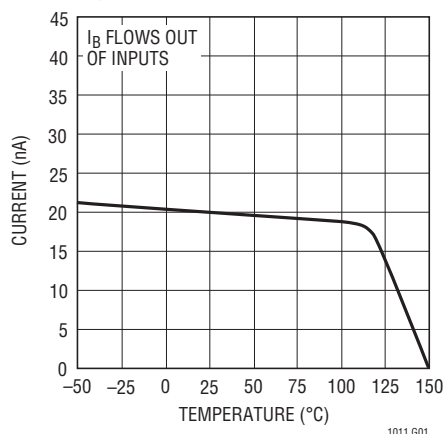
Note 7: Response time is measured with a 100mV step and 5mV overdrive. The output load is a 500 Ω resistor tied to 5V. Time measurement is taken when the output crosses 1.4V.

Note 8: Do not short the STROBE pin to ground. It should be current driven at 3mA to 5mA for the shortest strobe time. Currents as low as 500 μA will strobe the LT1011A if speed is not important. External leakage on the STROBE pin in excess of 0.2 μA when the strobe is "off" can cause offset voltage shifts.

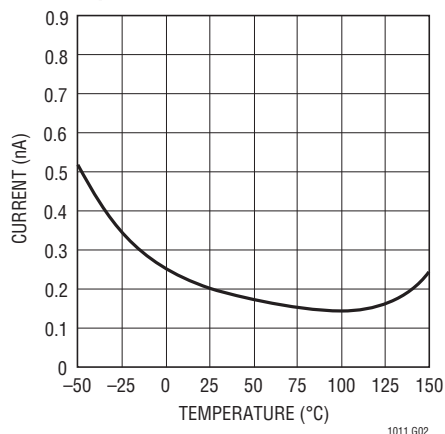
Note 9: See graph "Input Offset Voltage vs Common Mode Voltage."

TYPICAL PERFORMANCE CHARACTERISTICS

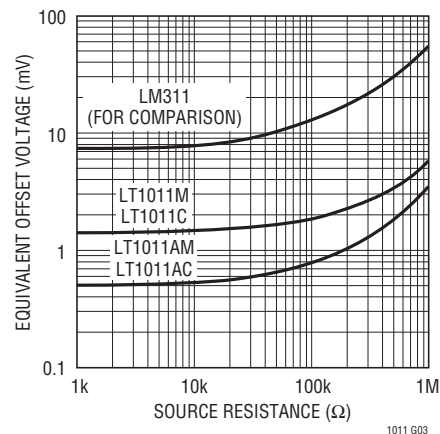
Input Bias Current



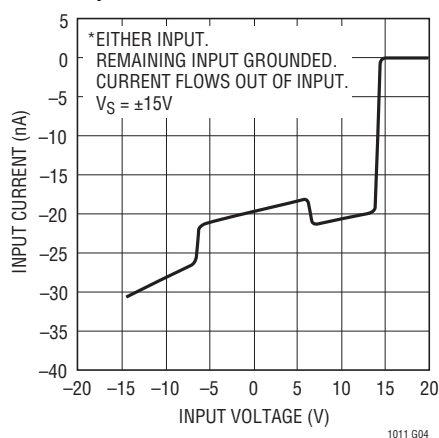
Input Offset Current



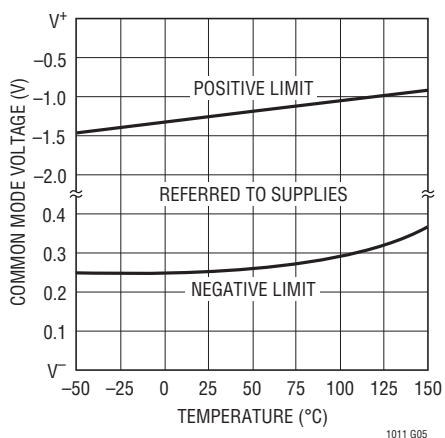
Worst-Case Offset Error



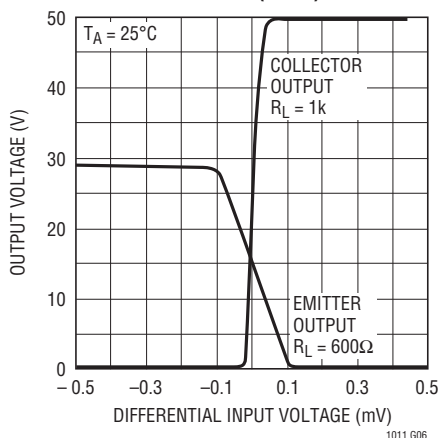
Input Characteristics*



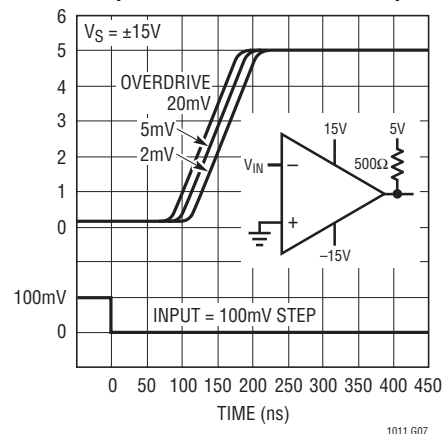
Common Mode Limits



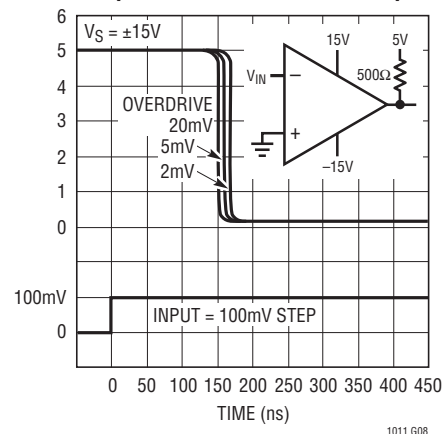
Transfer Function (Gain)



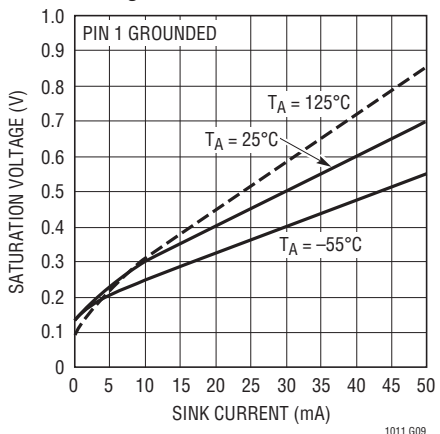
Response Time—Collector Output



Response Time—Collector Output

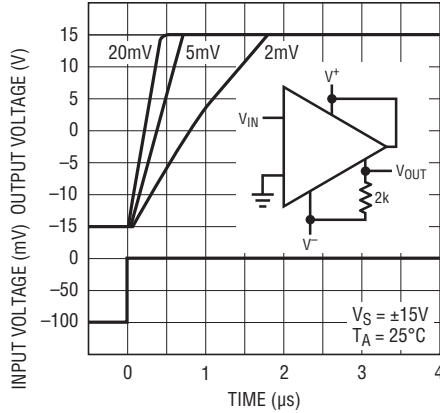


Collector Output Saturation Voltage

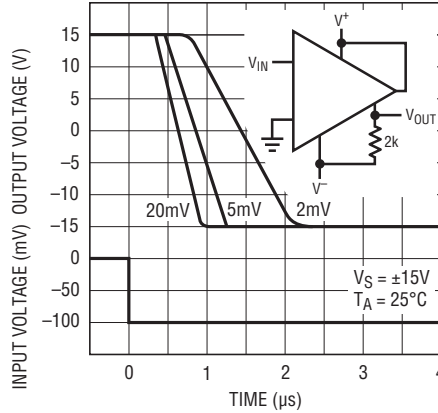


TYPICAL PERFORMANCE CHARACTERISTICS

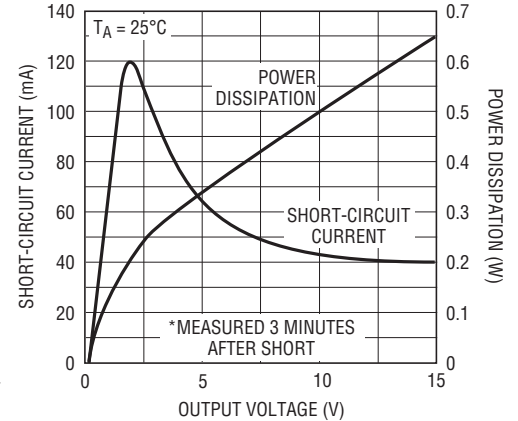
Response Time Using GND Pin as Output



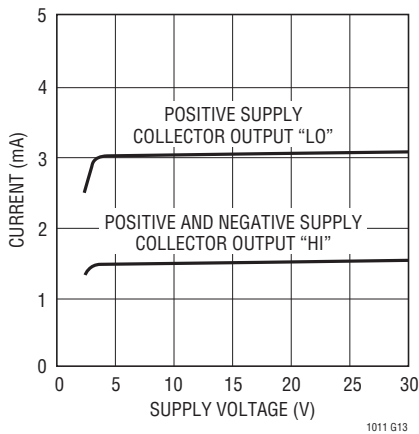
Response Time Using GND Pin as Output



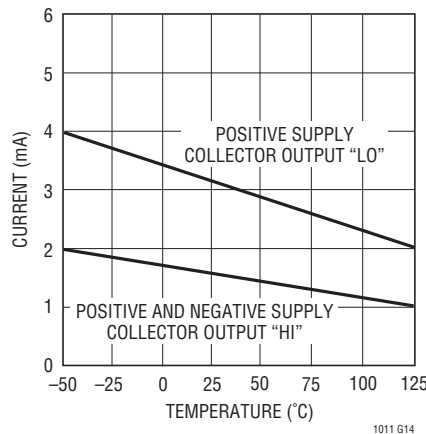
Output Limiting Characteristics*



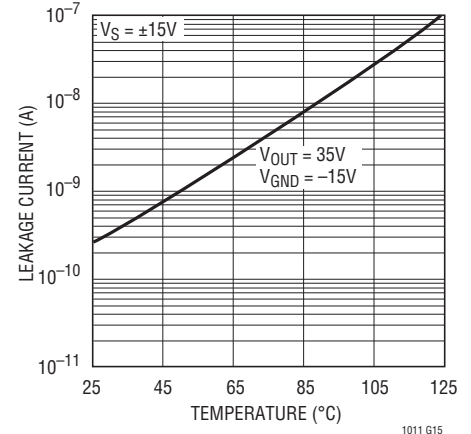
Supply Current vs Supply Voltage



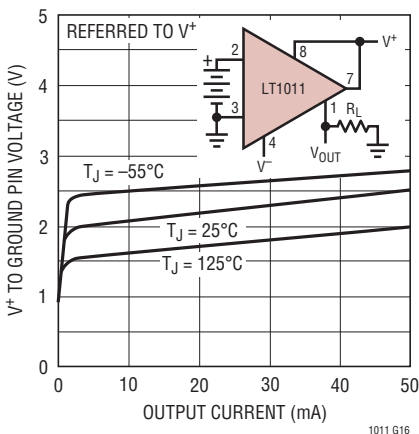
Supply Current vs Temperature



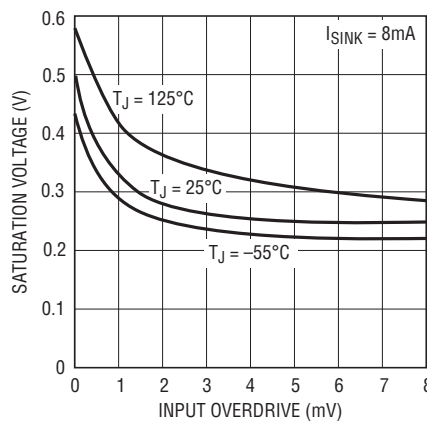
Output Leakage Current



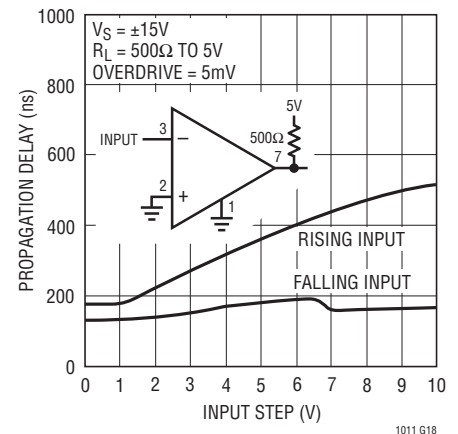
Output Saturation—Ground Output



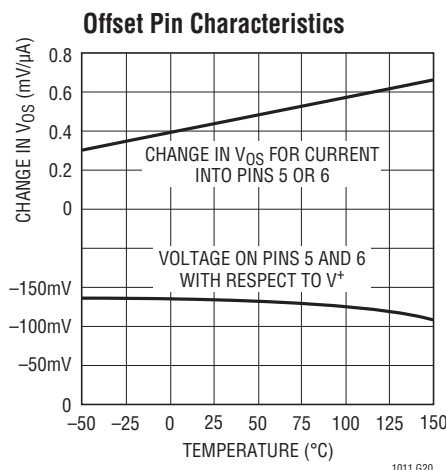
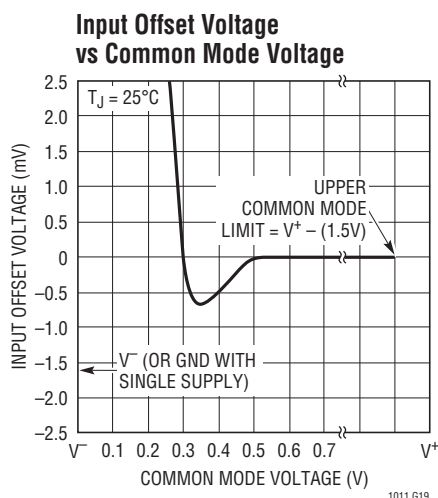
Output Saturation Voltage



Response Time vs Input Step Size



TYPICAL PERFORMANCE CHARACTERISTICS



APPLICATIONS INFORMATION

Preventing Oscillation Problems

Oscillation problems in comparators are nearly always caused by stray capacitance between the output and inputs or between the output and other sensitive pins on the comparator. This is especially true with high gain bandwidth comparators like the LT1011, which are designed for fast switching with millivolt input signals. The gain bandwidth product of the LT1011 is over 10GHz. Oscillation problems tend to occur at frequencies around 5MHz, where the LT1011 has a gain of ≈ 2000 . This implies that attenuation of output signals must be at least 2000:1 at 5MHz as measured at the inputs. If the source impedance is 1k Ω , the effective stray capacitance between output and input must have a reactance of more than $(2000)(1k\Omega) = 2M\Omega$, or less than 0.02pF. The actual interlead capacitance between input and output pins on the LT1011 is less than 0.002pF when cut to printed circuit mount length. Additional stray capacitance due to printed circuit traces must be minimized by routing the output trace directly away from input lines and, if possible, running ground traces next to input traces to provide shielding. Additional steps to ensure oscillation-free operation are:

1. Bypass the STROBE/BALANCE pins with a 0.01 μ F capacitor connected from Pin 5 to Pin 6. This eliminates stray capacitive feedback from the output to

the BALANCE pins, which are nearly as sensitive as the inputs.

2. Bypass the negative supply (Pin 4) with a 0.1 μ F ceramic capacitor close to the comparator. 0.1 μ F can also be used for the positive supply (Pin 8) if the pull-up load is tied to a separate supply. When the pull-up load is tied directly to Pin 8, use a 2 μ F solid tantalum bypass capacitor.
3. Bypass any slow moving or DC input with a capacitor ($\geq 0.01\mu$ F) close to the comparator to reduce high frequency source impedance.
4. Keep resistive source impedance as low as possible. If a resistor is added in series with one input to balance source impedances for DC accuracy, bypass it with a capacitor. The low input bias current of the LT1011 usually eliminates any need for source resistance balancing. A 5k Ω imbalance, for instance, will create only 0.25mV DC offset.
5. Use hysteresis. This consists of shifting the input offset voltage of the comparator when the output changes state. Hysteresis forces the comparator to move quickly through its linear region, eliminating oscillations by "overdriving" the comparator under all input conditions. Hysteresis may be either AC or DC. AC techniques do not shift the apparent offset voltage

APPLICATIONS INFORMATION

of the comparator, but require a *minimum* input signal slew rate to be effective. DC hysteresis works for all input slew rates, but creates a shift in offset voltage dependent on the previous condition of the input signal. The circuit shown in Figure 1 is an excellent compromise between AC and DC hysteresis.

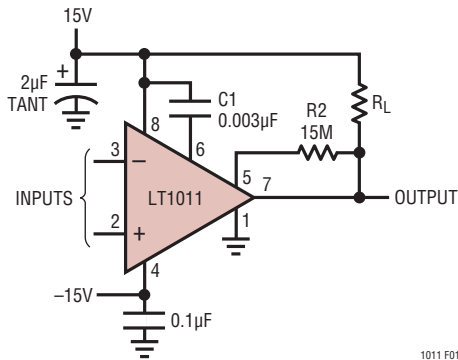


Figure 1. Comparator with Hysteresis

This circuit is especially useful for general purpose comparator applications because it does not force any signals directly back onto the input signal source. Instead, it takes advantage of the unique properties of the BALANCE pins to provide extremely fast, clean output switching even with low frequency input signals in the millivolt range. The $0.003\mu\text{F}$ capacitor from Pin 6 to Pin 8 generates AC hysteresis because the voltage on the BALANCE pins shifts slightly, depending on the state of the output. Both pins move about 4mV . If one pin (6) is bypassed, AC hysteresis is created. It is only a few millivolts referred to the inputs, but is sufficient to switch the output at nearly the maximum speed of which the comparator is capable. To prevent problems from low values of input slew rate, a slight amount of DC hysteresis is also used. The sensitivity of the BALANCE pins to current is about 0.5mV input referred offset for each micro-ampere of BALANCE pin current. The 15M resistor tied from OUTPUT to Pin 5 generates 0.5mV DC hysteresis. The combination of AC and DC hysteresis creates clean oscillation-free switching with very small input errors. Figure 2 plots input referred error versus switching frequency for the circuit as shown.

Note that at low frequencies, the error is simply the DC hysteresis, while at high frequencies, an additional

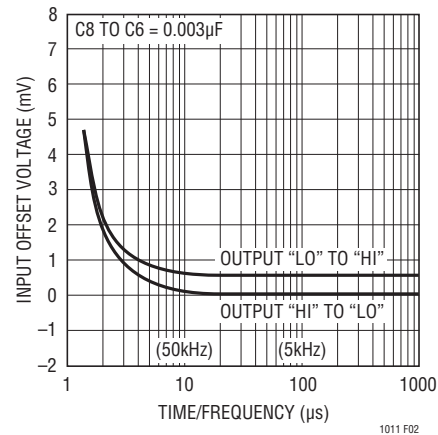


Figure 2. Input Offset Voltage vs Time to Last Transition

error is created by the AC hysteresis. The high frequency error can be reduced by reducing C_H , but lower values may not provide clean switching with very low slew rate input signals.

Input Protection

The inputs to the LT1011 are particularly suited to general purpose comparator applications because large differential and/or common mode voltages can be tolerated without damage to the comparator. Either or both inputs can be raised 40V above the negative supply, *independent of the positive supply voltage*. Internal forward biased diodes will conduct when the inputs are taken below the negative supply. In this condition, input current must be limited to 1mA. If very large (fault) input voltages must be accommodated, series resistors and clamp diodes should be used (see Figure 3).

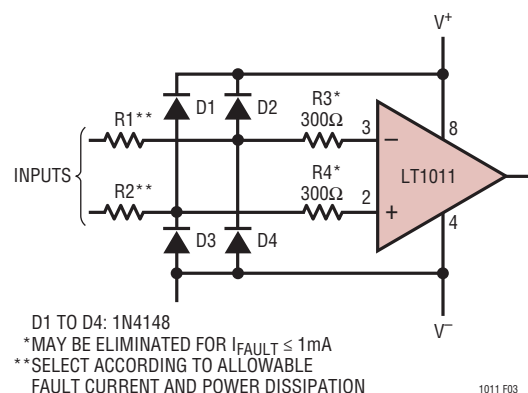


Figure 3. Limiting Fault Input Currents

APPLICATIONS INFORMATION

The input resistors should limit fault current to a reasonable value (0.1mA to 20mA). Power dissipation in the resistors must be considered for continuous faults, especially when the LT1011 supplies are off. One final caution: lightly loaded supplies may be forced to higher voltages by large fault currents flowing through D1-D4.

R3 and R4 limit input current to the LT1011 to less than 1mA when the input signals are held below V^- . They may be eliminated if R1 and R2 are large enough to limit fault current to less than 1mA.

Input Slew Rate Limitations

The response time of a comparator is typically measured with a 100mV step and a 5mV to 10mV overdrive. Unfortunately, this does not simulate many real world situations where the step size is typically much larger and overdrive can be significantly less. In the case of the LT1011, step size is important because the slew rate of internal nodes will limit response time for input step sizes larger than 1V. At 5V step size, for instance, response time increases from 150ns to 360ns. See the curve "Response Time vs Input Step Size" for more detail.

If response time is critical and large input signals are expected, clamp diodes across the inputs are recommended. The slew rate limitation can also affect performance when differential input voltage is low, but both inputs must slew quickly. Maximum suggested common mode slew rate is 10V/ μ s.

Strobing

The LT1011 can be strobed by pulling current out of the STROBE pin. The output transistor is forced to an "off" state, giving a "hi" output at the collector (Pin 7). Currents as low as 250 μ A will cause strobing, but at low strobe currents, strobe delay will be 200ns to 300ns. If strobe current is increased to 3mA, strobe delay drops to about 60ns. The voltage at the STROBE pin is about 150mV below V^+ at zero strobe current and about 2V below V^+ for 3mA strobe current. *Do not ground the STROBE pin. It must be current driven.* Figure 4 shows a typical strobe circuit.

Note that there is no bypass capacitor between Pins 5 and 6. This maximizes strobe speed, but leaves the comparator more sensitive to oscillation problems for slow, low

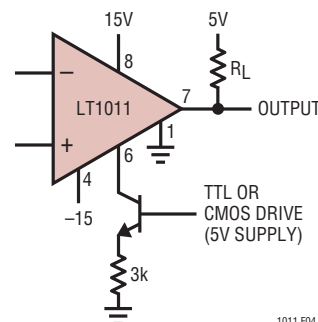


Figure 4. Typical Strobe Circuit

level inputs. A 1pF capacitor between the output and Pin 5 will greatly reduce oscillation problems without reducing strobe speed.

DC hysteresis can also be added by placing a resistor from output to Pin 5. See step 5 under "Preventing Oscillation Problems."

The pin (6) used for strobing is also one of the offset adjust pins. Current flow into or out of Pin 6 must be kept very low ($<0.2\mu$ A) when not strobing to prevent input offset voltage shifts.

Output Transistor

The LT1011 output transistor is truly floating in the sense that no current flows into or out of either the collector or emitter when the transistor is in the "off" state. The equivalent circuit is shown in Figure 5.

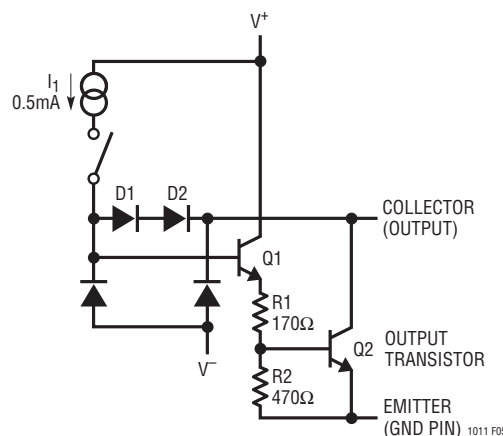


Figure 5. Output Transistor Circuitry

APPLICATIONS INFORMATION

In the “off” state, I_1 is switched off and both Q1 and Q2 turn off. The collector of Q2 can be now held at any voltage above V^- without conducting current, including voltages above the positive supply level. Maximum voltage above V^- is 50V for the LT1011M and 40V for the LT1011C/I. The emitter can be held at any voltage between V^+ and V^- as long as it is negative with respect to the collector.

In the “on” state, I_1 is connected, turning on Q1 and Q2. Diodes D1 and D2 prevent deep saturation of Q2 to improve speed and also limit the drive current of Q1. The R1/R2 divider sets the saturation voltage of Q2 and provides turn-off drive. Either the collector or emitter pin can be held at a voltage between V^+ and V^- . This allows the remaining pin to drive the load. In typical applications, the emitter is connected to V^- or ground and the collector drives a load tied to V^+ or a separate positive supply.

When the emitter is used as the output, the collector is typically tied to V^+ and the load is connected to ground or V^- . Note that the emitter output is phase reversed with respect to the collector output so that the “+” and “-” input designations must be reversed. When the collector

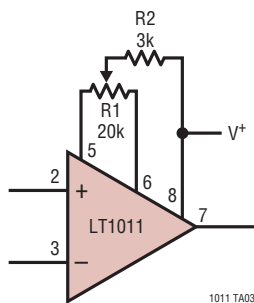
is tied to V^+ , the voltage at the emitter in the “on” state is about 2V below V^+ (see curves).

Input Signal Range

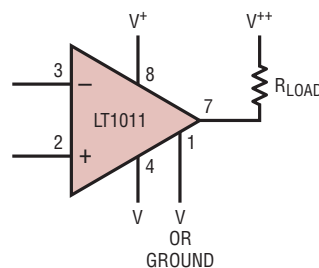
The common mode input voltage range of the LT1011 is about 300mV above the negative supply and 1.5V below the positive supply, independent of the actual supply voltages (see curve in the Typical Performance Characteristics). This is the voltage range over which the output will respond correctly when the common mode voltage is applied to one input and a higher or lower signal is applied to the remaining input. *If one input is inside the common mode range and one is outside, the output will be correct. If the inputs are outside the common mode range in opposite directions, the output will still be correct. If both inputs are outside the common mode range in the same direction, the output will not respond to the differential input; for temperatures of 25°C and above, the output will remain unconditionally high (collector output), for temperatures below 25°C, the output becomes undefined.*

TYPICAL APPLICATIONS

Offset Balancing

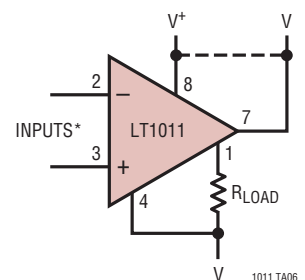


Driving Load Referenced to Positive Supply



V^{++} CAN BE GREATER OR LESS THAN V^+

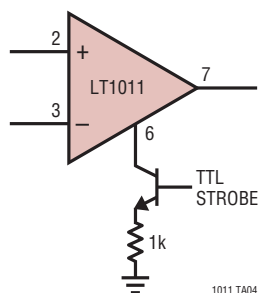
Driving Load Referenced to Negative Supply



*INPUT POLARITY IS REVERSED WHEN USING PIN 1 AS OUTPUT

TYPICAL APPLICATIONS

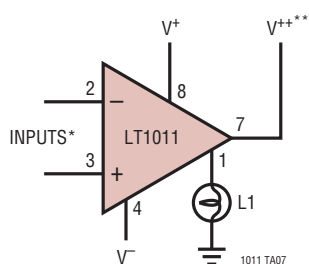
Strobing



NOTE: DO NOT GROUND STROBE PIN

1011 TA04

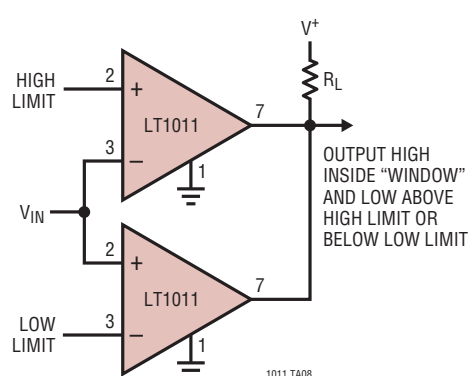
Driving Ground Referred Load



*INPUT POLARITY IS REVERSED WHEN USING PIN 1 AS OUTPUT
**V+ MAY BE ANY VOLTAGE ABOVE V-. PIN 1 SWINGS TO WITHIN $\approx 2V$ OF V+

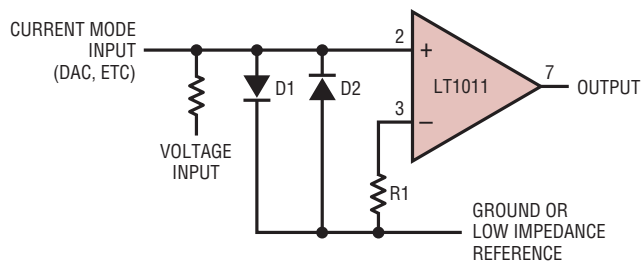
1011 TA07

Window Detector



1011 TA08

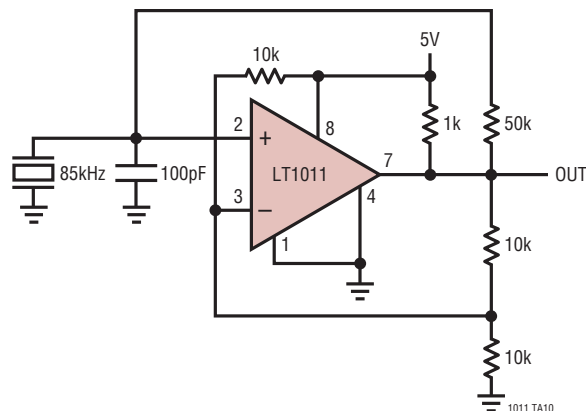
Using Clamp Diodes to Improve Frequency Response*



*SEE CURVE, "RESPONSE TIME vs INPUT STEP SIZE"

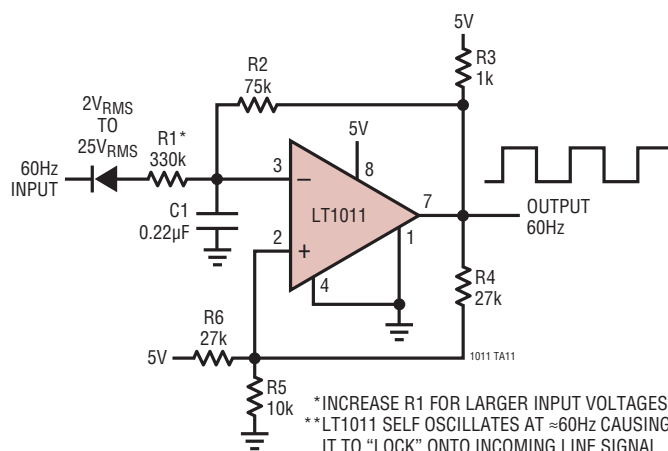
1011 TA09

Crystal Oscillator



1011 TA10

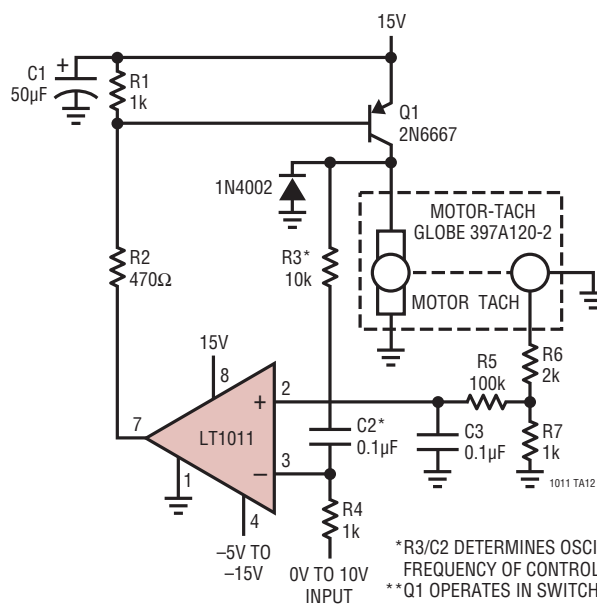
Noise Immune 60Hz Line Sync**



*INCREASE R1 FOR LARGER INPUT VOLTAGES
**LT1011 SELF OSCILLATES AT $\approx 60\text{Hz}$ CAUSING IT TO "LOCK" ONTO INCOMING LINE SIGNAL

1011 TA11

High Efficiency** Motor Speed Controller

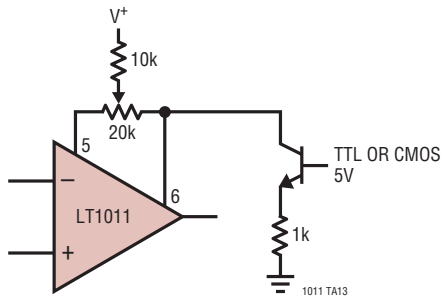


*R3/C2 DETERMINES OSCILLATION FREQUENCY OF CONTROLLER
**Q1 OPERATES IN SWITCH MODE

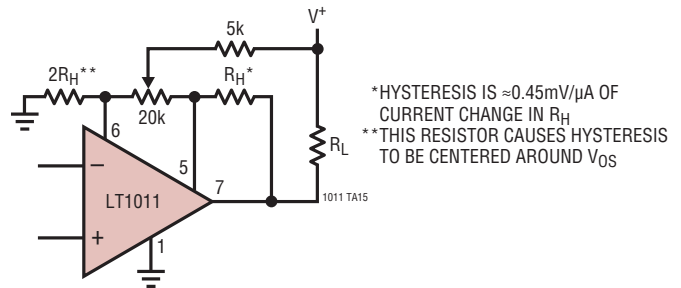
1011 TA12

TYPICAL APPLICATIONS

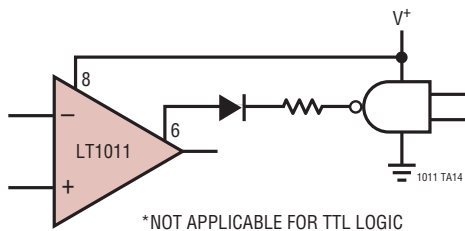
Combining Offset Adjust and Strobe



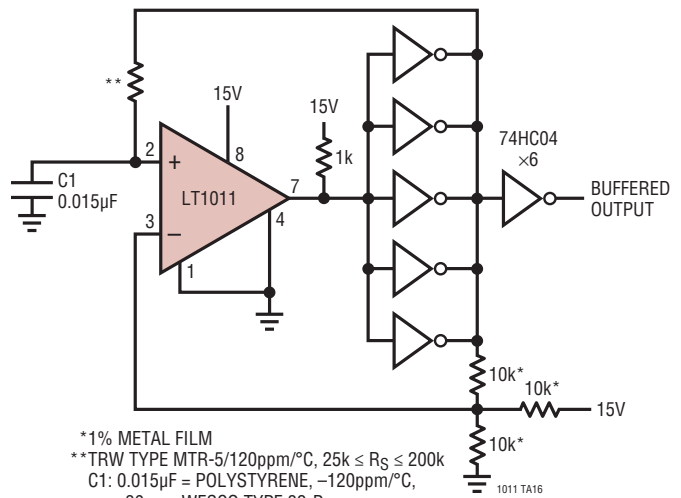
Combining Offset Adjustment and Hysteresis



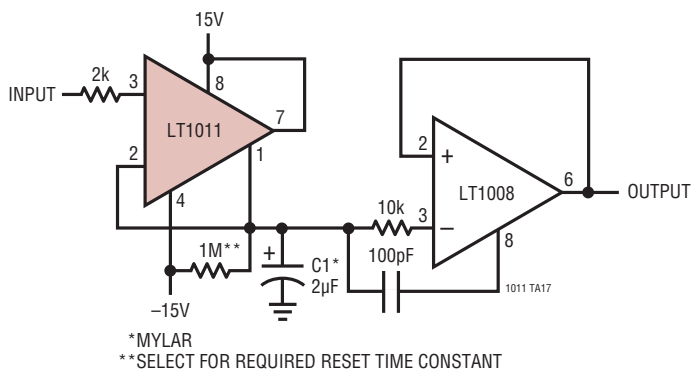
Direct Strobe Drive When CMOS* Logic Uses Same V^+ Supply as LT1011



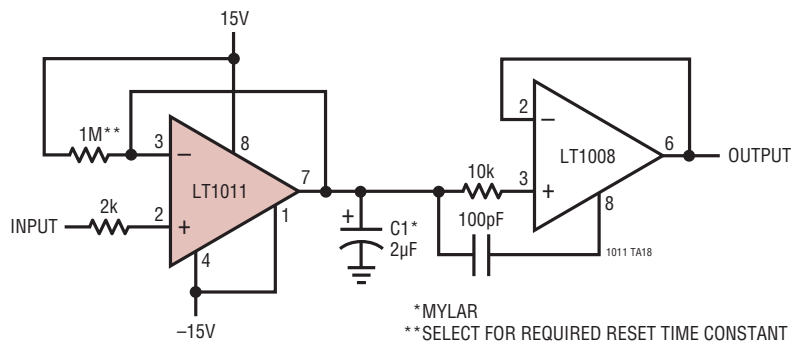
Low Drift R/C Oscillator†



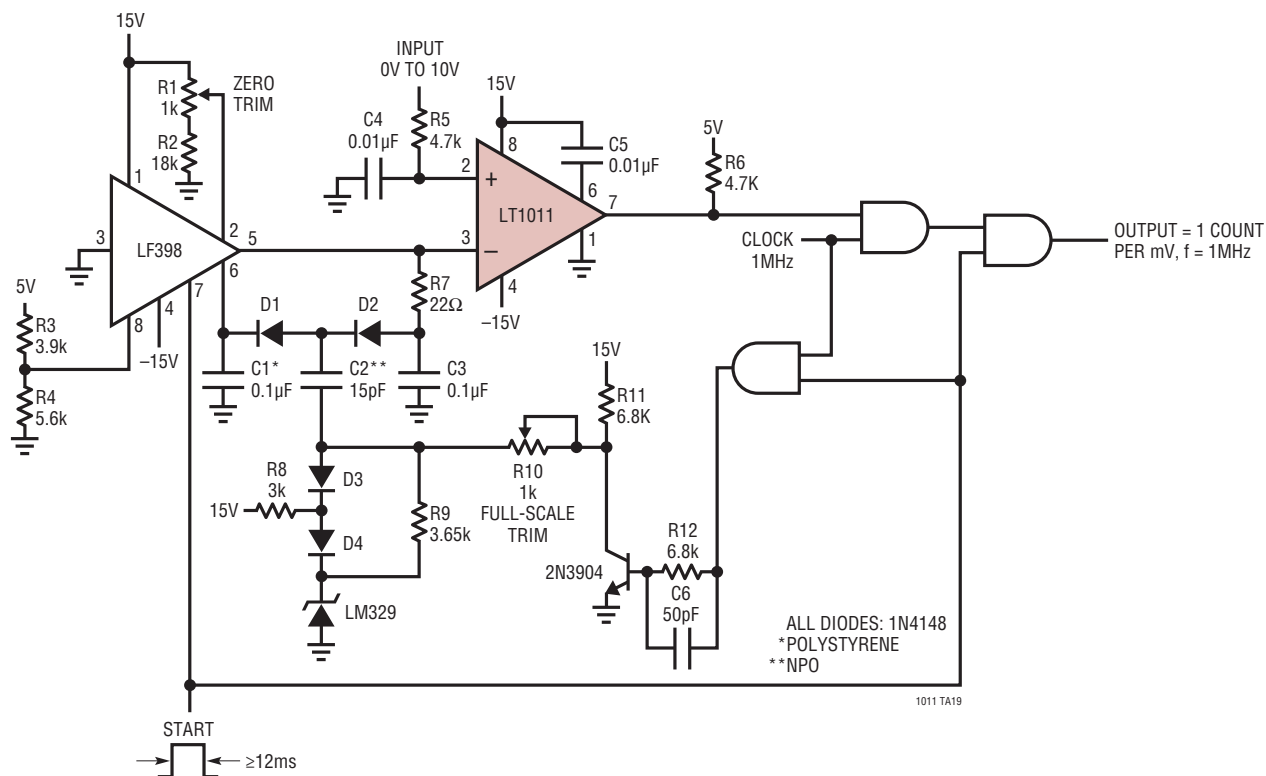
Positive Peak Detector



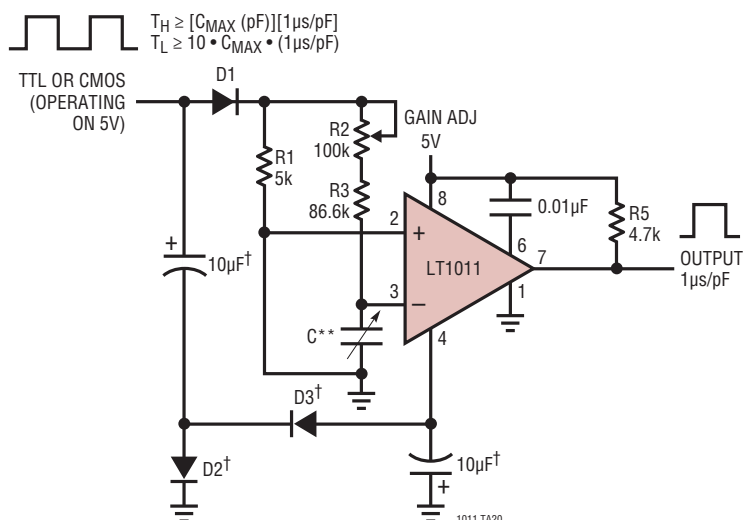
Negative Peak Detector



4-Digit (10,000 Count) A/D Converter



Capacitance to Pulse Width Converter


$$*PW = (R2 + R3)(C) \left(\frac{R1 + R4}{R1} \right), \text{ INPUT CAPACITANCE OF}$$

LT1011 IS $\approx 6\text{pF}$. THIS IS AN OFFSET TERM.

**TYPICAL 2 SECTIONS OF 365pF VARIABLE CAPACITOR WHEN USED AS SHAFT ANGLE INDICATION

†THESE COMPONENTS MAY BE ELIMINATED IF
NEGATIVE SUPPLY IS AVAILABLE (−1V TO −15V)

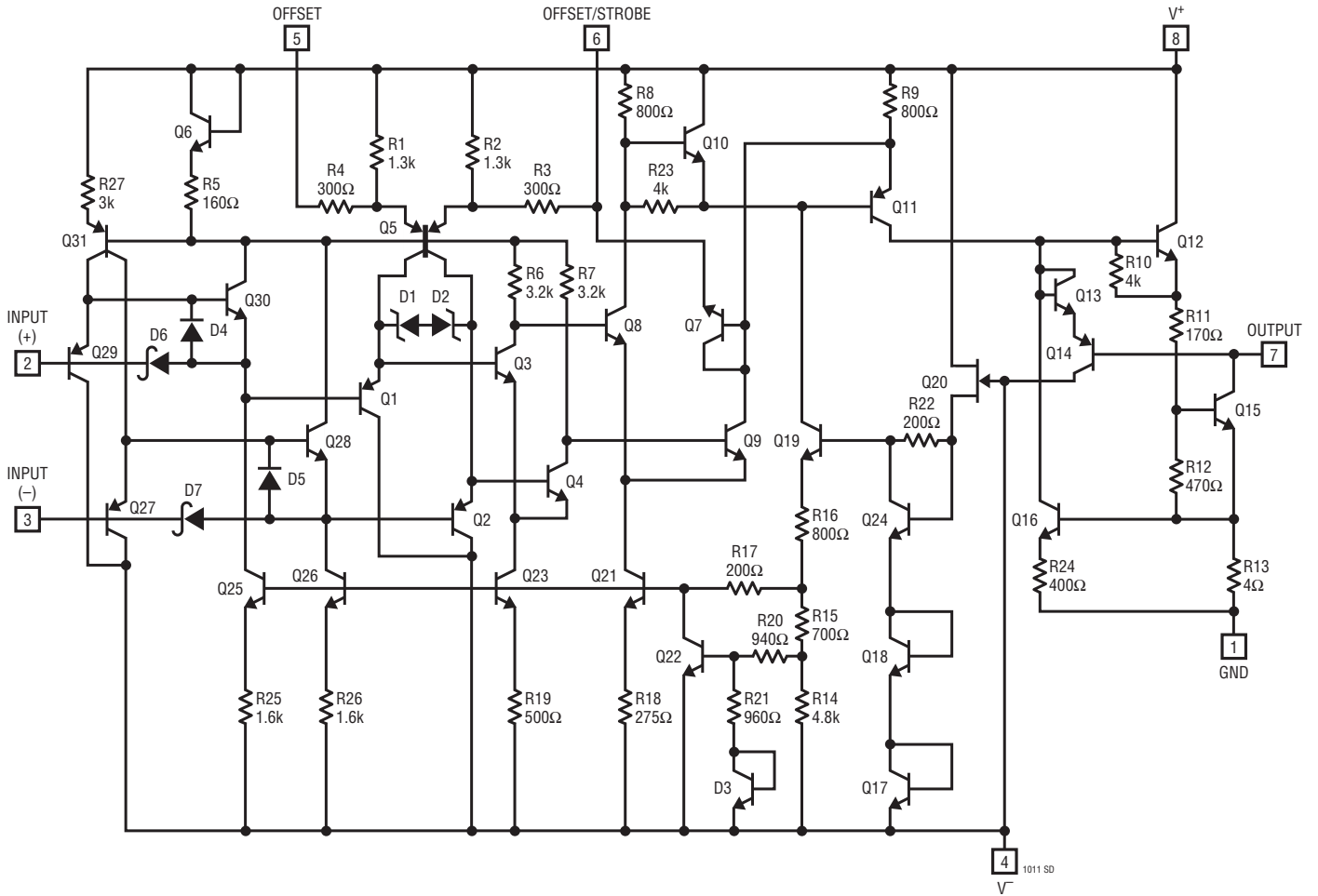
The circuit diagram shows a precision rectifier configuration. It consists of two LT1011 operational amplifiers and one LT1008C comparator.

- LT1011 Op-Amp 1:** The non-inverting input (+) is connected to ground through a 10k resistor. The inverting input (-) is connected to the input signal V_{IN} through a 4.7k resistor and to the output of the second LT1011 through a feedback loop containing a 100k resistor and a 0.1μF capacitor. The output of the first LT1011 is connected to the inverting input of the second LT1011 through a 1.5k resistor.
- LT1011 Op-Amp 2:** The non-inverting input (+) is connected to ground through a 10k resistor. The inverting input (-) is connected to the output of the first LT1011 through a 1.5k resistor. The output of the second LT1011 is connected back to its inverting input through a 4.7k resistor.
- LT1008C Comparator:** The non-inverting input (+) is connected to the output of the second LT1011. The inverting input (-) is connected to the output of the first LT1011 through a 1M resistor and to ground through a 1μF capacitor. The output of the comparator is connected to the output of the second LT1011 through a 1M resistor.

The circuit is powered by a -15V supply and a +15V supply. A threshold voltage is set by a 5k resistor connected to the +15V supply and another 5k resistor connected to the output of the second LT1011. A dashed box labeled "OFM-1A**" encloses the 1.5k resistor and the 1μF capacitor.

The diagram shows a precision rectifier circuit. An AC input signal is connected to the non-inverting input (pin 2) of an LT1011 op-amp. A feedback path from the output (pin 7) to the inverting input (pin 3) consists of a 100Ω resistor and a 0.033μF capacitor in parallel, followed by a 5kΩ resistor and a 'ZERO CROSS TRIM' potentiometer. The op-amp is powered by a 5V supply (pin 8) and a -5V supply (pin 4). The output of the op-amp (pin 7) is connected to the input of a 74C04 inverter. The output of this inverter is connected to the input of a second 74C04 inverter. The output of the second inverter is connected to the positive input of a full-wave bridge rectifier. The negative input of the bridge is connected to ground. The bridge consists of four diodes, with one diode labeled 'HP5082-2800 x4'. The output of the bridge is connected to a 1kΩ resistor to ground. The bridge is also connected to a 5V supply and a -5V supply through 12kΩ resistors. The output of the bridge is labeled 'RECTIFIED OUTPUT'.

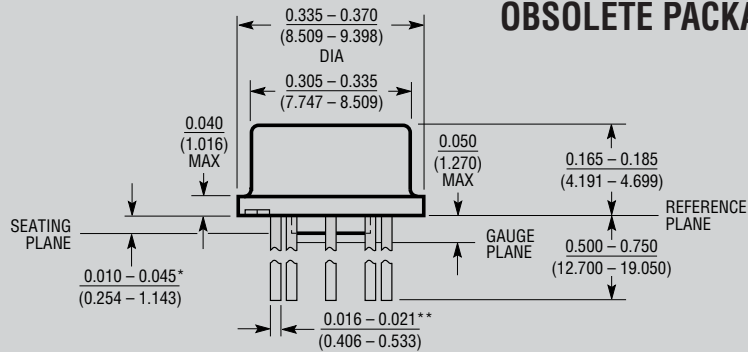
SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION

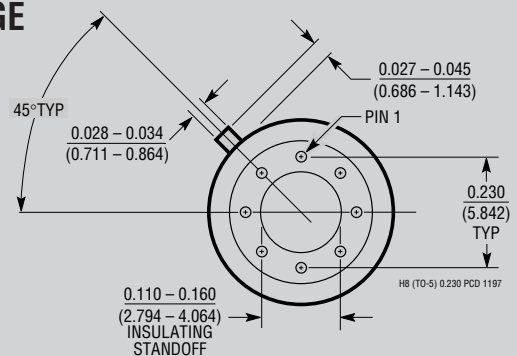
H Package
8-Lead TO-5 Metal Can (.230 Inch PCD)
 (Reference LTC DWG # 05-08-1321)

OBsolete PACKAGE



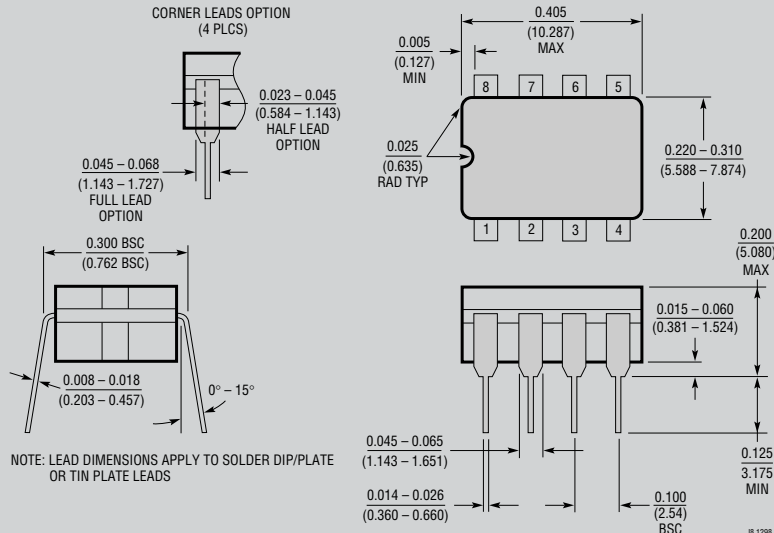
*LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND 0.045" BELOW THE REFERENCE PLANE

**FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS 0.016 - 0.024 (0.406 - 0.610)



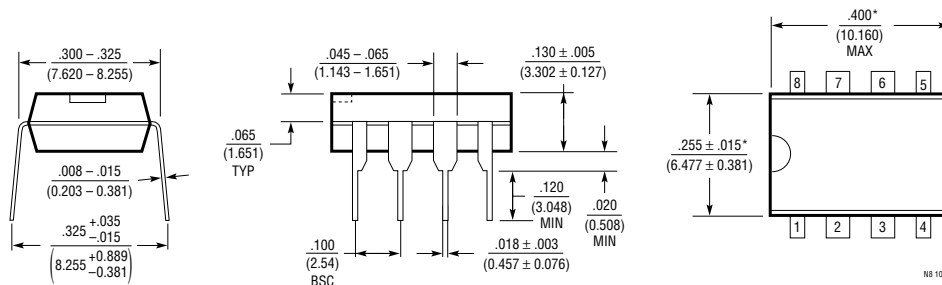
PACKAGE DESCRIPTION

J8 Package 8-Lead Cerdip (Narrow .300 Inch, Hermetic) (Reference LTC DWG # 05-08-1110)

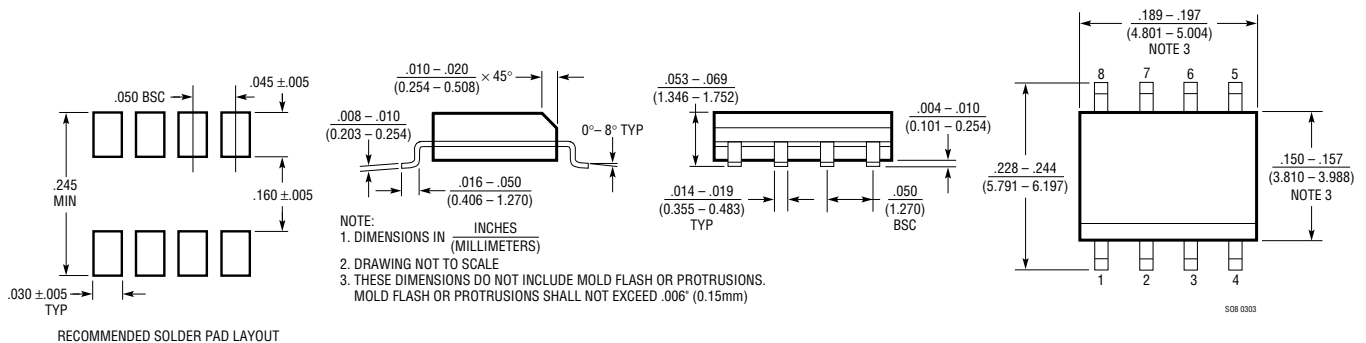


OBsolete PACKAGE

N8 Package 8-Lead PDIP (Narrow .300 Inch) (Reference LTC DWG # 05-08-1510)



S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)



ALL DIODES 1N4148
TRANSISTORS 2N3904
*USED ONLY TO GUARANTEE START-UP
†MAY BE INCREASED FOR BETTER 10Hz TRIM RESOLUTION

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1016	UltraFast™ Precision Comparator	Industry Standard 10ns Comparator
LT1116	12ns Single Supply Ground-Sensing Comparator	Single Supply Version of the LT1016
LT1394	UltraFast Single Supply Comparator	7ns, 6mA Single Supply Comparator
LT1671	60ns, Low Power Comparator	450µA Single Supply Comparator

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