TEXAS INSTRUMENTS

General TSB12LV23 (OHCILynx)

Implementation Guide

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Mixed Signal Products

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General TSB12LV23 (OHCILynx) Implementation Guide

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ABSTRACT

This implementation guide assists platform hardware developers designing with the TSB12LV23 1394 Open Host Controller Interface (OHCI) Link-Layer Controller (LLC), referred to herein as the OHCI-Lynx.

The document includes an overview of the TSB12LV23 function and features, terminal assignments and pinout illustrations, TSB12LV23 I/O electrical characteristics, identification of required passive components and recommendations for system implementation, and phy/link signal isolation considerations.

1 Product Support

1.1 Related Documentation

The following list specifies product names, part numbers, and literature numbers of corresponding TI documentation.

- *Galvanic Isolation of the IEEE 1394–1995 Serial Bus*, Literature number SLLA001
- *Reference Designs for Host System Boards* (SLLA049)*, Adapter Cards*, Literature number SLLA048 and SLLA052, and *Mobile*, Literature number SLLA047
- *TSB12LV23 Data Manual,* Literature number SLLS328

1.2 World Wide Web

Our World Wide Web site at www.ti.com contains the most up-to-date product information, revisions, and additions. Users registering with TI&ME can build custom information pages and receive new product updates automatically via email.

1.3 TSB12LV23 (OHCI-Lynx) Function and Features

The Texas Instruments TSB12LV23 is a PCI-to-1394 host controller compatible with the latest PCI local bus, PCI bus power management interface, IEEE 1394-1995, and 1394 open host controller interface (OHCI) specifications. The chip provides the IEEE 1394 link function, and is compatible with serial bus data rates of 100 Mbits/s, 200 Mbits/s, and 400 Mbits/s.

As required by the *1394 Open Host Controller Interface (OHCI)* and *IEEE 1394A* Specifications, internal control registers are memory-mapped and non-pre-fetchable. The PCI configuration header is accessed through configuration cycles specified by PCI, and provides Plug-and-Play (PnP) compatibility. Furthermore, the TSB12LV23 is compliant with the *PCI Bus Power Management Interface Specification*, per the *PC 98* requirements. TSB12LV23 supports the D0, D2, and D3 power states.

The TSB12LV23 design provides PCI bus master bursting, and is capable of transferring a cacheline of data at 132 Mbytes/s after connection to the memory controller. Since PCI latency can be large even on a PCI Revision 2.1 system, deep FIFOs are provided to buffer 1394 data.

The TSB12LV23 provides physical write posting buffers and a highly tuned physical data path for SBP-2 performance. The TSB12LV23 also provides multiple isochronous contexts, multiple cacheline burst transfers, advanced internal arbitration, and bus holding buffers on the PHY/Link interface, thus, making the TSB12LV23 the best-in-class 1394 OHCI solution.

An advanced CMOS process is used to achieve low power consumption while operating at PCI clock rates up to 33 MHz.

1.4 TSB12LV23 Feature Set

- IEEE1394 Open Host Controller Interface Specification 1.0 Compliant
- IEEE1394–1995 and 1394.A Compliant
- PCI Local Bus Specification Revision 2.1 Compliant and PCI 2.2 ready
- PCI Power Management Compliant
- 3.3-V Core Logic with Universal PCI Interface Compatible with 3.3-V and 5-V PCI Signalling Environment
- Supports Serial Bus Data Rates of 100, 200, and 400Mbit/s
- Provides Bus-Hold Buffers on Physical Interface for Low-Cost Single Capacitor Isolation
- Supports Physical Write Posting of up to Three Outstanding Transactions
- Serial ROM Interface Supports 2-Wire Devices
- Supports External Cycle Timer Control for Customized Synchronization
- Implements PCI Burst Transfers and Deep FIFOs to Tolerate Large Host Latency
- Provides Two General-Purpose I/Os
- Fabricated in Advanced Low-Power CMOS Process
- Packaged in 100-Pin (PZ) LQFP Package
- Supports $\overline{\text{CLKRUN}}$
- Drop-In Replacement for the TSB12LV22
- Supports PCI and CardBus Applications

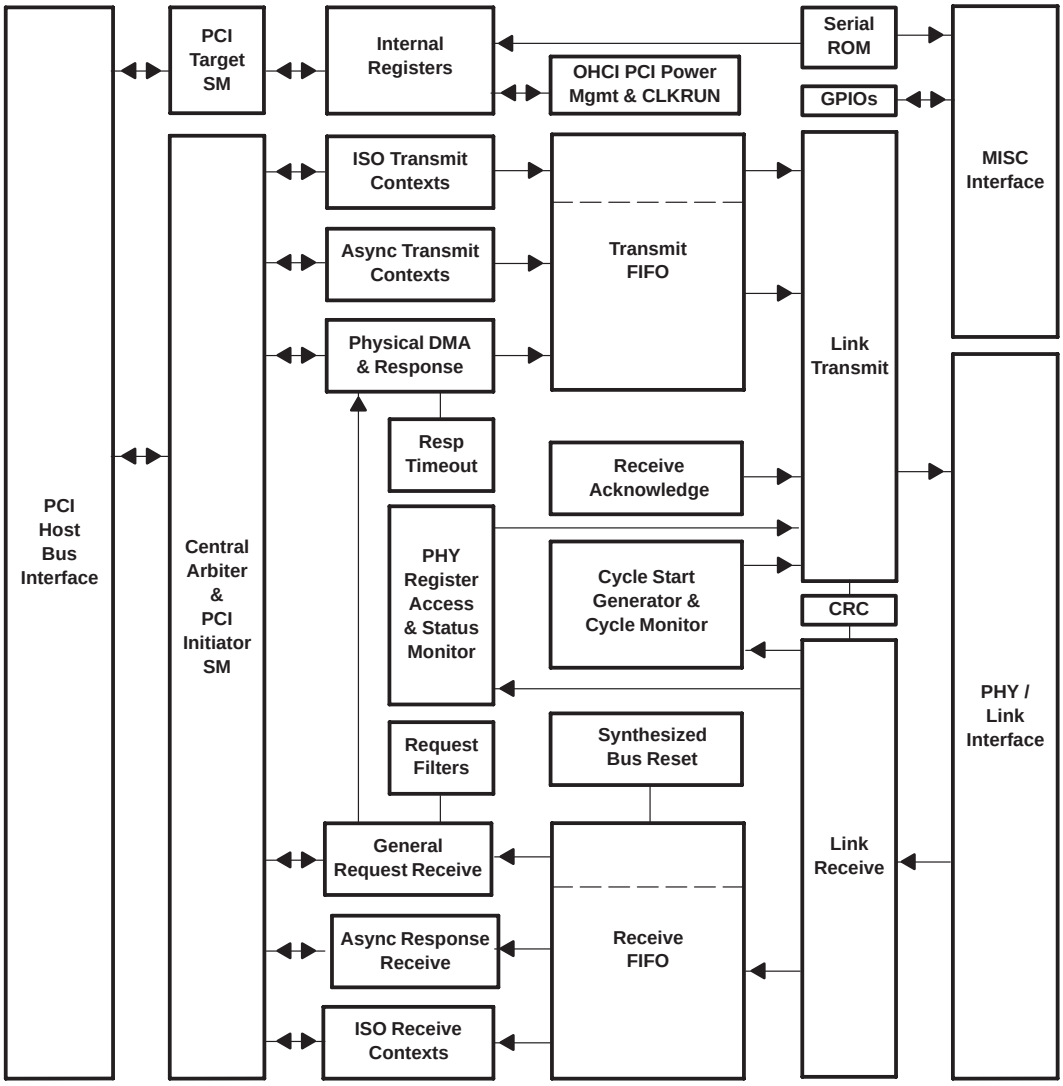


Figure 1. TSB12LV23 Block Diagram

1.5 OHCILynx System Implementation

Figure 1 illustrates a platform using the TSB12LV23, which, along with the TSB41LV03, provides the necessary interface to implement a three-port IEEE1394 node.

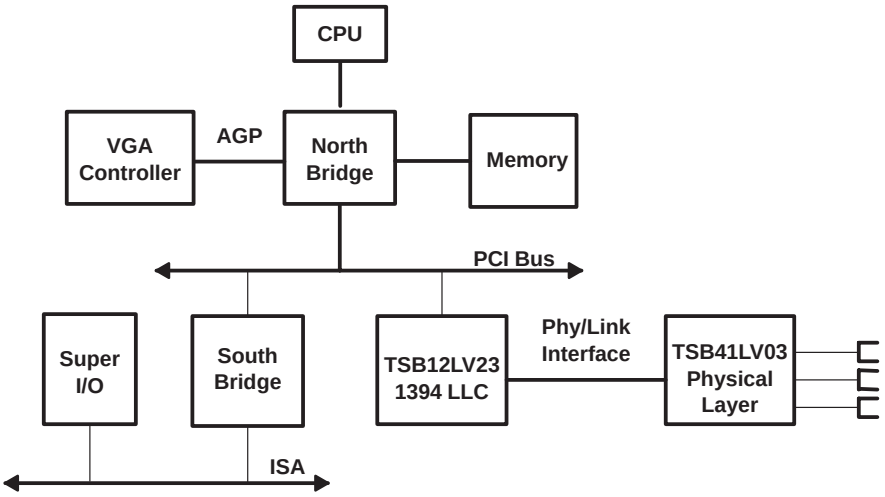


Figure 2. Typical System Architecture

1.6 Drop-In Compatibility with the TSB12LV22

The TSB12LV23 can be placed on a pad layout for the TSB12LV22 with no changes. It uses the exact same WDM drivers as the TSB12LV22 (i.e., 1394bus.sys and ohci1394.sys), which makes it a direct replacement for the TSB12LV22.

The TSB12LV23 is designed to be drop-in compatible with OHCI-Lynx designs. Some I/Os implement weak pullup or pulldown resistors for drop-in compatibility with OHCI-Lynx. These internal resistors and OHCI-Lynx implementation requirements are noted in the following table.

Table 1. Internal Resistors and OHCI-Lynx Implementation

TERMINAL		WEAK RESISTOR	DROP-IN COMPATIBILITY NOTE
TERMINAL NAME	NO.		
$\overline{\text{CARDBUS}}$/CYCLEOUT	77	Pullup	OHCI-Lynx CYCLEOUT must be tied high or pulled up
CLKRUN	7	Pulldown	OHCI-Lynx RSVD must be unconnected or pulled down
RST	10	Pullup	OHCI-Lynx TEST_EN must be tied high

Refer, also, to the *TSB12LV22 (OHCI-Lynx) Implementation Guide* (literature number: SLLA025) for more information.

1.6.1 Serial EEPROM Drop-In Compatibility Implementation

There has been no major change in the implementation of the serial EEPROM. However, The EEPROM programming code will need to be upgraded for the new TSB12LV23 register set.

The EEPROM is used to load the system specific registers, such as the GUID. The data file, which loads the EEPROM, will need to be modified. However, for new boards, the EEPROM should be programmed with the modified data from the start.

For retrofitted boards, the EEPROM should be reprogrammed so it loads all ,of the system specific registers correctly. If the EEPROM is being programmed from BIOS, programming the EEPROM is not a concern.

NOTE: Do not set GlobalByte swap bit via the EEPROM data file. This will cause problems (bit 0 at offset 13)

In Addition, use TI's latest version of the EEPROM software to program the EEPROM, and follow these steps.

The EEPROMs of all modified boards must be written, as the new registers beyond EEPROM word address 0xFh are written by the TSB12LV23 and the default value 0xFFh will set the GlobalSwap bit, which will effect operation. The following list of steps is a general procedure and should be used when modifying a PCB from the TSB12LV22 to the TSB12LV23.

NOTE: The following procedure assumes that the EEPROM has been previously programmed with valid data. If the EEPROM has not previously been programmed, use the TSB12LV23 data file as a template to edit and program the EEPROM accordingly.

1. After replacing the TSB12LV22 with the TSB12LV23, dump the current contents of the serial EEPROM using TI's EEPROM utility:

   ```
   eelynx /d temp.dat
   ```

2. Edit the temp.dat file, appending the following register data to the end of the file:

   ```
   010    0x10   ;00010000 Link Enhancement Byte 1
   011    0x00   ;00000000 PCI Misc Byte 0
   012    0x24   ;00100100 PCI Misc Byte 1
   013    0x00   ;00000000 PCI OHCI Control Byte 0
   014    0x00   ;00000000 CIS Offset
   ```

3. Program the EEPROM with the new file using the EELynx utility:

   ```
   eelynx /p temp.dat
   ```

This procedure will set the proper defaults for the TSB12LV23 and will maintain the existing GUID as previously programmed.

1.6.2 Connecting the Serial EEPROM

Implementation requires the connection of GPIO2 to SCL, and GPIO3 to SDA to enable on-board EEPROM programming.

- It is recommended that header and jumpers for SCL and SDA lines be used to meet 1394.a security requirements. Jumpers on the EEPROM with write control can also be used.
- Another alternative is to use a serial EEPROM with software write protection (SGS M34C02).

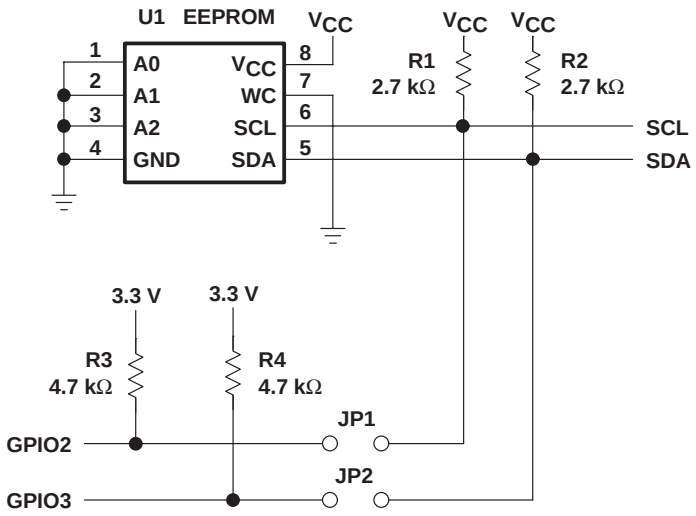


Figure 3. Connecting the Serial EEPROM

2 TSB12LV23 Implementation

2.1 Passive Component Requirements

2.1.1 Required Pullup/Pulldown Resistors

Several signals on the TSB12LV23 require a pullup or pulldown resistor. Table 2 provides a list of required resistors.

Table 2. Required Pullup/Pulldown Resistors (see Note 1)

SIGNAL	RESISTOR	RECOMMENDED VALUE (Ω)	CONDITION
SDA	Pullup	2.7 k	Required if implementation includes a serial EEPROM.
SCL	Pullup	2.7 k	Required if implementation includes a serial EEPROM.
$\overline{\text{RST}}$	Pullup	4.7 k	If the design does not use the D3_cold Power Management, then this terminal can be pulled up or $\overline{\text{RST}}$ can be connected to G_RST directly.
ISOLATED	Pullup (Default)	4.7 k	Required when **not** implementing bus holder isolation
	Pulldown	220	Required when bus holder isolation is implemented
CYCLEIN	Pullup	4.7 k	Required if not implementing optional external 8-kHz clock.
GPI02	Pulldown	220	Required
GPI03	Pulldown	220	Required

NOTE 1: All pullup/pulldown resistor value recommendations are provided as guidelines only. The best value for an individual design may vary depending upon board characteristics, standard design rules and practices, etc.

3 The PHY-Link Interface

The PHY-Link interface follows the IEEE 1394-1995 and 1394.a standards. No isolation is implemented in this schematic. The PHY and Link operate with common power and ground planes.

The schematic shows no adjustment for EMI considerations. To help minimize EMI, we suggest including a 0-Ω resistor on the SCLK signal as close as possible to the PHY. If EMI issues are a concern, the value of this resistor can be adjusted to reduce emissions. This will also reduce reflections that may occur when the distance between the PHY and Link is large (greater than 4 inches.)

The SCLK is a 49.152-MHz clock provided by the PHY to the Link. SCLK is essential for transactions on the PHY-Link interface as well as transactions within the Link.

The LREQ, or Link Request, signal is an input to the PHY from the Link. The Link uses this to initiate a service request to the PHY. CTL0 and CTL1 are bidirectional signals used to control communication between the PHY and the Link. These terminals should be directly connected between the PHY and Link.

Both the TSB12LV23 (Link layer) and the TSB41LV03 (Phy) are 400-Mbps devices, which use terminals D0–D7 to transport data bidirectionally, and should be connected directly to each other respectively (i.e., D0 ↔ D0 . . . D7 ↔ D7).

The Link's PHY_LPS (Link Power Status) terminal is asserted to indicate that the Link is powered on. The LPS input on the PHY can be tied to either the Link layer's PHY_LPS terminal or the Link layer's VCC. In addition, the line connecting the Link's PHY_LPS terminal with the PHY's LPS terminal should be pull down to ground through a 1-kΩ resistor.

As is shown in Figure 4, the BMC/PHY_LINKON terminal on the TSB12LV23 is connected to the TSB41LV03 C/LKON terminal through a 1-kΩ series resistor and 10-kΩ pulldown resistor on the TSB41LV03 side. The PHY's LKON signal is used to activate (wake) the Link when the Link is not active. This signal is driven low as long as the Link is not active.

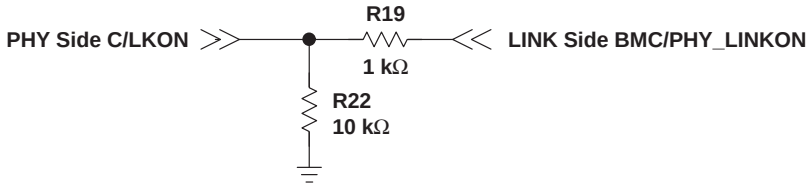


Figure 4. Link On

All of the above PHY-Link interface signals could also be connected to test header that would provide test points for new prototype.

4 The Link Layer - TSB12LV23 OHCI-Lynx

The TSB12LV23 is a 400-Mbps Link-layer specifically designed with power management and $\overline{\text{CARDBUS}}$ features.

All of the 3.3-V V_{CC} power terminals on the TSB12LV23 should be coupled together and grounded through a series of high-frequency decoupling capacitors.

- Place one 0.01-μF and one 0.1-μF capacitor as closely as possible to each power terminal on the Link. This will help minimize switching noise.
- Also use a single 47-μF capacitor to reduce dc ripple.

The VCCP power terminals provide a voltage clamping rail for 5-V tolerant inputs. The VCCP voltage is determine by the PCI bus voltage. Figure 5 illustrates the voltage clamping rail.

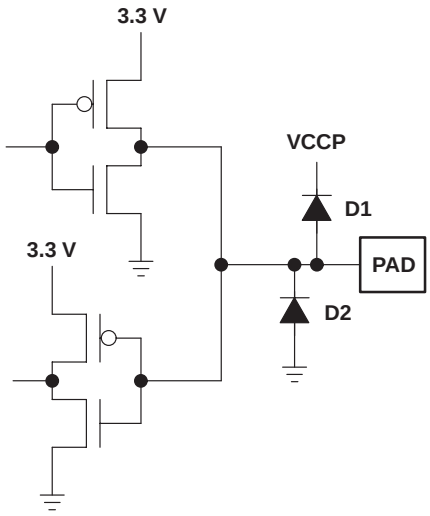


Figure 5. Clamping Voltage Diagram

If the design uses a 5-V supply, the VCCP terminals should be tied to the 5-V supply. Otherwise, VCCP should be connected to the 3.3-V.

The $\overline{\text{ISOLATED}}$ terminal is used to the enable bus holders for isolated designs. However, for most designs this is not required.

- To disable the bus-holders connect the $\overline{\text{ISOLATED}}$ terminal to 3.3 V through a 4.7-kΩ pullup resistor.
- To enable the bus-holders connect the $\overline{\text{ISOLATED}}$ terminal to GND through a 220-Ω pulldown resistor.

The $\overline{\text{CARDBUS}}$/CYCLEOUT terminal is sampled when $\overline{\text{G\_RST}}$ is asserted, and it selects between the PCI and CardBus buffers. After reset, this terminal may also function as CYCLEOUT which provides an 8-kHz cycle timer synchronization signal.

- To use the PCI bus buffers this terminal should be left unconnected, and an internal pullup resistor will enable the PCI buffers.
- To enable the CardBus buffers this terminal should be pulled down with a 220-Ω resistor. It is important that a weak pulldown resistor be used if the design is going to use the CYCLEOUT feature.

The CYCLEIN terminal can be used to receive an optional external 8-kHz clock used as a cycle timer, which provides synchronization with other system devices. If not implemented, a 4.7-kΩ pullup resistor should be used to tie this terminal to 3.3 V.

The TSB12LV23's $\overline{\text{G\_RST}}$ terminal allows for retaining context from a D3 to D0 transition when the PCI interface may transition from B3 to B0 and issue a PCI reset. The TSB12LV23 resets are illustrated in Figure 6.

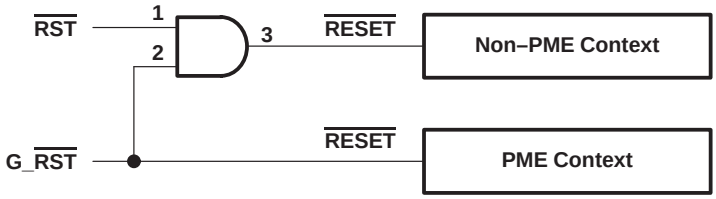
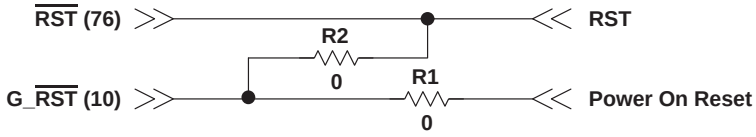


Figure 6. TSB12LV23 Reset Block Diagram

If the design supports D3_Wake, then the $\overline{\text{G\_RST}}$ terminal provides the hardware reset at power on, while the $\overline{\text{RST}}$ terminal should be connected to the PCI Bus $\overline{\text{RST}}$, which will provides resets that retain the PME context.

For designs that will not support D3_Wake, the $\overline{\text{RST}}$ terminal can either be pulled up to 3.3 V through a 4.7-kΩ resistor or tied together with the $\overline{\text{G\_RST}}$ terminal. An example implementation is shown in Figure 7.



NOTE: For normal operation populate R2 and do not populate R1
For Mobile or D3_Wake operation populate R1 and do not populate R2

Figure 7. Reset Schematic

The $\overline{\text{CLKRUN}}$ terminal is used to turn the clock on and off. This is useful in mobile design where conserving power is important. When implementing $\overline{\text{CLKRUN}}$, this terminal is connected to external circuitry that provides a common $\overline{\text{CLKRUN}}$ control signal. If the clock is never turned off, then this terminal should be left unconnected and an internal pulldown resistor will keep the clock active.

The GPIO2 and GPIO3 are general-purpose I/O terminals that should each be pulled down to GND through a 220-Ω resistors.

For more information on the TSB12LV23, consult the TI data manual, *TSB12LV23 (OHCI-LYNX) IEEE 1394-1995 Link-Layer Controller* (literature number SLLS328).

5 The Link Layer - Serial EEPROM

The Serial EEPROM provides a convenient mechanism to load system-specific data and is detected at reset via SDA and SCL terminals.

The following are the types of data stored in the EEPROM:

- PCI: Max latency, min grant, subsystem VID, subsystem ID, Link enhancements, miscellaneous control, and CIS offset
- OHCI: GUID, HCControl.programPhyEnable

The serial EEPROM is required for adapter cards, but it is optional for implementations where the BIOS is used to load GUID and other system-specific registers.

SDA and SCL should each be pulled up to EEPROM V_{CC} through 2.7-kΩ resistors, and then connected to the EPROM's SDA and SCL terminals respectively (as is illustrated in Figure 8). If no serial EEPROM is used, then both the SDA and SCL terminals should be connected to ground through 220-Ω pulldown resistors.

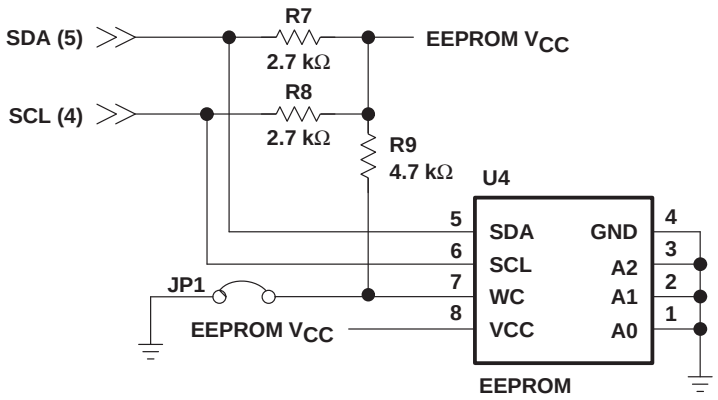


Figure 8. Serial EEPROM

If the EEPROM has a write enable terminal, it should be connected to EEPROM V_{CC} with a pullup resistor. In addition, a jumper to GND should be connected in series the pullup, as illustrated in Figure 8. This will allow the EEPROM to be write-enabled and write-disabled.

5.1 Isolation Considerations

5.1.1 Isolation vs Nonisolation

- Isolation provides protection against data corruption and/or physical harm that can be caused by ground potential differences between nodes.
- Typical PC usage models do not require isolation (i.e., all connected devices share a common green-wire ground).

NOTE: LAN type environments may be a special case

5.1.2 Isolated Designs that Require Special Consideration

- PHY/Link signal isolation
- Phy/Link ground return
- Isolated power supply

5.1.3 Special Considerations for Bus Holder Isolation

Phy/Link interface signals must be ac coupled.

- Single 0.001-μF (non-polarized) decoupled capacitor per signal
  SCLK, LREQ, CTL0, CTL1, D0 – D7
  LPS and LINKON require additional considerations

A current path must be provided between the PHY ground and the Link ground to ensure signal integrity.

5.1.4 Standard TSB12LV23 Considerations

- $\overline{\text{ISOLATED}}$ terminal must be pulled down to enable the bus holders
- VCCP clamp should be tied to 5 V only if a PCI-Bus voltage is 5 V. Otherwise, VCCP should be tied to 3.3 V.
- The serial EEPROM is required for adapter cards.

5.1.5 Power Requirements

- Alternate power providers
  - Requires isolated load output from the power supply – Alternate dc-to-dc converter, but expensive for power densities required
  - Single diode isolation of power source – Standard power provider or alternate power provider with launch voltage > 20 V requires per power diode isolation.
  - Per port current limit (1.5 A) required.
- PHY decoupling capacitor considerations apply.

5.1.6 Implementing Galvanic Isolation

For detailed information on galvanic isolation, refer to the *Galvanic Isolation Applications Note* (literature number: SLLA011).

5.2 Design Check List

5.2.1 Standard Requirements

- Required pullup and pulldown resistors
- Decoupling capacitors
- Clamping voltage VCCP
- $\overline{\text{ISOLATED}}$ terminal must be pulled up to disable the bus holders

5.2.2 Design Specific Requirements

- Drop-in replacement for the TSB12LV22
  - $\overline{\text{RST}}$ should either be pulled up or tied directly to $\overline{\text{G\_RST}}$ terminal ($\overline{\text{RST}}$ was $\overline{\text{TEST\_EN}}$ on the TSB12LV22).
  - $\overline{\text{CARDBUS}}$/CYCLEOUT is pulled up
  - $\overline{\text{CLKRUN}}$ unconnected
  - Serial EEPROM has been reprogrammed or programmed with the GlobalByte swap bit 0 at offset 13h has been cleared (set = 0)
- Adapter card design
  - Serial EEPROM required
  - 3.3-V supply for Link Core
  - $\overline{\text{CLKRUN}}$ unconnected
  - $\overline{\text{RST}}$ should either be pulled up or tied directly to $\overline{\text{G\_RST}}$ terminal ($\overline{\text{RST}}$ was $\overline{\text{TEST\_EN}}$ on the TSB12LV22).
- Mobile or Wake D3_cold Design
  - 3.3-V EEPROM if required
  - VCCP = 3.3 V
  - $\overline{\text{G\_RST}}$ and $\overline{\text{RST}}$ are configured for D3_cold
  - $\overline{\text{CLKRUN}}$ has optional 0-Ω resistor or has been connected to external $\overline{\text{CLKRUN}}$ circuitry
- Isolated Design

  In addition to one of the previous selections, this design will also be isolated.
  - $\overline{\text{ISOLATED}}$ terminal must be pulled down to enable the bus holders
  - Single 0.001-μF (non-polarized) decoupled capacitor per signal
    SCLK, LREQ, CTL0, CTL1, D0 – D7
    LPS and LINKON require additional considerations
  - PHY/Link signal isolation
  - Phy/Link ground return
  - Isolated power supply

Appendix A PCI Bus Requirements

A.1 PCI Bus Requirements

The following paragraph summarizes paragraph 4.3.3 of the PCI Local Bus Specification Revision 2.1 and is provided for reference only. Please refer to the PCI Local Bus Specification for a full discussion on pull-up resistors required for PCI local bus implementations.

All PCI control signals require pullup resistors on the motherboard to guarantee that they are at a stable state when no agent is actively driving the signal. Pullups should be implemented on the motherboard only. Expansion boards or add-in cards should not provide pullup resistors for the PCI control signals. The following PCI signals require pullup resistors:

- $\overline{\text{FRAME}}$
- $\overline{\text{TRDY}}$
- $\overline{\text{IRDY}}$
- $\overline{\text{DEVSEL}}$
- $\overline{\text{STOP}}$
- $\overline{\text{SERR}}$
- $\overline{\text{PERR}}$
- $\overline{\text{LOCK}}$
- $\overline{\text{INTA}}$
- $\overline{\text{INTB}}$
- $\overline{\text{INTC}}$
- $\overline{\text{INTD}}$
- $\overline{\text{REQ64}}$ (when used)
- $\overline{\text{ACK64}}$ (when used)

Pullups are not required on point-to-point or shared 32-bit signals, as bus parking guarantees their stability. If the 64-bit data path expansion signals, AD(63:32), C/BE(7:4)#, and PAR64, are connected they must be pulled-up as well. Table xxx lists the 32-bit PCI signals implemented on the TSB12LV23 that require pullup resistors on the system board.

Minimum and maximum values for required PCI pullup resistors can be calculated using the following formulas:

$$R_{min} = \frac{V_{CC(min)} - V_{ol}}{I_{ol} + (16 \times I_{il})}$$

Where 16 = maximum number of loads

$$R_{min} = \frac{V_{CC(min)} - V_{ol}}{num\_loads \times I_{il}}$$

Where:

V_X = 2.7V for 5-V signaling
V_X = 0.7 V_{CC} for 3.3-V signaling

Minimum and typical values for both 5-V and 3.3-V signaling environments are shown in the following table.

Table A–1. Minimum and Typical PCI Pull-Up Resistor Values

SIGNALING RAIL	R_{min}	R_{typ}	R_{max}
5 V	963 Ω	2.7 kΩ ± 10%	Dependent on number of loads (see formula)
3.3 V	2.42 kΩ	8.2 kΩ ± 10%	Dependent on number of loads (see formula)

Table A–2. 32-Bit PCI Signal System Board Pull-Up Requirements

PCI SIGNAL	PULL-UP VOLTAGE
$\overline{\text{FRAME}}$	V_{CCP}
$\overline{\text{TRDY}}$	V_{CCP}
$\overline{\text{IRDY}}$	V_{CCP}
$\overline{\text{DEVSEL}}$	V_{CCP}
$\overline{\text{STOP}}$	V_{CCP}
$\overline{\text{SERR}}$	V_{CCP}
$\overline{\text{PERR}}$	V_{CCP}
$\overline{\text{INTA}}$	V_{CCP}

A.2 Bypass Capacitors

Standard design rules for the supply bypass should be followed. Low inductance ceramic chip capacitors are best for bypass capacitors. A value of 0.1 µF is recommended for each of the power supply pins: V_{CC}, V_{CCS}, V_{CCP}.

Appendix B Serial EEPROM

B.1 GPIO Interface

The general-purpose input/output (GPIO) interface consists of two GPIO ports. GPIO2 and GPIO3 power up as general-purpose inputs and are programmable via the GPIO control register. B–1 shows the schematic for GPIO2 and GPIO3 implementation.

GPIO0 and GPIO1 are not implemented in the TSB12LV23. The terminals for these legacy GPIOs from the TSB12LV23 have been dedicated to BMC/LINKON and LPS, respectively.

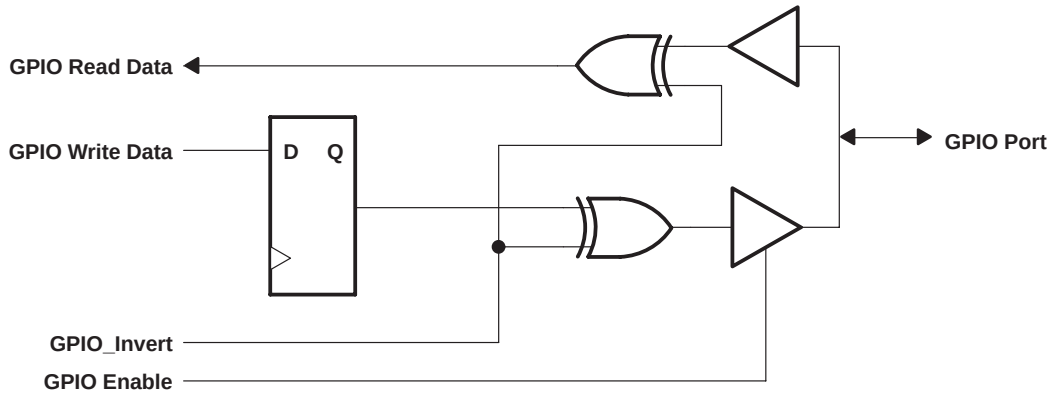


Figure B–1. GPIO2 and GPIO3

B.2 Serial Bus Interface

The TSB12LV23 provides a serial bus interface to initialize the 1394 global unique ID register and a few PCI configuration registers through a serial EEPROM. The TSB12LV23 communicates with the serial EEPROM via the 2-wire serial interface.

After power-up the serial interface initializes the locations listed in Table B–1. While the TSB12LV23 is accessing the serial ROM, all incoming PCI slave accesses are terminated with retry status. Table B–2 shows the serial ROM memory map required for initializing the TSB12LV23 registers.

Table B–1. Registers and Bits Loadable through Serial EEPROM

OFFSET	REGISTER	BITS LOADED FROM EEPROM
OHCI register (24h)	1394 GlobalUniqueIDHi	31–0
OHCI register(28h)	1394 GlobalUniqueIDLo	31–0
OHCI register (50h)	Host control register	23
PCI register (2Ch)	PCI subsystem ID	15–0
PCI register (2Dh)	PCI vendor ID	15–0
PCI register (3Eh)	PCI maximum latency, PCI minimum grant	15–0
PCI register (F4h)	Link enhancements control register	13, 12, 9, 8, 7, 2, 1
PCI register (F0h)	PCI miscellaneous register	15, 13, 10, 5–0
PCI register (40h)	PCI OHCI register	0

Table B–2. Serial EEPROM Map

BYTE ADDRESS	BYTE DESCRIPTION							
00	PCI maximum latency (0h)				PCI_minimum grant (0h)			
01	PCI vendor ID							
02	PCI vendor ID (msbyte)							
03	PCI subsystem ID (lsbyte)							
04	PCI subsystem ID							
05	[7] Link_enhancement-Control.enab_unfair	[6] HCControl. ProgramPhy Enable	[5] RSVD	[4] RSVD	[3] RSVD	[2] Link_enhancement-Control.enab_ insert_idle	[1] Link_enhancement-Control.enab_accel	[0] RSVD
06	Mini ROM address							
07	1394 GlobalUniqueIDHi (lsbyte 0)							
08	1394 GlobalUniqueIDHi (byte 1)							
09	1394 GlobalUniqueIDHi (byte 2)							
0A	1394 GlobalUniqueIDHi (msbyte 3)							
0B	1394 GlobalUniqueIDLo (lsbyte 0)							
0C	1394 GlobalUniqueIDLo (byte 1)							
0D	1394 GlobalUniqueIDLo (byte 2)							
0E	1394 GlobalUniqueIDLo (msbyte 3)							
0F	Checksum							
10	[15] RSVD	[14] RSVD	[13–12] AT threshold		[11] RSVD	[10] RSVD	[9] Enable audio timestamp	[8] Enable DV CIP timestamp
11	[7] RSVD	[6] RSVD	[5] RSVD	[4] Disable Target Abort	[3] GP2IIC	[2] Disable SCLK gate	[1] Disable PCI gate	[0] Keep PCI
12	[15] PME D3 Cold	[14] RSVD	[13] PME Support D2	[12] RSVD	[11] RSVD	[10] D2 support	[9] RSVD	[8] RSVD
13	[7] RSVD	[6] RSVD	[5] RSVD	[4] RSVD	[3] RSVD	[2] RSVD	[1] RSVD	[0] Global swap
14	CIS offset address							
15–1E	RSVD							
1F	RSVD							

Appendix C Terminal Descriptions and Functions

C.1 Terminal Assignments

This section provides the terminal assignments for the TSB12LV23.

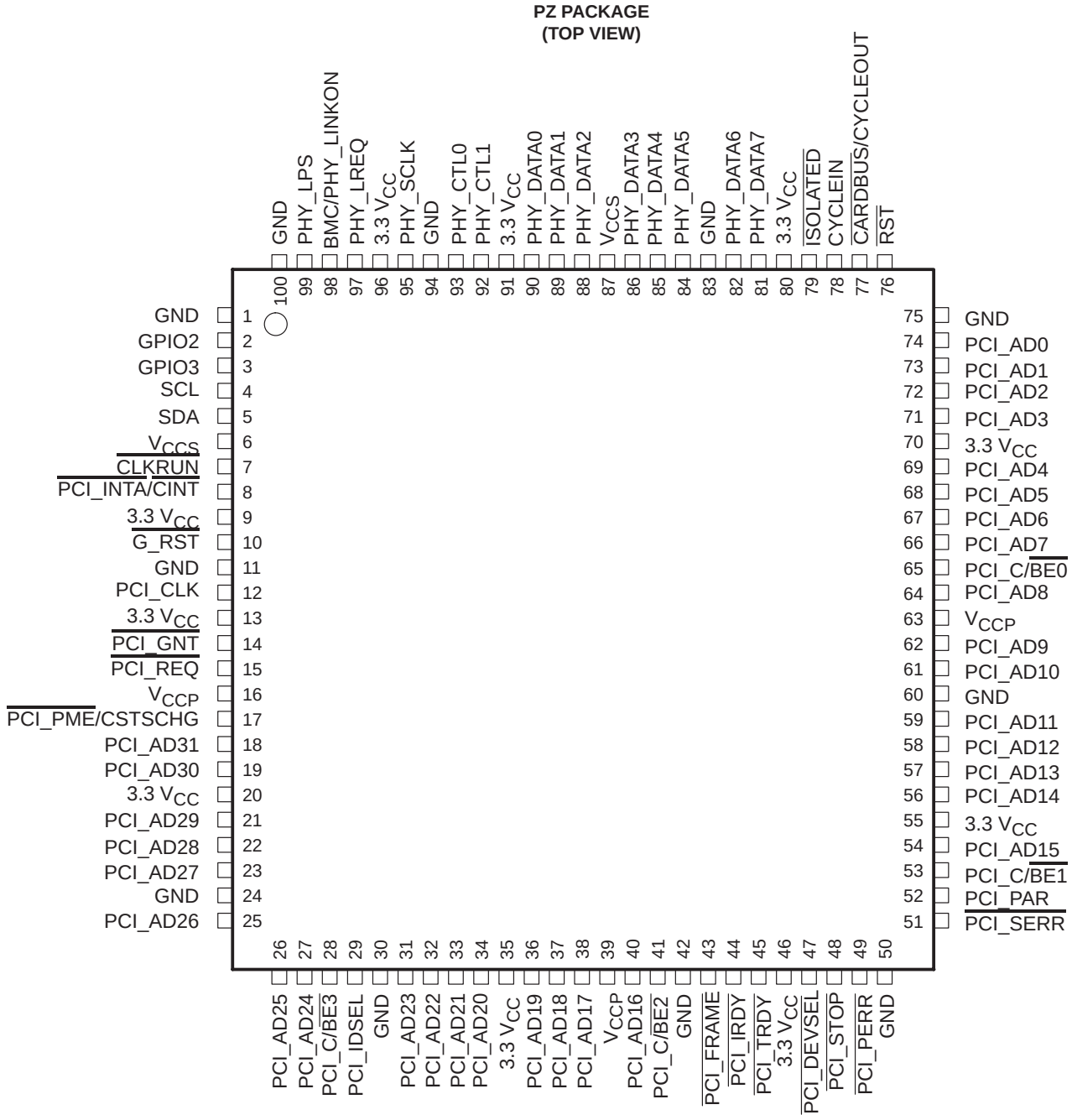


Figure C–1. Terminal Assignments

Table C–1. Signals Sorted by Pin Number

NO.	TERMINAL NAME	NO.	TERMINAL NAME	NO.	TERMINAL NAME	NO.	TERMINAL NAME
1	GND	26	PCI_AD25	51	$\overline{\text{PCI\_SERR}}$	76	$\overline{\text{RST}}$
2	GPIO2	27	PCI_AD24	52	PCI_PAR	77	$\overline{\text{CARDBUS}}$/CYCLEOUT
3	GPIO3	28	PCI_C/$\overline{\text{BE3}}$	53	PCI_C/$\overline{\text{BE1}}$	78	CYCLEIN
4	SCL	29	PCI_IDSEL	54	PCI_AD15	79	$\overline{\text{ISOLATED}}$
5	SDA	30	GND	55	3.3 V_{CC}	80	3.3 V_{CC}
6	V_{CCP}	31	PCI_AD23	56	PCI_AD14	81	PHY_DATA7
7	$\overline{\text{CLKRUN}}$	32	PCI_AD22	57	PCI_AD13	82	PHY_DATA6
8	$\overline{\text{PCI\_INTA}}$/$\overline{\text{CINT}}$	33	PCI_AD21	58	PCI_AD12	83	GND
9	3.3 V_{CC}	34	PCI_AD20	59	PCI_AD11	84	PHY_DATA5
10	$\overline{\text{G\_RST}}$	35	3.3 V_{CC}	60	GND	85	PHY_DATA4
11	GND	36	PCI_AD19	61	PCI_AD10	86	PHY_DATA3
12	PCI_CLK	37	PCI_AD18	62	PCI_AD9	87	V_{CCP}
13	3.3 V_{CC}	38	PCI_AD17	63	V_{CCP}	88	PHY_DATA2
14	$\overline{\text{PCI\_GNT}}$	39	V_{CCP}	64	PCI_AD8	89	PHY_DATA1
15	$\overline{\text{PCI\_REQ}}$	40	PCI_AD16	65	PCI_C/$\overline{\text{BE0}}$	90	PHY_DATA0
16	V_{CCP}	41	PCI_C/$\overline{\text{BE2}}$	66	PCI_AD7	91	3.3 V_{CC}
17	$\overline{\text{PCI\_PME}}$/CSTSCHG	42	GND	67	PCI_AD6	92	PHY_CTL1
18	PCI_AD31	43	$\overline{\text{PCI\_FRAME}}$	68	PCI_AD5	93	PHY_CTL0
19	PCI_AD30	44	$\overline{\text{PCI\_IRDY}}$	69	PCI_AD4	94	GND
20	3.3 V_{CC}	45	$\overline{\text{PCI\_TRDY}}$	70	3.3 V_{CC}	95	PHY_SCLK
21	PCI_AD29	46	3.3 V_{CC}	71	PCI_AD3	96	3.3 V_{CC}
22	PCI_AD28	47	$\overline{\text{PCI\_DEVSEL}}$	72	PCI_AD2	97	PHY_LREQ
23	PCI_AD27	48	$\overline{\text{PCI\_STOP}}$	73	PCI_AD1	98	PHY_LINKON
24	GND	49	$\overline{\text{PCI\_PERR}}$	74	PCI_AD0	99	PHY_LPS
25	PCI_AD26	50	GND	75	GND	100	GND

C.2 Terminal Functions

The terminals are grouped in tables by functionality, such as PCI system function, power supply function, etc. The terminal numbers are also listed for convenient reference.

Table C–2. Power Supply

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
GND	1, 11, 24, 30, 42, 50, 60, 75, 83, 94, 100	I	Device ground terminals
3.3 V_{CC}	9, 13, 20, 35, 46, 55, 70, 80, 91, 96	I	3.3-V power supply terminals
V_{CCP}	6, 16, 39, 63, 87	I	PCI signaling clamp voltage power input. PCI signals are clamped per the *PCI Local Bus Specification.*

Table C–3. PCI System

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
PCI_CLK	12	I	PCI bus clock. Provides timing for all transactions on the PCI bus. All PCI signals are sampled at rising edge of PCLK.
$\overline{\text{G\_RST}}$	10	I	Global power reset. This reset brings all of the TSB12LV23 to its default state, including those registers not reset by $\overline{\text{RST}}$. When asserted, the device is completely nonfunctional.
$\overline{\text{PCI\_INTA}}$/$\overline{\text{CINT}}$	8	O	Interrupt signal. This output indicates interrupts from the TSB12LV23 to the host. This terminal signals an interrupt based upon the $\overline{\text{CARDBUS}}$ input terminal.
$\overline{\text{RST}}$	76	I	PCI or CardBus reset. When this bus reset is asserted, the TSB12LV23 places all output buffers in a high impedance state and resets all internal registers except device power management context- and vendor-specific bits initialized by host power on software. When asserted, the device is completely nonfunctional.

Table C–4. PCI Address and Data

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
PCI_AD31	18	I/O	PCI address/data bus. These signals make up the multiplexed PCI address and data bus on the PCI interface during the address phase of a PCI cycle, AD31–AD0 contain a 32-bit address or other destination information. During the data phase, AD31–AD0 contain data.
PCI_AD30	19		
PCI_AD29	21		
PCI_AD28	22		
PCI_AD27	23		
PCI_AD26	25		
PCI_AD25	26		
PCI_AD24	27		
PCI_AD23	31		
PCI_AD22	32		
PCI_AD21	33		
PCI_AD20	34		
PCI_AD19	36		
PCI_AD18	37		
PCI_AD17	38		
PCI_AD16	40		
PCI_AD15	54		
PCI_AD14	56		
PCI_AD13	57		
PCI_AD12	58		
PCI_AD11	59		
PCI_AD10	61		
PCI_AD9	62		
PCI_AD8	64		
PCI_AD7	66		
PCI_AD6	67		
PCI_AD5	68		
PCI_AD4	69		
PCI_AD3	71		
PCI_AD2	72		
PCI_AD	73		
PCI_AD0	74		
PCI_C/$\overline{\text{BE0}}$	65	I/O	PCI bus commands and byte enables. The command and byte enable signals are multiplexed on the same PCI terminals. During the address phase of a bus cycle C/$\overline{\text{BE3}}$–C/$\overline{\text{BE0}}$ defines the bus command. During the data phase, this 4-bit bus is used as byte enables.
PCI_C/$\overline{\text{BE1}}$	53		
PCI_C/$\overline{\text{BE2}}$	41		
PCI_C/$\overline{\text{BE3}}$	28		
PCI_PAR	52	I/O	PCI parity. In all PCI bus read and write cycles, the TSB12LV23 calculates even parity across the AD and C/$\overline{\text{BE}}$ buses. As an initiator during PCI cycles, the TSB12LV23 outputs this parity indicator with a one PCLK delay. As a target during PCI cycles, the calculated parity is compared to the initiator's parity indicator; a miscompare can result in a parity error assertion ($\overline{\text{PERR}}$).

Table C–5. PCI Interface Control

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
PCI_DEVSEL	47	I/O	PCI device select. The TSB12LV23 asserts this signal to claim a PCI cycle as the target device. As a PCI initiator, the TSB12LV23 monitors this signal until a target responds. If no target responds before time-out occurs, then the TSB12LV23 terminates the cycle with an initiator abort.
PCI_FRAME	43	I/O	PCI cycle frame. This signal is driven by the initiator of a PCI bus cycle. FRAME is asserted to indicate that a bus transaction is beginning, and data transfers continue until while this signal is asserted. When FRAME is deasserted, the PCI bus transaction is in the final data phase.
PCI_GNT	14	I	PCI bus grant. This signal is driven by the PCI bus arbiter to grant the TSB12LV23 access to the PCI bus after the current data transaction has completed. This signal may or may not follow a PCI bus request depending upon the PCI bus parking algorithm.
PCI_IDSEL	29	I	Initialization device select. IDSEL selects the TSB12LV23 during configuration space accesses. IDSEL can be connected to 1 of the upper 24 PCI address lines on the PCI bus.
PCI_IRDY	44	I/O	PCI initiator ready. IRDY indicates the PCI bus initiator's ability to complete the current data phase of the transaction. A data phase is completed upon a rising edge of PCLK where both IRDY and TRDY are asserted; until which wait states are inserted.
PCI_STOP	48	I/O	PCI cycle stop signal. This signal is driven by a PCI target to request the initiator to stop the current PCI bus transaction. This signal is used for target disconnects, and is commonly asserted by target devices which do not support burst data transfers.
CLKRUN	7	I/O	Clock run. This terminal provides clock control through the CLKRUN protocol. An internal pulldown resistor is implemented on this terminal for TSB12LV22 drop-in compatibility.
PCI_PERR	49	I/O	PCI parity error indicator. This signal is driven by a PCI device to indicate that calculated parity does not match PAR when enabled through the command register.
PCI_PME/ CSTSCHG	17	O	PME or card status change. This terminal indicates wake events to the host. When in a CardBus configuration, per the CARDBUS sample, the CSTSCHG output is an active high.
PCI_REQ	15	O	PCI bus request. Asserted by the TSB12LV23 to request access to the bus as an initiator. The host arbiter asserts the GNT signal when the TSB12LV23 has been granted access to the bus.
PCI_SERR	51	O	PCI system error. Output pulsed from the TSB12LV23 when enabled indicating an address parity error has occurred. The TSB12LV23 needs not be the target of the PCI cycle to assert this signal.
PCI_TRDY	45	I/O	PCI target ready. TRDY indicates the PCI bus target's ability to complete the current data phase of the transaction. A data phase is completed upon a rising edge of PCLK where both IRDY and TRDY are asserted; until which wait states are inserted.

Table C–6. IEEE1394 PHY/Link

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
PHY_CTL1 PHY_CTL0	92 93	I/O	Phy-link interface control. These bidirectional signals control passage of information between the two devices. The TSB12LV23 can only drive these terminals after the PHY has granted permission following a link request (LREQ).
PHY_DATA7 PHY_DATA6 PHY_DATA5 PHY_DATA4 PHY_DATA3 PHY_DATA2 PHY_DATA1 PHY_DATA0	81 82 84 85 86 88 89 90	I/O	Phy-link interface data. These bidirectional signals pass data between the TSB12LV23 and the PHY device. These terminals are driven by the TSB12LV23 on transmissions and are driven by the PHY on reception. Only DATA1–DATA0 are valid for 100-Mbit speeds, DATA3–DATA0 are valid for 200-Mbit speeds, and DATA7–DATA0 are valid for 400-Mbit speeds.
PHY_SCLK	95	I	System clock. This input from the PHY provides a 49.152 MHz clock signal for data synchronization.
PHY_LREQ	97	O	Link request. This signal is driven by the TSB12LV23 to initiate a request for the PHY to perform some service.
PHY_LINKON	98	I/O	LinkOn wake indication. Used and defined by 1394A and 3.3-V signaling is required.
PHY_LPS	99	I/O	Link power status. Used and defined by 1394A and 3.3-V signaling is required.

Table C–7. Miscellaneous

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
SDA	5	I/O	Serial data. The TSB12LV23 determines whether a two-wire serial ROM, or no serial ROM is implemented at reset. If a two-wire serial ROM is detected, then this terminal provides the SDA serial data signaling. If no EEPROM is implemented, this terminal should be pulled down. Otherwise, it pullup is required.
SCL	4	I/O	Serial clock. The TSB12LV23 determines whether a two-wire, or no serial ROM is implemented at reset. If a two-wire serial ROM is implemented, then this terminal provides the SCL serial clock signaling. If implemented, this terminal should be pulled high with a resistor.
$\overline{\text{ISOLATED}}$	79	I	Phy-link isolation barrier mode. This terminal should be asserted when the PHY device is electrically isolated from the TSB12LV23. This input controls bus-hold I/Os. If bus holder isolation is not implemented, this terminal should be pulled high with a resistor.
CYCLEIN	78	I/O	The CYCLEIN terminal can provide an optional external 8 kHz clock set up as a cycle timer that can be used for synchronization with other system devices. This terminal should be pulled high with a resistor.
$\overline{\text{CARDBUS}}$/ CYCLEOUT	77	I/O	This terminal is sampled when $\overline{\text{G\_RST}}$ is asserted, and it selects between PCI buffers and CardBus buffers. After reset, this terminal may also function as CYCLEOUT which provides an 8 kHz cycle timer synchronization signal. For normal operation, this terminal should be left unconnected and an internal pullup will enable the PCI buffers.
GPIO3	3	I/O	General-purpose I/O [3]. This terminal requires a pull-down or pull-up resistor.
GPIO2	2	I/O	General-purpose I/O [2]. This terminal requires a pull-down or pull-up resistor.

Appendix D Definitions Used with the Application Examples

D.1 I/O Electrical Characteristics

Figure D–1 shows a 3-state bidirectional buffer for reference. Note that the PCI interface signals meet the AC requirements of the PCI release 2.1 specification.

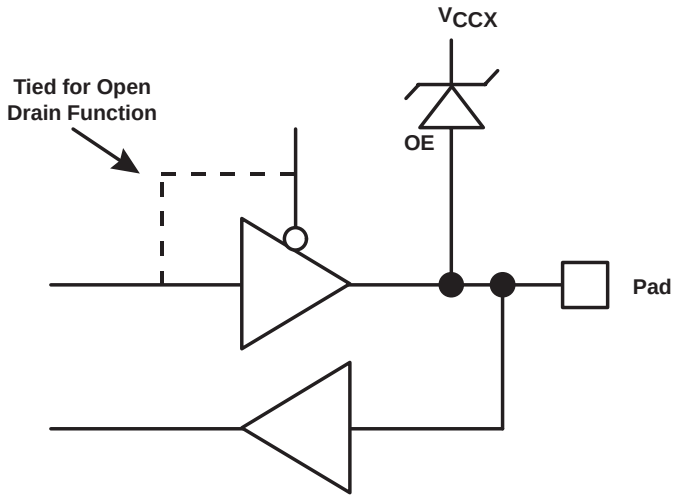


Figure D–1. 3-State Bidirectional Buffer