Am8048/8035

Single Chip 8-Bit Microcomputers

DISTINCTIVE CHARACTERISTICS

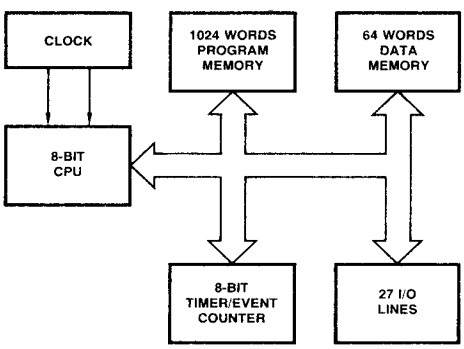
- 8-bit CPU, ROM, RAM, I/O in single package
- Single +5V supply
- All instructions 1 or 2 cycles
- Over 90 instructions: 70% single byte
- 1K x 8 ROM
- 64 x 8 RAM
- 27 I/O lines
- Interval timer/event counter
- Easily expandable memory and I/O
- Single level interrupt
- 100% reliability assurance testing to MIL-STD-883

GENERAL DESCRIPTION

The Am8048 contains a 1k x 8 program memory, a 64 x 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on board oscillator and clock circuits. For systems that require extra capability, the Am8048 can be expanded using standard memories and Am9080A peripherals. The Am8035 is the equivalent of an Am8048 without program memory.

The microprocessor is designed to be an efficient controller. The Am8048 has extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single byte instructions and no instructions over two bytes in length.

BLOCK DIAGRAM



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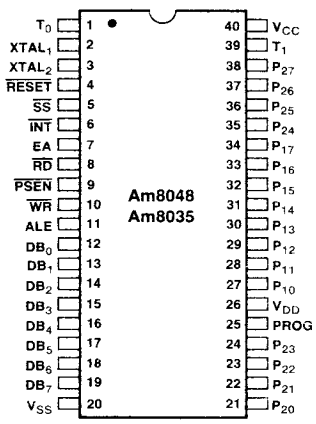
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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ORDERING INFORMATION

Package Type	Ambient Temperature Specification	Order Numbers	
Hermetic DIP*	0°C ≤ T_A ≤ +70°C	AM8048DC AM8048CC	AM8035DC AM8035CC
Molded DIP		AM8048PC	AM8035PC

*Hermetic = Ceramic = DC = CC = D-40-1.

MAXIMUM RATINGS (Above which useful life may be impaired)

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	0°C to +70°C
Voltage on Any Pin with Respect to Ground	−0.5V to +7.0V
Power Dissipation	1.5W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

DC AND OPERATING CHARACTERISTICS

T_A = 0 to 70°C, V_{CC} = V_{DD} = +5.0V ±10% (Note 1), V_{SS} = 0V

Parameters	Description	Test Conditions	Limits Min	Typ	Max	Units
V_{IL}	Input Low Voltage (All Except $\overline{RESET}$, X1, X2)		−.5		.8	Volts
V_{IL1}	Input Low Voltage ($\overline{RESET}$, X1, X2)		−.5		.6	Volts
V_{IH}	Input High Voltage (All Except XTAL1, XTAL2, $\overline{RESET}$)		2.0		V_{CC}	Volts
V_{IH1}	Input High Voltage (X1, X2, $\overline{RESET}$)		3.8		V_{CC}	Volts
V_{OL}	Output Low Voltage (BUS)	V_{OL} = 2.0mA			.45	Volts
V_{OL1}	Output Low Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	I_{OL} = 1.8mA			.45	Volts
V_{OL2}	Output Low Voltage (PROG)	I_{OL} = 1.0mA			.45	Volts
V_{OL3}	Output Low Voltage (All Other Outputs)	I_{OL} = 1.6mA			.45	Volts
V_{OH}	Output High Voltage (BUS)	I_{OH} = −400μA	2.4			Volts
V_{OH1}	Output High Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	I_{OH} = −100μA	2.4			Volts
V_{OH2}	Output High Voltage (All Other Outputs)	I_{OH} = −40μA	2.4			Volts
I_{LI}	Input Leakage Current (T1, $\overline{INT}$)	$V_{SS} \leq V_{IN} \leq V_{CC}$			±10	μA
I_{LI1}	Input Leakage Current (P10-P17, P20-P27, EA, $\overline{SS}$)	V_{SS} + .45 ≤ $V_{IN} \leq V_{CC}$			−500	μA
I_{LO}	Output Leakage Current (BUS, TO) (High Impedance State)	V_{SS} + .45 ≤ $V_{IN} \leq V_{CC}$			±10	μA
I_{DD}	V_{DD} Supply Current			5	15	mA
I_{DD} + I_{CC}	Total Supply Current			60	135	mA

INPUT AND OUTPUT WAVEFORMS FOR AC TESTS

AC CHARACTERISTICS

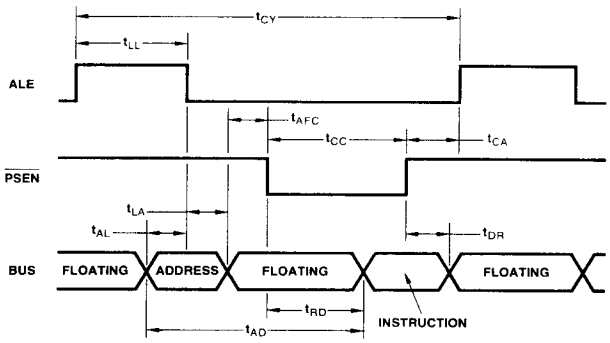
T_A = 0 to 70°C, V_{CC} = V_{DD} = +5.0V ±10% (Note 1), V_{SS} = 0V

Parameters	Description	Test Conditions (Note 2)	Am8048 Am8035 Min	Max	Units
t_{LL}	ALE Pulse Width		400		ns
t_{AL}	Address Set-up to ALE		120		ns
t_{LA}	Address Hold from ALE		80		ns
t_{CC}	Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)		700		ns
t_{DW}	Data Set-up Before $\overline{WR}$		500		ns
t_{WD}	Data Hold After $\overline{WR}$	C_L = 20pF	120		ns
t_{CY}	Cycle Time	6MHz XTAL (3.6MHz XTAL for -8)	2.5	15.0	μs
t_{DR}	Data Hold		0	200	ns
t_{RD}	PSEN, RD to Data In			500	ns
t_{AW}	Address Set-up to $\overline{WR}$		230		ns
t_{AD}	Address Set-up to Data In			950	ns
t_{AFC}	Address Float to $\overline{RD}$, $\overline{PSEN}$		0		ns
t_{CA}	Control Pulse to ALE		10		ns

Notes: 1. V_{CC} and V_{DD} for Am8035-8 are ±5%.
2. Control Outputs: C_L = 80pF.
Bus Outputs: C_L = 150pF, t_{CY} = 2.5μs.

WAVEFORMS

INSTRUCTION FETCH FROM EXTERNAL PROGRAM MEMORY



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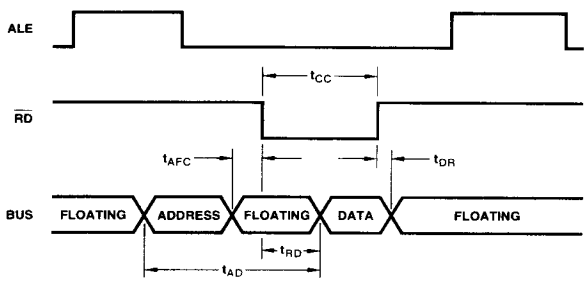
READ FROM EXTERNAL DATA MEMORY



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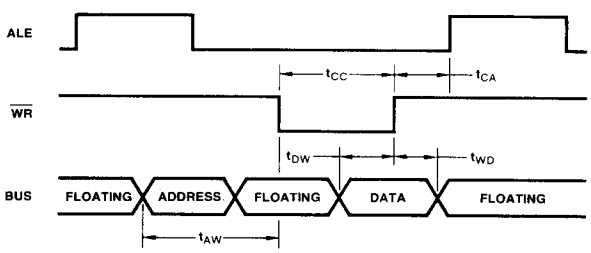
WRITE TO EXTERNAL DATA MEMORY



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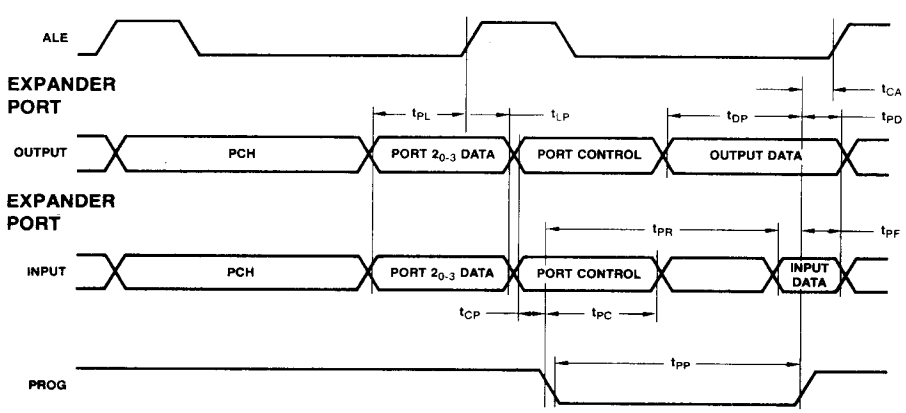
PORT 2 TIMING



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AC CHARACTERISTICS (Port 2 Timing)

T_A = 0 to 70°C, V_{CC} = 5V ±10% (Note 1), V_{SS} = 0V

Parameters	Description	Test Conditions	Am8048 Am8035 Min.	Max.	Units
t_{CP}	Port Control Set-up before Falling Edge of PROG		110		ns
t_{PC}	Port Control Hold after Falling Edge of PROG		100		ns
t_{PR}	PROG to Time P2 Input Must be Valid			810	ns
t_{DP}	Output Data Set-up Time		250		ns
t_{PD}	Output Data Hold Time		65		ns
t_{PF}	Input Data Hold Time		0	150	ns
t_{PP}	PROG Pulse Width		1200		ns
t_{PL}	Port 2 I/O Data Set-up		350		ns
t_{LP}	Port 2 I/O Data Hold		150		ns

PIN DESCRIPTION

V_{SS}

Circuit GND potential.

V_{DD}

Power supply; +5V during operation. Low power standby pin for Am8048 ROM.

V_{CC}

Main power supply; +5V.

PROG

Output strobe for Am8243 I/O expander.

P_{10}-P_{17} Port 1

8-bit quasi-bidirectional port.

P_{20}-P_{27} Port 2

8-bit quasi-bidirectional port.

P_{20}-P_{23} contain the four high order program counter bits during an exteral program memory fetch and serve as a 4-bit I/O expander bus for Am8243.

D_0-D_7 BUS

True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched.

Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of PSEN. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$ and $\overline{WR}$.

T_0

Input pin testable using the conditional transfer instructions JT_0 and JNT_0. T_0 can be designated as a clock output using ENT0 CLK instruction. T_0 is also used during programming.

T_1

Input pin testable using the JT_1, and JNT_1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.

$\overline{INT}$

Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction (Active low).

$\overline{RD}$

Output strobe activated during a BUS read. Can be used to enable data onto the BUS from an external device.

Used as a Read Strobe to External Data Memory (Active low).

$\overline{RESET}$

Input which is used to initialize the processor. Also used during power down (Active low).

$\overline{WR}$

Output strobe during a BUS write (Active low) (Non-TTL V_{IH}).

Used as write strobe to External Data Memory.

ALE

Address Latch Enable. This signal occurs once during each cycle and is useful as a clock output.

The negative edge of ALE strobes address into external data and program memory.

$\overline{PSEN}$

Program Store Enable. This output occurs only during a fetch to external program memory (Active low).

$\overline{SS}$

Single step input can be used in conjunction with ALE to "single step" the processor through each instruction (Active low).

EA

External Access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification (Active high).

$XTAL_1$

One side of crystal input for internal oscillator. Also input for external source (Not TTL compatible).

$XTAL_2$

Other side of crystal input.