PCA9620

60 x 8 LCD high-drive segment driver for automotive and industrial

Rev. 3 — 3 July 2013 Product data sheet

1. General description

The PCA9620 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD)[1] with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to eight backplanes, 60 segments, and up to 480 elements. The PCA9620 is compatible with most microprocessors or microcontrollers and communicates via a two-line bidirectional I^2C-bus. Communication overheads are minimized using a display RAM with auto-incremented addressing and display memory switching. The PCA9620 features an internal charge pump with internal capacitors for on-chip generation of the LCD driving voltages

2. Features and benefits

- AEC Q100 grade 2 compliant for automotive applications
- Low power consumption
- Extended operating temperature range from −40 °C to +105 °C
- 60 segments and 8 backplanes allowing to drive:
  - up to 60 7-segment alphanumeric characters
  - up to 30 14-segment alphanumeric characters
  - any graphics of up to 480 elements
- 480-bit RAM for display data storage
- Selectable backplane drive configuration: static, 2, 4, 6, or 8 backplane multiplexing
- Programmable internal charge pump for on-chip LCD voltage generation up to $3 \times V_{DD2}$
- 400 kHz I^2C-bus interface
- Selectable linear temperature compensation of V_{LCD}
- Selectable display bias configuration
- Wide range for digital and analog power supply: from 2.5 V to 5.5 V
- Wide LCD supply range: from 2.5 V for low threshold LCDs and up to 9.0 V for high threshold (automobile) twisted nematic LCDs
- Display memory bank switching in static, duplex, and quadruplex drive modes
- Programmable frame frequency in steps of 10 Hz in the range of 60 Hz to 300 Hz; factory calibrated with a tolerance of ±15 % covering the whole temperature and voltage range
- Selectable inversion scheme for LCD driving waveforms: frame or line inversion
- Integrated temperature sensor with temperature readout
- On chip calibration of internal oscillator frequency and V_{LCD}

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 20 on page 73.

3. Applications

- Automotive
  - Instrument cluster
  - Car radio
  - Climate control units
- Industrial
  - Machine control systems
  - Measuring equipment
- Signage
  - Information boards
  - Panels

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCA9620H	LQFP80	plastic low profile quad flat package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1
PCA9620U	bare die	80 bonding pads	PCA9620U

4.1 Ordering options

Table 2. Ordering options

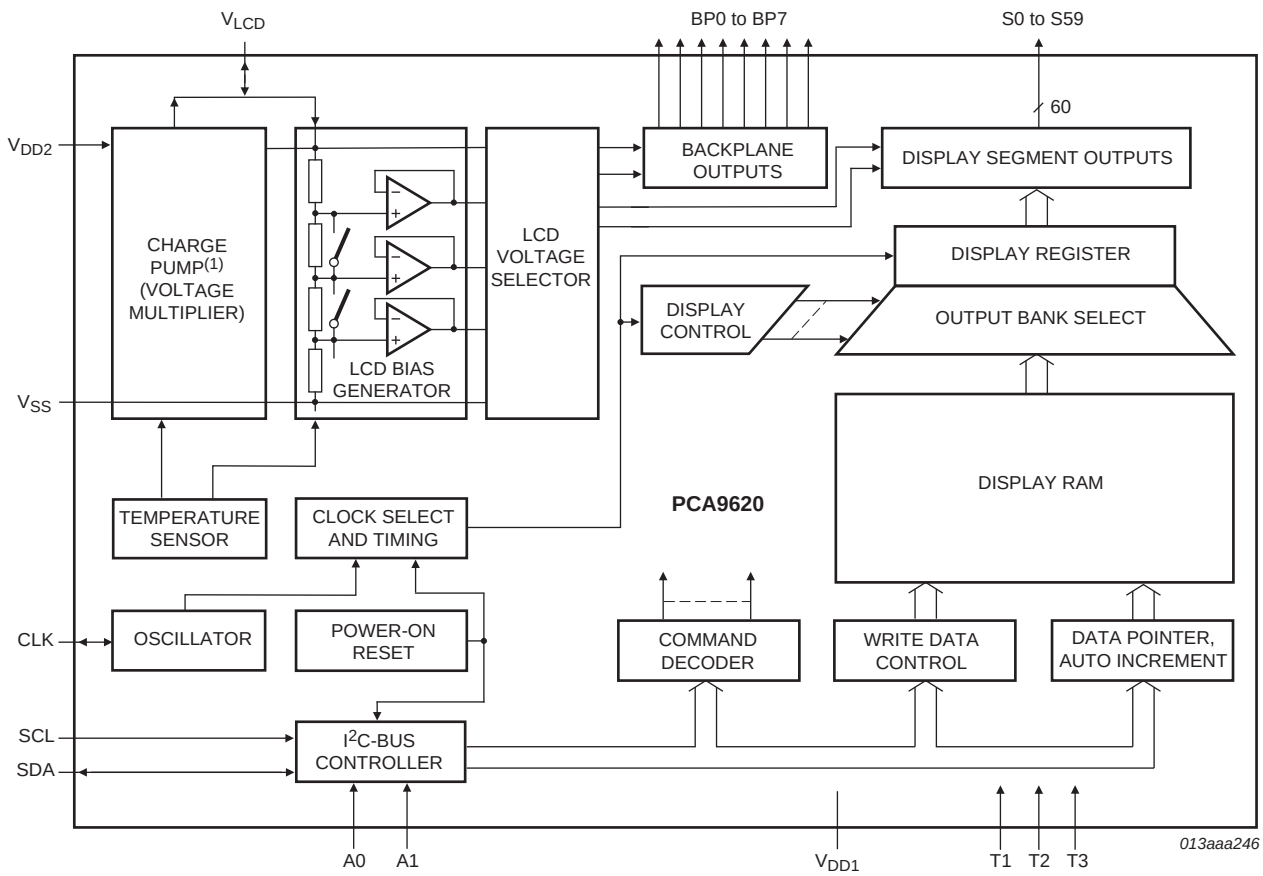
Product type number	Sales item (12NC)	Orderable part number	IC revision	Delivery form
PCA9620H/Q900/1	935291899518	PCA9620H/Q900/1,51	1	tape and reel, 13 inch, dry pack
PCA9620U/5GA/Q1	935295801015	PCA9620U/5GA/Q1,01	1	wafer, unsawn

5. Marking

Table 3. Marking codes

Type number	Marking code
PCA9620H	PCA9620H/Q900
PCA9620U	PC9620-1

6. Block diagram

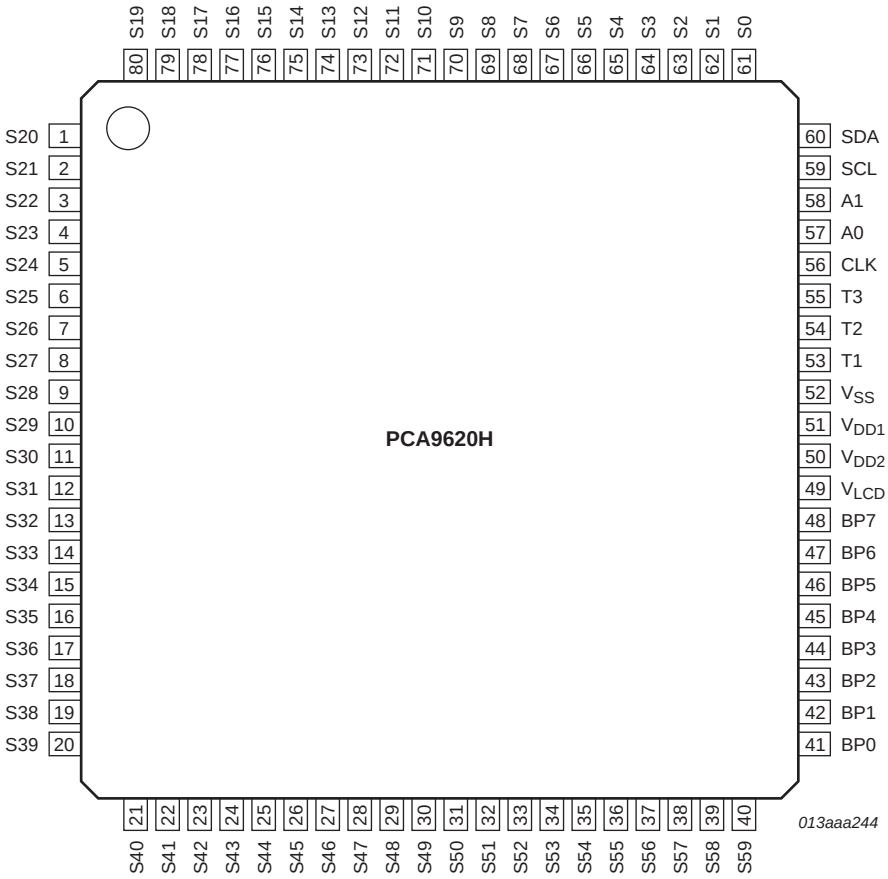


(1) The charge pump can generate a maximum output voltage of $3 \times V_{DD2}$.

Fig 1. Block diagram of PCA9620

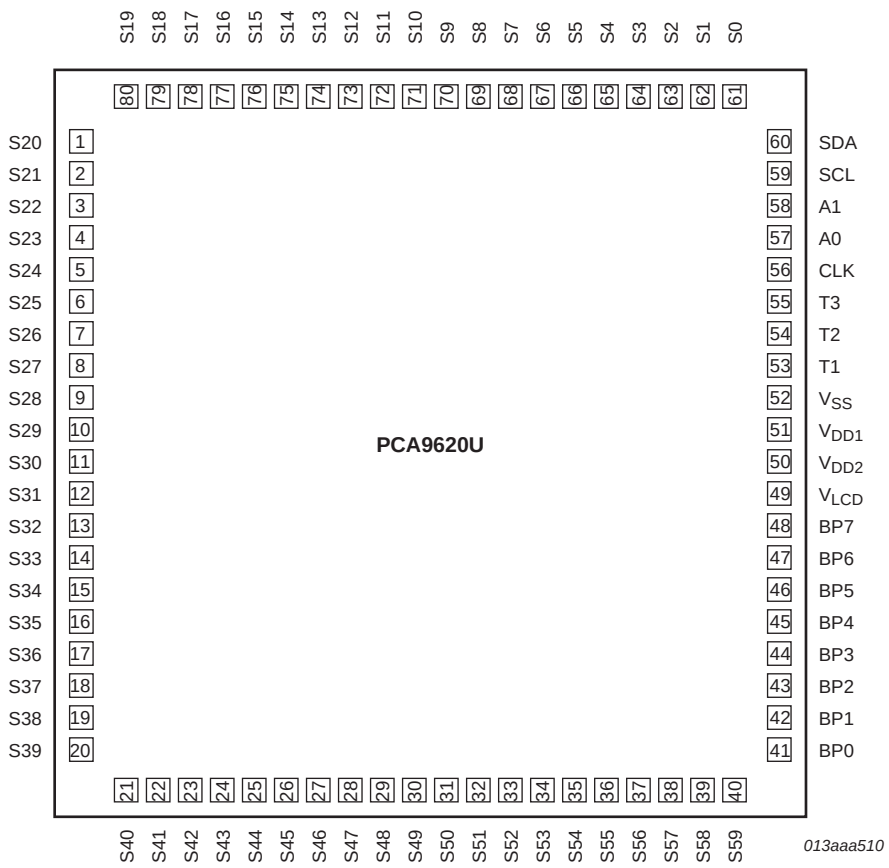
7. Pinning information

7.1 Pinning



Top view. For mechanical details, see Figure 58 on page 63.

Fig 2. Pin configuration for LQFP80 (PCA9620H)



Viewed from active side. For mechanical details, see Figure 59 on page 64.

Fig 3. Pin configuration for PCA9620U (bare die)

7.2 Pin description

Table 4. Pin description

Symbol	Pin	Type	Description
S0 to S59	61 to 80 and 1 to 40	output	LCD segment
BP0 to BP7	41 to 48	output	LCD backplane
V_{LCD}	49	supply/output[1]	LCD supply voltage
V_{DD2}	50	supply	supply voltage 2 (charge pump)
V_{DD1}	51	supply	supply voltage 1 (analog and digital)
V_{SS}	52	supply	ground supply voltage
T1 to T3	53 to 55	input	test pins; must be tied to V_{SS} in applications
CLK	56	input/output	internal oscillator output, external oscillator input
A0, A1	57, 58	input	I^2C-bus slave address selection bit
SCL	59	input	I^2C-bus serial clock
SDA	60	input/output	I^2C-bus serial data

[1] When the internal V_{LCD} generation is used, this pin drives the V_{LCD} voltage. In this case pin V_{LCD} is an output. When the external supply is requested, then pin V_{LCD} is an input and V_{LCD} can be supplied to it. In this case, the internal charge pump must be disabled (see Table 9 on page 9).

8. Functional description

The PCA9620 is a versatile peripheral device designed to interface any microprocessor or microcontroller to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to 480 elements.

8.1 Commands of PCA9620

The PCA9620 is controlled by 22 commands, which are defined in Table 5. Any other combinations of operation code bits that are not mentioned in this document may lead to undesired operation modes of PCA9620.

Table 5. Commands of PCA9620

Command name	Bits								Reference
	7	6	5	4	3	2	1	0	
initialize	0	0	1	1	1	0	1	0	Section 8.1.1
OTP-refresh	1	1	0	1	0	0	0	0	Section 8.1.2
oscillator-ctrl	1	1	0	0	1	1	COE	OSC	Section 8.1.3
charge-pump-ctrl	1	1	0	0	0	0	CPE	CPC	Section 8.1.4
temp-msr-ctrl	1	1	0	0	1	0	TCE	TME	Section 8.1.5
temp-comp-SLA	0	0	0	1	1	SLA[2:0]			Table 30
temp-comp-SLB	0	0	1	0	0	SLB[2:0]			
temp-comp-SLC	0	0	1	0	1	SLC[2:0]			
temp-comp-SLD	0	0	1	1	0	SLD[2:0]			
set-VPR-MSB	0	1	0	0	VPR[7:4]				Section 8.1.6
set-VPR-LSB	0	1	0	1	VPR[3:0]				
display-enable	0	0	1	1	1	0	0	E	Section 8.1.7
set-MUX-mode	0	0	0	0	0	M[2:0]			Section 8.1.8
set-bias-mode	1	1	0	0	0	1	B[1:0]		Section 8.1.9
load-data-pointer	1	0	P[5:0]						Section 8.1.10
frame-frequency	0	1	1	F[4:0]					Section 8.1.11
input-bank-select	0	0	0	0	1	IB[2:0]			Section 8.1.12.1
output-bank-select	0	0	0	1	0	OB[2:0]			
write-RAM-data	B[7:0]								Section 8.1.13
temp-read	TD[7:0]								Section 8.1.14, Section 8.4.7
invmode_CPF_ctrl	1	1	0	1	0	1	LF	CPF	Section 8.1.15
temp-filter	1	1	0	1	0	0	1	TFE	Section 8.1.16

8.1.1 Command: initialize

This command generates a chip-wide reset which resets all command values to their default values (see Table 26 on page 17). It must be sent to the PCA9620 after power-on. After this command is sent, it is possible to send additional commands without the need to re-initialize the interface. Reset takes 100 ns to complete.

For further information, see Section 8.3 on page 16.

Table 6. Initialize - initialize command bit description

Bit	Symbol	Value	Description
7 to 0	-	00111010	fixed value

8.1.2 Command: OTP-refresh

In order to achieve the specified accuracy of V_{LCD}, the frame frequency, and the temperature measurement, each IC is calibrated during production and testing of the device. This calibration is performed on EPROM cells called One Time Programmable (OTP) cells. These cells are read by the device at power-on, after a reset, and every time when the initialize command or the OTP-refresh command is sent. This command will take approximately 10 ms to finish.

Table 7. OTP-refresh - OTP-refresh command bit description

Bit	Symbol	Value	Description
7 to 0	-	11010000	fixed value

8.1.3 Command: oscillator-ctrl

The oscillator-ctrl command switches between internal and external oscillator and enables or disables pin CLK.

Table 8. Oscillator-ctrl - oscillator control command bit description

For further information, see Section 8.5 on page 40.

Bit	Symbol	Value	Description
7 to 2	-	110011	fixed value
1	COE		control pin CLK
		0[1]	clock signal not available on pin CLK; pin CLK is in 3-state and may be left floating
		1	clock signal available on pin CLK
0	OSC		oscillator source
		0[1]	internal oscillator running
		1	external oscillator used; pin CLK becomes an input

[1] Default value.

8.1.4 Command: charge-pump-ctrl

The charge-pump-ctrl command enables or disables the internal V_{LCD} generation and controls the charge pump voltage multiplier setting.

Table 9. Charge-pump-ctrl - charge pump control command bit description

Bit	Symbol	Value	Description
7 to 2	-	110000	fixed value
1	CPE		charge pump switch
		0[1]	charge pump disabled; no internal V_{LCD} generation; external supply of V_{LCD}
		1	charge pump enabled
0	CPC		charge pump voltage multiplier setting
		0[1]	$V_{LCD} = 2 \times V_{DD2}$
		1	$V_{LCD} = 3 \times V_{DD2}$

[1] Default value.

8.1.5 Command: temp-msr-ctrl

The temp-msr-ctrl command enables or disables the temperature measurement block and the temperature compensation of V_{LCD}.

Table 10. Temp-msr-ctrl - temperature measurement control command bit description
For further information, see Section 8.4.8 on page 38.

Bit	Symbol	Value	Description
7 to 2	-	110010	fixed value
1	TCE		temperature compensation switch
		0	no temperature compensation of V_{LCD} possible
		1[1]	temperature compensation of V_{LCD} possible
0	TME		temperature measurement switch
		0	temperature measurement disabled; no temperature readout possible
		1[1]	temperature measurement enabled; temperature readout possible

[1] Default value.

8.1.6 Command: set-VPR-MSB and set-VPR-LSB

With these two instructions, it is possible to set the target V_{LCD} voltage for the internal charge pump, see Section 8.4.3 on page 33.

Table 11. Set-VPR-MSB - set VPR MSB command bit description

Bit	Symbol	Value	Description
7 to 4	-	0100	fixed value
3 to 0	VPR[7:4]	0000[1] to 1111	the four most significant bits of VPR[7:0]

[1] Default value.

Table 12. Set-VPR-LSB - set VPR LSB command bit description

Bit	Symbol	Value	Description
7 to 4	-	0101	fixed value
3 to 0	VPR[3:0]	0000[1] to 1111	the four least significant bits of VPR[7:0]

[1] Default value.

8.1.7 Command: display-enable

Table 13. Display-enable - display enable command bit description

Bit	Symbol	Value	Description
7 to 1	-	0011100	fixed value
0	E	0[1]	display disabled; backplane and segment outputs are internally connected to V_{SS}
		1	display enabled

[1] Default value.

8.1.8 Command: set-MUX-mode

Table 14. Set-MUX-mode - set multiplex drive mode command bit description

Bit	Symbol	Value	Description
7 to 3	-	00000	fixed value
2 to 0	M[2:0]	000[1], 011, 110, 111	1:8 multiplex drive mode: 8 backplanes
		001	static drive mode: 1 backplane
		010	1:2 multiplex drive mode: 2 backplanes
		100	1:4 multiplex drive mode: 4 backplanes
		101	1:6 multiplex drive mode: 6 backplanes

[1] Default value.

8.1.9 Command: set-bias-mode

Table 15. Set-bias-mode - set bias mode command bit description

Bit	Symbol	Value	Description
7 to 2	-	110001	fixed value
1 to 0	B[1:0]	00[1], 01	$\frac{1}{4}$ bias
		11	$\frac{1}{3}$ bias
		10	$\frac{1}{2}$ bias

[1] Default value.

8.1.10 Command: load-data-pointer

The load-data-pointer command defines one of the 60 display RAM addresses where the following display data will be sent to. For further information, see Section 8.9.1 on page 43.

Table 16. Load-data-pointer - load data pointer command bit description

Bit	Symbol	Value	Description
7 to 6	-	10	fixed value
5 to 0	P[5:0]	000000 to 111111	6-bit binary value of 0 to 59

8.1.11 Command: frame-frequency

With the frame-frequency command, the frame frequency and the output clock frequency can be configured.

Table 17. Frame frequency - frame frequency and output clock frequency command bit description

Bit	Symbol	Value	Description
7 to 5	-	011	fixed value
4 to 0	F[4:0]	see Table 18	nominal frame frequency (Hz)

Table 18. Frame frequency values

F[4:0]	Nominal frame frequency, f_{fr} (Hz)[1]	Resultant oscillator frequency, f_{osc} (Hz)	Duty cycle (%)[2]
00000	60	2880	20 : 80
00001	70	3360	7 : 93
00010	80	3840	47 : 53
00011	91	4368	40 : 60
00100	100	4800	33 : 67
00101	109	5232	27 : 73
00110	120	5760	20 : 80
00111	129.7	6226	13 : 87
01000	141.2	6778	5 : 95
01001	150	7200	50 : 50
01010	160	7680	47 : 53
01011	171.4	8227	43 : 57
01100	177.8	8534	41 : 59
01101	192	9216	36 : 64
01110[3]	200	9600	33 : 67
01111	208.7	10018	30 : 70
10000	218.2	10474	27 : 73
10001	228.6	10973	23 : 77
10010	240	11520	20 : 80
10011	252.6	12125	16 : 84
10100, 10101	266.7	12802	10 : 90
10110, 10111	282.4	13555	5 : 95
11000 to 11111	300	14400	50 : 50

[1] Nominal frame frequency calculated for the default clock frequency of 9600 Hz.

[2] Duty cycle definition: % HIGH-level time : % LOW-level time.

[3] Default value.

8.1.12 Bank select commands

For multiplex drive modes 1:4, 1:2 and static drive mode, it is possible to write data to one area of the RAM while displaying from another. These areas are named as RAM banks. Input and output banks can be set independently from one another with the input-bank-select and the output-bank-select command. For further information, see Section 8.9.2 on page 48.

8.1.12.1 Command: input-bank-select

Table 19. Input-bank-select - input bank select command bit description[1]

Bit	Symbol	Value	Description		
7 to 3	-	00001	fixed value		
2 to 0	IB[2:0]		selects RAM bank to write to		
			static drive mode	**1:2 drive mode**	**1:4 drive mode**
		000[2]	bank 0: RAM-row 0	bank 0: RAM-rows 0 and 1	bank 0: RAM-rows 0, 1, 2, and 3
		001	bank 1: RAM-row 1		
		010	bank 2: RAM-row 2	bank 2: RAM-rows 2 and 3	
		011	bank 3: RAM-row 3		
		100	bank 4: RAM-row 4	bank 4: RAM-rows 4 and 5	bank 4: RAM-rows 4, 5, 6, and 7
		101	bank 5: RAM-row 5		
		110	bank 6: RAM-row 6	bank 6: RAM-rows 6 and 7	
		111	bank 7: RAM-row 7		

[1] Not applicable for multiplex drive mode 1:6 and 1:8.

[2] Default value.

8.1.12.2 Command: output-bank-select

Table 20. Output-bank-select - output bank select command bit description[1]

Bit	Symbol	Value	Description		
7 to 3	-	00010	fixed value		
2 to 0	OB[2:0]		selects RAM bank to read from to the LCD		
			static drive mode	**1:2 drive mode**	**1:4 drive mode**
		000[2]	bank 0: RAM-row 0	bank 0: RAM-rows 0 and 1	bank 0: RAM-rows 0, 1, 2, and 3
		001	bank 1: RAM-row 1		
		010	bank 2: RAM-row 2	bank 2: RAM-rows 2 and 3	
		011	bank 3: RAM-row 3		
		100	bank 4: RAM-row 4	bank 4: RAM-rows 4 and 5	bank 4: RAM-rows 4, 5, 6, and 7
		101	bank 5: RAM-row 5		
		110	bank 6: RAM-row 6	bank 6: RAM-rows 6 and 7	
		111	bank 7: RAM-row 7		

[1] Not applicable for multiplex drive mode 1:6 and 1:8.

[2] Default value.

8.1.13 Command: write-RAM-data

The write-RAM-data command writes data byte-wise to the RAM. After Power-On Reset (POR) the RAM content is random and should be brought to a defined status by clearing it (setting it logic 0).

Table 21. Write-RAM-data - write RAM data command bit description[1]

Bit	Symbol	Value	Description
7 to 0	B[7:0]	00000000 to 11111111	writing data byte-wise to RAM

[1] For this command bit RS of the control byte has to be set logic 1 (see Table 34 on page 54).

More information about the display RAM can be found in Section 8.9 on page 42.

8.1.14 Command: temp-read

The temp-read command allows reading out the temperature values measured by the internal temperature sensor.

Table 22. Temp-read - temperature readout command bit description[1]
For further information, see Table 10 on page 9 and Section 8.4.7 on page 37.

Bit	Symbol	Value	Description
7 to 0	TD[7:0]	00000000 to 11111111	readout representing the digital temperature

[1] For this command bit R/$\overline{W}$ of the I^2C-bus slave address byte has to be set logic 1 (see Table 33 on page 53).

8.1.15 Command: invmode_CPF_ctrl

The invmode_CPF_ctrl command allows changing the drive scheme inversion mode and the charge pump frequency.

The waveforms used to drive LCD displays inherently produce a DC voltage across the display cell. The PCA9620 compensates for the DC voltage by inverting the waveforms on alternate frames or alternate lines. The choice of compensation method is determined with the LF bit.

Table 23. Invmode_CPF_ctrl - inversion mode and charge pump frequency prescaler command bit description

Bit	Symbol	Value	Description
7 to 2	-	110101	fixed value
1	LF		set inversion mode
		0[1]	line inversion mode
		1	frame inversion mode
0	CPF		set charge pump oscillator frequency
		0[1]	$f_{osc(cp)}$ ~ 1 MHz
		1	$f_{osc(cp)}$ ~ 500 kHz

[1] Default value.

In frame inversion mode, the DC value is compensated across two frames and not within one frame. Changing the inversion mode to frame inversion reduces the power consumption, therefore it is useful when power consumption is a key point in the application.

Frame inversion may not be suitable for all applications. The RMS voltage across a segment is better defined, however since the switching frequency is reduced there is possibility for flicker to occur.

The waveforms of Figure 16 on page 25 to Figure 22 on page 31 are showing line inversion mode. Figure 23 on page 32 shows one example of frame inversion.

8.1.16 Command: temp-filter

Table 24. Temp-filter - digital temperature filter command bit description

Bit	Symbol	Value	Description
7 to 1	-	1101001	fixed value
0	TFE		digital temperature filter switch
		0[1]	digital temperature filter disabled; the unfiltered digital value of TD[7:0] is immediately available for the readout and V_{LCD} compensation, see Section 8.4.7 on page 37
		1	digital temperature filter enabled

[1] Default value.

8.2 Possible display configurations

The PCA9620 is a versatile peripheral device designed to interface between any microcontroller to a wide variety of LCD segment or dot matrix displays (see Figure 4). It can directly drive any static or multiplexed LCD containing up to eight backplanes and up to 60 segments.

The display configurations possible with the PCA9620 depend on the number of active backplane outputs required. A selection of possible display configurations is given in Table 25.

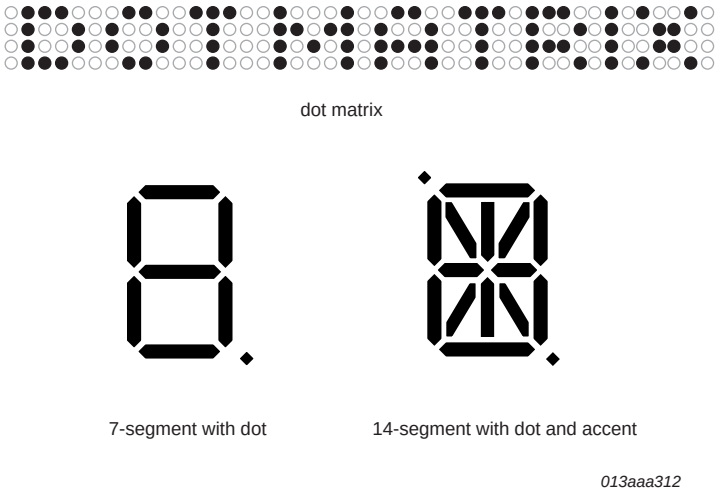
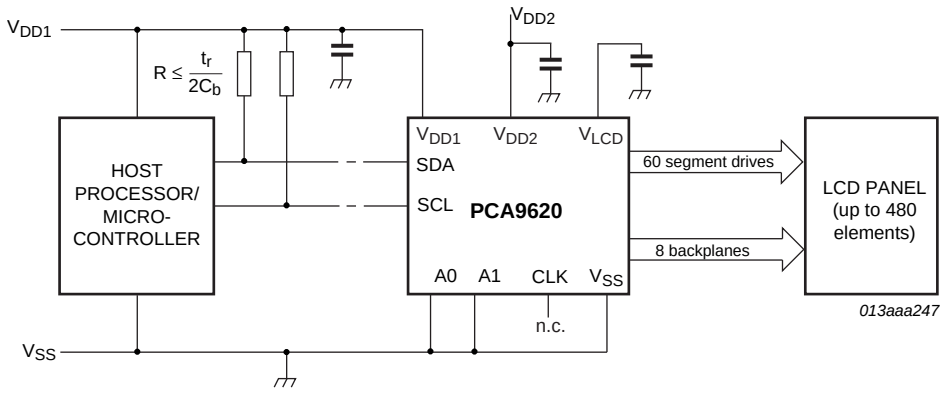


Fig 4. Example of displays suitable for PCA9620

Table 25. Selection of possible display configurations

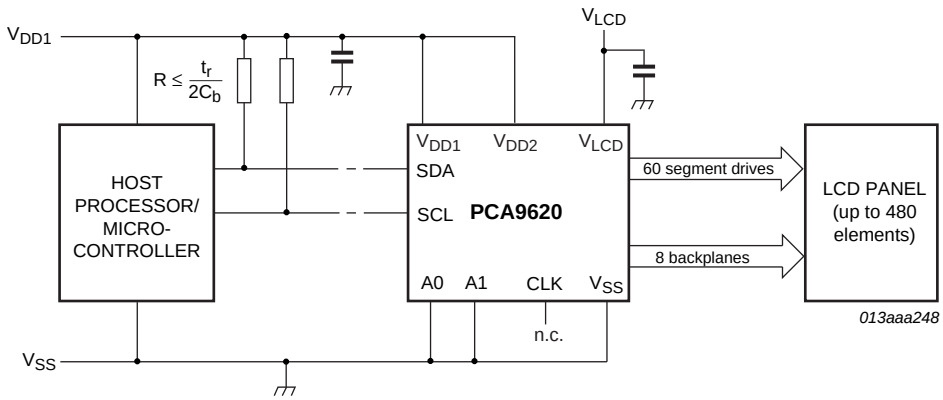
Number of Backplanes	Icons	Digits/Characters		Dot matrix/ Elements
		7-segment	14-segment	
8	480	60	30	480 dots (8 × 60)
6	320	45	22	360 dots (6 × 60)
4	240	30	15	240 dots (4 × 60)
2	120	15	7	120 dots (2 × 60)
1	60	7	3	60 dots (1 × 60)

All of the display configurations in Table 25 can be implemented in the typical systems shown in Figure 5 (internal V_{LCD}) and in Figure 6 (external V_{LCD}).



V_{DD1} from 2.5 V to 5.5 V and V_{DD2} from 2.5 V to 5.5 V.

Fig 5. Typical system configuration when using the internal V_{LCD} generation



V_{DD1} from 2.5 V to 5.5 V, V_{DD2} from 2.5 V to 5.5 V and V_{LCD} from 2.5 V to 9.0 V.

Fig 6. Typical system configuration when using an external V_{LCD}

The host microcontroller maintains the two line I²C-bus communication channel with the PCA9620. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are the power supplies (V_{DD1}, V_{DD2}, V_{SS}, V_{LCD}), the external capacitors, and the LCD panel selected for the application.

The minimum recommended values for external capacitors on V_{DD1}, V_{DD2}, and V_{LCD} are nominal 100 nF. When using bigger capacitors, especially on the V_{LCD}, the generated ripple will be consequently smaller. However it will take longer for the internal charge pump to reach the target V_{LCD} voltage first.

If V_{DD1} and V_{DD2} are connected externally, the capacitors on V_{DD1} and V_{DD2} can be replaced by a single capacitor with a minimum value of 200 nF.

Remark: In the case of insufficient decoupling, ripple of V_{DD1} and V_{DD2} will create additional V_{LCD} ripple. The ripple on V_{LCD} can be reduced by making the V_{SS} connection as low-ohmic as possible. Excessive ripple on V_{LCD} may cause flicker on the display.

8.3 Start-up and shut-down

8.3.1 Power-On Reset (POR)

At power-on, the PCA9620 resets to starting conditions as follows:

1. All backplane outputs are set to V_{SS}.
2. All segment outputs are set to V_{SS}.
3. Selected drive mode is: 1:8 with ¼ bias.
4. Input and output bank selectors are reset.
5. The I²C-bus interface is initialized.
6. The data pointer is cleared (set logic 0).
7. The Internal oscillator is running; no clock signal is available on pin CLK; pin CLK is in 3-state.
8. Temperature measurement is enabled.

9. Temperature filter is disabled.
10. The internal V_{LCD} voltage generation is disabled. The charge pump is switched off.
11. The V_{LCD} temperature compensation is enabled.
12. The display is disabled.

Remark: Do not transfer data on the I^2C-bus for at least 1 ms after a power-on to allow the reset action to complete.

The first command sent to the device after the power-on event must be the initialize command (see Section 8.1.1 on page 7).

After Power-On Reset (POR) and before enabling the display, the RAM content should be brought to a defined status

- by clearing it (setting it all logic 0) or
- by writing meaningful content (for example, a graphic)

otherwise unwanted display artifacts may appear on the display.

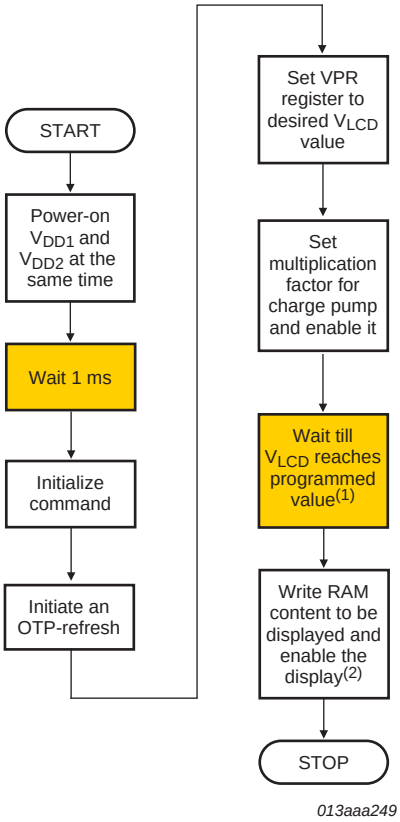
Table 26. Reset states

Bits labeled - are undefined at power-on.

Command name	Bits							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
initialize	0	0	1	1	1	0	1	0
OTP-refresh	1	1	0	1	0	0	0	0
oscillator-ctrl	1	1	0	0	1	1	0	0
charge-pump-ctrl	1	1	0	0	0	0	0	0
temp-msr-ctrl	1	1	0	0	1	0	1	1
temp-comp-SLA	0	0	0	1	1	0	0	0
temp-comp-SLB	0	0	1	0	0	0	0	0
temp-comp-SLC	0	0	1	0	1	0	0	0
temp-comp-SLD	0	0	1	1	0	0	0	0
set-VPR-MSB	0	1	0	0	0	0	0	0
set-VPR-LSB	0	1	0	1	0	0	0	0
display-enable	0	0	1	1	1	0	0	0
set-MUX-mode	0	0	0	0	0	0	0	0
set-bias-mode	1	1	0	0	0	1	0	0
load-data-pointer	1	0	0	0	0	0	0	0
frame-frequency	0	1	1	0	1	1	1	0
input-bank-select	0	0	0	0	1	0	0	0
output-bank-select	0	0	0	1	0	0	0	0
write-RAM-data	-	-	-	-	-	-	-	-
temp-read	0	1	0	0	0	0	0	0
invmode_CPF_ctrl	1	1	0	1	0	1	0	0
temp-filter	1	1	0	1	0	0	1	0

8.3.2 Recommended start-up sequences

This chapter describes how to proceed with the initialization of the chip in different application modes.



(1) This time depends on the external capacitor on pin V_{LCD}. For a capacitor of 100 nF a delay of 5 ms to 15 ms is expected.

When using the internal V_{LCD} generation, the display must not be enabled before the generation of V_{LCD} with the internal charge pump is completed. Otherwise unwanted display artifacts may appear on the display.

(2) RAM data may be written before or during the ramp-up of V_{LCD}.

Fig 7. Recommended start-up sequence when using the internal charge pump and the internal clock signal

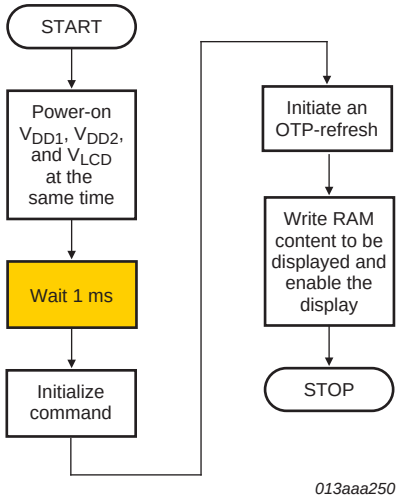
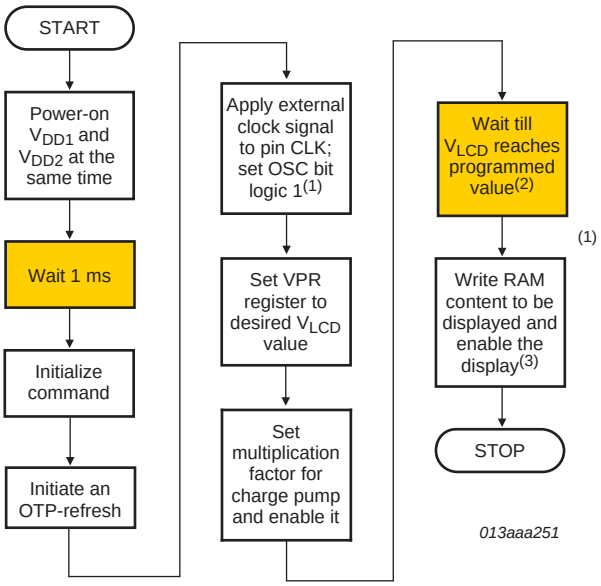


Fig 8. Recommended start-up sequence when using an external supplied V_{LCD} and the internal clock signal



(1) The external clock signal can be applied after the generation of the V_{LCD} voltage as well.

(2) This time depends on the external capacitor on pin V_{LCD}. For a capacitor of 100 nF a delay of 5 ms to 15 ms is expected.

(3) RAM data may be written before or during the ramp-up of V_{LCD}.

Fig 9. Recommended start-up sequence when using the internal charge pump and an external clock signal

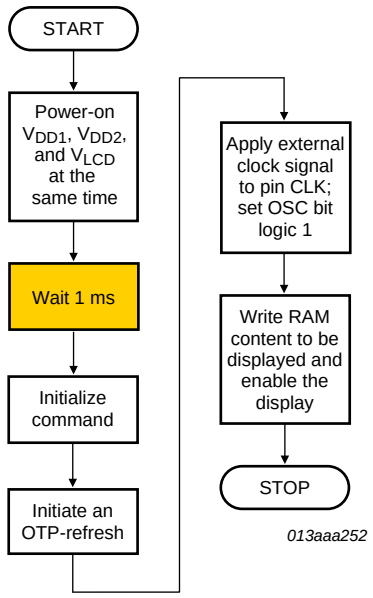


Fig 10. Recommended start-up sequence when using an external supplied V_{LCD} and an external clock signal

8.3.3 Recommended power-down sequences

With the following sequences, the PCA9620 can be set to a state of minimum power consumption, called power-down mode.

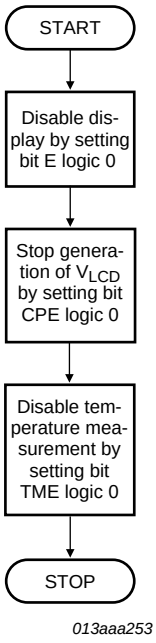


Fig 11. Recommended power-down sequence for minimum power-down current when using the internal charge pump and the internal clock signal

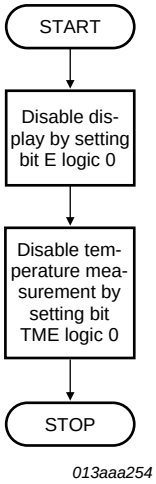


Fig 12. Recommended power-down sequence when using an external supplied V_{LCD} and the internal clock signal

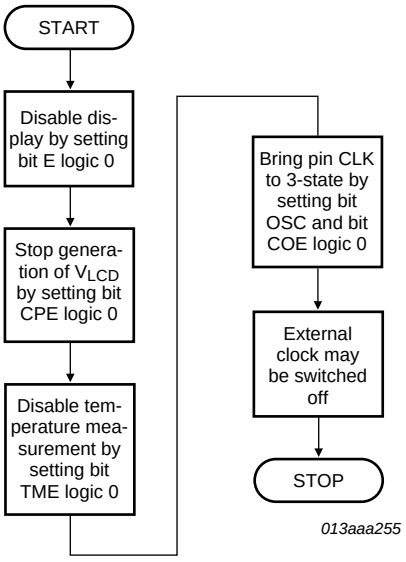


Fig 13. Recommended power-down sequence when using the internal charge pump and an external clock signal

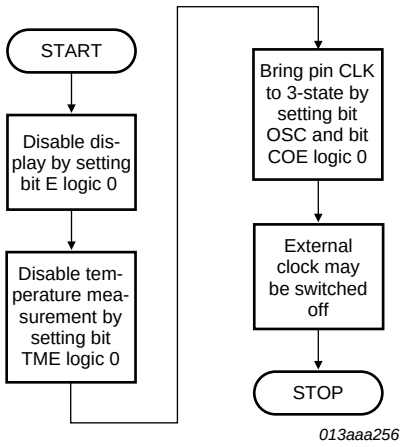


Fig 14. Recommended power-down sequence when using an external supplied V_{LCD} and an external clock signal

Remark: It is necessary to run the power-down sequence before removing the supplies. Depending on the application, care must be taken that no other signals are present at the chip input or output pins when removing the supplies (refer to Section 10 on page 55). Otherwise it may cause unwanted display artifacts. The PCA9620 will not be damaged by uncontrolled removal of supply voltages

Remark: Static voltages across the liquid crystal display can build up when the external LCD supply voltage (V_{LCD}) is on while the IC supply voltage (V_{DD1} or V_{DD2}) is off, or vice versa. It may cause unwanted display artifacts. To avoid such artifacts, external V_{LCD}, V_{DD1}, and V_{DD2} must be applied or removed together.

Remark: A clock signal must always be supplied to the device when the device is active; removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal. It is recommended to first disable the display and afterwards to remove the clock signal.

8.4 LCD voltage

8.4.1 LCD voltage selector

The LCD voltage selector co-ordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the set-bias-mode command (see Table 15 on page 10) and the set-MUX-mode command (see Table 14 on page 10).

Intermediate LCD biasing voltages are obtained from an internal voltage divider. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{LCD} and the resulting discrimination ratios (D), are given in Table 27.

Discrimination is a term which is defined as the ratio of the $V_{on(RMS)}$ and $V_{off(RMS)}$ across a segment. It can be thought of as a measurement of contrast.

Table 27. LCD drive modes: summary of characteristics

LCD drive mode	Number of:		LCD bias configuration	$\frac{V_{off(RMS)}}{V_{LCD}}$	$\frac{V_{on(RMS)}}{V_{LCD}}$	$D = \frac{V_{on(RMS)}}{V_{off(RMS)}}$ [1]	V_{LCD}[2]
	Backplanes	Levels					
static	1	2	static	0	1	∞	$V_{on(RMS)}$
1:2 multiplex	2	3	½	0.354	0.791	2.236	$2.828 \times V_{off(RMS)}$
1:2 multiplex	2	4	⅓	0.333	0.745	2.236	$3.0 \times V_{off(RMS)}$
1:2 multiplex[3]	2	5	¼	0.395	0.729	1.845	$2.529 \times V_{off(RMS)}$
1:4 multiplex[3]	4	3	½	0.433	0.661	1.527	$2.309 \times V_{off(RMS)}$
1:4 multiplex	4	4	⅓	0.333	0.577	1.732	$3.0 \times V_{off(RMS)}$
1:4 multiplex[3]	4	5	¼	0.331	0.545	1.646	$3.024 \times V_{off(RMS)}$
1:6 multiplex[3]	6	3	½	0.456	0.612	1.341	$2.191 \times V_{off(RMS)}$
1:6 multiplex	6	4	⅓	0.333	0.509	1.527	$3.0 \times V_{off(RMS)}$
1:6 multiplex	6	5	¼	0.306	0.467	1.527	$3.266 \times V_{off(RMS)}$
1:8 multiplex[3]	8	3	½	0.467	0.586	1.254	$2.138 \times V_{off(RMS)}$
1:8 multiplex[3]	8	4	⅓	0.333	0.471	1.414	$3.0 \times V_{off(RMS)}$
1:8 multiplex	8	5	¼	0.293	0.424	1.447	$3.411 \times V_{off(RMS)}$

[1] Determined from Equation 3.

[2] Determined from Equation 2.

[3] In these examples the discrimination factor and hence the contrast ratios are smaller. The advantage of these LCD drive modes is a power saving from a reduction of the LCD voltage V_{LCD}.

A practical value for V_{LCD} is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage ($V_{th(off)}$), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode a suitable choice is $V_{LCD} > 3V_{th(off)}$.

Bias is calculated by $\frac{1}{1+a}$, where the values for a are

a = 1 for ½ bias

a = 2 for ⅓ bias

a = 3 for ¼ bias

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with Equation 1:

$$V_{on(RMS)} = V_{LCD}\sqrt{\frac{a^2 + 2a + n}{n \times (1+a)^2}} \quad (1)$$

where V_{LCD} is the resultant voltage at the LCD segment and where the values for n are

n = 1 for static mode

n = 2 for 1:2 multiplex

n = 4 for 1:4 multiplex

n = 6 for 1:6 multiplex

n = 8 for 1:8 multiplex

The RMS off-state voltage ($V_{off(RMS)}$) for the LCD is calculated with Equation 2:

$$V_{off(RMS)} = V_{LCD}\sqrt{\frac{a^2 - 2a + n}{n \times (1 + a)^2}} \quad (2)$$

Discrimination is the ratio of $V_{on(RMS)}$ to $V_{off(RMS)}$ and is determined from Equation 3:

$$\frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{(a + 1)^2 + (n - 1)}{(a - 1)^2 + (n - 1)}} \quad (3)$$

It should be noted that V_{LCD} is sometimes referred as the LCD operating voltage.

8.4.1.1 Electro-optical performance

Suitable values for $V_{on(RMS)}$ and $V_{off(RMS)}$ are dependent on the LCD liquid used. The RMS voltage, at which a pixel will be switched on or off, determine the transmissibility of the pixel.

For any given liquid, there are two threshold values defined. One point is at 10 % relative transmission (at $V_{th(off)}$) and the other at 90 % relative transmission (at $V_{th(on)}$), see Figure 15. For a good contrast performance, the following rules should be followed:

$$V_{on(RMS)} \geq V_{th(on)} \quad (4)$$

$$V_{off(RMS)} \leq V_{th(off)} \quad (5)$$

$V_{on(RMS)}$ and $V_{off(RMS)}$ are properties of the display driver and are affected by the selection of a, n (see Equation 1 to Equation 3) and the V_{LCD} voltage.

$V_{th(off)}$ and $V_{th(on)}$ are properties of the LCD liquid and can be provided by the module manufacturer.

It is important to match the module properties to those of the driver in order to achieve optimum performance.

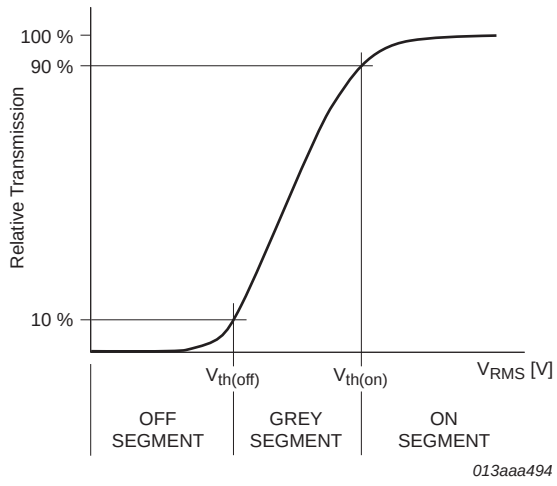
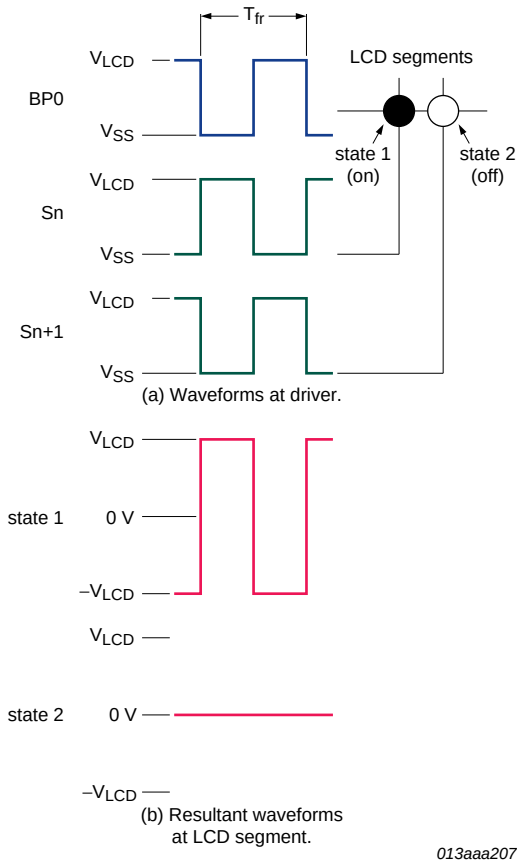


Fig 15. Electro-optical characteristic: relative transmission curve of the liquid

8.4.2 LCD drive mode waveforms

8.4.2.1 Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

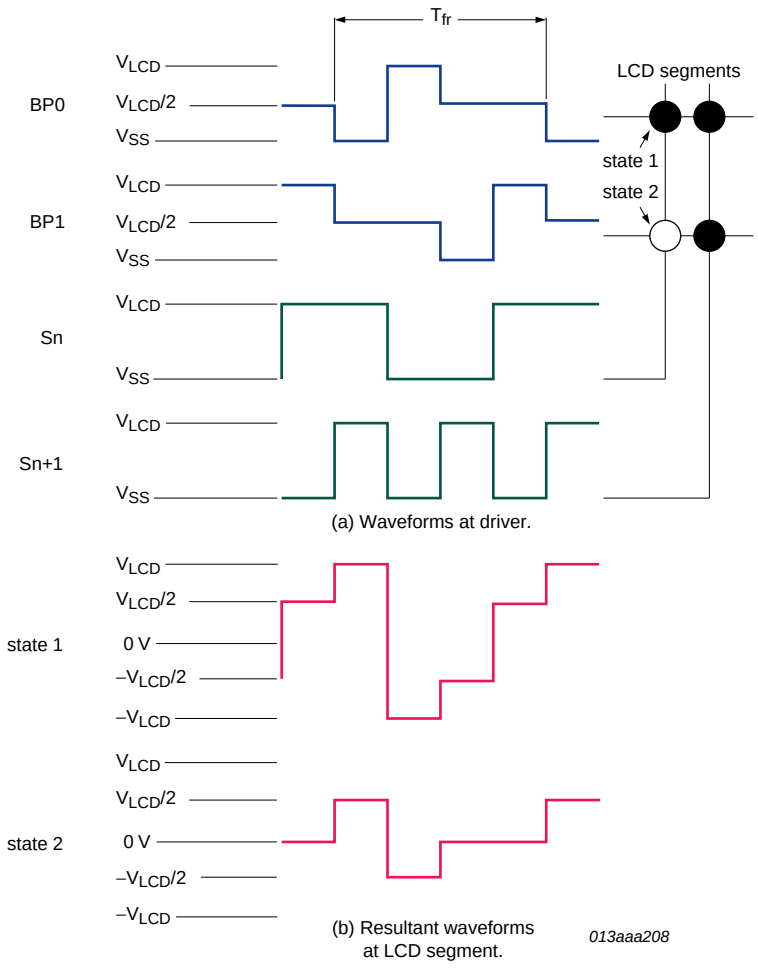
$V_{state2}(t) = V_{(Sn + 1)}(t) - V_{BP0}(t)$.

$V_{on(RMS)}(t) = V_{LCD}$. $V_{off(RMS)}(t) = 0$ V.

Fig 16. Static drive mode waveforms (line inversion mode)

8.4.2.2 1:2 Multiplex drive mode

When two backplanes are provided in the LCD, the 1:2 multiplex mode applies. The PCA9620 allows the use of ½ bias or ⅓ bias in this mode as shown in Figure 17 and Figure 18.

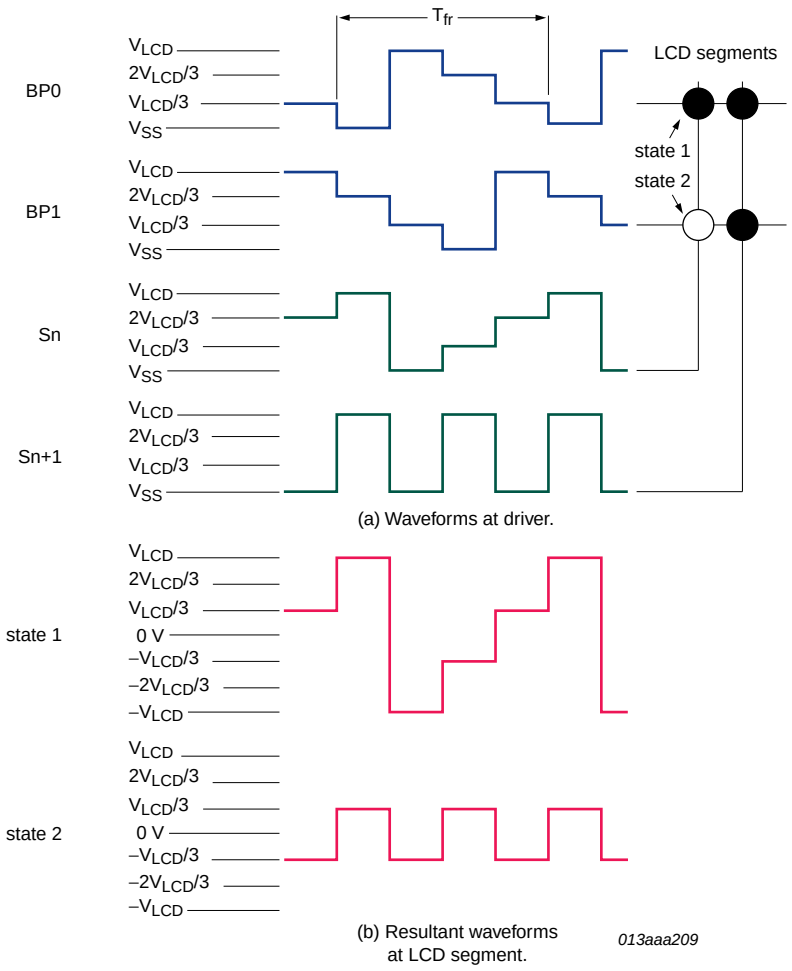


$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{on(RMS)}(t) = 0.791V_{LCD}$. $V_{off(RMS)}(t) = 0.354V_{LCD}$.

Fig 17. Waveforms for the 1:2 multiplex drive mode with ½ bias (line inversion mode)



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

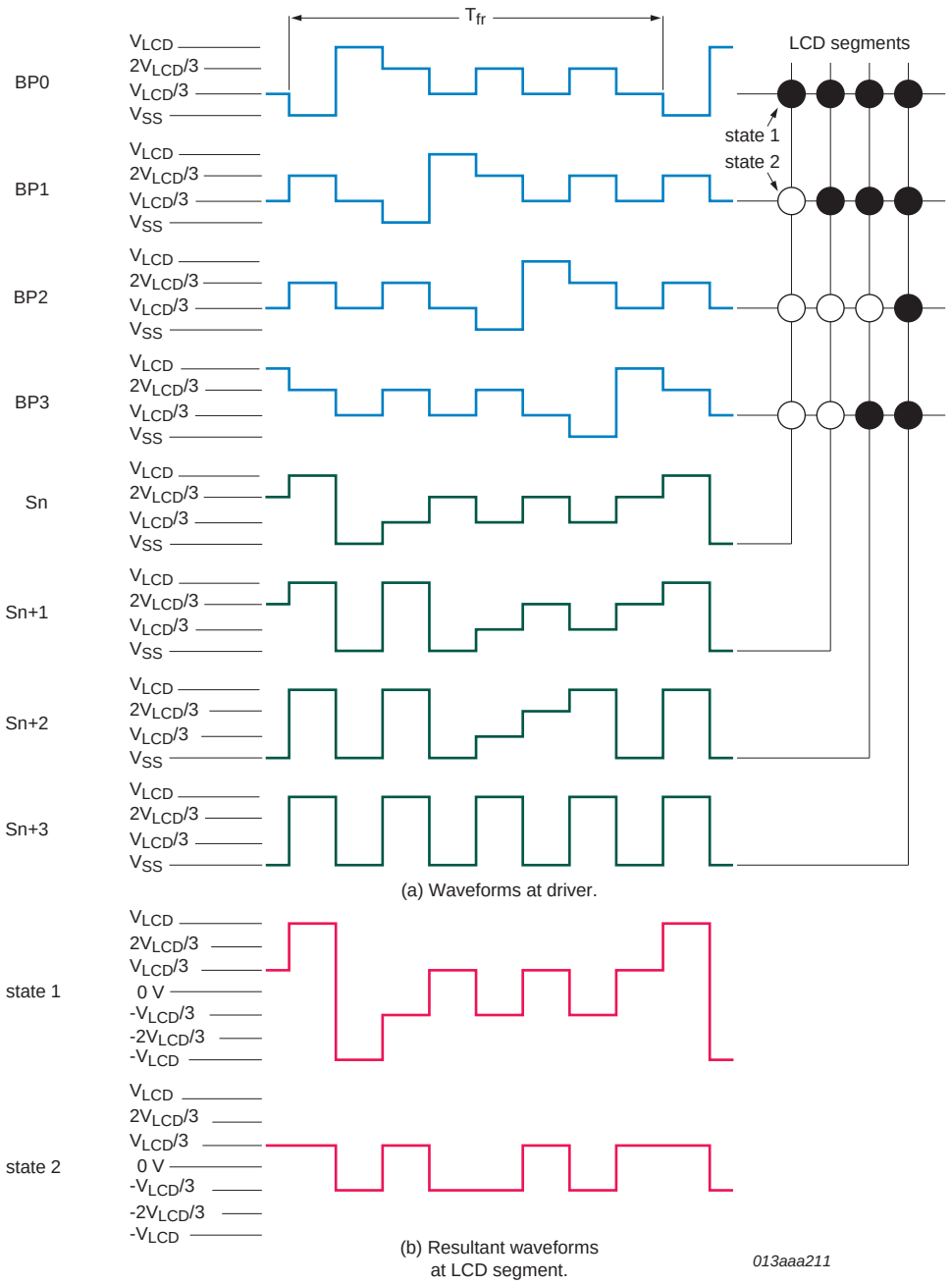
$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{on(RMS)}(t) = 0.745V_{LCD}$. $V_{off(RMS)}(t) = 0.333V_{LCD}$.

Fig 18. Waveforms for the 1:2 multiplex drive mode with ⅓ bias (line inversion mode)

8.4.2.3 1:4 Multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies, as shown in Figure 19.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

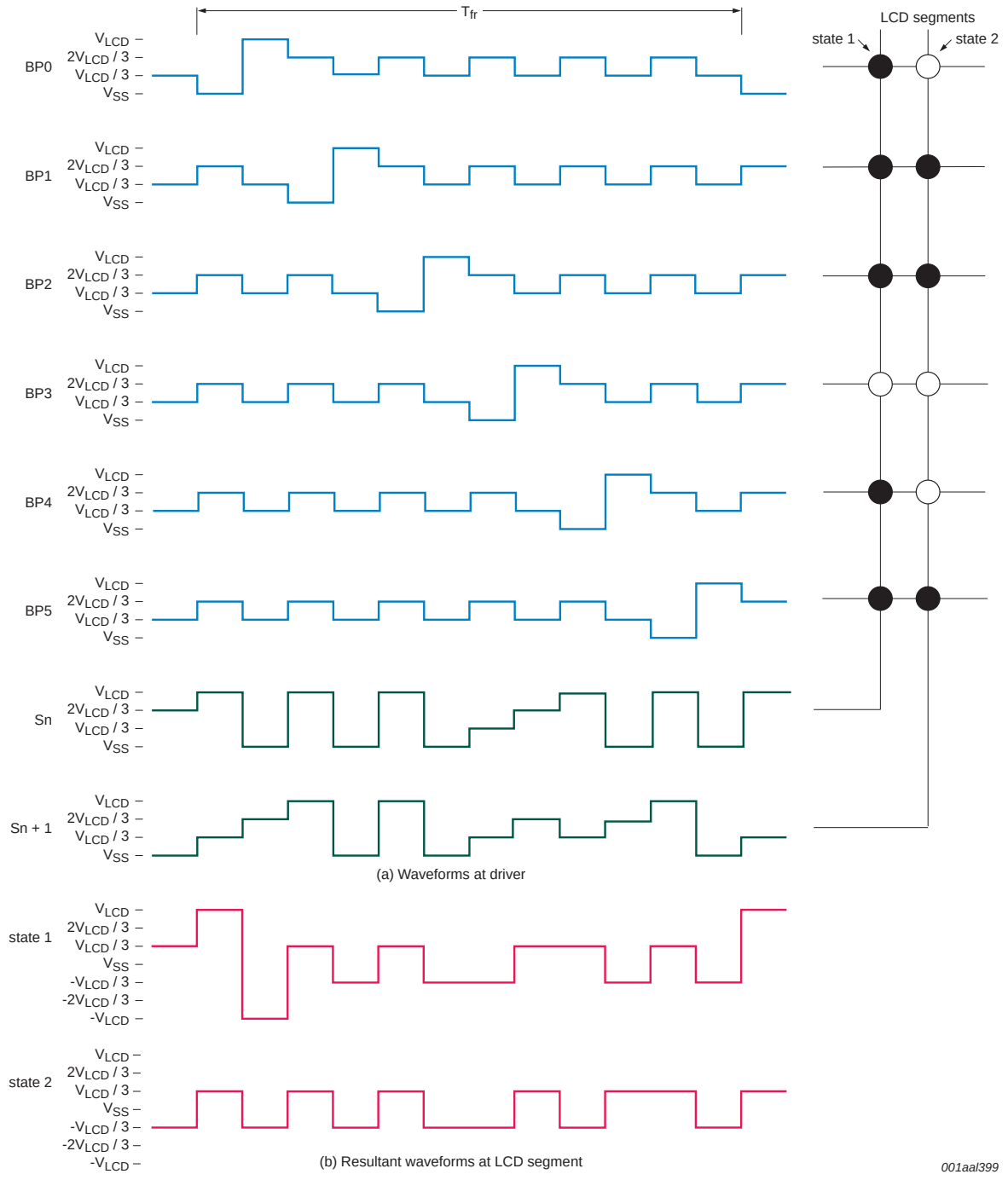
$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{on(RMS)}(t) = 0.577V_{LCD}$. $V_{off(RMS)}(t) = 0.333V_{LCD}$.

Fig 19. Waveforms for the 1:4 multiplex drive mode with ⅓ bias (line inversion mode)

8.4.2.4 1:6 Multiplex drive mode

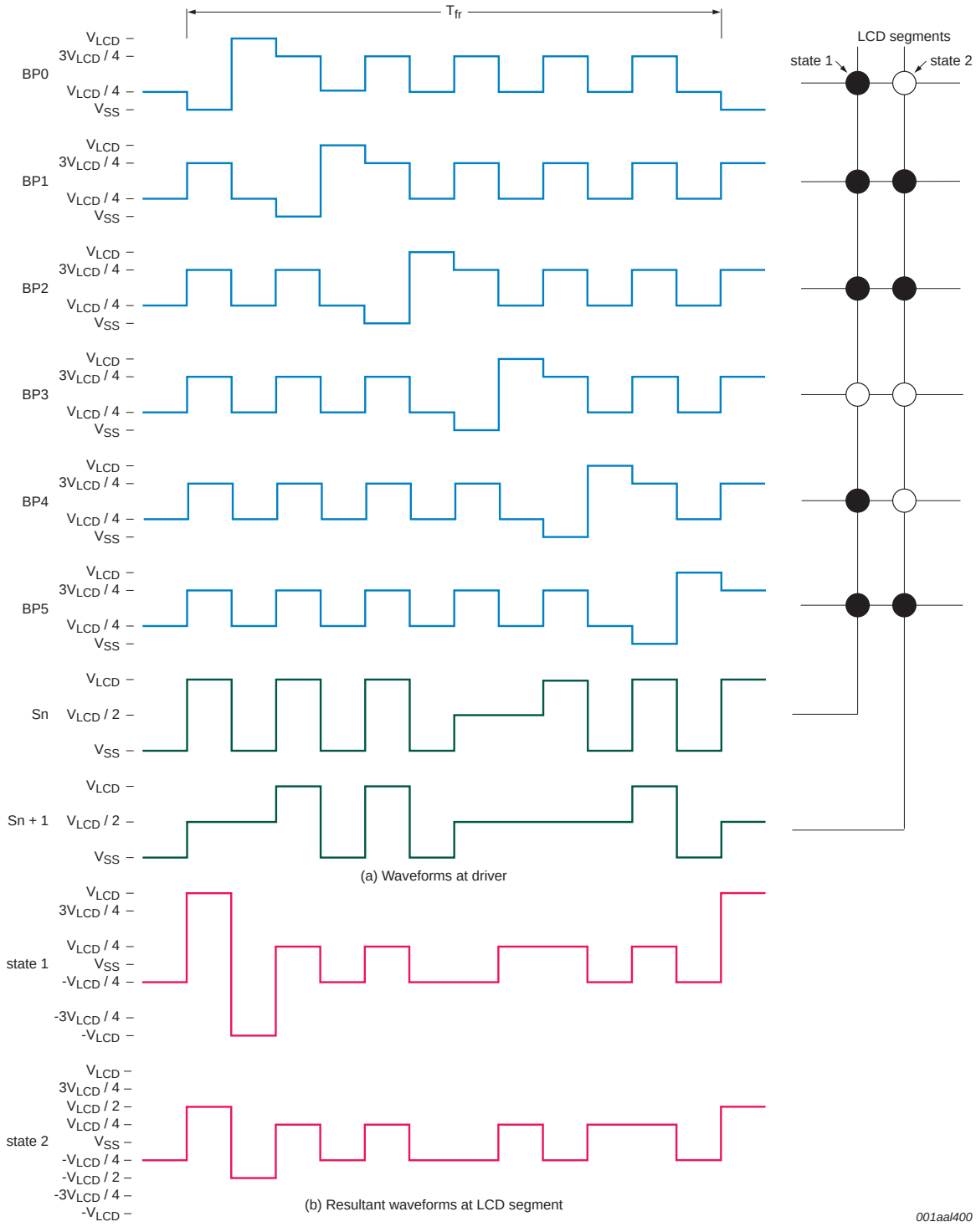
When six backplanes are provided in the LCD, the 1:6 multiplex drive mode applies. The PCA9620 allows the use of ⅓ bias or ¼ bias in this mode as shown in Figure 20 and Figure 21.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$. $V_{state2}(t) = V_{Sn+1}(t) - V_{BP0}(t)$.

$V_{on(RMS)}(t) = 0.509V_{LCD}$. $V_{off(RMS)}(t) = 0.333V_{LCD}$.

Fig 20. Waveforms for 1:6 multiplex drive mode with ⅓ bias (line inversion mode)

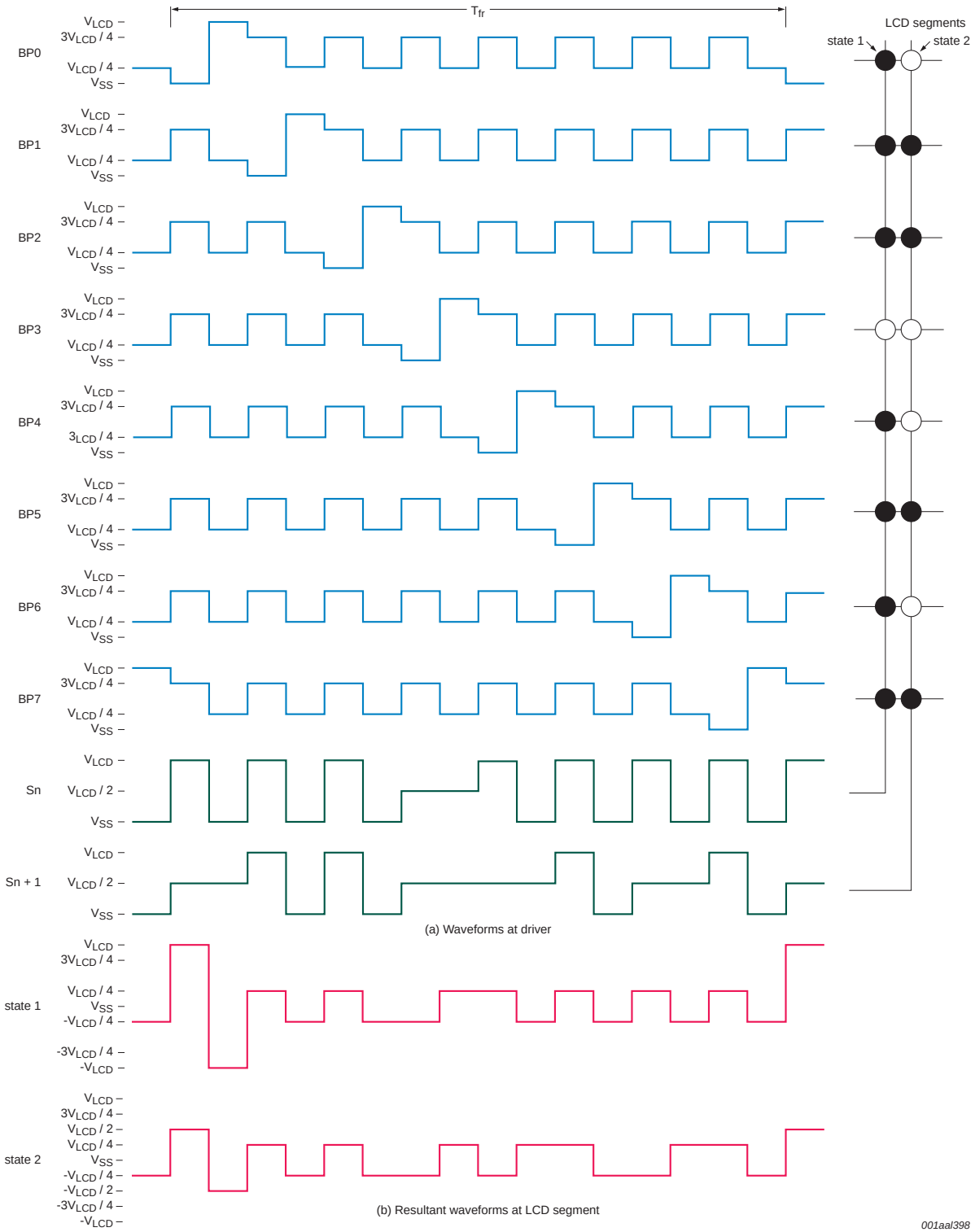


$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$. $V_{state2}(t) = V_{Sn+1}(t) - V_{BP0}(t)$.

$V_{on(RMS)}(t) = 0.467V_{LCD}$. $V_{off(RMS)}(t) = 0.306V_{LCD}$.

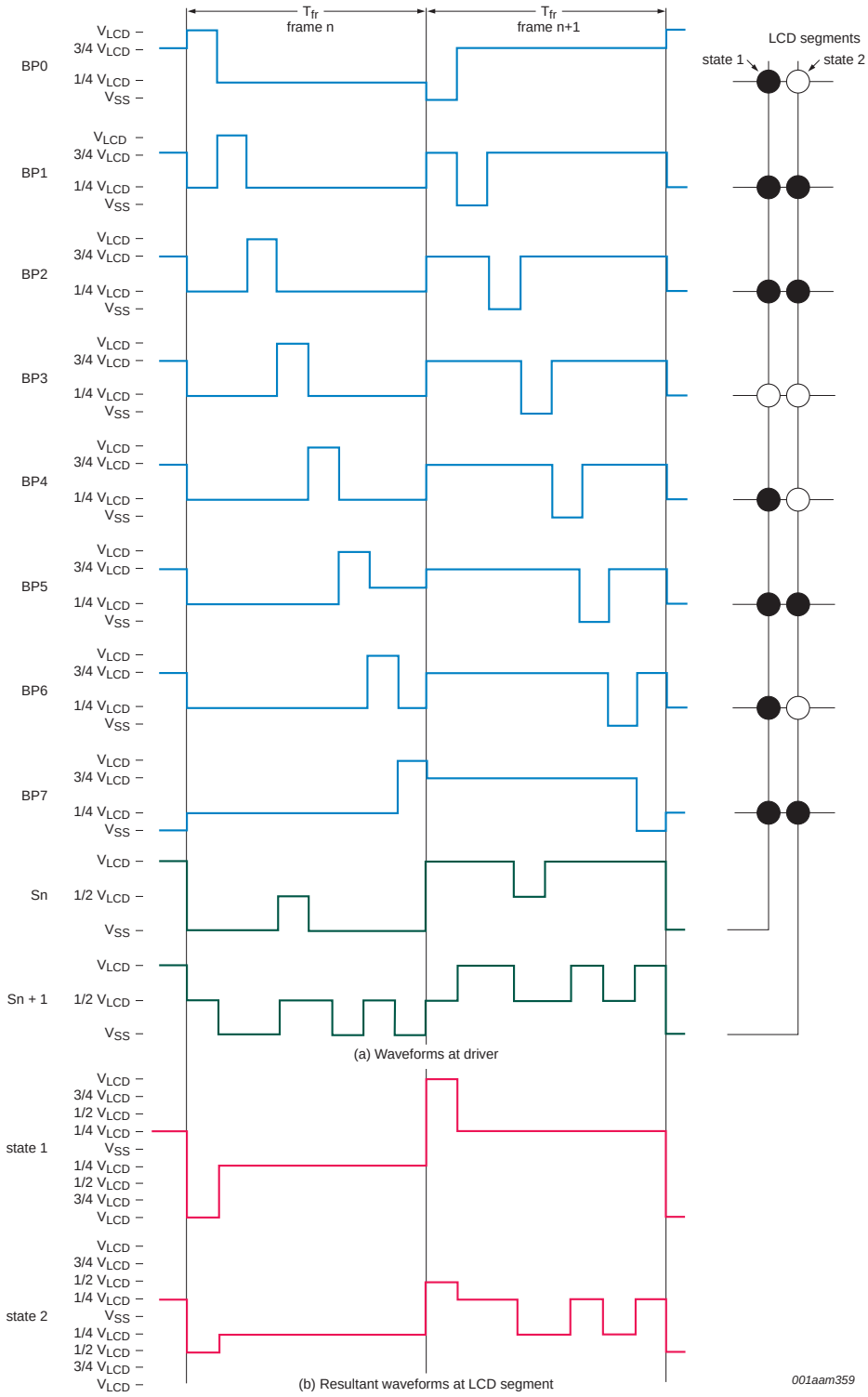
Fig 21. Waveforms for 1:6 multiplex drive mode with ¼ bias (line inversion mode)

8.4.2.5 1:8 Multiplex drive mode



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$. $V_{state2}(t) = V_{Sn+1}(t) - V_{BP0}(t)$. $V_{on(RMS)}(t) = 0.424V_{LCD}$. $V_{off(RMS)}(t) = 0.293V_{LCD}$.

Fig 22. Waveforms for 1:8 multiplex drive mode with ¼ bias (line inversion mode)



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$. $V_{state2}(t) = V_{Sn+1}(t) - V_{BP0}(t)$. $V_{on(RMS)}(t) = 0.424V_{LCD}$. $V_{off(RMS)}(t) = 0.293V_{LCD}$.

Fig 23. Waveforms for 1:8 multiplex drive mode with ¼ bias (frame inversion mode)

When eight backplanes are provided in the LCD, the 1:8 multiplex drive mode applies, as shown in Figure 22 and Figure 23.

8.4.3 V_{LCD} generation

V_{LCD} can be generated and controlled on the chip by using software commands. When the internal charge pump is used, the programmed V_{LCD} is available on pin V_{LCD}. The charge pump generates a V_{LCD} of up to $3 \times V_{DD2}$.

The charge pump can be enabled or disabled with the CPE bit (see Table 9 on page 9). With bit CPC, the charge pump multiplier setting can be configured.

The final value of V_{LCD} is a combination of the programmed VPR[7:0] value and the output of the temperature compensation block, VT[7:0]. The system is shown in Figure 24.

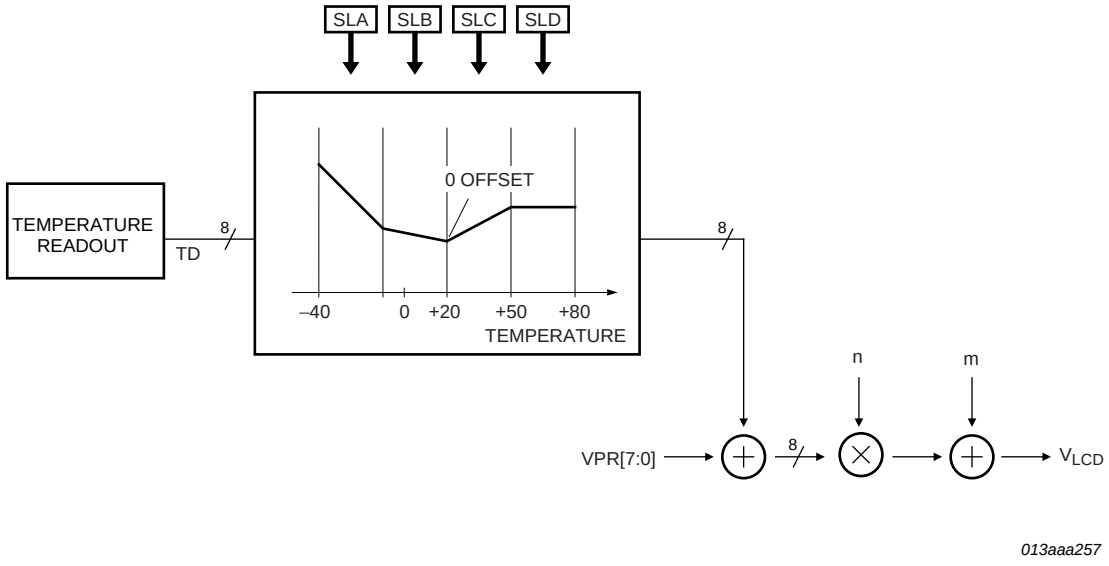


Fig 24. V_{LCD} generation including temperature compensation

In Equation 6 the main parameters are the programmed digital value term and the compensated temperature term.

$$V_{LCD} = [VPR[7{:}0] + VT[7{:}0]] \times n + m \quad (6)$$

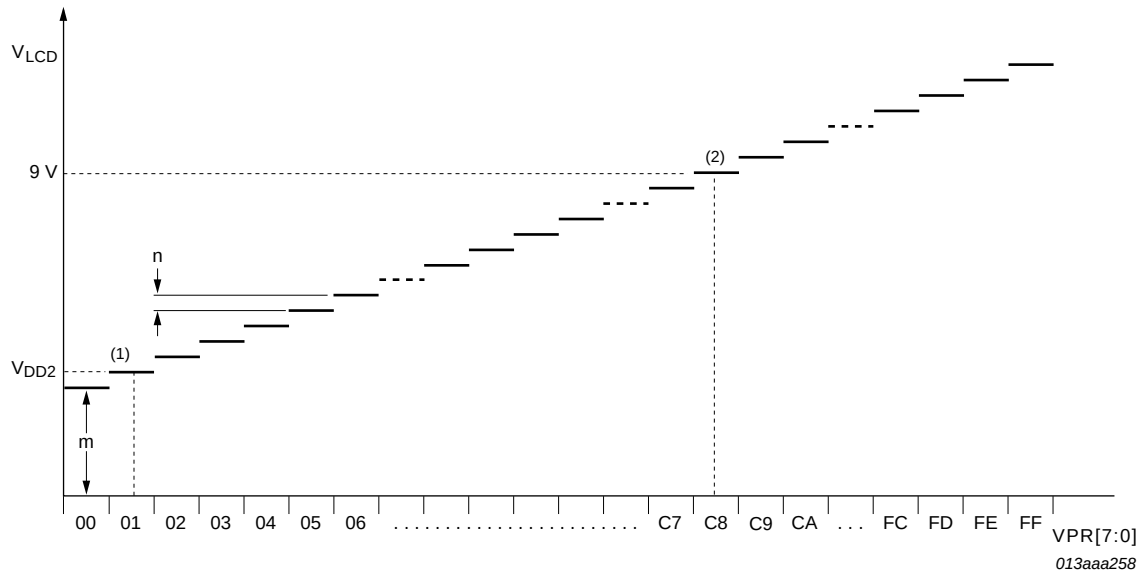
1. VPR[7:0] is the binary value of the programmed voltage.
2. VT[7:0] is the binary value of the temperature compensated voltage. Its value comes from the temperature compensation block and is a two's complement which has the value 0h at 20 °C.
3. m and n are fixed values (see Table 28).

Table 28. Parameters of V_{LCD} generation

Symbol	Value	Unit
m	3	V
n	0.03	V

Figure 25 shows how V_{LCD} changes with the programmed value of VPR[7:0].

It has to be taken into account that the charge pump has to be configured (via bit CPC) properly to obtain the desired voltage range. For example, if V_{DD2} = 3.0 V and CPC is set to 2 × V_{DD2} (logic 0) then the maximum theoretical value that the charge pump can reach is V_{LCD} = 6.0 V. But in reality, lower values will be reached due to internal resistances, see Section 8.4.5. So, if the requested value for V_{LCD} = 7.0 V then the charge pump has to be configured with CPC set to 3 × V_{DD2} (logic 1).



(1) If V_{DD2} > 3.0 V then VPR[7:0] must be set so that V_{LCD} > V_{DD2}.

(2) Automatic limitation for V_{LCD} > 9.0 V.

Fig 25. V_{LCD} programming of PCA9620 (assuming VT[7:0] = 0h)

Programmable range of VPR[7:0] is from 0h to FFh. This would allow achieving V_{LCD} > 9.0 V, but the PCA9620 has a built-in automatic limitation of V_{LCD} at 9.0 V.

If V_{DD2} is higher than 3.0 V, then it is important that VPR[7:0] is set to a value such that the resultant V_{LCD} (including the temperature correction of VT[7:0]) is higher than V_{DD2}.

8.4.4 External V_{LCD} supply

V_{LCD} can be directly supplied to the V_{LCD} pin. In this case, the internal charge pump must not be enabled otherwise a high current may occur on pin V_{DD2} and pin V_{LCD}. When V_{LCD} is supplied externally, no internal temperature compensation occurs on this voltage even if bit TCE is set logic 1 (see Section 8.4.8 on page 38). The V_{LCD} voltage which is supplied externally will be available at the segments and backplanes of the device through the chosen bias system. Also programming the VPR[7:0] bit field has no effect on the V_{LCD} which is externally supplied.

8.4.5 Charge pump driving capability

Figure 26 illustrates the main factor determining how much current the charge pump can deliver.

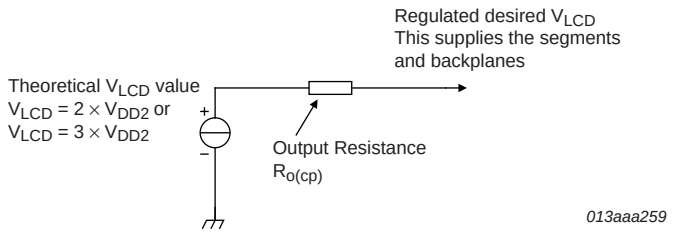


Fig 26. Charge pump model (used to characterize the driving strength)

The output resistance of the charge pump is specified in Table 36 on page 57. With these values, it can be calculated how much current the charge pump can drive under certain conditions.

Example: Assuming that the normal operation point is at 25 °C with V_{LCD} = 7.0 V and V_{DD2} = 5.0 V and the charge pump is set to 2 × V_{DD2}. Then the theoretical value of V_{LCD} is 10.0 V and the desired one is 7.0 V. The difference between the theoretical maximum value and desired one is 3.0 V. The charge pump resistance is nominally 0.85 kΩ. Equation 7 shows the possible current that the charge pump could deliver:

$$I_{load} = \Delta V_{LCD} / R_{o(cp)} \quad (7)$$

The result of this example is: $I_{load} = 3.0\ \text{V} / 0.85\ \text{k}\Omega = 3.5\ \text{mA}$

In cases where no extreme driving capability is needed, a command is available for decreasing the charge pump frequency (see Table 23 on page 13) and thus reducing the total current consumption. If the charge pump frequency is halved, then the driving capability is halved as well, whereas the output resistance doubles.

8.4.6 Charge pump frequency settings and power efficiency

The PCA9620 offers the possibility to use different frequency settings for the charge pump. Bit CPF controls the frequency at which the charge pump is running (see Table 23 on page 13). This frequency has a direct influence on the current consumption of the IC but also on the charge pump driving capability. Using a lower charge pump frequency decreases the current consumption and the driving capability.

The power efficiency of the charge pump determines in certain applications which frequency settings to choose for the CPF bit. Concerning the example shown in Figure 27: The current consumption was measured with

- charge pump set to 2 × V_{DD2}
- V_{DD2} = 3.0 V
- VPR[7:0] set to maximum to obtain the highest possible V_{LCD} with this setup, which is close to 6.0 V

The current load on pin V_{LCD} determines the output power delivered by the IC:

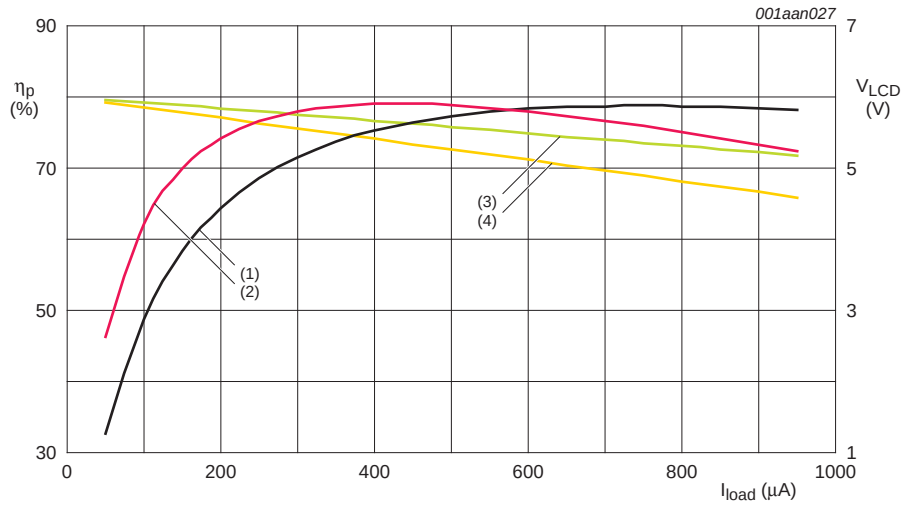
$$P_o = I_{load} \times V_{LCD} \quad (8)$$

The current consumption on pin V_{DD2} determines the input power taken by the IC:

$$P_i = I_{DD2} \times V_{DD2} \quad (9)$$

The ratio between these two numbers determines the charge pump power efficiency:

$$\eta_p = P_o / P_i \quad (10)$$



Charge pump set to 2 × V_{DD2}; V_{DD2} = 3 V.

(1) η_p, full charge pump frequency.

(2) η_p, half charge pump frequency.

(3) V_{LCD}, full frequency.

(4) V_{LCD}, half frequency.

Fig 27. Power efficiency of the charge pump

Loading the charge pump with higher currents decreases the output voltage. This decrease is determined by the charge pump driving capability, respectively by the output resistance of the charge pump (see Table 36 on page 57).

The power efficiency calculation is only valid when the charge pump is running at its maximum peak frequency and regulates the generated V_{LCD} voltage with full speed. In this case, the ripple on the V_{LCD} voltage equals the internal charge pump frequency. Approximately, this could also be calculated with the parameter of the output resistance of the charge pump (see Table 36 on page 57), the load current, and the voltage needed to be provided by using Equation 7 on page 35. This value of I_{load} is close to the value of the load current needed for the application.

If the application runs with V_{DD2} = 3.0 V, the load currents are up to 400 μA (DC measured), and the V_{LCD} generated voltages are up to 5.0 V, then - concerning power efficiency - it would be the best to have a charge pump frequency set to half frequency.

If it is desired to change the charge pump frequency, it is recommended to make a graph like Figure 27 and understand what the application requirements are. This would basically imply to find out what would be the maximum V_{LCD} requirements and what would be the maximum load currents required. Then it can be decided which is the best setting of bit CPF.

Tuning the charge pump frequency might be a difficult task to do. It requires good knowledge of the application in which the IC is being used; therefore, NXP is recommending to keep the CPF bit set logic 0 to have the maximum charge pump frequency, thus having the maximum driving strength.

8.4.7 Temperature readout

The PCA9620 has a built-in temperature sensor which provides an 8 bit digital value, TD[7:0], of the ambient temperature. This value can be read through the I^2C interface (see Figure 50 on page 54). The actual temperature is determined from TD[7:0] using Equation 11:

$$T\,(°C) = 0.9375 \times TD[7:0] - 40 \quad (11)$$

The measurement needs about 5 ms to complete. it is repeated periodically as soon as bit TME is set logic 1 (see Table 10 on page 9). The time between measurements is linked to the system clock and hence varies with changes in the chosen frame frequency, see Table 29.

Table 29. Temperature measurement update rate

Selected frame frequency	Temperature measurement update rate
60 Hz	3.3 s
200 Hz	1 s
300 Hz	0.67 s

Due to the nature of a temperature sensor, oscillations on the V_{LCD} may occur. To avoid it, a filter has been implemented in PCA9620. The system is shown in Figure 28.

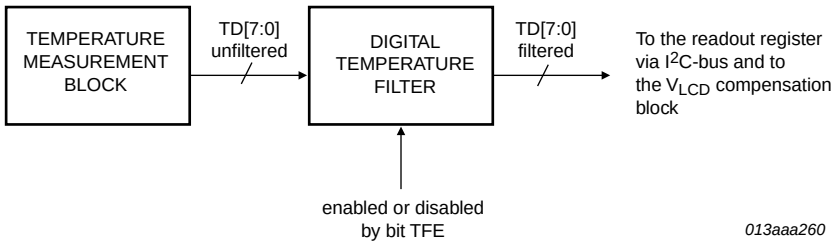
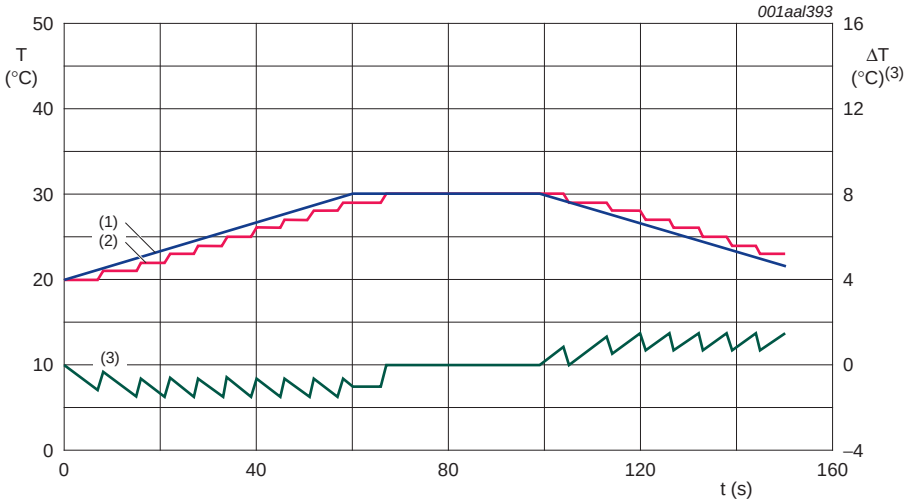


Fig 28. Temperature measurement block with digital temperature filter

Like any other filtering, the digital temperature filter (see Figure 28) introduces a certain delay in the measurement of temperature. This behavior is illustrated in Figure 29.



(1) Environment temperature, T1 (°C).

(2) Measured temperature, T2 (°C).

(3) Temperature deviation, ΔT = T2 – T1.

Fig 29. Temperature measurement delay

This delay may cause undesired effects at start-up when the environment temperature may be different than the reset value of the PCA9620 which is 20 °C. In this case, it takes up to 30 s until the correct measured temperature value will be available. A control bit, TFE, is implemented to enable or disable the digital temperature filter. This bit is set logic 0 by default which means that the filter is disabled and the unfiltered environment temperature value is available to calculate the desired V_{LCD}.

8.4.8 Temperature compensation of V_{LCD}

Due to the temperature dependency of the liquid crystal viscosity, the LCD controlling voltage V_{LCD} might have to be adjusted at different temperatures to maintain optimal contrast. The temperature behavior of the liquid comes from the LCD manufacturer. The slope has to be set to compensate for the liquid behavior. Internal temperature compensation may be enabled via bit TCE.

The ambient temperature range is split up into four equally sized regions and a different temperature coefficient can be applied to each (see Figure 30). Each coefficient can be selected from a choice of eight different slopes. Each one of these coefficients (see Table 30) may be independently selected via the temp-comp-SLA to temp-comp-SLD commands (see Table 5 on page 7).

Table 30. Temperature coefficients

SLA[2:0] to SLD[2:0] value	Corresponding slope factor (mV/°C)	Temperature coefficients MA, MB, MC, MD[1]
000[2]	0	0.00
001	–4	–0.125
010	–8	–0.25
011	–16	–0.5
100	–40	–1.25
101	+4	0.125
110	+8	0.25
111	+16	0.5

[1] The relationship between the temperature coefficients MA to MD and the slope factor is derived from the following equation: $Mx = \frac{0.9375}{0.03} \times \frac{slope}{1000}$.

[2] Default value.

The slope factors imply a linear correction, however the implementation is set in steps of 30 mV (parameter n in Table 28 on page 33).

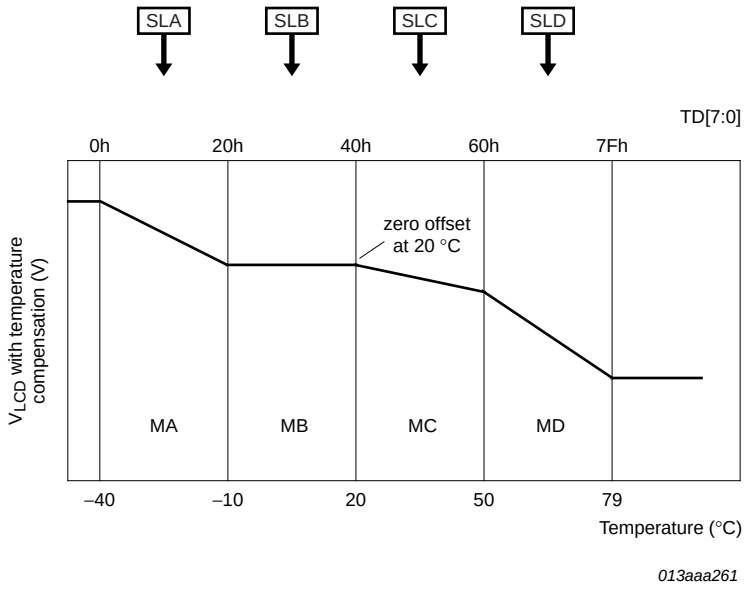


Fig 30. Example of segmented temperature coefficients

Remark: After reset, V_{LCD} is fixed because the VPR[7:0] bit field is reset logic 0. The value of VT[7:0] is generated by the reset value of TD[7:0] (40h, representing 20 °C). Temperature compensation is implemented by adding an offset VT[7:0] to the VPR[7:0] value. VT[7:0] is a two's complement number that equals 0h at 20 °C. The final result for V_{LCD} calculation is an 8-bit positive number (see Equation 6 on page 33).

Remark: Care must be taken that the ranges of VPR[7:0] and VT[7:0] do not cause clipping and hence undesired results. The device will not permit overflow or underflow and will clamp results to either end of the range.

The $V_{offset(LCD)}$ value can be calculated with the equations given in Table 31:

$$V_{offset(LCD)} = m \times V_T \quad (12)$$

Table 31. Calculation of the temperature compensated voltage V_T

Temperature range	TD[7:0]	Offset equation for V_T
T ≤ –40 °C	0h	$V_T = -32 \times MA - 32 \times MB$
–40 °C ≤ T ≤ –10 °C	0h to 20h	$V_T = (TD[7{:}0] - 32) \times MA - 32 \times MB$
–10 °C < T ≤ 20 °C	21h to 40h	$V_T = (TD[7{:}0](-64)) \times MB$
20 °C < T ≤ 50 °C	41h to 60h	$V_T = (TD[7{:}0] - 64) \times MC$
50 °C < T < 80 °C	61h to 7Eh	$V_T = (TD[7{:}0] - 96) \times MD + 32 \times MC$
80 °C ≤ T	7Fh[1]	$V_T = 31 \times MD + 32 \times MC$

[1] No temperature compensation is possible above 80 °C. Above this value, the system maintains the compensation value from 80 °C.

Example: Assumed that T_{amb} = –8 °C; TD[7:0] = 22h; MB = –0.5:

$$V_{offset(LCD)} = m \times V_T = m \times (TD[7{:}0] - 64) \times MB = 30mV \times ((34 - 64) \times -0.5) = 30mV \times -30 \times -0.5 = 450mV \quad (13)$$

The VT[7:0] term is calculated using the digital temperature value TD[7:0] which is provided by the temperature measurement block (Section 8.4.7). Therefore the accuracy of the temperature measurement block (T_{acc}, see Table 36 on page 57) will be directly translated to the LCD voltage deviation ΔV_{LCD}.

Since VT[7:0] = f[T,slope] and T_{acc} = ±6 °C then $\Delta V_T = T_{acc} \times slope$, where slope has one of the possible values specified in Table 30. This term will be added to the total LCD voltage deviation $\Delta V_{offset(LCD)tot}$ over the temperature range. So the total V_{LCD} offset will be: $\Delta V_{offset(LCD)tot} = \Delta V_{LCD} + \Delta V_T$.

8.5 Oscillator

The internal logic and LCD drive signals of the PCA9620 are timed by a frequency f_{clk} which either is the built-in oscillator frequency f_{osc} or equals an external clock frequency.

8.5.1 Internal oscillator

When the internal oscillator is used, it is possible to make the clock signal available on pin CLK by using the oscillator-ctrl command (see Table 8 on page 8). If this is not intended, pin CLK should be left open. At power-on the signal at pin CLK is disabled and pin CLK is in 3-state.

The duty cycle of the output clock provided on the CLK pin is not always 50 : 50. Table 18 on page 11 shows the expected duty cycle for each of the chosen frame frequencies.

8.5.2 External clock

In applications where an external clock needs to be applied to the PCA9620, bit OSC (see Table 8 on page 8) must be set logic 1. In this case pin CLK becomes an input.

The CLK signal is a signal that is fed into the V_{DD1} domain so it must have an amplitude equal to the V_{DD1} voltage supplied to the chip and be referenced to V_{SS}.

The clock frequency (f_{clk}) determines the LCD frame frequency f_{fr}.

Remark: If an external clock is used then this clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal. Removal of the clock is possible when following the correct procedures. See Figure 13 on page 21 and Figure 14 on page 22.

8.5.3 Timing and frame frequency

The timing of the PCA9620 organizes the internal data flow of the device. It includes the transfer of display data from the display RAM to the display segment outputs. The timing also generates the LCD frame frequency which it derives as an integer division of the clock frequency. The frame frequency is a fixed division of the internal clock or of the frequency applied to pin CLK when an external clock is used:

$$f_{fr} = \frac{f_{clk}}{48} \tag{14}$$

When the internal clock is used, the clock and frame frequency can be programmed by software such that the nominal frame frequency can be chosen in steps of 10 Hz in the range of 60 Hz to 300 Hz (see Table 18 on page 11). Furthermore the nominal frame frequency is factory-calibrated with an accuracy of ±15 %.

When the internal clock is enabled at pin CLK by using bit COE, the duty ratio of the clock may change when choosing different values for the frame frequency prescaler. Table 18 on page 11 shows the different output duty ratios for each frame frequency prescaler setting.

8.6 Backplane outputs

The LCD drive section includes eight backplane outputs: BP0 to BP7. The backplane output signals are generated based on the selected LCD multiplex drive mode.

Table 32 describes which outputs are active for each of the multiplex drive modes and what signal is generated.

Table 32. Mapping of output pins and corresponding output signals with respect to the multiplex driving mode

Multiplex drive mode	Output pin							
	BP0	BP1	BP2	BP3	BP4	BP5	BP6	BP7
	Signal							
1:8	BP0	BP1	BP2	BP3	BP4	BP5	BP6	BP7
1:6	BP0	BP1	BP2	BP3	BP4	BP5	BP0[1]	BP1[1]
1:4	BP0	BP1	BP2	BP3	BP0[1]	BP1[1]	BP2[1]	BP3[1]
1:2	BP0	BP1	BP0[1]	BP1[1]	BP0[1]	BP1[1]	BP0[1]	BP1[1]
static	BP0	BP0[1]	BP0[1]	BP0[1]	BP0[1]	BP0[1]	BP0[1]	BP0[1]

[1] These pins may optionally be connected to the display to improve drive strength. Connect only with the corresponding output pin carrying the same signal. If not required, they can be left open-circuit.

8.7 Segment outputs

The LCD drive section includes 60 segment outputs (S0 to S59) which must be connected directly to the LCD. The segment output signals are generated based on the multiplexed backplane signals and with data resident in the display register. When less than 60 segment outputs are required, the unused segment outputs must be left open-circuit.

8.8 Display register

The display register holds the display data while the corresponding multiplex signals are generated.

8.9 Display RAM

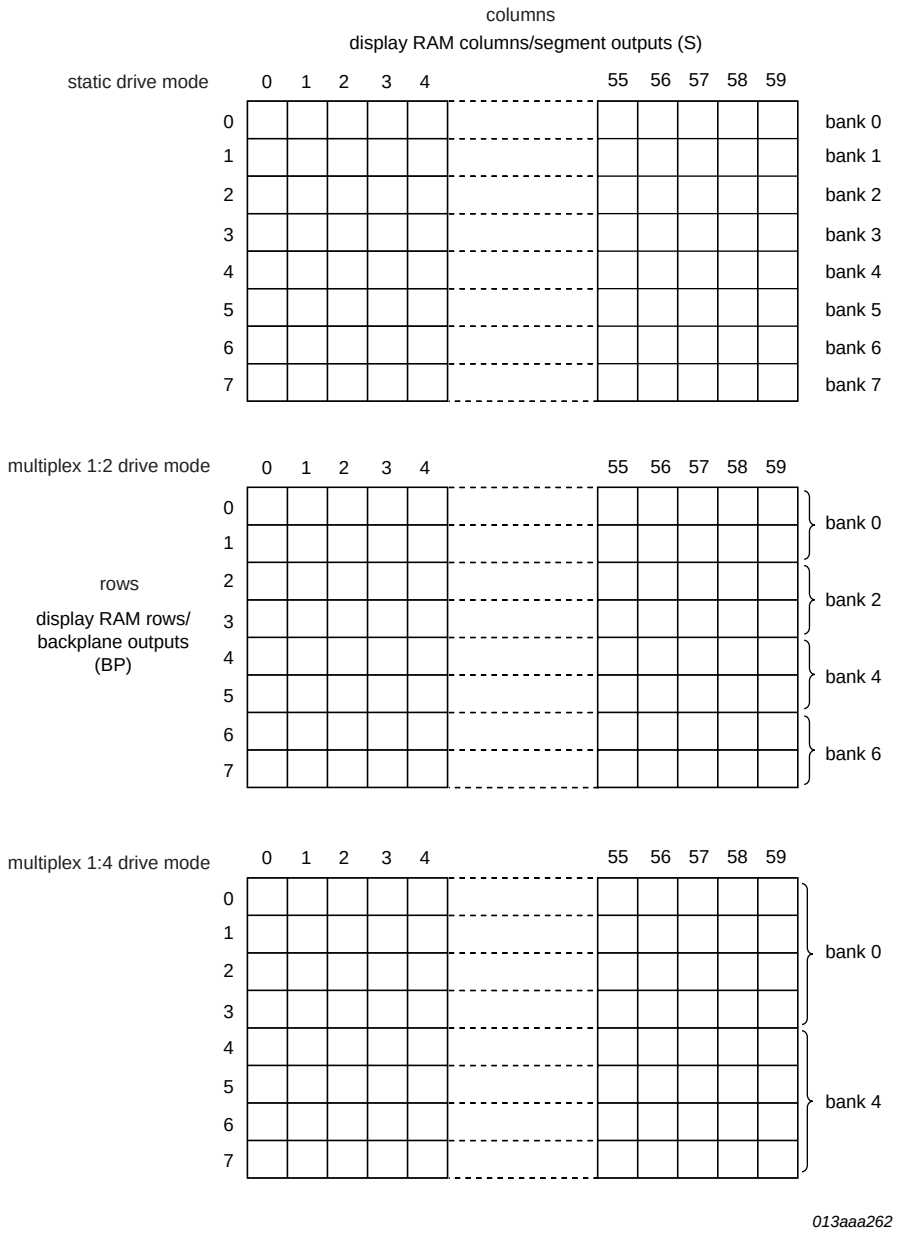
The display RAM is a static 60 × 8-bit RAM which stores LCD data. Logic 1 in the RAM bit map indicates the on-state of the corresponding LCD element; similarly, logic 0 indicates the off-state.

There is a one-to-one correspondence between

- the bits in the RAM bitmap and the LCD elements
- the RAM columns and the segment outputs
- the RAM rows and the backplane outputs.

The display RAM bit map, Figure 31, shows row 0 to row 7 which correspond with the backplane outputs BP0 to BP7, and column 0 to column 59 which correspond with the segment outputs S0 to S59. In multiplexed LCD applications, the data of each row of the display RAM is time-multiplexed with the corresponding backplane (row 0 with BP0, row 1 with BP1, and so on).

When display data is transmitted to the PCA9620, the display bytes received are stored in the display RAM in accordance with the selected LCD multiplex drive mode. The data is stored as it arrives and does not wait for the acknowledge cycle as with the commands. Depending on the current multiplex drive mode, data is stored singularly, in pairs, quadruples, sextuples or bytes.



The display RAM bitmap shows the direct relationship between the display RAM column and the segment outputs, between the bits in a RAM row and the backplane outputs, and between the RAM rows and banks.

Fig 31. Display RAM bitmap

8.9.1 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. It allows the loading of an individual display data byte, or a series of display data bytes into any location of the display RAM. The sequence commences with the initialization of the data pointer by the load-data-pointer command. Following this command, an arriving data byte is stored starting at the display RAM address indicated by the data pointer.

The data pointer is automatically incremented in accordance with the chosen LCD multiplex drive mode configuration. That is, after each byte is stored, the contents of the data pointer are incremented

- by eight (static drive mode)
- by four (1:2 multiplex drive mode)
- by two (1:4 multiplex drive mode)
- by one or two (1:6 multiplex drive mode), see Figure 38 on page 47
- by one (1:8 multiplex drive mode)

If the data pointer reaches the end of the RAM row, it is automatically wrapped around to address 0. This means that it can be continuously written to or read from the display RAM.

The data pointer should always be set to an address where the remaining RAM is divisible by eight because odd bits will be discarded (see Figure 33). This behavior is only shown in static drive mode because the 60 RAM cells cannot be divided by eight without remainder.

If an I^2C-bus data access is terminated early, then the state of the data pointer is unknown. The data pointer must then be re-written before further RAM accesses.

8.9.1.1 RAM filling in static drive mode

In the static drive mode the eight transmitted data bits are placed in eight successive display RAM columns in row 0 (see Figure 32).

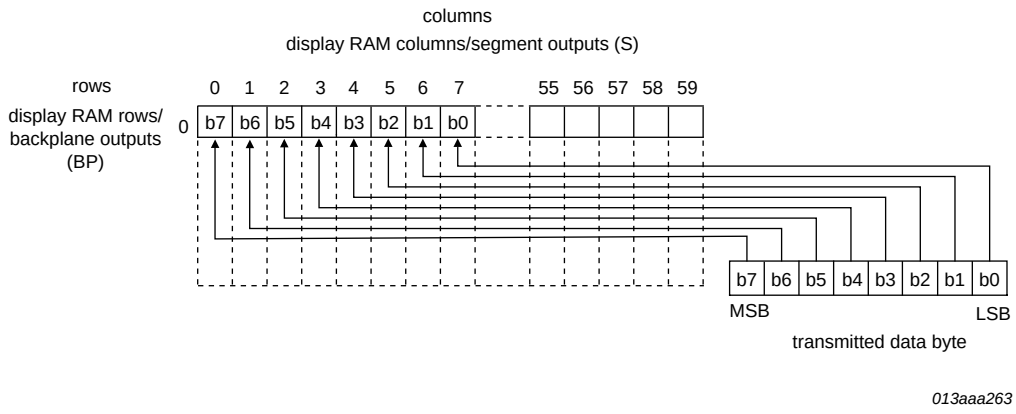


Fig 32. Display RAM filling order in static drive mode

In order to fill the whole RAM row, 8 bytes must be sent to the PCA9620, but the last 4 bits from the last byte are discarded, and the data pointer is wrapped around to column 0 to start a possible RAM content update (see Figure 33).

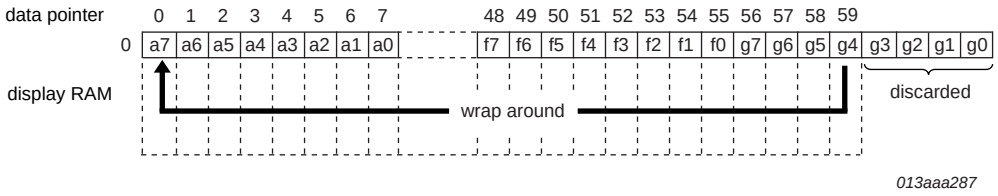


Fig 33. Discarded bits and data pointer wrap around at the end of data transmission

8.9.1.2 RAM filling in 1:2 multiplex drive mode

In the 1:2 multiplex drive mode the eight transmitted data bits are placed in four successive display RAM columns of two rows (see Figure 34).

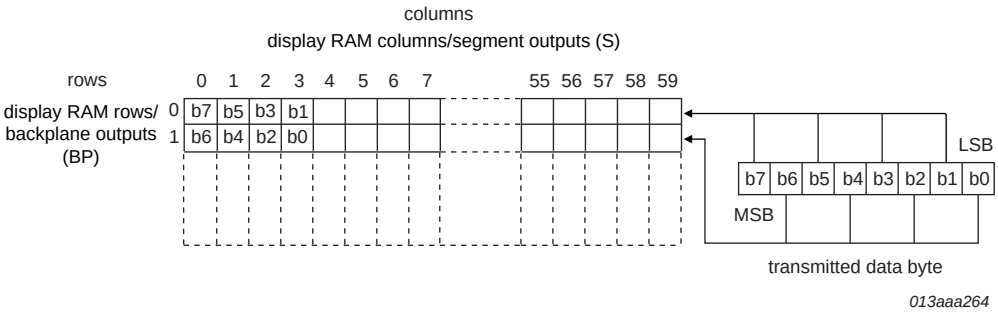


Fig 34. Display RAM filling order in 1:2 multiplex drive mode

In order to fill the whole two RAM rows 15 bytes need to be sent to the PCA9620. After the last byte sent, the data pointer is wrapped around to column 0 to start a possible RAM content update (see Figure 35). Even if a data byte is transmitted during the wrapping of the data pointer, then all the bits in the byte will be written correctly.

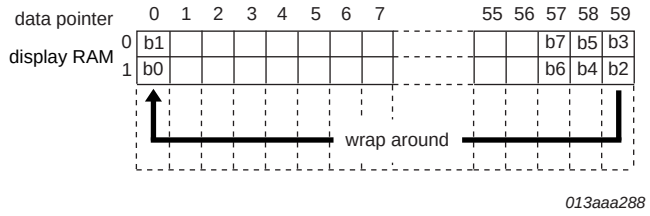


Fig 35. Data pointer wrap around in 1:2 multiplex drive mode

8.9.1.3 RAM filling in 1:4 multiplex drive mode

In the 1:4 multiplex drive mode the eight transmitted data bits are placed in two successive display RAM columns of four rows (see Figure 36).

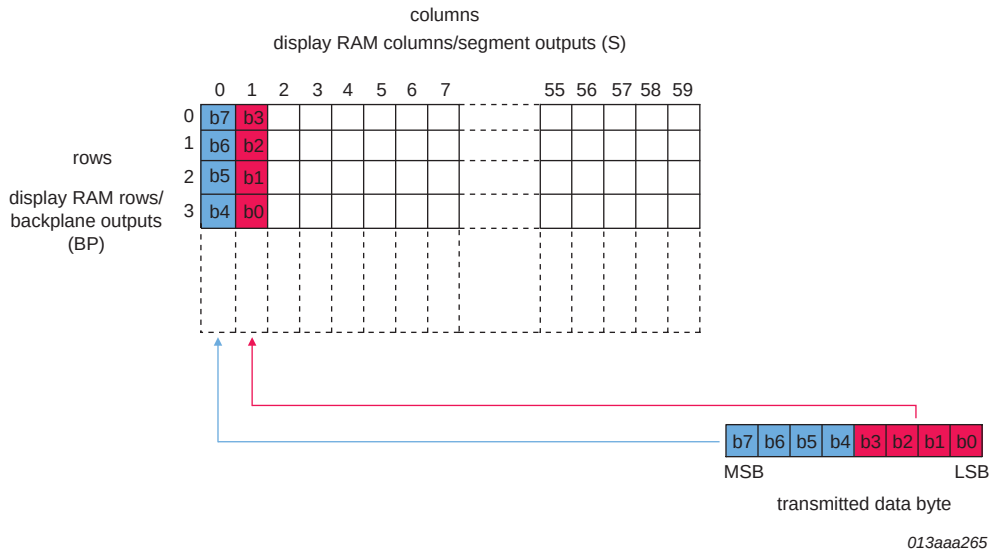


Fig 36. Display RAM filling order in 1:4 multiplex drive mode

In order to fill the whole four RAM rows 30 bytes need to be sent to the PCA9620. After the last byte sent, the data pointer is wrapped around to column 0 to start a possible RAM content update (see Figure 37). Even if a data byte is transmitted during the wrapping of the data pointer, all the bits in the byte will be written correctly.

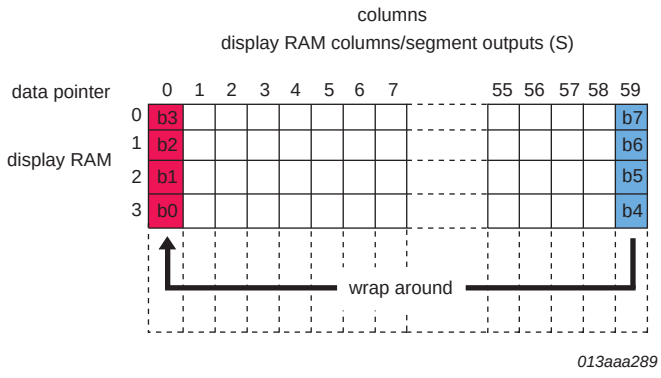


Fig 37. Data pointer wrap around in 1:4 multiplex drive mode

8.9.1.4 RAM filling in 1:6 multiplex drive mode

In the 1:6 multiplex drive mode the RAM is organized in six rows and 60 columns. The eight transmitted data bits are placed in such a way, that a column is filled up (see Figure 38).

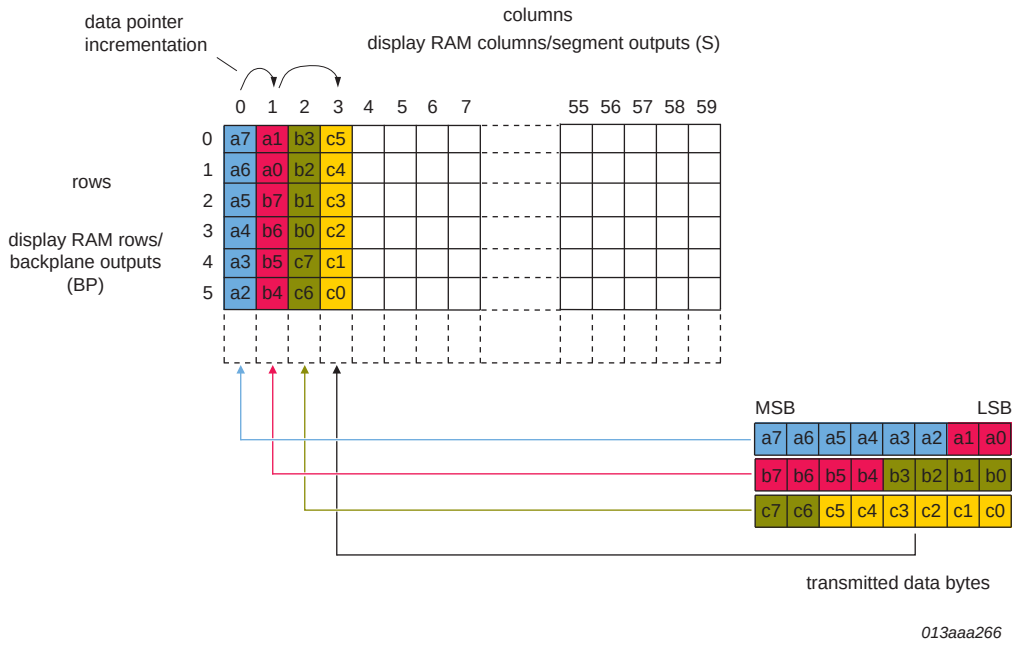


Fig 38. Display RAM filling order in 1:6 multiplex drive mode

The remaining bits are wrapped up into the next column. In order to fill the whole RAM addresses 45 bytes need to be sent to the PCA9620. After the last byte sent, the data pointer is wrapped around to column 0 to start a possible RAM content update (see Figure 39). Even if a data byte is transmitted during the wrapping of the data pointer, all the bits in the byte will be written correctly.

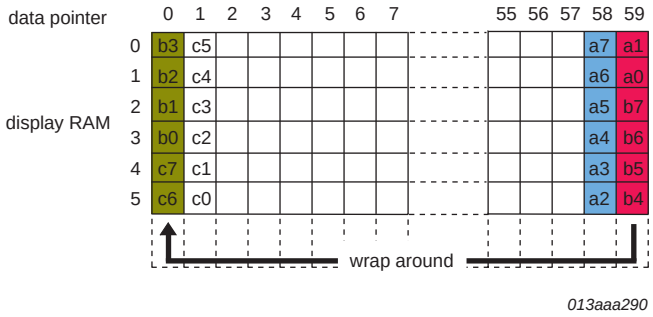


Fig 39. Data pointer wrap around in 1:6 multiplex drive mode

8.9.1.5 RAM filling in 1:8 multiplex drive mode

In the 1:8 multiplex drive mode the eight transmitted data bits are placed into eight rows of one display RAM column (see Figure 40).

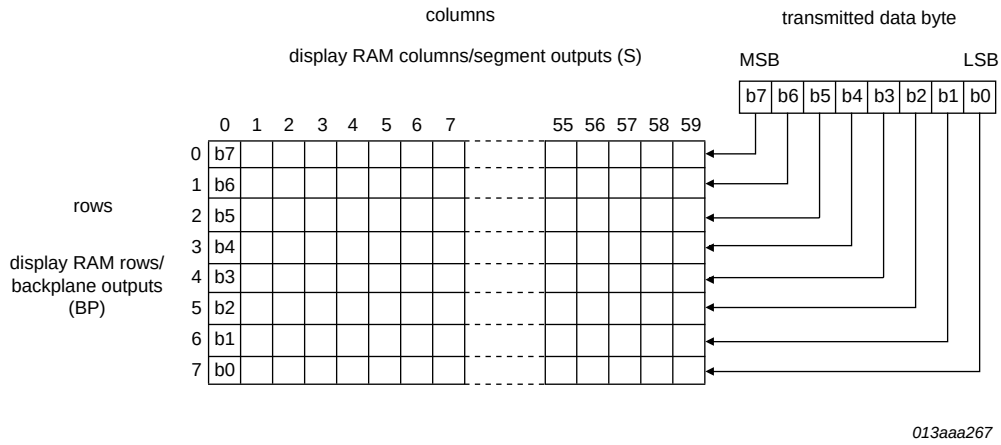


Fig 40. Display RAM filling order in 1:8 multiplex drive mode

In order to fill the whole RAM addresses 60 bytes need to be sent to the PCA9620. After the last byte sent, the data pointer is wrapped around to column 0 to start a possible RAM content update (see Figure 41). In this case, there is no situation possible where a transmitted data byte can be written over the RAM boundary.

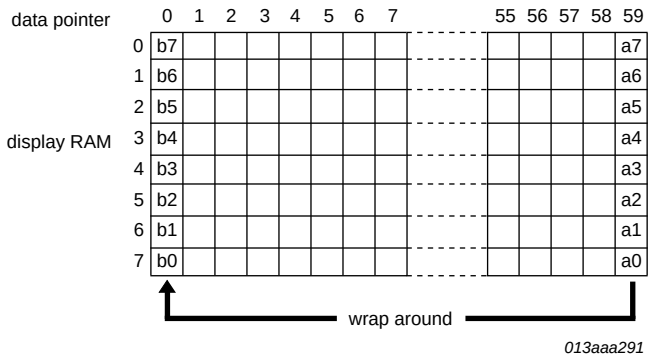


Fig 41. Data pointer wrap around in 1:8 multiplex drive mode

8.9.2 Bank selection

A RAM bank can be thought of as a collection of RAM rows. The PCA9620 includes a RAM bank switching feature in the static, 1:2, and 1:4 multiplex drive modes.

The RAM bank switching gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is complete. Input and output banks can be set independently from one another with the input-bank-select and the output-bank-select commands; Figure 42 shows the concept.

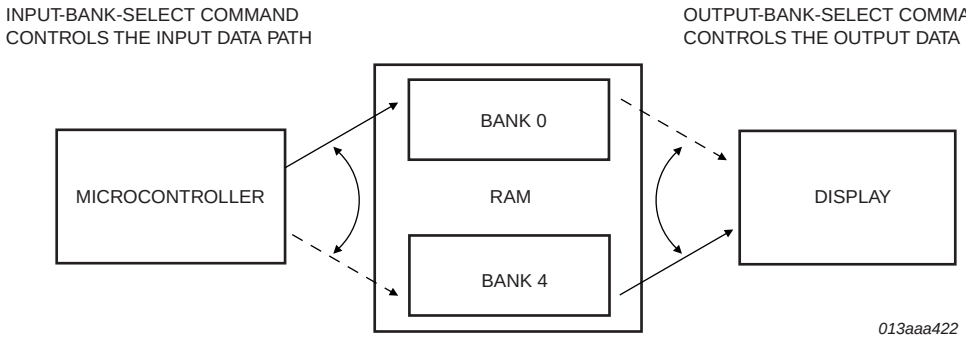


Fig 42. Example of bank selection in 1:4 multiplex mode

In Figure 42 an example is shown for 1:4 multiplex drive mode. The displayed data is read from the first four rows of the memory (bank 0), while the transmitted data is stored in the second four rows of the memory (bank 4) which is currently not accessed for the reading. Therefore different content can be loaded into the first and second four RAM rows which will be immediately displayed on the LCD by switching it with the output-bank-select command (see Figure 43).

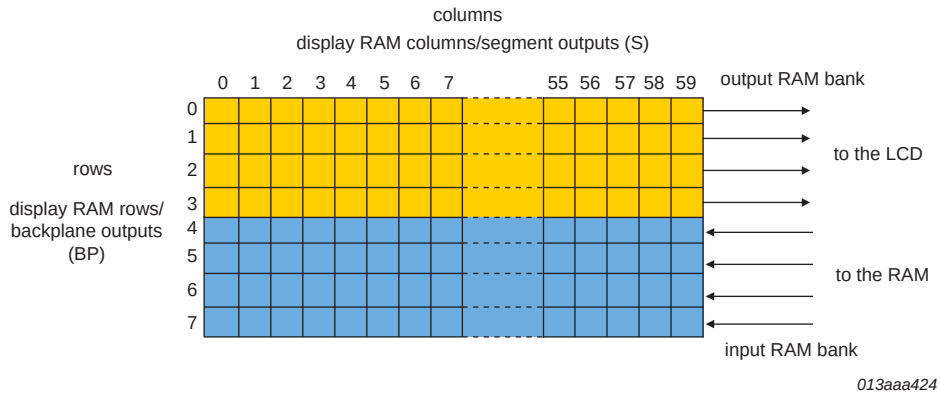


Fig 43. Example of the input-bank-select and the output-bank-select command with multiplex drive mode 1:4

8.9.2.1 Input-bank-select

The input-bank-select command (see Table 19 on page 12) loads display data into the display RAM in accordance with the selected LCD drive configuration.

- In static drive mode, an individual content can be stored in each RAM bank (bank 0 to bank 7 which corresponds to row 0 to row 7).
- In 1:2 multiplex drive mode, individual content for RAM bank 0 (row 0 and row 1), RAM bank 2 (row 2 and row 3), RAM bank 4 (row 4 and 5) and RAM bank 6 (row 6 and row 7) can be stored.
- In 1:4 multiplex drive mode individual content can be stored in RAM bank 0 (row 0 to row 3) and RAM bank 4 (row 4 to row 7).

The input-bank-select command works independently to the output-bank-select.

8.9.2.2 Output-bank-select

The output-bank-select command (see Table 20 on page 12) selects the display RAM transferring it to the display register in accordance with the selected LCD drive configuration.

- In the static drive mode, it is possible to request the content of RAM bank 1 (row 1) to RAM bank 7 (row 7) for display instead of the default RAM bank 0 (row 0).
- In 1:2 multiplex drive mode, the content of RAM bank 2 (row 2 and row 3) or of RAM bank 4 (row 4 and row 5) or of RAM bank 6 (row 6 and row 7) may be selected instead of the default RAM bank 0 (row 0 and row 1).
- In 1:4 multiplex drive mode, the content of RAM bank 4 (row 4, 5, 6, and 7) may be selected instead of RAM bank 0 (row 0, 1, 2, and 3).

The output-bank-select command works independently to the input-bank-select.

9. I²C-bus interface characteristics

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DAta line (SDA) and a Serial CLock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

9.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal (see Figure 44).

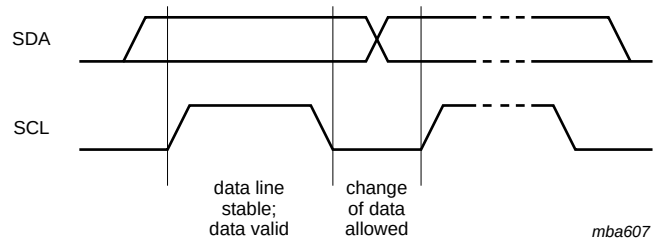


Fig 44. Bit transfer

9.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW change of the data line, while the clock is HIGH is defined as the START condition (S).

A LOW-to-HIGH change of the data line while the clock is HIGH is defined as the STOP condition (P).

The START and STOP conditions are shown in Figure 45.

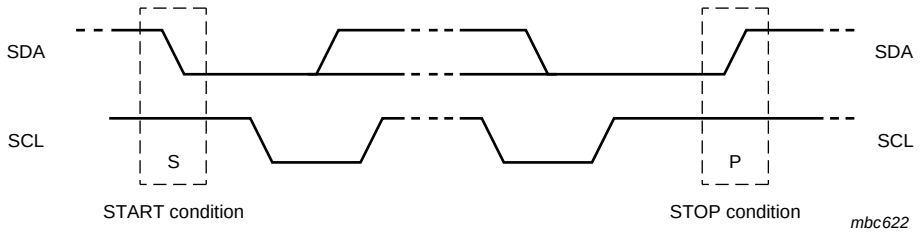


Fig 45. Definition of START and STOP conditions

9.3 System configuration

A device generating a message is a transmitter; a device receiving a message is the receiver. The device that controls the message is the master; and the devices which are controlled by the master are the slaves. The system configuration is shown in Figure 46.

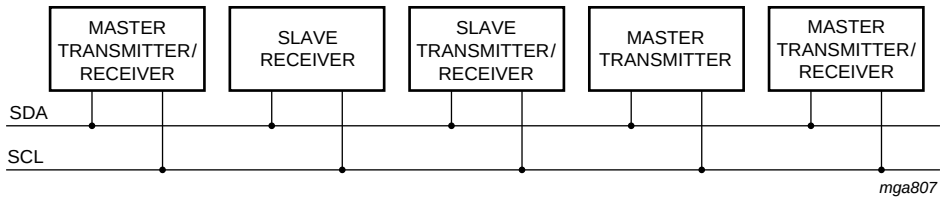


Fig 46. System configuration

9.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge cycle.

- A slave receiver which is addressed must generate an acknowledge after the reception of each byte.
- Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I^2C-bus is shown in Figure 47.

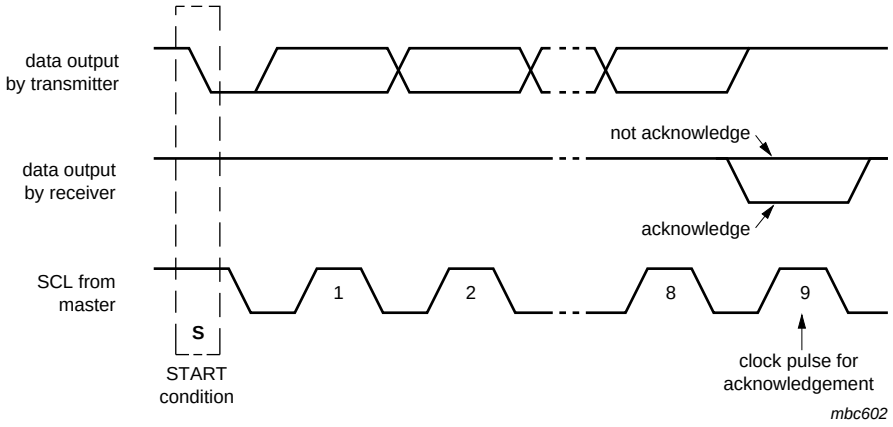


Fig 47. Acknowledgement on the I^2C-bus

9.5 I²C-bus controller

The PCA9620 acts as an I²C-bus slave receiver. It does not initiate I²C-bus transfers or transmit data to an I²C-bus master receiver. The only data output from PCA9620 are the acknowledge signals and the temperature readout byte of the selected device.

9.6 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

9.7 I²C-bus slave address

Device selection depends on the I²C-bus slave address.

Four different I²C-bus slave addresses can be used to address the PCA9620 (see Table 33).

Table 33. I²C slave address

Bit	Slave address							
	7 MSB	6	5	4	3	2	1	0 LSB
slave address	0	1	1	1	0	A1	A0	R/$\overline{W}$

The least significant bit of the slave address byte is bit R/$\overline{W}$. Bit 1 and bit 2 of the slave address are defined by connecting the inputs A0 and A1 to either V_{SS} (logic 0) or V_{DD} (logic 1). Therefore, four instances of PCA9620 can be distinguished on the same I²C-bus.

9.8 I²C-bus protocol

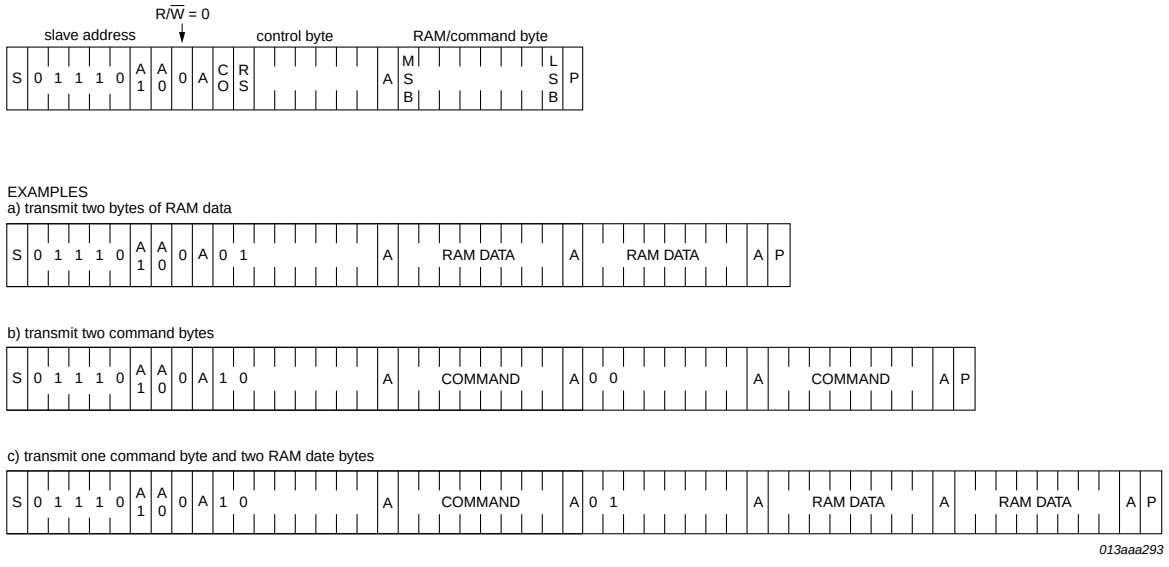


Fig 48. I²C-bus protocol write mode

The I²C-bus protocol is shown in Figure 48. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by one of the four PCA9620 slave addresses available. All PCA9620's with the corresponding A1 and A0 level acknowledge in parallel to the slave address, but all PCA9620 with the alternative A1 and A0 levels ignore the whole I²C-bus transfer.

After acknowledgement, a control byte follows which defines if the next byte is RAM or command information. The control byte also defines if the next byte is a control byte or further RAM or command data.

Table 34. Control byte description

Bit	Symbol	Value	Description
7	CO		**continue bit**
		0	last control byte
		1	control bytes continue
6	RS		**register selection**
		0	command register
		1	data register
5 to 0	-	-	not relevant

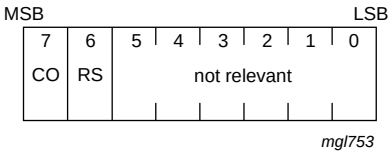


Fig 49. Control byte format

In this way it is possible to configure the device and then fill the display RAM with little overhead.

The display bytes are stored in the display RAM at the address specified by the data pointer.

The acknowledgement after each byte is made only by the (A0 and A1) addressed PCA9620. After the last display byte, the I²C-bus master issues a STOP condition (P). Alternatively a START may be issued to RESTART an I²C-bus access.

If a temperature readout (byte TD[7:0]) is made the R/$\overline{W}$ bit must be logic 1 and then the next data byte following is provided by the PCA9620 as shown in Figure 50.

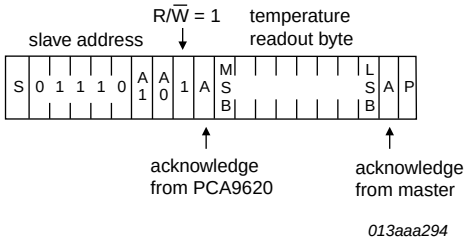


Fig 50. I²C-bus protocol read mode

10. Internal circuitry

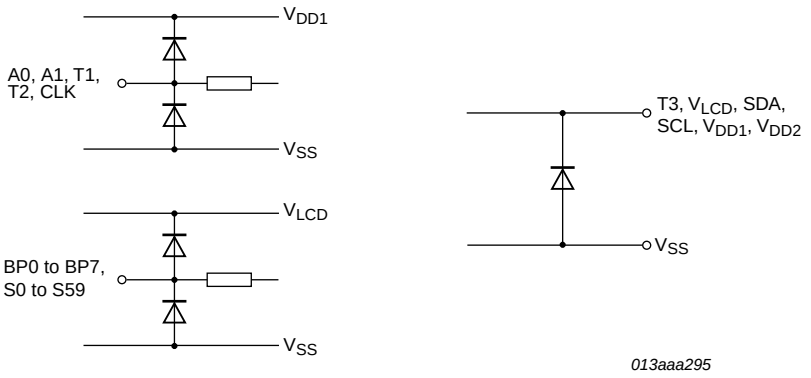


Fig 51. Device protection diagram

11. Safety notes

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

CAUTION

Static voltages across the liquid crystal display can build up when the LCD supply voltage (V_{LCD}) is on while the IC supply voltage (V_{DD}) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, V_{LCD} and V_{DD} must be applied or removed together.

CAUTION

Semiconductors are light sensitive. Exposure to light sources can cause the IC to malfunction. The IC must be protected against light. The protection must be applied to all sides of the IC.

12. Limiting values

Table 35. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD1}	supply voltage 1	analog and digital		–0.5	+6.5	V
V_{DD2}	supply voltage 2	charge pump		–0.5	+6.5	V
I_{DD1}	supply current 1	analog and digital		–50	+50	mA
I_{DD2}	supply current 2	charge pump		–50	+50	mA
V_{LCD}	LCD supply voltage			–0.5	+10	V
$I_{DD(LCD)}$	LCD supply current			–50	+50	mA
V_i	input voltage	on pins CLK, SDA, SCL, A0, A1, T1, T2, T3		–0.5	+6.5	V
I_I	input current			–10	+10	mA
V_O	output voltage	on pins S0 to S59, BP0 to BP7		–0.5	+10	V
		on pins SDA, CLK		–0.5	+6.5	V
I_O	output current			–10	+10	mA
I_{SS}	ground supply current			–50	+50	mA
P_{tot}	total power dissipation			-	400	mW
P/out	power dissipation per output			-	100	mW
V_{ESD}	electrostatic discharge voltage	HBM	[1]	-	±4000	V
		CDM	[2]	-	±1500	V
I_{lu}	latch-up current		[3]	-	100	mA
T_{stg}	storage temperature		[4]	–65	+150	°C
T_{amb}	ambient temperature	operating device		–40	+105	°C

[1] Pass level; Human Body Model (HBM), according to Ref. 8 “JESD22-A114”.

[2] Pass level; Charged-Device Model (CDM), according to Ref. 9 “JESD22-C101”.

[3] Pass level; latch-up testing according to Ref. 10 “JESD78” at maximum ambient temperature ($T_{amb(max)}$).

[4] According to the store and transport requirements (see Ref. 14 “UM10569”) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

13. Static characteristics

Table 36. Static characteristics

V_{DD1} = 2.5 V to 5.5 V; V_{DD2} = 2.5 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 9.0 V; T_{amb} = −40 °C to +105 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD1}	supply voltage 1			2.5	-	5.5	V
V_{DD2}	supply voltage 2	$V_{DD2} \geq V_{DD1}$		2.5	-	5.5	V
V_{LCD}	LCD supply voltage	$V_{LCD} \geq V_{DD2}$	[1]	2.5	-	9.0	V
ΔV_{LCD}	LCD voltage variation	$V_{DD1} = V_{DD2}$ = 5.0 V; V_{LCD} = 6.99 V	[2][3]	−0.10	-	+0.10	V
$I_{DD(pd)}$	power-down mode supply current	on pin V_{DD1}	[4][5]	-	1.0	3.0	µA
I_{DD1}	supply current 1		[5][6]	-	100	200	µA
I_{DD2}	supply current 2	f_{osc} = 9.6 kHz					
		charge pump off; external V_{LCD}	[5][6]	-	0.5	3.0	µA
		charge pump on; internal V_{LCD}	[5][7]	-	250	550	µA
$I_{DD(LCD)}$	LCD supply current	external V_{LCD}	[5][8]	-	125	250	µA
$I_{LCD(pd)}$	power-down LCD current	external V_{LCD}	[4][5]	-	12	35	µA
R_O	output resistance	of charge pump (driving capabilities)					
		charge pump set to 2 × V_{DD2}; I_{load} = 3 mA (on pin V_{LCD})	[9]	0.2	0.85	1.6	kΩ
		charge pump set to 3 × V_{DD2}; I_{load} = 2 mA (on pin V_{LCD})	[10]	2.0	3.2	4.5	kΩ
T_{acc}	temperature accuracy	readout temperature error; V_{DD1} = 5.0 V					
		T_{amb} = −40 °C to +105 °C		−6	-	+6	°C
		T_{amb} = 27 °C		−4	-	+4	°C
Logic							
V_I	input voltage			V_{SS} − 0.5	-	V_{DD} + 0.5	V
V_{IL}	LOW-level input voltage	on pins CLK, A1, A0		-	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage	on pins CLK, A1, A0		$0.7V_{DD}$	-	-	V
V_O	output voltage			−0.5	-	V_{DD} + 0.5	V
V_{OH}	HIGH-level output voltage	on pin CLK		$0.8V_{DD}$	-	-	V
V_{OL}	LOW-level output voltage	on pin CLK		-	-	$0.2V_{DD}$	V
I_{OH}	HIGH-level output current	output source current; V_{OH} = 4.6 V; V_{DD} = 5 V; on pin CLK		1	-	-	mA
I_{OL}	LOW-level output current	output sink current; V_{OL} = 0.4 V; V_{DD} = 5 V; on pin CLK		1	-	-	mA
V_{POR}	power-on reset voltage		[11]	-	-	1.6	V
I_L	leakage current	$V_i = V_{DD}$ or V_{SS}; on pins CLK, A1, A0, T1, T2, T3	[12]	-	0	-	µA

Table 36. Static characteristics *...continued*

V_{DD1} = 2.5 V to 5.5 V; V_{DD2} = 2.5 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 9.0 V; T_{amb} = −40 °C to +105 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I²C-bus; pins SDA and SCL							
V_I	input voltage			V_{SS} − 0.5	-	5.5	V
V_{IL}	LOW-level input voltage	pins SCL, SDA		-	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage	pins SCL, SDA		$0.7V_{DD}$	-	-	V
V_O	output voltage	pins SCL, SDA		−0.5	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 5 V; on pin SDA		3	-	-	mA
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	[12]	-	0	-	µA
LCD outputs							
ΔV_O	output voltage variation	on pins BP0 to BP7	[13]	−15	-	+15	mV
		on pins S0 to S59	[14]	−15	-	+15	mV
R_O	output resistance	V_{LCD} = 7 V; on pins BP0 to BP7	[15]	0.3	0.8	1.5	kΩ
		V_{LCD} = 7 V; on pins S0 to S59	[15]	0.6	1.5	3	kΩ

[1] When supplying external V_{LCD} it must be $V_{LCD} \geq V_{DD2}$. Also when using the internal charge pump to generate a certain V_{LCD}, VPR[7:0] must be set to a value that the voltage is higher than V_{DD2} (see Section 8.4.3 on page 33).

[2] Calibrated at testing stage. V_{LCD} temperature compensation is disabled.

[3] According to Equation 6 on page 33: $V_{LCD} = 133 \times 0.03 + 3 = 6.99$ V.

[4] Display is disabled; I²C-bus inactive; temperature measurement disabled.

[5] The typical value is defined at $V_{DD1} = V_{DD2}$ = 5.0 V, V_{LCD} = 7.0 V and 30 °C.

[6] Temperature measurement enabled; 1:8 multiplex drive mode; ¼ bias; display enabled; LCD outputs are open circuit; RAM is all written with logic 1; inputs at V_{SS} or V_{DD}; internal clock with the default prescale factor; I²C-bus inactive.

[7] V_{DD2} = 5.0 V; charge pump set to $2 \times V_{DD2}$; VPR[7:0] set for V_{LCD} = 7.0 V; 1:8 multiplex drive mode; ¼ bias; temperature measurement enabled; display enabled; LCD outputs are open circuit; RAM is all written with logic 1; inputs at V_{SS} or V_{DD}; external clock with 50 % duty factor; I²C-bus inactive.

[8] External supplied V_{LCD} = 7.0 V; 1:8 multiplex drive mode; ¼ bias; temperature measurement enabled; display enabled; LCD outputs are open circuit; RAM is all written with logic 1; inputs at V_{SS} or V_{DD}; external clock with 50 % duty factor; I²C-bus inactive.

[9] V_{DD2} = 5.0 V; charge pump set to $2 \times V_{DD2}$; VPR[7:0] set for V_{LCD} = 9.0 V; display disabled; CPF (see Table 23 on page 13) set logic 0.

[10] V_{DD2} = 4.0 V; charge pump set to $3 \times V_{DD2}$; VPR[7:0] set for V_{LCD} = 9.0 V; display disabled; CPF (see Table 23 on page 13) set logic 0.

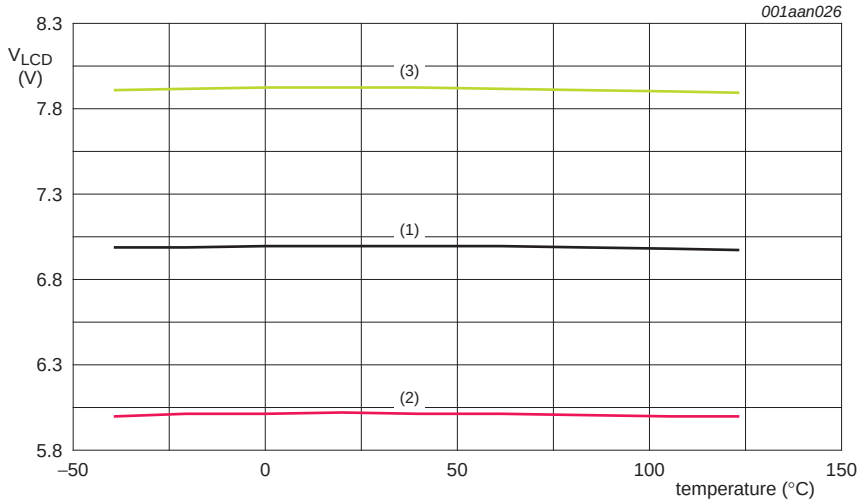
[11] If $V_{DD1} > V_{POR}$ then no reset occurs.

[12] In case of an ESD event, the value may increase slightly.

[13] Variation between any 2 backplanes on a given voltage level; static measured.

[14] Variation between any 2 segments on a given voltage level; static measured.

[15] Outputs measured one at a time.



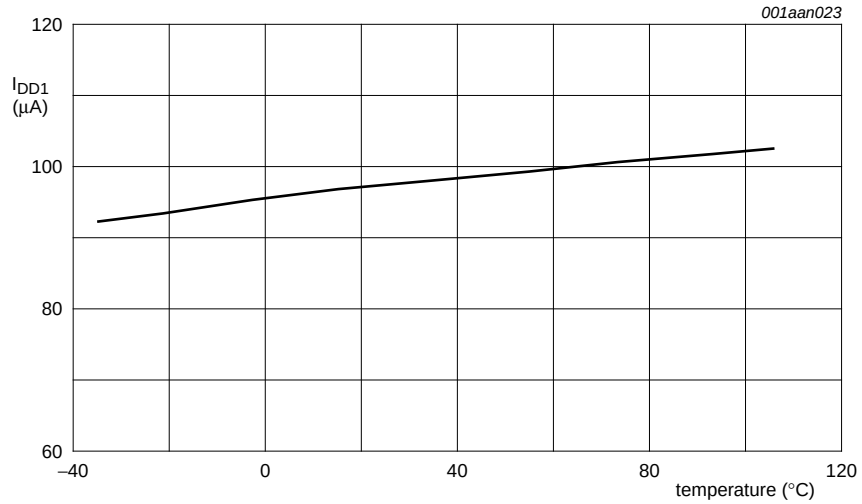
(1) VPR[7:0] = 85h.

(2) VPR[7:0] = 64h.

(3) VPR[7:0] = A4h.

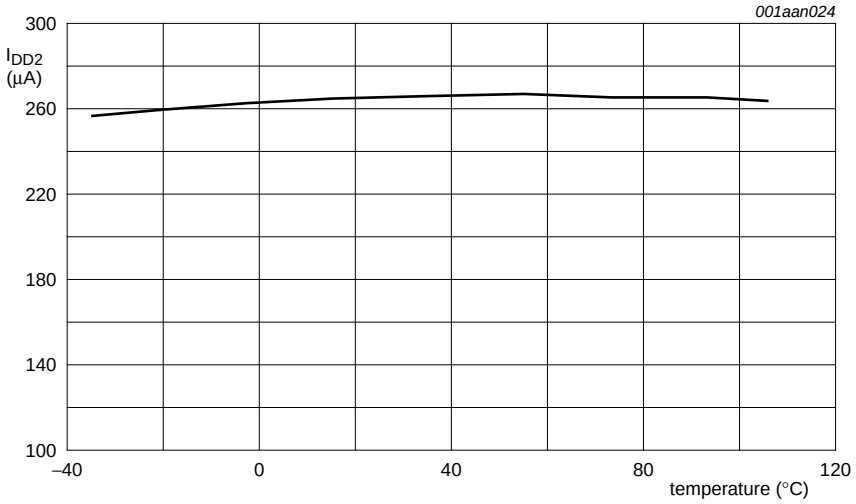
Temperature compensation disabled.

Fig 52. Typical V_{LCD} with respect to temperature



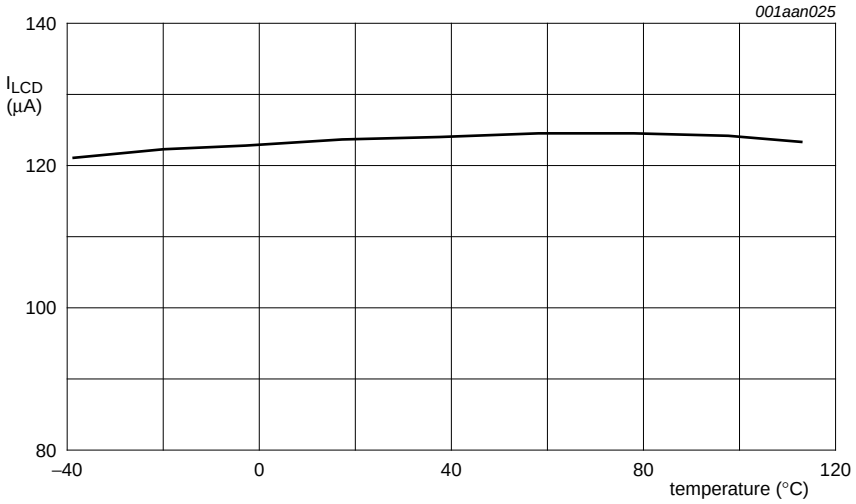
V_{DD1} = 5.0 V.

Fig 53. Typical I_{DD1} with respect to temperature



Charge pump set to 2 × V_{DD2}; V_{LCD} = 7.0 V; V_{DD1} = V_{DD2} = 5.0 V.

Fig 54. Typical I_{DD2} with respect to temperature



V_{LCD} = 7.0 V, external supplied; V_{DD1} = V_{DD2} = 5.0 V; display enabled, but no display attached.

Fig 55. Typical I_{LCD} with respect to temperature

14. Dynamic characteristics

Table 37. Dynamic characteristics

V_{DD1} = 2.5 V to 5.5 V; V_{DD2} = 2.5 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 9.0 V; T_{amb} = −40 °C to +105 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{osc}	oscillator frequency	on pin CLK; see Table 18 on page 11	[1][2]	8160	9600	11040	Hz
$f_{clk(ext)}$	external clock frequency			450	-	14500	Hz
$t_{clk(H)}$	HIGH-level clock time	external clock source used		33	-	-	µs
$t_{clk(L)}$	LOW-level clock time			33	-	-	µs
Timing characteristics: I²C-bus[3]							
f_{SCL}	SCL frequency			-	-	400	kHz
t_{BUF}	bus free time between a STOP and START condition			1.3	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition			0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			0.6	-	-	µs
$t_{VD;DAT}$	data valid time		[4]	-	-	0.9	µs
$t_{VD;ACK}$	data valid acknowledge time		[5]	-	-	0.9	µs
t_{LOW}	LOW period of the SCL clock			1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock			0.6	-	-	µs
t_f	fall time	of both SDA and SCL signals		-	-	0.3	µs
t_r	rise time	of both SDA and SCL signals		-	-	0.3	µs
C_b	capacitive load for each bus line			-	-	400	pF
$t_{SU;DAT}$	data set-up time			100	-	-	ns
$t_{HD;DAT}$	data hold time			0	-	-	ns
$t_{SU;STO}$	set-up time for STOP condition			0.6	-	-	µs
$t_{w(spike)}$	spike pulse width			-	-	50	ns

[1] Internal calibration made with OTP so that the maximum variation is ±15 % over whole temperature and voltage range. The typical f_{osc} generates a typical frame frequency of 200 Hz when the default frequency division factor is used (see Section 8.5.3 on page 41).

[2] The typical value is defined at V_{DD1} = V_{DD2} = 5.0 V and 30 °C.

[3] All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

[4] $t_{VD;DAT}$ = minimum time for valid SDA output following SCL LOW.

[5] $t_{VD;ACK}$ = time for acknowledgement signal from SCL LOW to SDA output LOW.

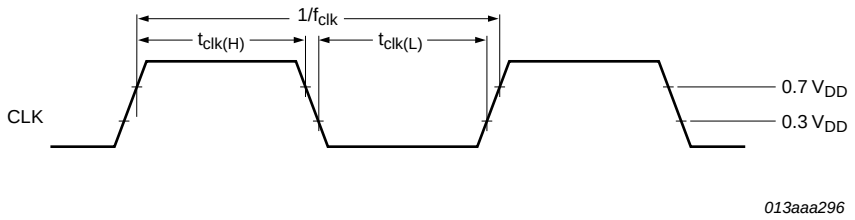


Fig 56. Driver timing waveforms

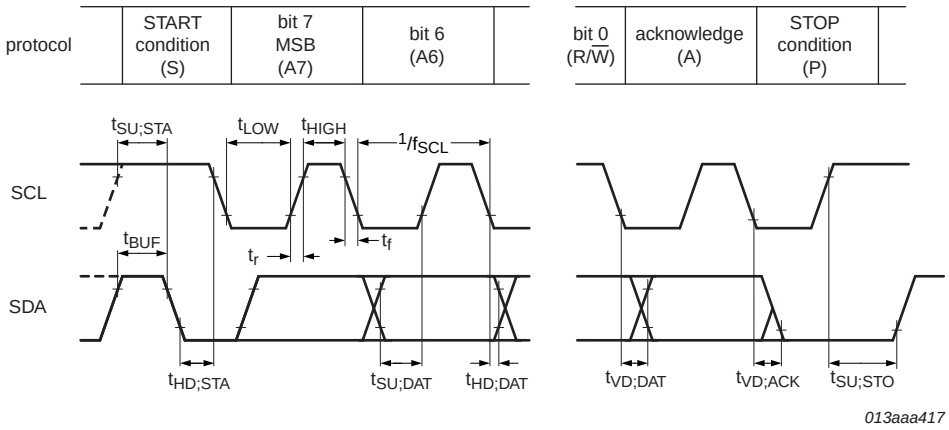


Fig 57. I²C-bus timing waveforms

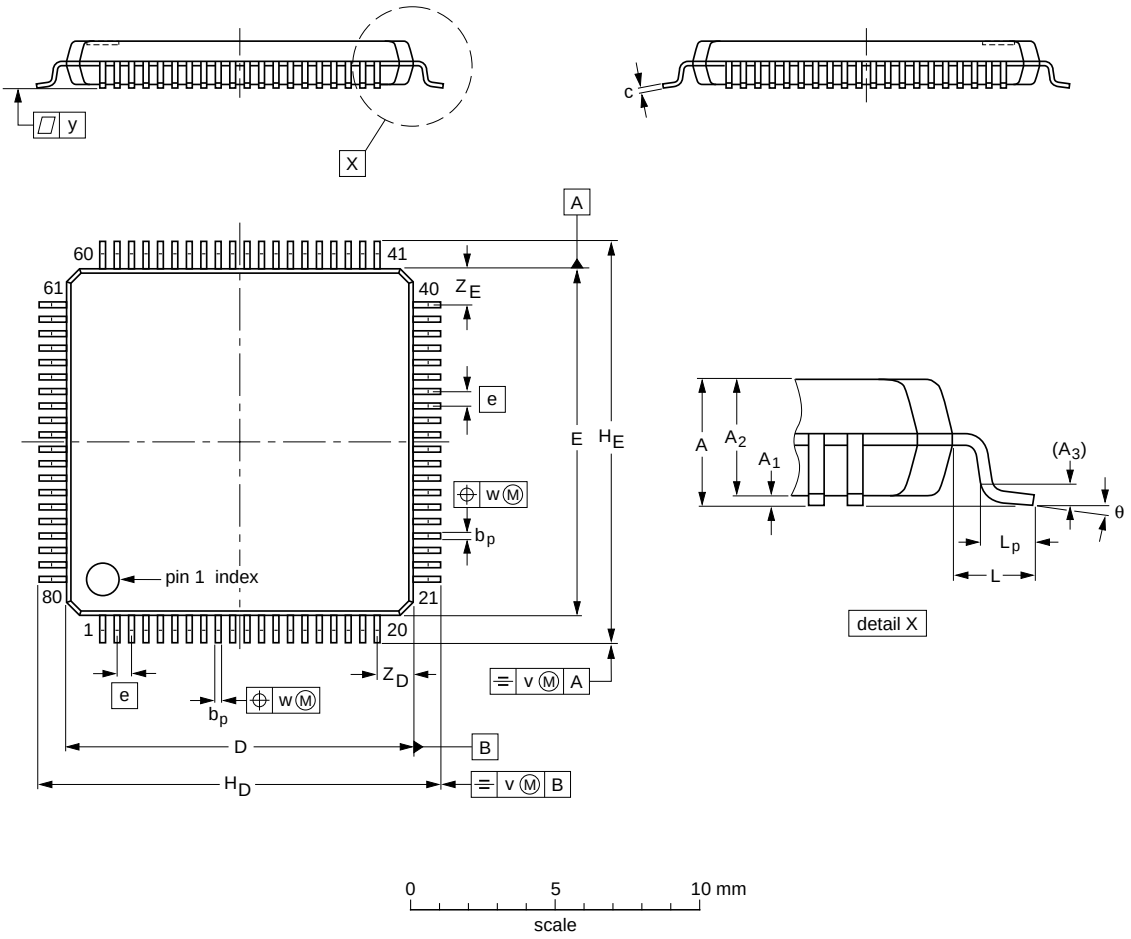
15. Test information

15.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

16. Package outline

LQFP80: plastic low profile quad flat package; 80 leads; body 12 x 12 x 1.4 mm **SOT315-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.16 0.04	1.5 1.3	0.25	0.27 0.13	0.18 0.12	12.1 11.9	12.1 11.9	0.5	14.15 13.85	14.15 13.85	1	0.75 0.30	0.2	0.15	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

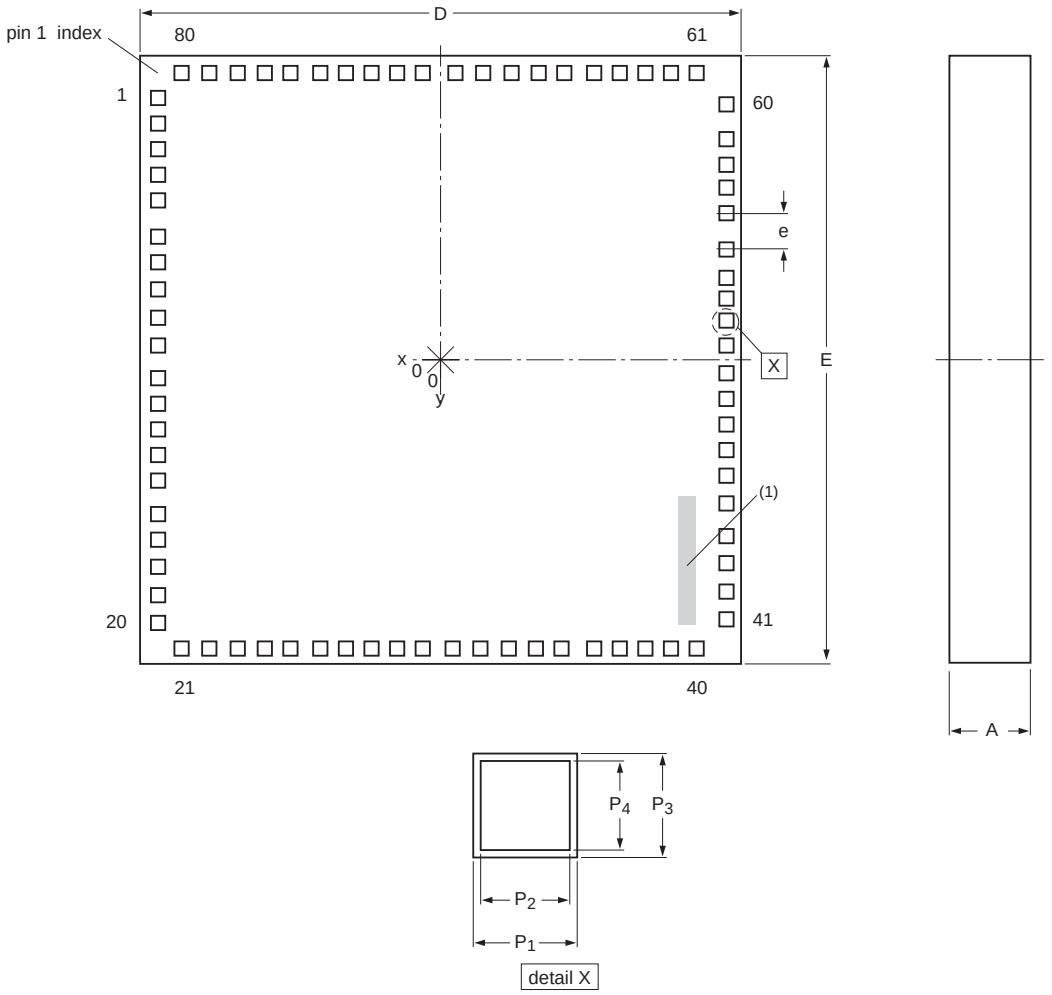
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT315-1	136E15	MS-026				~~00-01-19~~ 03-02-25

Fig 58. Package outline SOT315-1 (LQFP80)

17. Bare die outline

Bare die; 80 bonding pads **PCA9620U**



Notes
1. Marking code: PC9620-1

pca9620u_do

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PCA9620U						~~11-09-15~~ 11-09-26

Fig 59. Bare die outline of PCA9620

Table 38. Dimensions of PCA9620

Original dimensions are in mm.

Unit (mm)	A	D[1]	E[1]	e[2]	P_1[3]	P_2[4]	P_3[3]	P_4[4]
max	-	-	-	0.203	-	-	-	-
nom	0.38	3.166	3.166	-	0.065	0.056	0.065	0.056
min	-	-	-	0.075	-	-	-	-

[1] Dimension includes saw lane (70 μm).

[2] See Table 39.

[3] P_1 and P_3: pad size.

[4] P_2 and P_4: passivation opening.

Table 39. Bonding pad description of PCA9620

All x/y coordinates represent the position of the center of each pad with respect to the center (x/y = 0) of the chip; see Figure 59.

Symbol	Pad	Location		Pitch		Description
		X(μm)	Y(μm)	X(μm)	Y(μm)	
S20	1	−1497.3	1208.7	-	-	LCD segment output
S21	2	−1497.3	1086.3	0	122.4	
S22	3	−1497.3	963.9	0	122.4	
S23	4	−1497.3	841.5	0	122.4	
S24	5	−1497.3	719.1	0	122.4	
S25	6	−1497.3	568.8	0	150.3	
S26	7	−1497.3	446.4	0	122.4	
S27	8	−1497.3	324.0	0	122.4	
S28	9	−1497.3	201.6	0	122.4	
S29	10	−1497.3	79.2	0	150.3	
S30	11	−1497.3	−71.1	0	122.4	
S31	12	−1497.3	−193.5	0	122.4	
S32	13	−1497.3	−315.9	0	122.4	
S33	14	−1497.3	−438.3	0	122.4	
S34	15	−1497.3	−560.7	0	122.4	
S35	16	−1497.3	−711.0	0	122.4	
S36	17	−1497.3	−833.4	0	122.4	
S37	18	−1497.3	−955.8	0	122.4	
S38	19	−1497.3	−1078.2	0	122.4	
S39	20	−1497.3	−1200.6	0	122.4	
S40	21	−1204.2	−1497.3	-	-	
S41	22	−1081.8	−1497.3	122.4	0	
S42	23	−959.4	−1497.3	122.4	0	
S43	24	−837.0	−1497.3	122.4	0	
S44	25	−714.6	−1497.3	122.4	0	
S45	26	−564.3	−1497.3	150.3	0	
S46	27	−441.9	−1497.3	122.4	0	

Table 39. Bonding pad description of PCA9620 *…continued*

All x/y coordinates represent the position of the center of each pad with respect to the center (x/y = 0) of the chip; see Figure 59.

Symbol	Pad	Location		Pitch		Description
		X(µm)	Y(µm)	X(µm)	Y(µm)	
S47	28	−319.5	−1497.3	122.4	0	LCD segment output
S48	29	−197.1	−1497.3	122.4	0	
S49	30	−74.7	−1497.3	122.4	0	
S50	31	75.6	−1497.3	150.3	0	
S51	32	198.0	−1497.3	122.4	0	
S52	33	320.4	−1497.3	122.4	0	
S53	34	442.8	−1497.3	122.4	0	
S54	35	565.2	−1497.3	122.4	0	
S55	36	715.5	−1497.3	150.3	0	
S56	37	837.9	−1497.3	122.4	0	
S57	38	960.3	−1497.3	122.4	0	
S58	39	1082.7	−1497.3	122.4	0	
S59	40	1205.1	−1497.3	122.4	0	
BP0	41	1497.3	−1201.5	-	-	LCD backplane output
BP1	42	1497.3	−1077.3	0	124.2	
BP2	43	1497.3	−953.1	0	124.2	
BP3	44	1497.3	−828.9	0	124.2	
BP4	45	1497.3	−676.8	0	152.1	
BP5	46	1497.3	−552.6	0	124.2	
BP6	47	1497.3	−428.4	0	124.2	
BP7	48	1497.3	−304.2	0	124.2	
V_{LCD}	49	1497.3	−171.9	0	132.3	LCD supply voltage
V_{DD2}	50	1497.3	−47.7	0	124.2	supply voltage 2 (charge pump)
V_{DD1}	51	1497.3	76.5	0	124.2	supply voltage 1 (analog and digital)
V_{SS}	52	1497.3	166.5	0	90	ground supply voltage
T1	53	1497.3	241.2	0	74.7	test pin
T2	54	1497.3	315.9	0	74.7	
T3	55	1497.3	430.2	0	114.3	
CLK	56	1497.3	620.1	0	189.9	internal oscillator output, external oscillator input
A0	57	1497.3	729.9	0	109.8	I^2C-bus slave address selection bit
A1	58	1497.3	806.4	0	76.5	
SCL	59	1497.3	913.5	0	107.1	I^2C-bus serial clock
SDA	60	1497.3	1116.9	0	203.4	I^2C-bus serial data
S0	61	1205.1	1497.3	-	-	LCD segment output
S1	62	1082.7	1497.3	122.4	0	
S2	63	960.3	1497.3	122.4	0	
S3	64	837.9	1497.3	122.4	0	
S4	65	715.5	1497.3	122.4	0	

Table 39. Bonding pad description of PCA9620 *…continued*

All x/y coordinates represent the position of the center of each pad with respect to the center (x/y = 0) of the chip; see Figure 59.

Symbol	Pad	Location		Pitch		Description
		X(µm)	Y(µm)	X(µm)	Y(µm)	
S5	66	565.2	1497.3	150.3	0	LCD segment output
S6	67	442.8	1497.3	122.4	0	
S7	68	320.4	1497.3	122.4	0	
S8	69	198.0	1497.3	122.4	0	
S9	70	75.6	1497.3	122.4	0	
S10	71	−74.7	1497.3	150.3	0	
S11	72	−197.1	1497.3	122.4	0	
S12	73	−319.5	1497.3	122.4	0	
S13	74	−441.9	1497.3	122.4	0	
S14	75	−564.3	1497.3	122.4	0	
S15	76	−714.6	1497.3	150.3	0	
S16	77	−837.0	1497.3	122.4	0	
S17	78	−959.4	1497.3	122.4	0	
S18	79	−1081.8	1497.3	122.4	0	
S19	80	−1204.2	1497.3	122.4	0	

Table 40. Alignment mark dimension and location of all PCA9620 types

Coordinates	
X (µm)	Y (µm)
Location[1]	
1495.8	1395.0
Dimension[2]	
52.5	63.72

[1] The x/y coordinates of the alignment mark location represent the position of the REF point (see Figure 60) with respect to the center (x/y = 0) of the chip; see Figure 59.

[2] The x/y values of the dimensions represent the extensions of the alignment mark in direction of the coordinate axis (see Figure 60).

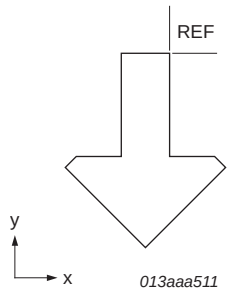
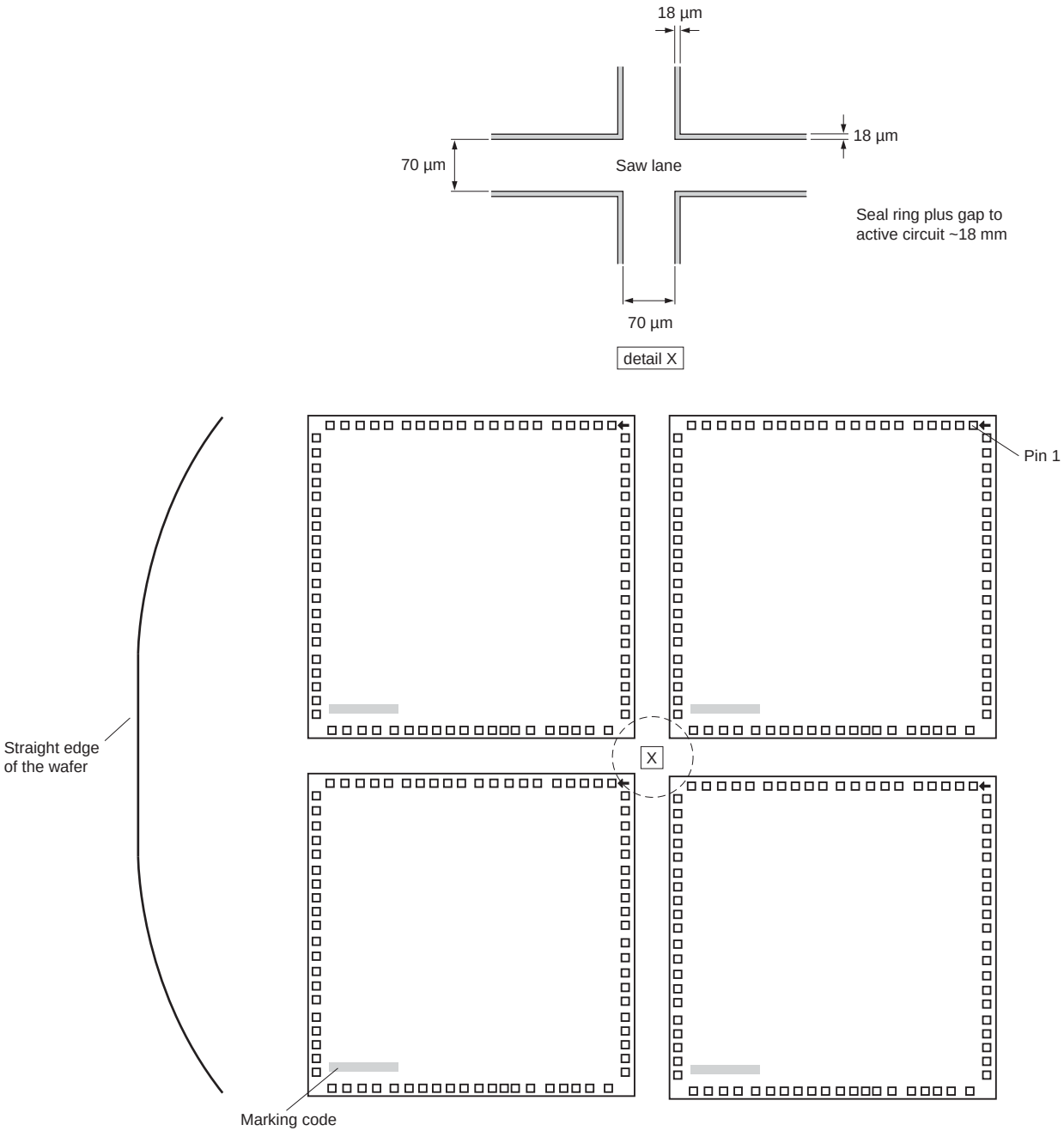


Fig 60. Alignment mark

18. Packing information

18.1 Wafer information



Wafer thickness, see Table 41.

Fig 61. Wafer layout of PCA9620

Table 41. PCA9620 wafer information

Type number	Wafer thickness	Wafer diameter	Marking of bad die
PCA9620/5GA/Q1	0.687 mm	6 inch	wafer mapping

19. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

19.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

19.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

19.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

19.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 62) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 42 and 43

Table 42. SnPb eutectic process (from J-STD-020D)

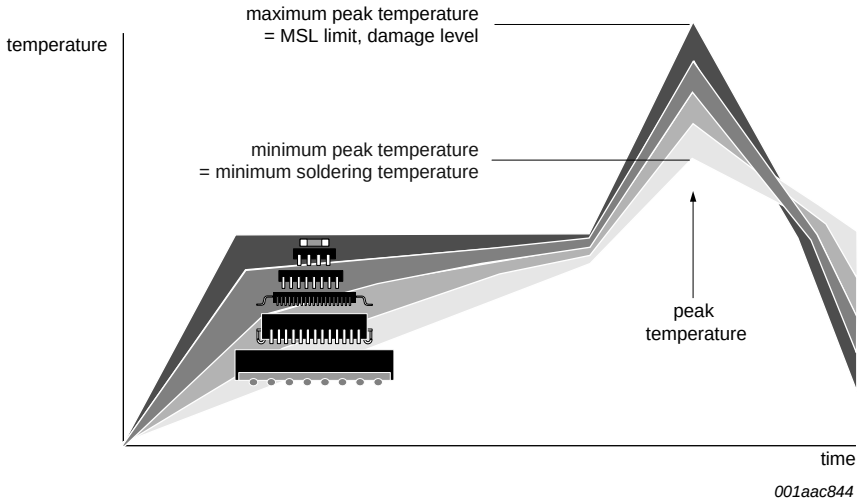
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 43. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 62.



MSL: Moisture Sensitivity Level

Fig 62. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

20. Abbreviations

Table 44. Abbreviations

Acronym	Description
AEC	Automotive Electronics Council
CDM	Charged-Device Model
DC	Direct Current
EPROM	Erasable Programmable Read-Only Memory
ESD	ElectroStatic Discharge
HBM	Human Body Model
I^2C	Inter-Integrated Circuit bus
IC	Integrated Circuit
LCD	Liquid Crystal Display
LSB	Least Significant Bit
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
MUX	Multiplexer
OTP	One Time Programmable
PCB	Printed-Circuit Board
POR	Power-On Reset
RC	Resistance-Capacitance
RAM	Random Access Memory
RMS	Root Mean Square
SCL	Serial CLock line
SDA	Serial DAta line
SMD	Surface Mount Device

21. References

[1] **AN10365 —** Surface mount reflow soldering description

[2] **AN10706 —** Handling bare die

[3] **AN10853 —** ESD and EMC sensitivity of IC

[4] **AN11267 —** EMC and system level ESD design guidelines for LCD drivers

[5] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[6] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[7] **IPC/JEDEC J-STD-020D —** Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

[8] **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[9] **JESD22-C101 —** Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components

[10] **JESD78 —** IC Latch-Up Test

[11] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[12] **SNV-FA-01-02 —** Marking Formats Integrated Circuits

[13] **UM10204 —** I^2C-bus specification and user manual

[14] **UM10569 —** Store and transport requirements

22. Revision history

Table 45. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9620 v.3	20130703	Product data sheet	-	PCA9620 v.2
Modifications:	• Changed ΔV_{LCD} specification (Table 36)			
PCA9620 v.2	20111108	Product data sheet	-	PCA9620 v.1
PCA9620 v.1	20101209	Product data sheet	-	-

23. Legal information

23.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 3 July 2013
Document identifier: PCA9620