TJF1051

High-speed CAN transceiver

Rev. 3 — 8 February 2013 Product data sheet

1. General description

The TJF1051 is a high-speed CAN transceiver that provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The transceiver is designed for high-speed (up to 1 Mbit/s) CAN industrial applications, providing differential transmit and receive capability to (a microcontroller with) a CAN protocol controller.

The TJF1051 belongs to the third generation of high-speed CAN transceivers from NXP Semiconductors, offering significant improvements over first- and second-generation devices such as the TJA1050. It offers improved ElectroMagnetic Compatibility (EMC) and ElectroStatic Discharge (ESD) performance, and also features ideal passive behavior to the CAN bus when the supply voltage is off.

The TJF1051T/3 can be interfaced directly to microcontrollers with supply voltages from 3 V to 5 V

These features make the TJF1051 an excellent choice for all types of HS-CAN networks, in nodes that do not require a standby mode with wake-up capability via the bus.

2. Features and benefits

2.1 General

- Fully ISO 11898-2 compliant
- Low ElectroMagnetic Emission (EME) and high ElectroMagnetic Immunity (EMI)
- V_{IO} input on the TJF1051T/3 allows for direct interfacing with 3 V to 5 V microcontrollers

2.2 Low-power management

- Functional behavior predictable under all supply conditions
- Transceiver disengages from the bus when not powered up (zero load)

2.3 Protection

- High ESD handling capability on the bus pins
- Transmit Data (TXD) dominant time-out function
- Undervoltage detection on pins V_{CC} and V_{IO}
- Thermally protected

3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
$V_{uvd(VCC)}$	undervoltage detection voltage on pin V_{CC}		3.5	-	4.5	V
I_{CC}	supply current	Silent mode	0.1	1	2.5	mA
		Normal mode; bus recessive	2.5	5	10	mA
		Normal mode; bus dominant	20	50	70	mA
V_{ESD}	electrostatic discharge voltage	HBM on pins CANH and CANL	−8	-	+8	kV
V_{CANH}	voltage on pin CANH	no time limit; DC limiting value	−58	-	+58	V
V_{CANL}	voltage on pin CANL	no time limit; DC limiting value	−58	-	+58	V

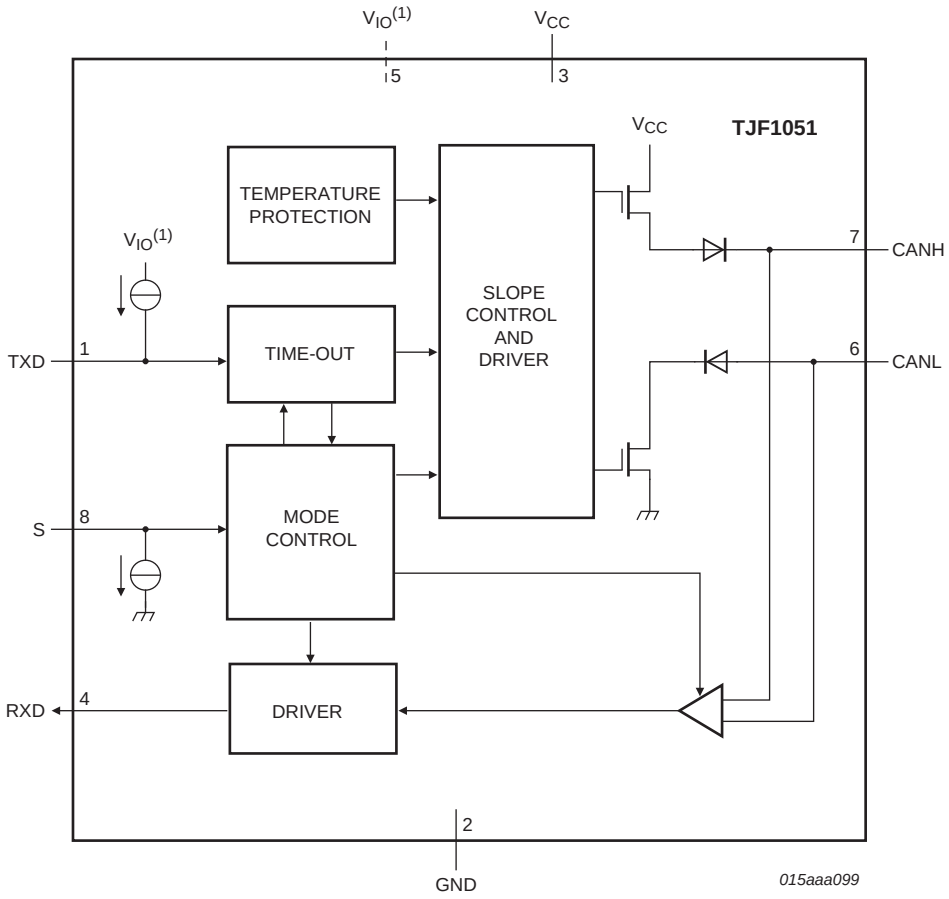
4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TJF1051T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
TJF1051T/3[1]	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

[1] TJF1051T/3 with V_{IO} pin.

5. Block diagram

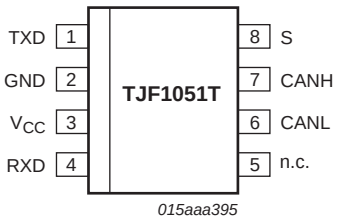


(1) In the TJF1051T, the V_{IO} input is connected internally to V_{CC}.

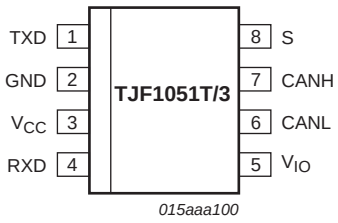
Fig 1. Block diagram

6. Pinning information

6.1 Pinning



a. TJF1051T



b. TJF1051T/3

Fig 2. Pin configuration diagrams

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
TXD	1	transmit data input
GND	2	ground
V_{CC}	3	supply voltage
RXD	4	receive data output; reads out data from the bus lines
n.c.	5	not connected; in TJF1051T
V_{IO}	5	supply voltage for I/O level adapter; TJF1051T/3 only
CANL	6	LOW-level CAN bus line
CANH	7	HIGH-level CAN bus line
S	8	Silent mode control input

7. Functional description

The TJF1051 is a stand-alone high-speed CAN transceiver with Silent mode. It combines the functionality of the TJA1050 transceiver with improved EMC and ESD handling capability. Improved slope control and high DC handling capability on the bus pins provides additional application flexibility. The TJF1051T/3 allows for direct interfacing to microcontrollers with supply voltages down to 3 V.

7.1 Operating modes

The TJF1051 supports two operating modes, Normal and Silent. The operating mode is selected via pin S. See Table 4 for a description of the operating modes under normal supply conditions.

Table 4. Operating modes

Mode	Inputs		Outputs	
	Pin S	Pin TXD	CAN driver	Pin RXD
Normal	LOW	LOW	dominant	active[1]
	LOW	HIGH	recessive	active[1]
Silent	HIGH	X[2]	recessive	active[1]

[1] LOW if the CAN bus is dominant, HIGH if the CAN bus is recessive.

[2] X = don't care.

7.1.1 Normal mode

A LOW level on pin S selects Normal mode. In this mode, the transceiver is able to transmit and receive data via bus lines CANH and CANL (see Figure 1 for the block diagram). The differential receiver converts the analog data on the bus lines into digital data which is output to pin RXD. The slope of the output signals on the bus lines is controlled and optimized in a way that guarantees the lowest possible EME levels.

7.1.2 Silent mode

A HIGH level on pin S selects Silent mode. In Silent mode the transmitter is disabled, releasing the bus pins to recessive state. All other IC functions, including the receiver, continue to operate as in Normal mode. Silent mode can be used to prevent a faulty CAN controller from disrupting all network communications.

7.2 Fail-safe features

7.2.1 TXD dominant time-out function

A ‘TXD dominant time-out’ timer is started when pin TXD is set LOW. If the LOW state on pin TXD persists for longer than $t_{to(dom)TXD}$, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD is set HIGH. The TXD dominant time-out time also defines the minimum possible bit rate of 40 kbit/s.

7.2.2 Internal biasing of TXD and S input pins

Pin TXD has an internal pull-up to V_{IO} and pin S has an internal pull-down to GND. This ensures a safe, defined state in case one (or both) of these pins is left floating.

7.2.3 Undervoltage detection on pins V_{CC} and V_{IO}

Should V_{CC} or V_{IO} drop below their respective undervoltage detection levels ($V_{uvd(VCC)}$ and $V_{uvd\ (VIO)}$; see Table 7), the transceiver will switch off and disengage from the bus (zero load) until V_{CC} and V_{IO} have recovered.

7.2.4 Overtemperature protection

The output drivers are protected against overtemperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature, $T_{j(sd)}$, the output drivers will be disabled until the virtual junction temperature falls below $T_{j(sd)}$ and TXD becomes recessive again. Including the TXD condition ensures that output driver oscillations due to temperature drift are avoided.

7.3 V_{IO} supply pin (TJF1051T/3)

Pin V_{IO} on the TJF1051T/3 should be connected to the microcontroller supply voltage (see Figure 5). This adjusts the signal levels on pins TXD, RXD and S to the I/O levels of the microcontroller. In the TJF1051T, the V_{IO} input is internally connected to V_{CC}. This sets the signal levels of pins TXD, RXD and S to levels compatible with 5 V microcontrollers.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_x	voltage on pin x	no time limit; DC value			
		on pins CANH and CANL	−58	+58	V
		on any other pin	−0.3	+7	V
V_{ESD}	electrostatic discharge voltage	HBM [1]			
		pins CANH and CANL	−8	+8	kV
		any other pin	−4	+4	kV
		MM [2]			
		any pin	−300	+300	V
T_{vj}	virtual junction temperature	[3]	−40	+125	°C
T_{stg}	storage temperature		−55	+150	°C

[1] Human Body Model (HBM): 100 pF, 1.5 kΩ.

[2] Machine Model (MM): 200 pF, 0.75 μH, 10 Ω.

[3] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \times R_{th(vj-a)}$, where $R_{th(vj-a)}$ is a fixed value to be used for the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

9. Thermal characteristics

Table 6. Thermal characteristics

According to IEC 60747-1.

Symbol	Parameter	Conditions	Value	Unit
$R_{th(vj-a)}$	thermal resistance from virtual junction to ambient	in free air	120	K/W

10. Static characteristics

Table 7. Static characteristics

T_{amb} = −40 °C to +105 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.8 V to 5.5 V[1]; R_L = 60 Ω; unless otherwise specified; all voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply; pin V_{CC}						
V_{CC}	supply voltage		4.5	-	5.5	V
I_{CC}	supply current	Silent mode	0.1	1	2.5	mA
		Normal mode				
		recessive	2.5	5	10	mA
		dominant; V_{TXD} = 0 V	20	50	70	mA
$V_{uvd(VCC)}$	undervoltage detection voltage on pin V_{CC}		3.5	-	4.5	V
I/O level adapter supply; pin V_{IO}[1]						
V_{IO}	supply voltage on pin V_{IO}		2.8	-	5.5	V
I_{IO}	supply current on pin V_{IO}	Normal and Silent modes				
		recessive; V_{TXD} = V_{IO}	10	80	250	µA
		dominant; V_{TXD} = 0 V	50	350	500	µA
$V_{uvd(VIO)}$	undervoltage detection voltage on pin V_{IO}		1.3	-	2.7	V
Mode control input; pin S						
V_{IH}	HIGH-level input voltage		0.7V_{IO}	-	V_{IO} + 0.3	V
V_{IL}	LOW-level input voltage		−0.3	-	+0.3V_{IO}	V
I_{IH}	HIGH-level input current		1	4	10	µA
I_{IL}	LOW-level input current	V_S = 0 V	−1	0	+1	µA
CAN transmit data input; pin TXD						
V_{IH}	HIGH-level input voltage		0.7V_{IO}	-	V_{IO} + 0.3	V
V_{IL}	LOW-level input voltage		−0.3	-	+0.3V_{IO}	V
I_{IH}	HIGH-level input current	V_{TXD} = V_{IO}	−5	0	+5	µA
I_{IL}	LOW-level input current	Normal mode; V_{TXD} = 0 V	−260	−150	−30	µA
C_i	input capacitance		-	5	10	pF
CAN receive data output; pin RXD						
I_{OH}	HIGH-level output current	V_{RXD} = V_{IO} − 0.4 V	−8	−3	−1	mA
I_{OL}	LOW-level output current	V_{RXD} = 0.4 V; bus dominant	2	5	12	mA
Bus lines; pins CANH and CANL						
$V_{O(dom)}$	dominant output voltage	V_{TXD} = 0 V; t < $t_{to(dom)TXD}$				
		pin CANH	2.75	3.5	4.5	V
		pin CANL	0.5	1.5	2.25	V
$V_{dom(TX)sym}$	transmitter dominant voltage symmetry	$V_{dom(TX)sym}$ = V_{CC} − V_{CANH} − V_{CANL}	−400	0	+400	mV
$V_{O(dif)bus}$	bus differential output voltage	V_{TXD} = 0 V; t < $t_{to(dom)TXD}$	1.5	-	3	V
		V_{TXD} = V_{IO}; recessive; no load	−50	-	+50	mV

Table 7. Static characteristics *...continued*

T_{amb} = −40 °C to +105 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.8 V to 5.5 V[1]; R_L = 60 Ω; unless otherwise specified; all voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{O(rec)}$	recessive output voltage	Normal and Silent modes; $V_{TXD} = V_{IO}$; no load	2	$0.5V_{CC}$	3	V
$V_{th(RX)dif}$	differential receiver threshold voltage	Normal and Silent modes $V_{cm(CAN)}$[2] = −12 V to +12 V	0.5	0.7	0.9	V
$V_{hys(RX)dif}$	differential receiver hysteresis voltage	Normal and Silent modes $V_{cm(CAN)}$ = −12 V to +12 V	50	120	400	mV
$I_{O(dom)}$	dominant output current	V_{TXD} = 0 V; t < $t_{to(dom)TXD}$; V_{CC} = 5 V				
		pin CANH; V_{CANH} = 0 V	−120	−70	−40	mA
		pin CANL; V_{CANL} = 5 V/40 V	40	70	120	mA
$I_{O(rec)}$	recessive output current	Normal and Silent modes; $V_{TXD} = V_{CC}$; $V_{CANH} = V_{CANL}$ = −27 V to +32 V	−5	-	+5	mA
I_L	leakage current	V_{CC} = 0 V; $V_{CANH} = V_{CANL}$ = 5 V	−5	0	+5	µA
R_i	input resistance		9	15	28	kΩ
ΔR_i	input resistance deviation	between V_{CANH} and V_{CANL}	−3	0	+3	%
$R_{i(dif)}$	differential input resistance		19	30	52	kΩ
$C_{i(cm)}$	common-mode input capacitance		-	-	20	pF
$C_{i(dif)}$	differential input capacitance		-	-	10	pF
Temperature protection						
$T_{j(sd)}$	shutdown junction temperature		-	190	-	°C

[1] Only the TJF1051T/3 has a V_{IO} pin; in the TJF1051T, the V_{IO} input is internally connected to V_{CC}.

[2] $V_{cm(CAN)}$ is the common mode voltage of CANH and CANL.

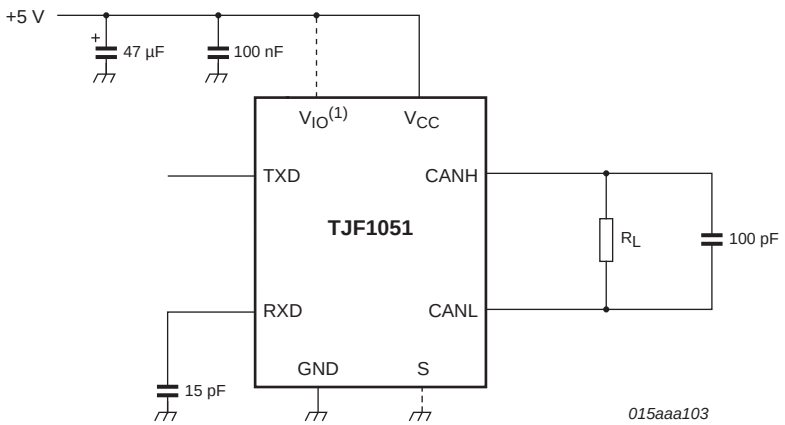
11. Dynamic characteristics

Table 8. Dynamic characteristics

T_{amb} = −40 °C to +105 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.8 V to 5.5 V[1]; R_L = 60 Ω unless specified otherwise. All voltages are defined with respect to ground. Positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Transceiver timing; pins CANH, CANL, TXD and RXD; see Figure 3 and Figure 4						
$t_{d(TXD-busdom)}$	delay time from TXD to bus dominant	Normal mode	-	65	-	ns
$t_{d(TXD-busrec)}$	delay time from TXD to bus recessive	Normal mode	-	90	-	ns
$t_{d(busdom-RXD)}$	delay time from bus dominant to RXD	Normal and Silent modes	-	60	-	ns
$t_{d(busrec-RXD)}$	delay time from bus recessive to RXD	Normal and Silent modes	-	65	-	ns
$t_{PD(TXD-RXD)}$	propagation delay from TXD to RXD	2.8 V < V_{IO} < 4.5 V Normal mode	40	-	250	ns
		4.5 V > V_{CC} = V_{IO} < 5.5 V Normal mode	40	-	220	ns
$t_{to(dom)TXD}$	TXD dominant time-out time	V_{TXD} = 0 V; Normal mode	0.3	1	12	ms

[1] Only the TJF1051T/3 has a V_{IO} pin. In the TJF1051T, the V_{IO} input is internally connected to V_{CC}.



(1) In the TJF1051T/3, pin V_{IO} connected V_{CC}.

Fig 3. Timing test circuit for CAN transceiver

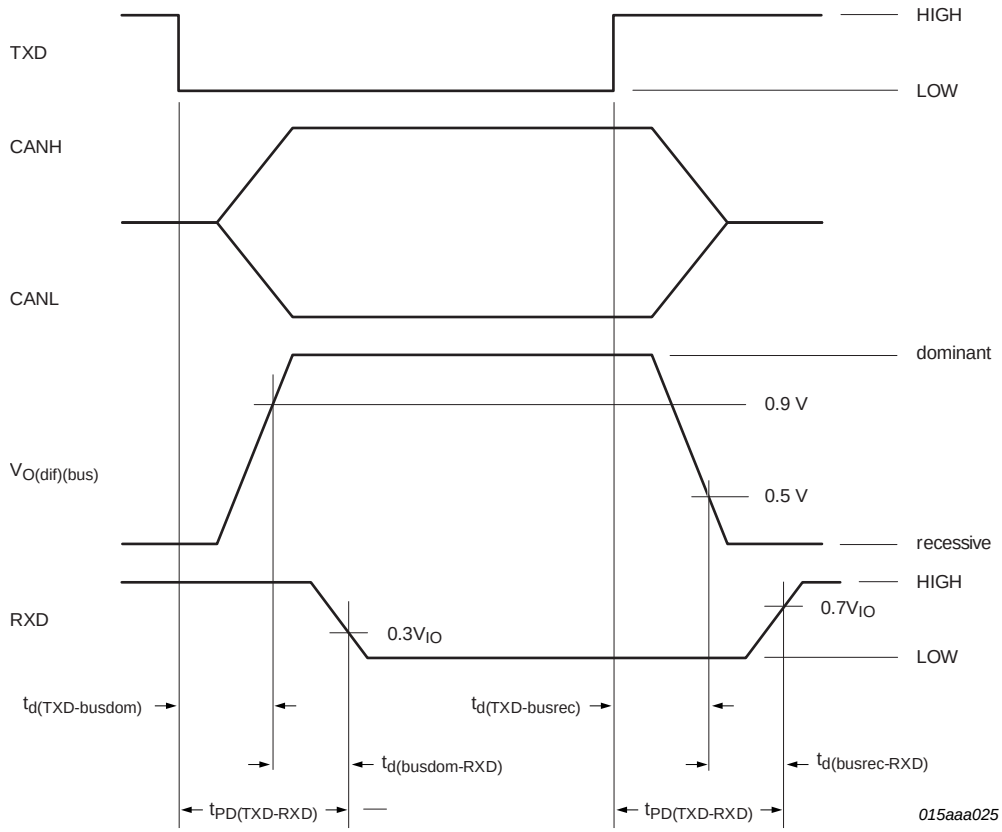


Fig 4. CAN transceiver timing diagram

12. Application information

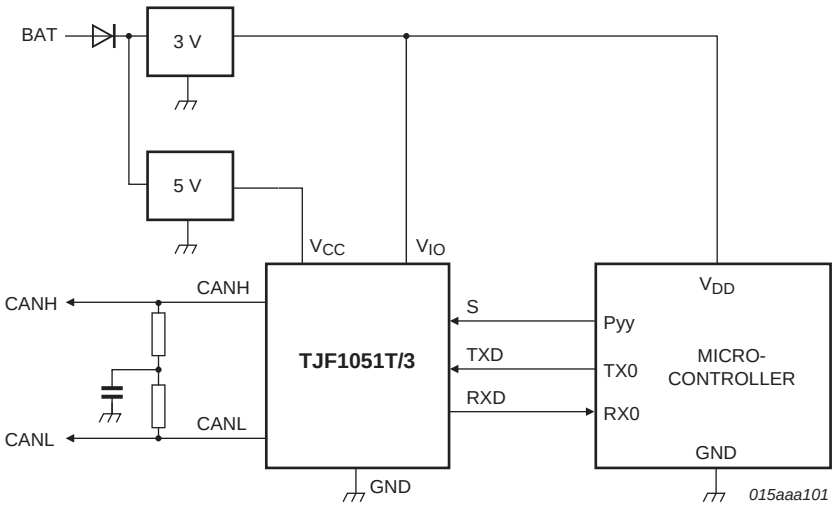
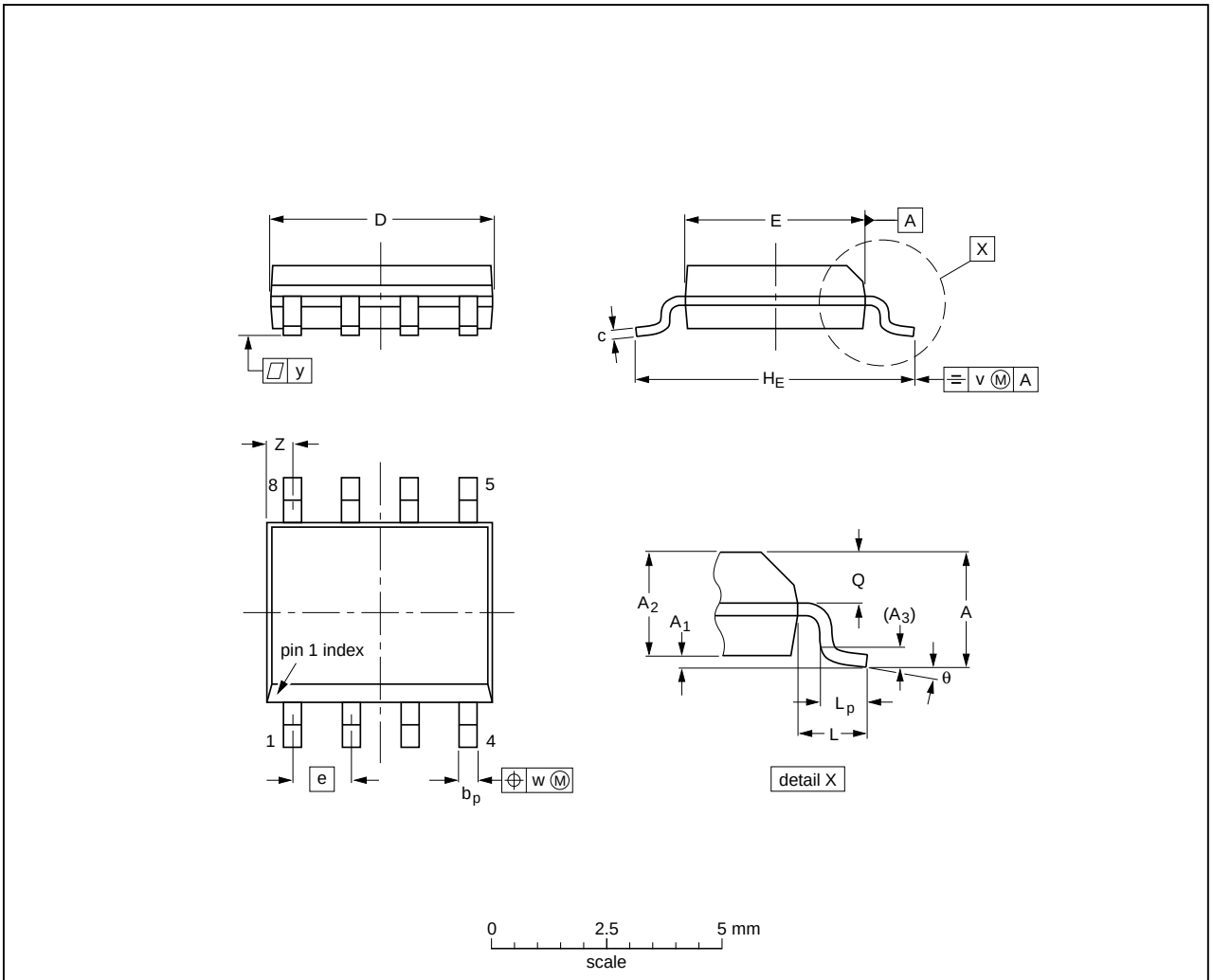


Fig 5. Typical application of the TJF1051T/3

13. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 6. Package outline SOT96-1 (SO8)

14. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 7) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 9 and 10

Table 9. SnPb eutectic process (from J-STD-020C)

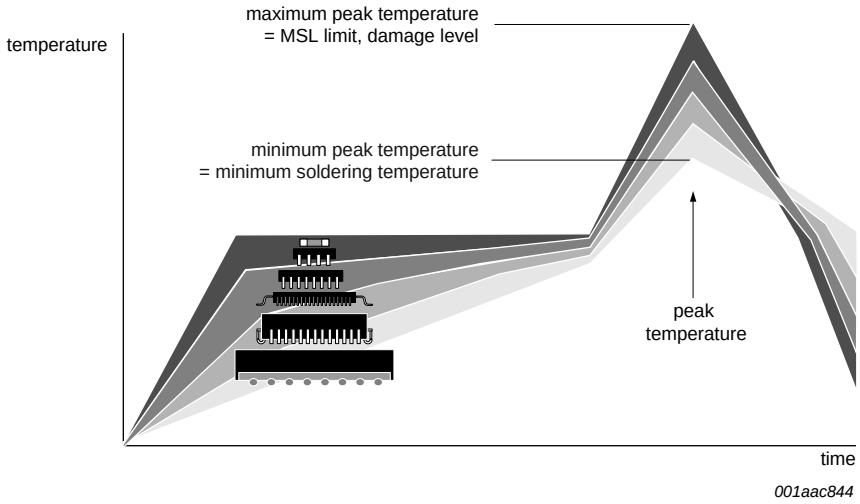
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 10. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 7.



MSL: Moisture Sensitivity Level

Fig 7. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

16. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TJF1051 v.3	20130208	Product data sheet	-	TJF1051 v.2
Modifications:	• Added TJF1051T variant • Table 1: deleted parameter T_{vj} • Table 5: parameter value changed - T_{vj} • Table 6: parameter value changed - $R_{th(vj-a)}$ • Table 7, Table 8: parameter value changed in table header- T_{amb} • Table 8: parameter added in table header- V_{IO}			
TJF1051 v.2	20110512	Product data sheet	-	TJF1051 v.1
TJF1051 v.1	20100810	Product data sheet	-	-

17. Legal information

18. Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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19. Contact information

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For sales office addresses, please send an email to: **salesaddresses@nxp.com**

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