USE DELTA39K™ FOR ALL NEW DESIGNS

Quantum38K™ ISR™ CPLD Family

CPLDs Designed for Migration

Features

- High density
  - 30K to 100K usable gates
  - 512 to 1536 macrocells
  - 136 to 302 maximum I/O pins
  - Eight dedicated inputs including four clock pins and four global I/O control signal pins; four JTAG interface pins for reconfigurability/boundary scan
- Embedded memory
  - 16-Kb to 48-Kb embedded dual-port channel memory
- 125-MHz in-system operation
- AnyVolt™ interface
  - 3.3V and 2.5V V_{CC} operation
  - 3.3V, 2.5V and 1.8V I/O capability
- Low-power operation
  - 0.18-mm 6-layer metal SRAM-based logic process
  - Full-CMOS implementation of product term array
- Simple timing model
  - No penalty for using full 16 product terms/macrocell
  - No delay for single product term steering or sharing
- Flexible clocking
  - Four synchronous clocks per device
  - Locally generated product term clock
  - Clock polarity control at each register
- Carry-chain logic for fast and efficient arithmetic operations
- Multiple I/O standards supported
  - LVCMOS (3.3/3.0/2.5/1.8V), LVTTL, 3.3V PCI
- Compatible with NoBL™, ZBT™, and QDR™ SRAMs
- Programmable slew rate control on each I/O pin
- User-programmable Bus Hold capability on each I/O pin
- Fully 3.3V PCI-compliant (as per PCI spec rev. 2.2)
- Compact PCI hot swap ready
- Multiple package/pinout offering across all densities
  - 208 to 484 pins in PQFP and FBGA packages
  - Simplifies design migration across density
- In-System Reprogrammable™ (ISR™)
  - JTAG-compliant on-board configuration
  - Design changes do not cause pinout changes
- IEEE1149.1 JTAG boundary scan
- Pin-to-pin-compatible with Cypress's high-end Delta39K™ CPLDs allowing easy migration path to
  - More embedded memory
  - Spread Aware™ PLL
  - Higher density and higher speed devices
  - High speed I/O standards and more

Development Software

- *Warp®*
  - IEEE 1076/1164 VHDL or IEEE 1364 Verilog context sensitive editing
  - Active-HDL FSM graphical finite state machine editor
  - Active-HDL SIM post-synthesis timing simulator
  - Architecture Explorer for detailed design analysis
  - Static Timing Analyzer for critical path analysis
  - Available on Windows 98™, Windows NT™, Windows ME™, Windows 2000™, and Sun Solaris™ 2.5 and later for $99
  - Supports all Cypress programmable logic products

Quantum38K™ ISR CPLD Family Members

Device	Typical Gates[1]	Macrocells	Channel memory (Kb)	Maximum I/O Pins	f_{MAX2} (MHz)	Speed — t_{PD} Pin-to-Pin (ns)	Standby I_{CC}[2] T_A=25×C
							3.3/2.5V
38K30	16K–48K	512	16	174	125	10	5 mA
38K50	23K–72K	768	24	218	125	10	5 mA
38K100	46K–144K	1536	48	302	125	10	10 mA

Notes:
1. Upper limit of typical gates is calculated by assuming that only 50% of the channel memory is used.
2. Standby I_{CC} values are with no output load and stable inputs.

Quantum38K Speed Bins[3]

Device	125	83
38K30	X	X
38K50	X	X
38K100	X	X

Device Package Offering and I/O Count Including Dedicated Clock and Control Inputs

Device	208-EQFP 28x28 mm 0.5-mm pitch	256-FBGA 17x17 mm 1.0-mm pitch	484-FBGA 23x23 mm 1.0-mm pitch
38K30	136	174	
38K50	136	180	218
38K100	136	180	302

Note:

3. Speed bins shown here are for commercial operating ranges. Please refer to the Quantum38K Part Numbers (Ordering Information) on page 24 for industrial-range speed bins.

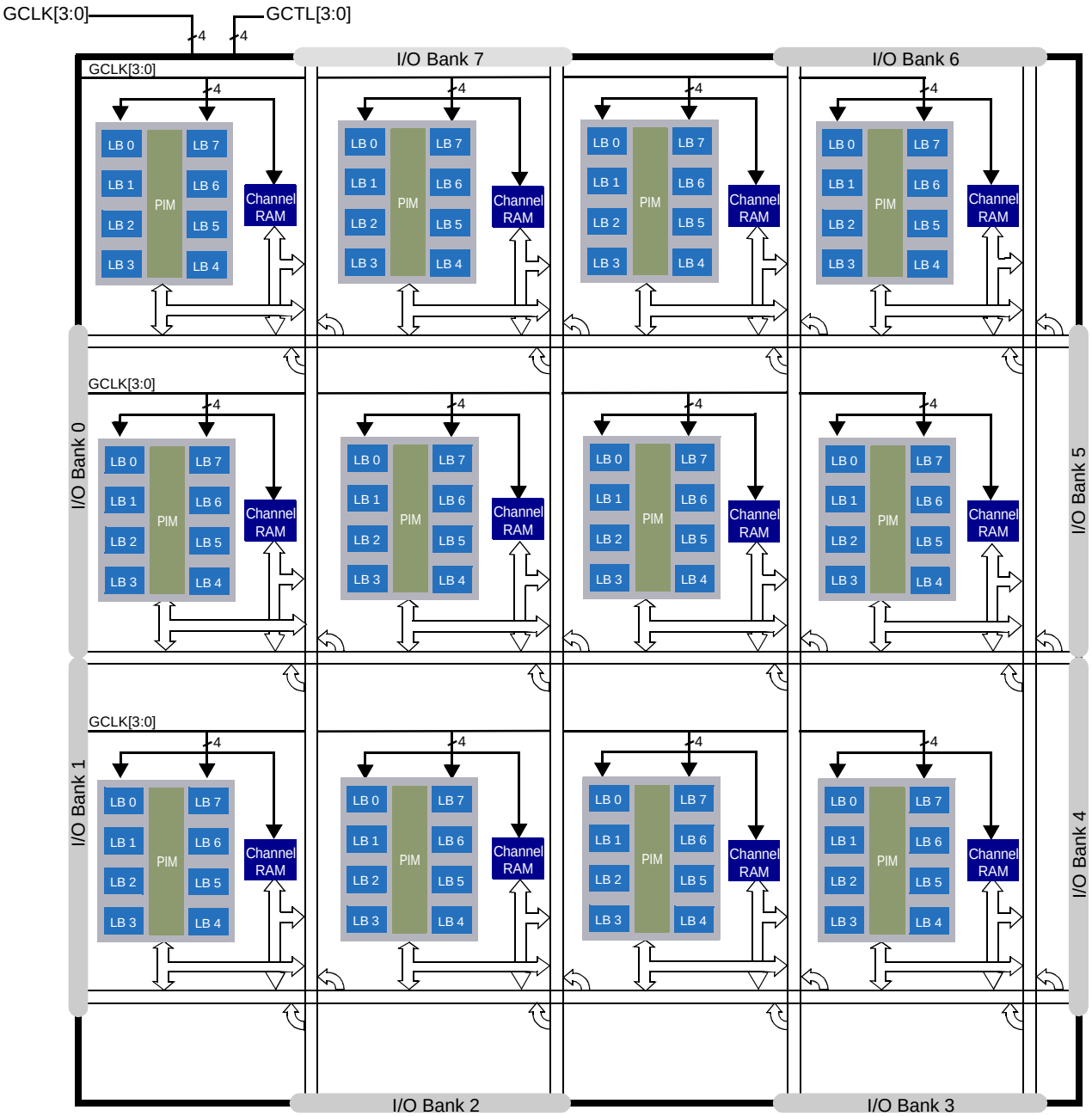


Figure 1. Quantum38K100 Block Diagram (3 Rows x 4 Columns) with I/O Bank Structure

General Description

The Quantum38K family, based on a 0.18-mm, six-layer metal CMOS logic process, offers a wide range of solutions at very high system performance. With devices ranging from 512 to 1536 macrocells, Quantum38K is the highest density CPLD in the market besides Cypress's Delta39K. Specifically designed to address high-volume communication applications, this family also integrates Cypress's dual-port memory technology onto a CPLD.

The architecture is based on Logic Block Clusters (LBC) that are connected by Horizontal and Vertical (H&V) routing channels. Each LBC features eight individual Logic Blocks (LB). Adjacent to each LBC is a channel memory block, which can be accessed directly from the I/O pins. These channel memory blocks are highly configurable and can be cascaded in width and depth. See *Figure 1* for a block diagram of the Quantum38K architecture.

All the members of the Quantum38K family have Cypress's highly regarded In-System Reprogrammability (ISR) feature, which simplifies both design and manufacturing flows, thereby reducing costs. The ISR feature provides the ability to reconfigure the devices without having design changes cause pinout or timing changes in most cases. The Cypress ISR function is implemented through a JTAG-compliant serial interface. Data is shifted in and out through the TDI and TDO pins respectively. Superior routability, simple timing, and the ISR allows users to change existing logic designs while simultaneously fixing pinout assignments and maintaining system performance.

The entire family features JTAG for ISR and boundary scan, and is compatible with the PCI Local Bus specification, meeting the electrical and timing requirements. The Quantum38K family also features user programmable bus-hold and slew rate control capabilities on each I/O pin.

AnyVolt Interface

All Quantum38K devices feature an on-chip regulator, which accepts 3.3V or 2.5V on the V_{CC} supply pins and steps it down to 1.8V internally, the voltage level at which the core operates.

With Quantum38K's AnyVolt technology, the I/O pins can be connected to either 1.8V 2.5V, or 3.3V. All Quantum38K devices are 3.3V tolerant regardless of V_{CCIO} or V_{CC} settings.

Device	V_{CC}	V_{CCIO}
38K	3.3V or 2.5V	3.3V or 2.5V or 1.8V

Global Routing Description

The routing architecture of the Quantum38K is made up of H&V routing channels. These routing channels allow signals from each of the Quantum38K architectural components to communicate with one another. In addition to the horizontal and vertical routing channels that interconnect the I/O banks, channel memory blocks, and logic block clusters, each LBC contains a Programmable Interconnect Matrix (PIM™), which is used to route signals among the logic blocks.

Figure 2 is a block diagram of the routing channels that interface within the Quantum38K architecture. The LBC is exactly the same for every member of the Quantum38K CPLD family.

Logic Block Cluster (LBC)

The Quantum38K architecture consists of several logic block clusters, each of which have eight Logic Blocks (LB) connected via a PIM, as shown in *Figure 3*. All LBCs interface with each other via horizontal and vertical routing channels.

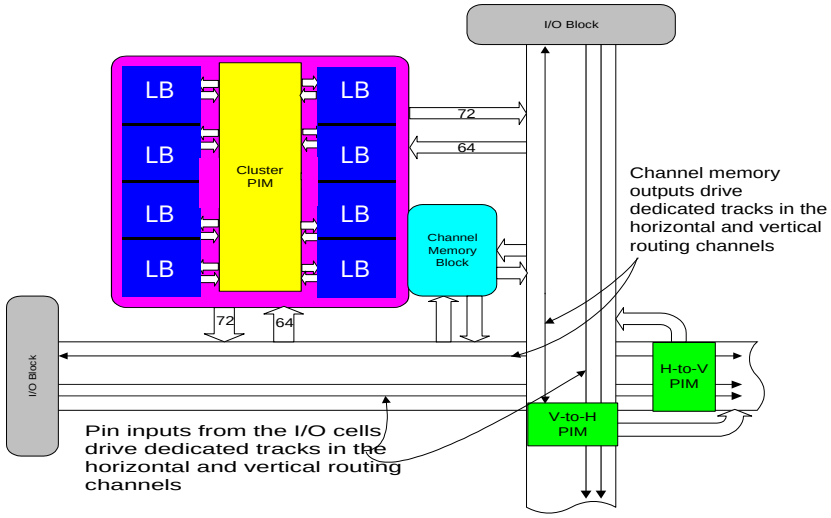


Figure 2. Quantum38K Routing Interface

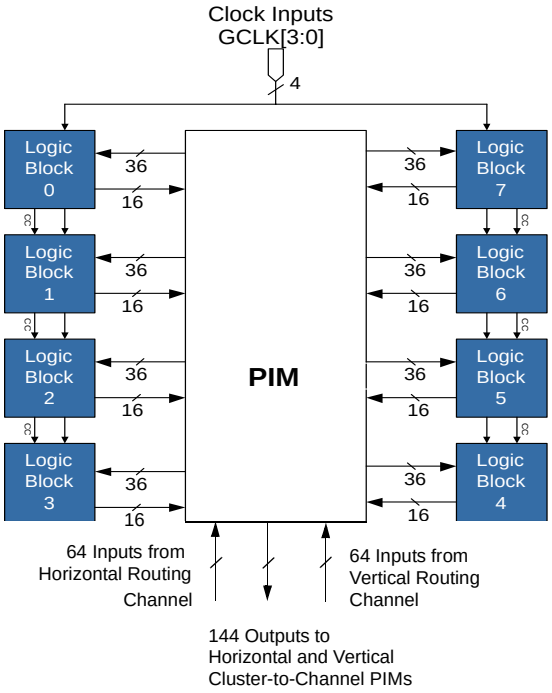


Figure 3. Quantum38K Logic Block Cluster Diagram

Logic Block (LB)

The logic block is the basic building block of the Quantum38K architecture. It consists of a product term array, an intelligent product-term allocator, and 16 macrocells.

Product Term Array

Each logic block features a 72 x 83 programmable product term array. This array accepts 36 inputs from the PIM. These inputs originate from device pins and macrocell feedbacks as well as channel memory feedbacks. Active LOW and active HIGH versions of each of these inputs are generated to create the full 72-input field. The 83 product terms in the array can be created from any of the 72 inputs.

Of the 83 product terms, 80 are for general-purpose use for the 16 macrocells in the logic block. Two of the remaining three product terms in the logic block are used as asynchronous set and asynchronous reset product terms. The final product term is the Product Term clock (PTCLK) and is shared by all 16 macrocells within a logic block.

Product Term Allocator

Through the product term allocator, *Warp* software automatically distributes the 80 product terms as needed among the 16 macrocells in the logic block. The product term allocator provides two important capabilities without affecting performance: product term steering and product term sharing.

Product Term Steering

Product term steering is the process of assigning product terms to macrocells as needed. For example, if one macrocell requires ten product terms while another needs just three, the product term allocator will “steer” ten product terms to one macrocell and three to the other. On Quantum38K devices, product terms are steered on an individual basis. Any number between 1 and 16 product terms can be steered to any macrocell.

Product Term Sharing

Product term sharing is the process of using the same product term among multiple macrocells. For example, if more than one function has one or more product terms in its equation that are common to other functions, those product terms are only programmed once. The Quantum38K product term allocator allows sharing across groups of four macrocells in a variable fashion. The software automatically takes advantage of this capability so that the user does not have to intervene.

Note that neither product term sharing nor product term steering have any effect on the speed of the product. All steering and sharing configurations have been incorporated in the timing specifications for the Quantum38K devices.

Macrocell

Within each logic block there are 16 macrocells. Each macrocell accepts a sum of up to 16 product terms from the product term array. The sum of these 16 product terms can be output in either registered or combinatorial mode. *Figure 4* displays the block diagram of the macrocell. The register can be asynchronously preset or asynchronously reset at the macrocell level with the separate preset and reset product terms. Each of these product terms features programmable polarity. This allows the registers to be preset or reset based on an AND expression or an OR expression.

An XOR gate in the Quantum38K macrocell allows for many different types of equations to be realized. It can be used as a polarity mux to implement the true or complement form of an equation in the product term array or as a toggle to turn the D flip-flop into a T flip-flop. The carry-chain input mux allows additional flexibility for the implementation of different types of logic. The macrocell can utilize the carry chain logic to

implement adders, subtractors, magnitude comparators, parity tree, or even generic XOR logic. The output of the macrocell is either registered or combinatorial.

Carry Chain Logic

The Quantum38K macrocell features carry chain logic which is used for fast and efficient implementation of arithmetic operations. The carry logic connects macrocells in up to four logic blocks for a total of 64 macrocells. Effective data path operations are implemented through the use of carry-in arithmetic, which drives through the circuit quickly. *Figure 4* shows that the carry chain logic within the macrocell consists of two product terms (CPT0 and CPT1) from the PTA and an input carry-in for carry logic. The inputs to the carry chain mux are connected directly to the product terms in the PTA. The output of the carry chain mux generates the carry-out for the next macrocell in the logic block as well as the local carry input that is connected to an input of the XOR input mux. Carry-in and a configuration bit are inputs to an AND gate. This AND gate provides a method of segmenting the carry chain in any macrocell in the logic block.

Macrocell Clocks

Clocking of the register is highly flexible. Four global synchronous clocks (GCLK[3:0]) and a Product Term clock (PTCLK) are available at each macrocell register. Furthermore, a clock polarity mux within each macrocell allows the register to be clocked on the rising or the falling edge (see macrocell diagram in *Figure 4*).

PRESET/RESET Configurations

The macrocell register can be asynchronously preset and reset using the PRESET and RESET mux. Both signals are active high and can be controlled by either of two Preset/Reset product terms (PRC[1:0] in *Figure 4*) or GND. In situations where the PRESET and RESET are active at the same time, RESET takes priority over PRESET.

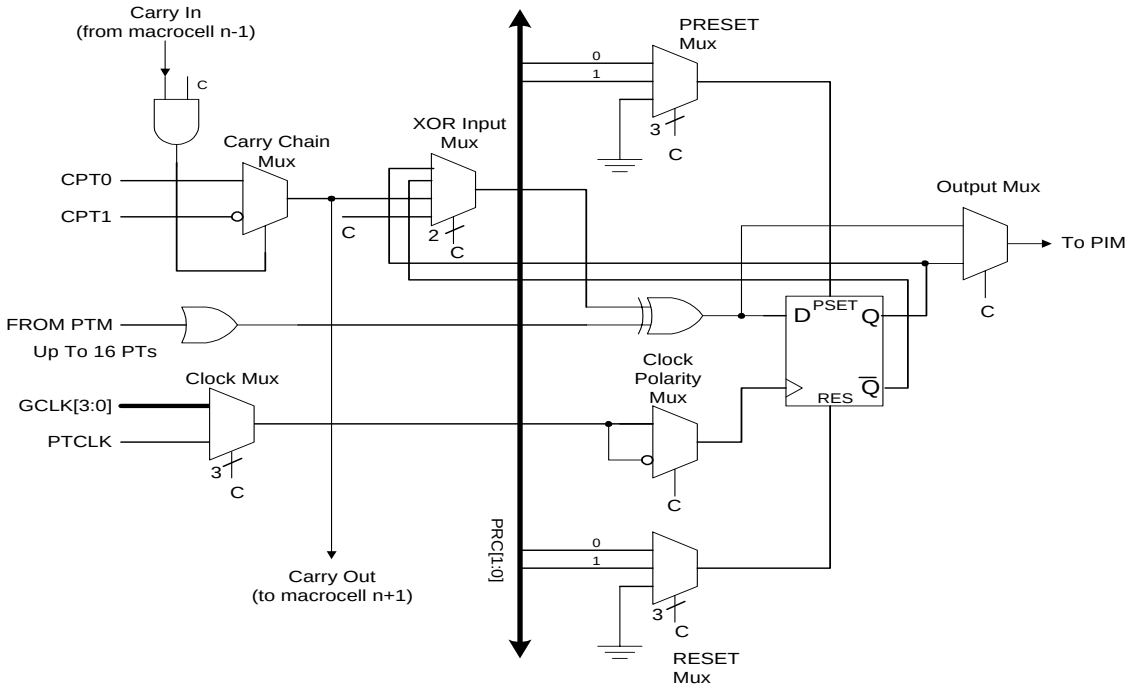


Figure 4. Quantum38K Macrocell

Embedded Memory

The Quantum38K architecture includes an embedded channel memory block at each crossing point of horizontal and vertical routing channels. The channel memory is a 4096-bit memory block that can be configured as asynchronous or synchronous Single-Port RAM, Dual-Port RAM, or Read-Only memory (ROM). The memory organization is configurable as 4Kx1, 2Kx2, 1Kx4, or 512x8.

Data, address, and control inputs to the channel memory are driven from horizontal and vertical routing channels. All data logic outputs drive dedicated tracks in the horizontal and vertical routing channels. The clocks for the channel memory block are selected from four global clocks and pin inputs from the horizontal and vertical channels. The clock muxes also include a polarity mux for each clock so that the user can choose an inverted clock.

Dual-Port (Channel Memory) Configuration

Each port has distinct address inputs, as well as separate data and control inputs that can be accessed simultaneously. The inputs to the Dual-Port memory are driven from the horizontal and vertical routing channels. The data outputs drive dedicated tracks in the routing channels. The interface to the routing is such that Port A of the Dual-Port interfaces primarily with the horizontal routing channel and Port B interfaces primarily with the vertical routing channel.

The clocks for each port of the Dual-Port configuration are selected from four global clocks and two local clocks. One local clock is sourced from the horizontal channel and the other from the vertical channel. The data outputs of the dual-port memory can also be registered. Clocks for the output registers are also selected from four global clocks and two local clocks. One clock polarity mux per port allows the use of true or complement polarity for input and output clocking purposes.

Arbitration

The Dual-Port configuration of the Channel Memory Block provides arbitration when both ports access the same address at the same time. Depending on the memory operations being attempted, one port always gets priority. See *Table 1* for details on which port gets priority for read and write operations. An active-LOW ‘Address Match’ signal is generated when an address collision occurs.

Table 1. Arbitration Result: Address Match Signal Becomes Active

Port A	Port B	Result of Arbitration	Comment
Read	Read	No arbitration required	Both ports read at the same time
Write	Read	Port A gets priority	If Port B requests first then it will read the current data. The output will then change to the newly written data by Port A
Read	Write	Port B gets priority	If Port A requests first then it will read the current data. The output will then change to the newly written data by Port B
Write	Write	Port A gets priority	Port B is blocked until Port A is finished writing

Channel Memory Initialization

The channel memory powers up in an undefined state, but is set to a user-defined known state during configuration. To facilitate the use of look-up-table (LUT) logic and ROM applications, the channel memory blocks can be initialized with a given set of data when the device is configured at power up. For LUT and ROM applications, the user cannot write to memory blocks.

Channel Memory Routing Interface

Similar to LBC outputs, the channel memory blocks feature dedicated tracks in the horizontal and vertical routing channels for the data outputs and the flag outputs, as shown in *Figure 5*. This allows the channel memory blocks to be expanded easily. These dedicated lines can be routed to I/O pins as chip outputs or to other logic block clusters to be used in logic equations.

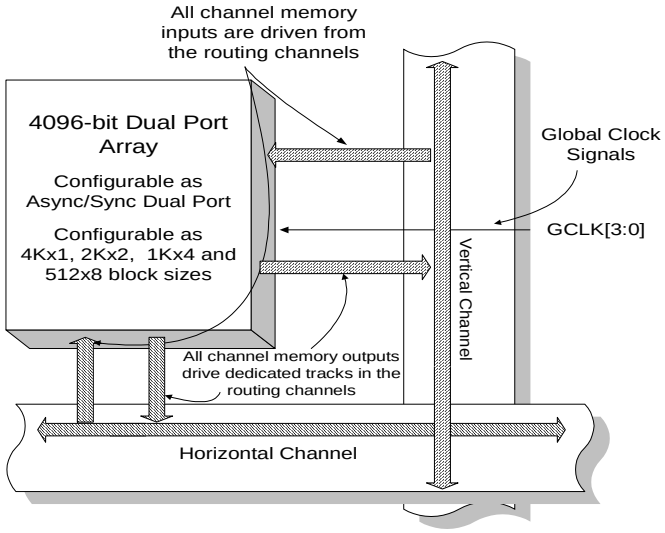


Figure 5. Block Diagram of Channel Memory Block

I/O Banks

The Quantum38K interfaces the horizontal and vertical routing channels to the pins through I/O banks. There are eight I/O banks per device as shown in *Figure 6*, and all I/Os from an I/O bank are located in the same section of a package for PCB layout convenience.

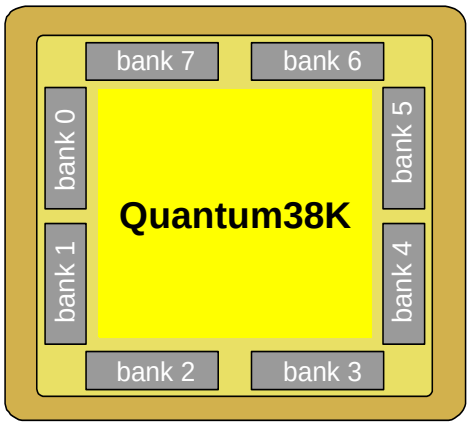


Figure 6. Quantum38K I/O Bank Block Diagram

Quantum38K devices support True Vertical Migration™, i.e., for each package type, Quantum38K devices of different densities keep given pins in the same I/O banks. This allows for easy and simple implementation of multiple I/O standards during the design and prototyping phase, before a final density has been determined.

Each I/O bank contains several I/O cells, and each I/O cell contains an input/output register, an output enable register, programmable slew rate control and programmable bus hold control logic. Each I/O cell drives a pin output of the device; the cell also supplies an input to the device that connects to a dedicated track in the associated routing channel.

Each I/O bank can use any supported I/O standard by supplying appropriate V_{CCIO} voltages. All the V_{CCIO} pins in an I/O bank must be connected to the same V_{CCIO} voltage. This requirement restricts the number of I/O standards supported by an I/O bank at any given time.

The number of I/Os which can be used in each I/O bank depend on the type of I/O standards and the number of V_{CCIO} and GND pins being used. This restriction is derived from the electromigration limit of the V_{CCIO} and GND bussing on the chip. Please refer to the note on page 14 and the application note titled “Delta39K Family Device I/O Standards and Configurations” for details.

I/O Cell

Figure 7 is a block diagram of the Quantum38K I/O cell. The I/O cell contains a three-state input buffer, an output buffer, and a register that can be configured as an input or output register. The output buffer has a slew rate control option that can be used to configure the output for a slower slew rate. The input of the device and the pin output can each be configured as registered or combinatorial; however, only one path can be configured as registered in a given design.

The output enable can be selected from one of the four global I/O control signals or from one of two Output Control Channel (OCC) signals. The output enable can be configured as always enabled or always disabled or it can be controlled by one of the remaining inputs to the mux. The selection is done via a mux that includes V_{CC} and GND as inputs.

I/O Signals

There are four dedicated inputs (GCTL[3:0]) that are used as Global I/O Control Signals available to every I/O cell. These global I/O control signals may be used as output enables, register resets and register clock enables as shown in *Figure 7*. These global control signals, driven from four dedicated pins, can only be used as active-high signals and are available only to the I/O cells thereby implementing fast resets, register and output enables.

In addition, there are six Output Control Channel (OCC) signals available to each I/O cell. These control signals may be used as output enables, register resets and register clock enables as shown in *Figure 7*. Unlike global control signals, these OCC signal can be driven from internal logic or and I/O pin.

One of the four global clocks can be selected as the clock for the I/O cell register. The clock mux output is an input to a clock polarity mux that allows the input/output register to be clocked on either edge of the clock.

IO Standards

I/O Standard	V_{CCIO}
LVTTL (2 mA – 24 mA)	3.3V
LVCMOS	3.3V
LVCMOS3	3.0V
LVCMOS2	2.5V
LVCMOS18	1.8V
3.3V PCI	3.3V

Slew Rate Control

The ouput buffer has a slew rate control option. This allows the output buffer to slew at a fast rate (3 V/ns) or a slow rate (1 V/ns). All I/Os default to fast slew rate. For designs concerned with meeting FCC emissions standards the slow edge provides for lower system noise. For designs requiring very high performance the fast edge rate provides maximum system performance.

Programmable Bus Hold

On each I/O pin, user-programmable-bus-hold is included. Bus-hold, which is an improved version of the popular internal pull-up resistor, is a weak latch connected to the pin that does not degrade the device's performance. As a latch, bus-hold maintains the last state of a pin when the pin is placed in a high-impedance state, thus reducing system noise in bus-interface applications. Bus-hold additionally allows unused device pins to remain unconnected on the board, which is particularly useful during prototyping as designers can route new signals to the device without cutting trace connections to V_{CC} or GND. For more information, see the application note "Understanding Bus-Hold–A Feature of Cypress CPLDs".

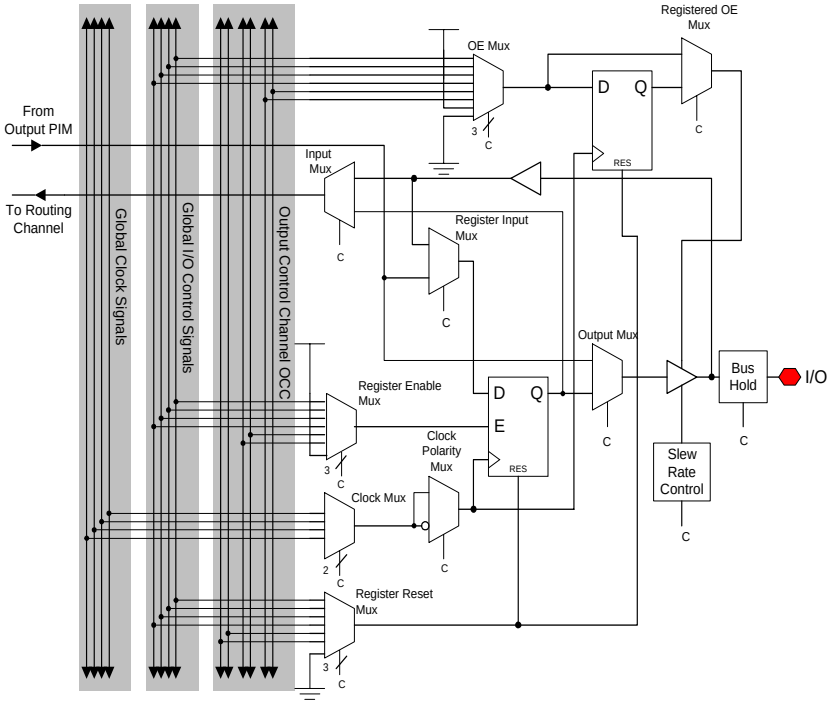


Figure 7. Block Diagram of I/O Cell

Clocks

Quantum38K has four dedicated clock input pins (GCLK[3:0]) to accept system clocks.

The global clock tree for a Quantum38K device is driven by the dedicated clock pins, consisting of four global clocks that go to every macrocell, memory block, and I/O cell.

Clock Tree Distribution

The clock tree distributes the four global clocks to every cluster, channel memory, and I/O block on the die. The global clock tree is designed such that the clock skew is minimized while maintaining an acceptable clock delay.

CompactPCI Hot Swap

CompactPCI Hot Swap specification allows the removal and insertion of cards into CompactPCI sockets without switching-off the bus. Quantum38K CPLDs can be used as a CompactPCI host or target on these cards.

This feature is useful in telecommunication and networking applications as it allows implementation of high availability systems, where repairs and upgrades can be done without downtime.

Quantum38K CPLDs are CompactPCI Hot Swap Ready per CompactPCI Hot Swap specification R1.0, with the following exception:

- The I/O cells do not provide bias voltage support. External resistors can be used to achieve this per section 3.1.3.1 of the CompactPCI Hot Swap specification R2.0.

  A simple board-level solution is provided in the application note titled “Hot-Swapping Delta39K and Quantum38K CPLDs.”

Family, Package, and Density Migration in Quantum38K CPLDs

The Quantum38K CPLDs combine dense logic with embedded communications memory. Further design flexibility is added by the easy migration options available between different packages, densities and even between Quantum38K and Delta39K CPLD families.

By making each package offering of Quantum38K CPLD pin-to-pin compatible with packages of Delta39K CPLD, a seamless migration path is offered to the users of Quantum38K CPLDs as their design needs grow. Delta39K CPLDs offer following enhancements:

- More embedded memory
- Spread Aware PLL
- High-speed I/Os (GTL+, SSTL+, HSTL etc.)
- Higher density devices (up to 200K or 3072 macrocells)
- Higher speed devices (up to 233 MHz)
- Dedicated FIFOs with built-in flag logic
- 1.8V operation
- Self-boot (one chip) solution eliminates need of a boot EEPROM.

For details on Delta39K CPLD family refer to the data sheet titled *Delta39K ISR CPLD family*.

This migration flexibility makes changes or additions to designs simple even after PCB layout. It also provides the ability for experimental designs to be used on production PCBs. Please refer to the application note titled *“Family, Package, and Density Migration in Delta39K and Quantum38K CPLDs”*.

Timing Model

One important feature of the Quantum38K family is the simplicity of its timing. All combinatorial and registered/synchronous delays are worst case and system performance is static (as shown in the AC specs section) as long as data is routed through the same horizontal and vertical channels. *Figure 8* illustrates the true timing model for the 38K100 devices. For synchronous clocking of macrocells, a delay is incurred from macrocell clock to macrocell clock of separate Logic Blocks within the same cluster, as well as separate Logic Blocks within different clusters. This is respectively shown as t_{SCS} and t_{SCS2} in *Figure 8.* For combinatorial paths, any input to any output (from corner to corner on the device), incurs a worst-case delay in the 38K100 regardless of the amount of logic or which horizontal and vertical channels are used. This is the t_{PD} shown in *Figure 8.* For synchronous systems, the input set-up time to the output macrocell register and the clock to output time are shown as the parameters t_{MCS} and t_{MCCO} shown in the *Figure 8.* These measurements are for any output and synchronous clock, regardless of the logic placement.

The Quantum38K features:

- no dedicated vs. I/O pin delays
- no penalty for using 0–16 product terms
- no added delay for steering product terms
- no added delay for sharing product terms
- no output bypass delays.

The simple timing model of the Quantum38K family eliminates unexpected performance penalties.

IEEE 1149.1-compliant JTAG Operation

The Quantum38K family has an IEEE 1149.1 JTAG interface for both Boundary Scan and ISR operations.

Four dedicated pins are reserved on each device for use by the Test Access Port (TAP).

Boundary Scan

The Quantum38K family supports Bypass, Sample/Preload, Extest, Intest, Idcode and Usercode boundary scan instructions. The JTAG interface is shown in *Figure 9*.

In-System Reprogramming (ISR)

In-System Reprogramming is the combination of the capability to program or reprogram a device on-board, and the ability to support design changes without changing the system timing or device pinout. This combination means design changes during debug or field upgrades do not cause board respins. The Quantum38K family implements ISR by providing a IEEE std 1149.1 JTAG compliant interface for on-board configuration. Robust routing resources offer pinout flexibility and a simple timing model provides consistent system performance.

Configuration

Quantum38K is a SRAM based volatile device family that uses Cypress’s CY3LV series of CPLD boot EEPROM to store configuration data. Please refer to the data sheet titled “CPLD Boot EEPROM” and the application note titled “Configuring Delta39K/Quantum38K” for more details on configuration and interface set-up between Quantum38K and CPLD boot PROM. These documents can be found at http://www.cypress.com.

For Quantum38K design, configuration is defined as the loading of a user’s design into the volatile Quantum38K die. Programming, on the other hand, is the loading of a user’s design into the serial boot PROM.

Device configuration can begin in two ways. It can be initiated by toggling the *Reconfig* pin from LOW to HIGH, or by issuing the appropriate IEEE std 1149.1 JTAG instruction to the Quantum38K device via the JTAG interface. There are two IEEE std 1149.1 JTAG instructions that initiate configuration of the Quantum38K. The *Self Config* instruction causes the Quantum38K to (re)configure with data stored in the serial boot PROM. The *Load Config* instruction causes the Quantum38K to (re)configure according to data provided by other sources such as a PC, automatic test equipment (ATE), or an embedded micro-controller/processor via the JTAG interface.

There are two configuration options available for issuing the IEEE std 1149.1 JTAG instructions to the Quantum38K. The first method is to use a PC with the C3 ISR programming cable and software. With this method, the ISR pins of the Quantum38K devices in the system are routed to a connector at the edge of the printed circuit board. The C3 ISR

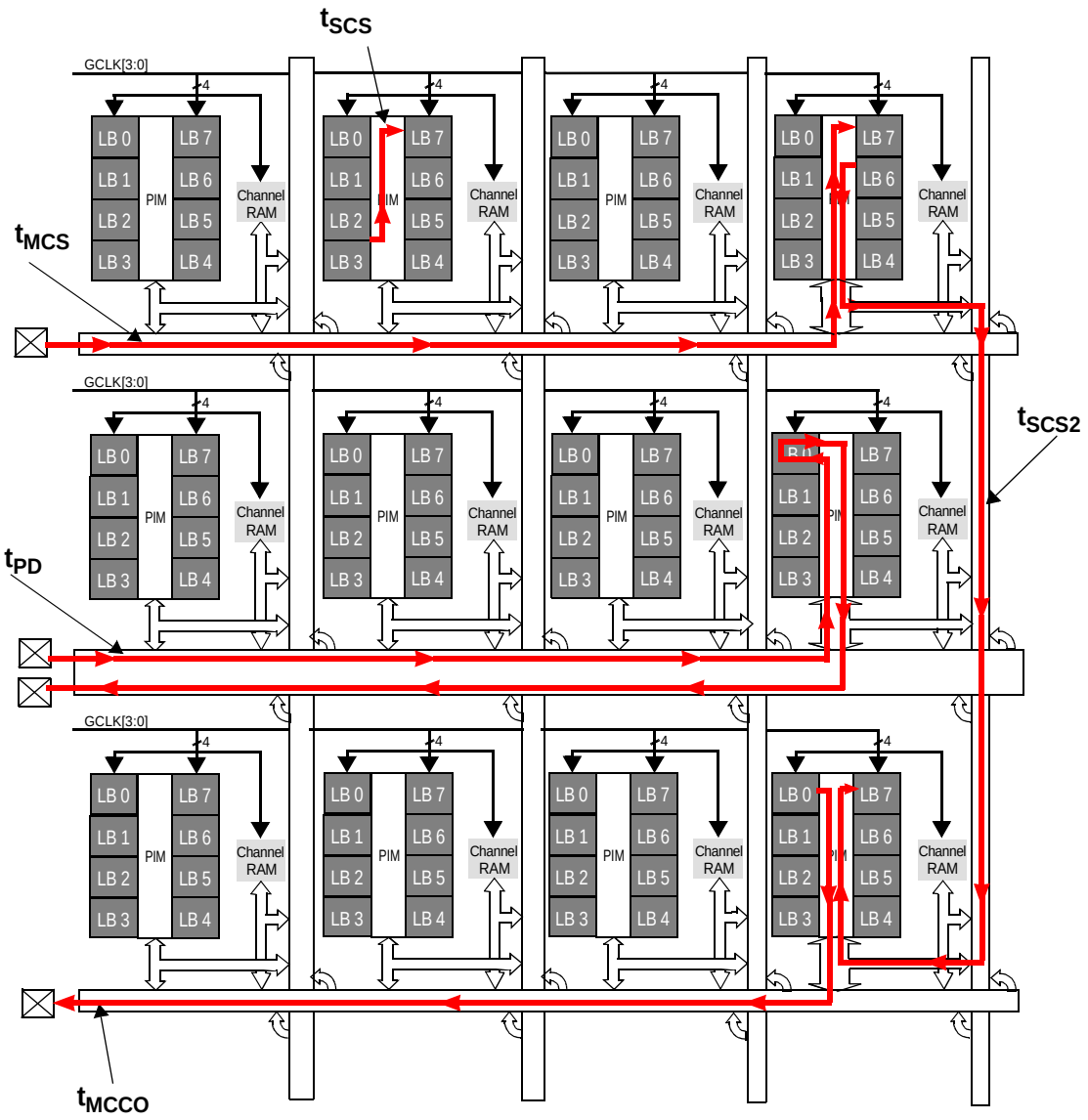


Figure 8. Timing Model for 38K100 Device

programming cable is then connected between the PC and this connector. A simple configuration file instructs the ISR software of the programming operations to be performed on the Quantum38K devices in the system. The ISR software then automatically completes all of the necessary data manipulations required to accomplish configuration, reading, verifying, and other ISR functions. For more information on the Cypress ISR interface, see the ISR Programming Kit data sheet (CY3900i).

The second configuration option for the Quantum38K is to utilize the embedded controller or processor that already exists in the system. The Quantum38K ISR software assists in this method by converting the device HEX file into the ISR serial stream that contains the ISR instruction information and the addresses and data of locations to be configured. The embedded controller then simply directs this ISR stream to the chain of Quantum38K devices to complete the desired reconfiguration or diagnostic operations. Contact your local sales office for information on availability of this option.

Programming

There are multiple methods available for programming the serial boot PROM. The first method uses Cypress's CYDH2200E CPLD Boot PROM Programming Kit to program via a two-wire interface.

The second method is through third-party programmers. Programming support for CY3LV series of boot PROMs is available on a wide variety of third-party programmers. All major programmers (including BP Micro, Data I/O, System General, Hi-Lo) support boot PROM programming.

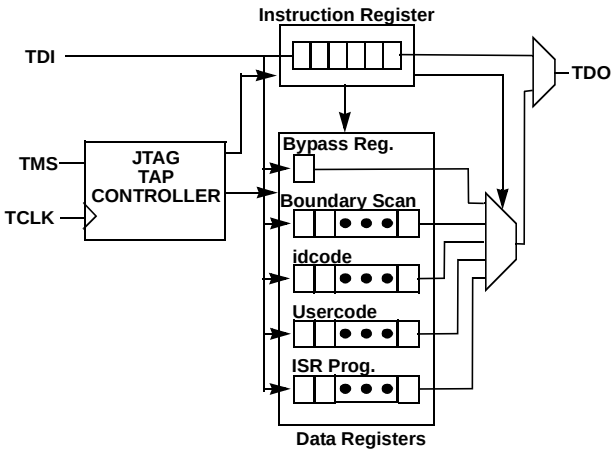


Figure 9. JTAG Interface

Development Software Support

Warp

Warp is a state-of-the-art design environment for designing with Cypress programmable logic. *Warp* utilizes a subset of IEEE 1076/1164 VHDL and IEEE 1364 as the Hardware Description Language (HDL) for design entry. *Warp* accepts VHDL or Verilog input, synthesizes and optimizes the entered design, and outputs a configuration bitstream for the desired Quantum38K device. For simulation, *Warp* provides a graphical waveform simulator as well as VHDL and Verilog Timing Models.

VHDL and Verilog are open, powerful, non-proprietary Hardware Description Languages (HDLs) that are standards for behavioral design entry and simulation. HDL allows designers to learn a single language that is useful for all facets of the design process.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C
Soldering Temperature.....220°C
Ambient Temperature with Power Applied.....–40°C to +85°C
Junction Temperature .....135°C

V_{CC} to Ground Potential.....–0.5V to 4.6V
V_{CCIO} to Ground Potential.....–0.5V to 4.6V
DC Voltage Applied to Outputs in High-Z State –0.5V to 4.5V
DC Input voltage.....–0.5V to 4.5V
DC Current into Outputs.....±20 mA
Static Discharge Voltage (per JEDEC EIA/JESD22-A114A) .....> 2001V
Latch-up Current.....> 200 mA

Operating Range[4]

Range	Ambient Temperature	Junction Temperature	Output Condition	V_{CCIO}	V_{CC}	V_{CCJTAG}/ V_{CCCNFG}
Commercial	0°C to +70°C	0°C to +85°C	3.3V	3.3V ± 0.3V	3.3V ± 0.3V or 2.5V ± 0.2V	Same as V_{CCIO}
			2.5V	2.5V ± 0.2V		
			1.8V	1.8 ± 0.15V		
Industrial	–40°C to +85°C	–40°C to +100°C	3.3V	3.3V ± 0.3V		
			2.5V	2.5V ± 0.2V		
			1.8V	1.8 ± 0.15V		

DC Characteristics

Parameter	Description	Test Conditions	V_{CCIO} = 3.3V		V_{CCIO} = 2.5V		V_{CCIO} = 1.8V		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{DRINT}	Data Retention V_{CC} Voltage (config data may be lost below this)		1.5		1.5		1.5		V
V_{DRIO}	Data Retention V_{CCIO} Voltage (config data may be lost below this)		1.2		1.2		1.2		V
I_{IX}[5]	Input Leakage Current	$GND \le V_I \le 3.6V$	–10	10	–10	10	–10	10	µA
I_{OZ}	Output Leakage Current	$GND \le V_O \le V_{CCIO}$	–10	10	–10	10	–10	10	µA
I_{OS}[6]	Output Short Circuit Current	V_{CCIO} = Max., V_{OUT} = 0.5V		–160		–160		–160	µA
I_{BHL}	Input Bus Hold LOW Sustaining Current	V_{CC} = Min., $V_{PIN} = V_{IL}$	+40		+30		+25		µA
I_{BHH}	Input Bus Hold HIGH Sustaining Current	V_{CC} = Min., $V_{PIN} = V_{IH}$	–40		–30		–25		µA
I_{BHLO}	Input Bus Hold LOW Overdrive Current	V_{CC} = Max.		+250		+200		+150	µA
I_{BHHO}	Input Bus Hold HIGH Overdrive Current	V_{CC} = Max.		–250		–200		–150	µA

Parameter	Description	Device	V_{CC}= 3.3 V/2.5V		Unit
			Min.	Max	
I_{CC0}	Standby Current	38K30		20	mA
		38K50		20	mA
		38K100		30	mA

Notes:

4. The Voltage on any input or I/O pin cannot exceed the power pin during power-up.
5. Input Leakage current is ±10 µA for all the pins on all the Quantum38K package except the following pins in Quantum 38K100 packages: The input leakage current spec for these pins in ±200 µA.

Quantum 38K100	
Package	Pins
484-FBGA	B8, G9

6. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation. Tested initially and after any design or process changes that may affect this parameter.

Capacitance

Parameter	Description	Test Conditions	Min.	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	$V_{in}=V_{CCIO}$ @ f = 1 MHz 25°C		10	pF
C_{CLK}	Clock Signal Capacitance	$V_{in}=V_{CCIO}$ @ f = 1 MHz 25°C	5	12	pF
C_{PCI}	PCI-compliant[7] Capacitance	$V_{in}=V_{CCIO}$ @ f = 1 MHz 25°C		8	pF

DC Characteristics[8] (IO)

Input/Output Standard	V_{CCIO} (V)	V_{OH} (V)		V_{OL} (V)		V_{IH} (V)		V_{IL} (V)	
		@ I_{OH} =	V_{OH} (min.)	@ I_{OL} =	V_{OL} (max.)	Min.	Max.	Min.	Max.
LVTTL – 2 mA	3.3	–2 mA	2.4	2 mA	0.4	2.0 V	V_{CCIO}+0.3	–0.3V	0.8V
LVTTL – 4 mA	3.3	–4 mA	2.4	4 mA	0.4	2.0 V	V_{CCIO}+0.3	–0.3V	0.8V
LVTTL – 6 mA	3.3	–6 mA	2.4	6 mA	0.4	2.0 V	V_{CCIO}+0.3	–0.3V	0.8V
LVTTL – 8 mA	3.3	–8 mA	2.4	8 mA	0.4	2.0 V	V_{CCIO}+0.3	–0.3V	0.8V
LVTTL – 12 mA	3.3	–12 mA	2.4	12 mA	0.4	2.0 V	V_{CCIO}+0.3	–0.3V	0.8V
LVTTL – 16 mA	3.3	–16 mA	2.4	16 mA	0.4	2.0 V	V_{CCIO}+0.3	–0.3V	0.8V
LVTTL – 24 mA	3.3	–24 mA	2.4	24 mA	0.4	2.0 V	V_{CCIO}+0.3	–0.3V	0.8V
LVCMOS	3.3	–0.1 mA	V_{CCIO}–0.2v	0.1 mA	0.2	2.0 V	V_{CCIO}+0.3	–0.3V	0.8V
LVCMOS3	3.0	–0.1 mA	V_{CCIO}–0.2v	0.1mA	0.2	2.0 V	V_{CCIO}+0.3	–0.3V	0.8V
LVCMOS2	2.5	–0.1 mA	2.1	0.1 mA	0.2	1.7 V	V_{CCIO}+0.3	–0.3V	0.7V
		–1.0 mA	2.0	1.0 mA	0.4				
		–2.0 mA	1.7	2.0 mA	0.7				
LVCMOS18	1.8	–0.1 mA	V_{CCIO}–0.2v	0.1 mA	0.2	0.65V_{CCIO}	V_{CCIO}+0.3	–0.3V	0.35V_{CCIO}
		–2 mA	V_{CCIO}–0.45v	2.0 mA	0.45				
3.3V PCI	3.3	–0.5 mA	0.9V_{CCIO}	1.5 mA	0.1V_{CCIO}	0.5V_{CCIO}	V_{CCIO}+0.5	–0.5V	0.3V_{CCIO}

Configuration Parameters

Parameter	Description	Min.	Unit
$t_{RECONFIG}$	*Reconfig* pin LOW time before it goes HIGH	200	ns

Power-up Sequence Requirements

- Upon power-up, all the outputs remain three-stated until all the V_{CC} pins have powered-up to the nominal voltage and the part has completed configuration.
- The part will not start configuration until V_{CC}, V_{CCIO}, V_{CCJTAG}, and V_{CCCNFG} have reached nominal voltage.
- V_{CC} pins can be powered up in any order. This includes V_{CC}, V_{CCIO}, V_{CCJTAG}, and V_{CCCNFG}.
- All V_{CCIO}s on a bank should be tied to the same potential and powered up together.
- All V_{CCIO}s (even the unused banks) need to be powered up to at least 1.5V before configuration has completed.
- Maximum ramp time for all V_{CC}s should be 0V to nominal voltage in 100 ms.

Notes:

7. PCI spec (rev 2.2) requires the IDSEL pin to have capacitance less than or equal to 8 pF. Section titled “Pin Tables” on page 27 identifies all the I/O pins, in a given package, which can be used as IDSEL in a PCI design. All other I/O pins meet the PCI requirement of capacitance less than or equal to 10 pF.
8. The number of I/Os that can be used in each I/O bank depends on the type of I/O standards and the number of V_{CCIO} and GND pins being used. Please refer to the application note titled “Delta39K and Quantum38K I/O Standards and Configurations” for details.
   - The source current limit per I/O bank per V_{CCIO} pin is 165 mA.
   - The sink current limit per I/O bank per GND pin is 230 mA.

Switching Characteristics—Parameter Descriptions Over the Operating Range [9]

Parameter	Description
Combinatorial Mode Parameters	
t_{PD}	Delay from any pin input, through any cluster on the channel associated with that pin input, to any pin output on the horizontal or vertical channel associated with that cluster
t_{EA}	Global control to output enable
t_{ER}	Global control to output disable
t_{PRR}	Asynchronous macrocell RESET or PRESET recovery time from any pin input on the horizontal or vertical channel associated with the cluster the macrocell is in
t_{PRO}	Asynchronous macrocell RESET or PRESET from any pin input on the horizontal or vertical channel associated with the cluster that the macrocell is in to any pin output on those same channels
t_{PRW}	Asynchronous macrocell RESET or PRESET minimum pulse width, from any pin input to a macrocell in the farthest cluster on the horizontal or vertical channel the pin is associated with
Synchronous Clocking Parameters	
t_{MCS}	Set-up time of any input pin to a macrocell in any cluster on the channel associated with that input pin, relative to a global clock
t_{MCH}	Hold time of any input pin to a macrocell in any cluster on the channel associated with that input pin, relative to a global clock
t_{MCCO}	Global clock to output of any macrocell to any output pin on the horizontal or vertical channel associated with the cluster that macrocell is in
t_{IOS}	Set-up time of any input pin to the I/O cell register associated with that pin, relative to a global clock
t_{IOH}	Hold time of any input pin to the I/O cell register associated with that pin, relative to a global clock
t_{IOCO}	Clock to output of an I/O cell register to the output pin associated with that register
t_{SCS}	Macrocell clock to macrocell clock through array logic within the same cluster
t_{SCS2}	Macrocell clock to macrocell clock through array logic in different clusters on the same channel
t_{ICS}	I/O register clock to any macrocell clock in a cluster on the channel the I/O register is associated with
t_{OCS}	Macrocell clock to any I/O register clock on the horizontal or vertical channel associated with the cluster that the macrocell is in
t_{CHZ}	Clock to output disable (high-impedance)
t_{CLZ}	Clock to output enable (low-impedance)
f_{MAX}	Maximum frequency with internal feedback—within the same cluster
f_{MAX2}	Maximum frequency with internal feedback—within different clusters at the opposite ends of a horizontal or vertical channel
Product Term Clock	
t_{MCSPT}	Set-up time for macrocell used as input register, from input to product term clock
t_{MCHPT}	Hold time of macrocell used as an input register
t_{MCCOPT}	Product term clock to output delay from input pin
t_{SCS2PT}	Register to register delay through array logic in different clusters on the same channel using a product term clock
Channel Interconnect Parameters	
t_{CHSW}	Adder for a signal to switch from a horizontal to vertical channel and vice-versa
t_{CL2CL}	Cluster to Cluster delay adder (through channels and channel PIM)
Miscellaneous Delays	
t_{CPLD}	Delay from the input of a cluster PIM, through a macrocell in the cluster, back to a cluster PIM input. This parameter can be added to the t_{PD} and t_{SCS} parameters for each extra pass through the AND/OR array required by a given signal path
t_{MCCD}	Adder for carry chain logic per macrocell
t_{IOD}	Delay from the input of the output buffer to the I/O pin

Note:
9. Add t_{CHSW} to signals making a horizontal to vertical channel switch or vice-versa.

Switching Characteristics—Parameter Descriptions Over the Operating Range [9] (continued)

Parameter	Description
t_{IOIN}	Delay from the I/O pin to the input of the channel buffer
t_{CKIN}	Delay from the clock pin to the input of the clock driver
$t_{IOREGPIN}$	Delay from the I/O pin to the input of the I/O register
JTAG Parameters	
t_{JCKH}	TCLK HIGH time
t_{JCKL}	TCLK LOW time
t_{JCP}	TCLK clock period
t_{JSU}	JTAG port set-up time (TDI/TMS inputs)
t_{JH}	JTAG port hold time (TDI/TMS inputs)
t_{JCO}	JTAG port clock to output time (TDO)
t_{JXZ}	JTAG port valid output to high impedance (TDO)
t_{JZX}	JTAG port high impedance to valid output (TDO)

Channel Memory Timing Parameter Descriptions Over the Operating Range

Parameter	Description
Dual Port Asynchronous Mode Parameters	
t_{CHMAA}	Channel memory access time. Delay from address change to read data out
t_{CHMPWE}	Write enable pulse width
t_{CHMSA}	Address set-up to the beginning of write enable
t_{CHMHA}	Address hold after the end of write enable with both signals from the same I/O block
t_{CHMSD}	Data set-up to the end of write enable
t_{CHMHD}	Data hold after the end of write enable
t_{CHMBA}	Channel memory asynchronous dual port address match (busy access time)
Dual-Port Synchronous Mode Parameters	
$t_{CHMCYC1}$	Clock cycle time for flow through read and write operations (from macrocell register through channel memory back to a macrocell register in the same cluster)
$t_{CHMCYC2}$	Clock cycle time for pipelined read and write operations (from channel memory input register through the memory to channel memory output register)
t_{CHMS}	Address, data, and WE set-up time of pin inputs, relative to a global clock
t_{CHMH}	Address, data, and WE hold time of pin inputs, relative to a global clock
t_{CHMDV1}	Global clock to data valid on output pins for flow through data
t_{CHMDV2}	Global clock to data valid on output pins for pipelined data
t_{CHMBDV}	Channel memory synchronous dual-port address match (busy, clock to data valid)
$t_{CHMMACS1}$	Channel memory input clock to macrocell clock in the same cluster
$t_{CHMMACS2}$	Channel memory output clock to macrocell clock in the same cluster
$t_{MACCHMS1}$	Macrocell clock to channel memory input clock in the same cluster
$t_{MACCHMS2}$	Macrocell clock to channel memory output clock in the same cluster
Internal Parameters	
$t_{CHMCHAA}$	Asynchronous channel memory access time from input of channel memory to output of channel memory

Switching Characteristics—Parameter Values Over the Operating Range

Parameter	125		83		Unit
	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters					
t_{PD}		10		15	ns
t_{EA}		9		10	ns
t_{ER}		9		10	ns
t_{PRR}	8.0		10		ns
t_{PRO}	13		15		ns
t_{PRW}	6.0		7.0		ns
Synchronous Clocking Parameters					
t_{MCS}	5.0		6.7		ns
t_{MCH}	0.0		0.0		ns
t_{MCCO}		10		12	ns
t_{IOS}	2.0		2.5		ns
t_{IOH}	2.0		2.5		ns
t_{IOCO}		7.0		8.0	ns
t_{SCS}	6.4		9.6		ns
t_{SCS2}	8.0		12		ns
t_{ICS}	8.0		12		ns
t_{OCS}	8.0		12		ns
t_{CHZ}		6.0		7.0	ns
t_{CLZ}	1.5		1.5		ns
f_{MAX}		156		104	MHz
f_{MAX2}		125		83	MHz
Product Term Clocking Parameters					
t_{MCSPT}	5.0		6.0		ns
t_{MCHPT}	2.0		2.5		ns
t_{MCCOPT}		11.0		15.0	ns
t_{SCS2PT}	10.0		15.0		ns
Channel Interconnect Parameters					
t_{CHSW}		1.7		2.0	ns
t_{CL2CL}		2.8		3.0	ns
Miscellaneous Parameters					
t_{CPLD}		4.0		5.0	ns
t_{MCCD}		0.35		0.38	ns
JTAG Parameters					
t_{JCKH}	25		25		ns
t_{JCKL}	25		25		ns
t_{JCP}	50		50		ns
t_{JSU}	10		10		ns
t_{JH}	10		10		ns
t_{JCO}		20		20	ns
t_{JXZ}		20		20	ns
t_{JZX}		20		20	ns

Input and Output Standard Timing Delay Adjustments

All the timing specifications in this data sheet are specified based on LVCMOS-compliant inputs and outputs (fast slew rates[10]). Apply the following adjustments if the inputs and outputs are configured to operate at the following standards.

Input/Output Standard	Output Delay Adjustments						Input Delay Adjustments		
	Fast Slew Rate			Slow Slew Rate (additional delay to fast slew rate)					
	t_{IOD}	t_{EA}	t_{ER}	$t_{IODSLOW}$	t_{EASLOW}	t_{ERSlow}	t_{IOIN}	t_{CKIN}	$t_{IOREGPIN}$
LVTTL – 2 mA	2.75	0	0	2.6	2.0	2.0	0	0	0
LVTTL – 4 mA	1.8	0	0	2.5	2.0	2.0	0	0	0
LVTTL – 6 mA	1.8	0	0	2.5	2.0	2.0	0	0	0
LVTTL – 8 mA	1.2	0	0	2.4	2.0	2.0	0	0	0
LVTTL – 12 mA	0.6	0	0	2.3	2.0	2.0	0	0	0
LVTTL – 16 mA	0.16	0	0	2.0	2.0	2.0	0	0	0
LVTTL – 24 mA	0.0	0	0	1.6	2.0	2.0	0	0	0
LVCMOS	0.0	0	0	2.0	2.0	2.0	0	0	0
LVCMOS3	0.14	0.05	0	2.0	2.0	2.0	0.1	0.1	0.2
LVCMOS2	0.41	0.1	0	2.0	2.0	2.0	0.2	0.2	0.4
LVCMOS18	1.6	0.7	0.1	2.1	2.0	2.0	0.5	0.4	0.3
3.3V PCI	–0.14	0	0	2.0	2.0	2.0	0	0	0

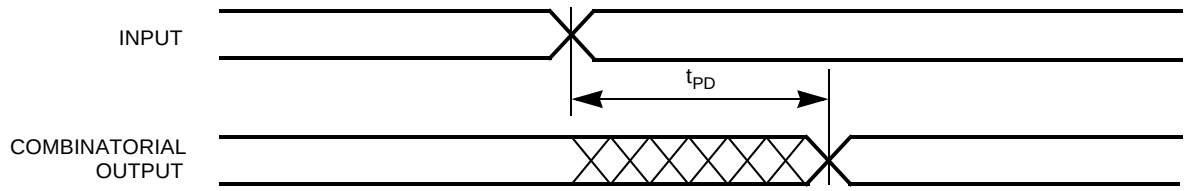
Channel Memory Timing Parameter Values

Parameter	125		83		Unit
	Min.	Max.	Min.	Max.	
Dual-Port Asynchronous Mode Parameters					
t_{CHMAA}		17		20	ns
t_{CHMPWE}	10		12		ns
t_{CHMSA}	3.2		4.0		ns
t_{CHMHA}	1.8		2.0		ns
t_{CHMSD}	10		12		ns
t_{CHMHD}	0.9		1.0		ns
t_{CHMBA}		14.0		16.0	ns
Dual-Port Synchronous Mode Parameters					
$t_{CHMCYC1}$	15		20		ns
$t_{CHMCYC2}$	7.4		10.6		ns
t_{CHMS}	5.0		6.0		ns
t_{CHMH}	0.0		0.0		ns
t_{CHMDV1}		17		20	ns
t_{CHMDV2}		10		15	ns
t_{CHMBDV}		14.0		16.0	ns
$t_{CHMMACS1}$	14.0		16.0		ns
$t_{CHMMACS2}$	8.0		10		ns
$t_{MACCHMS1}$	7.6		9.0		ns
$t_{MACCHMS2}$	10.0		13.0		ns
Internal Parameters					
$t_{CHMCHAA}$	10.0		13.0		ns

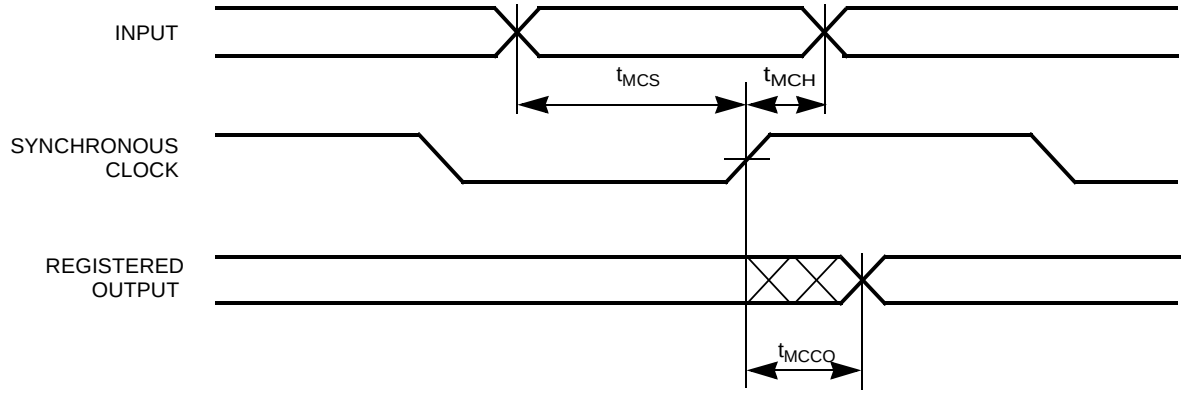
Note:
10. For “slow slew rate” output delay adjustments, refer to *Warp* software’s static timing analyzer results.

Switching Waveforms

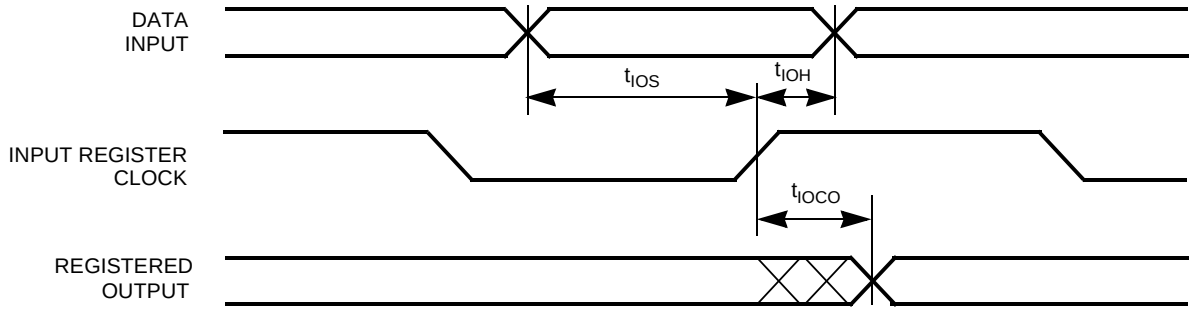
Combinatorial Output



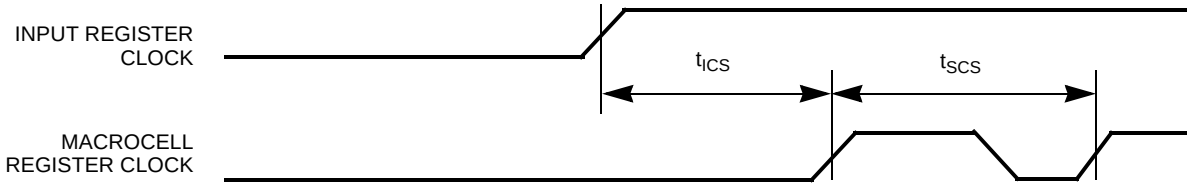
Registered Output with Synchronous Clocking (Macrocell)



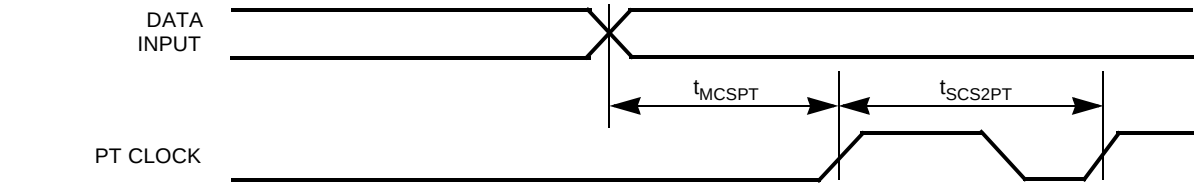
Registered Input in I/O Cell



Clock to Clock

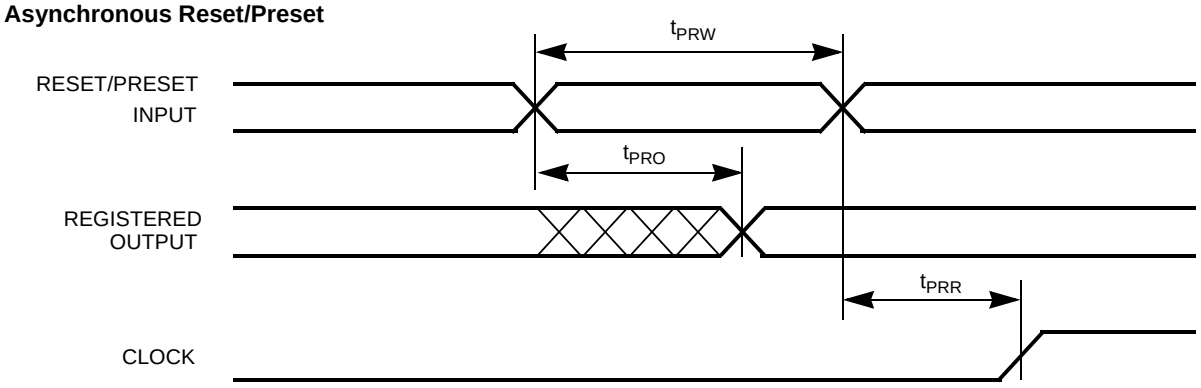


PT Clock to PT Clock

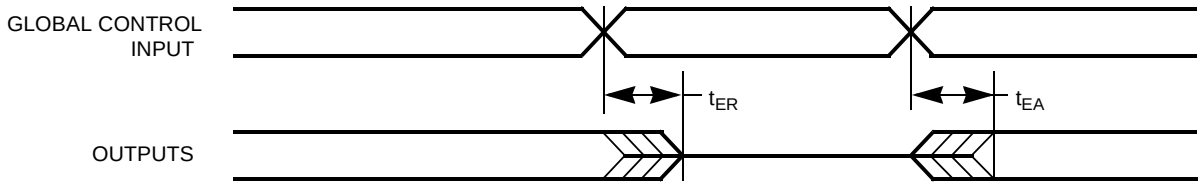


Switching Waveforms (continued)

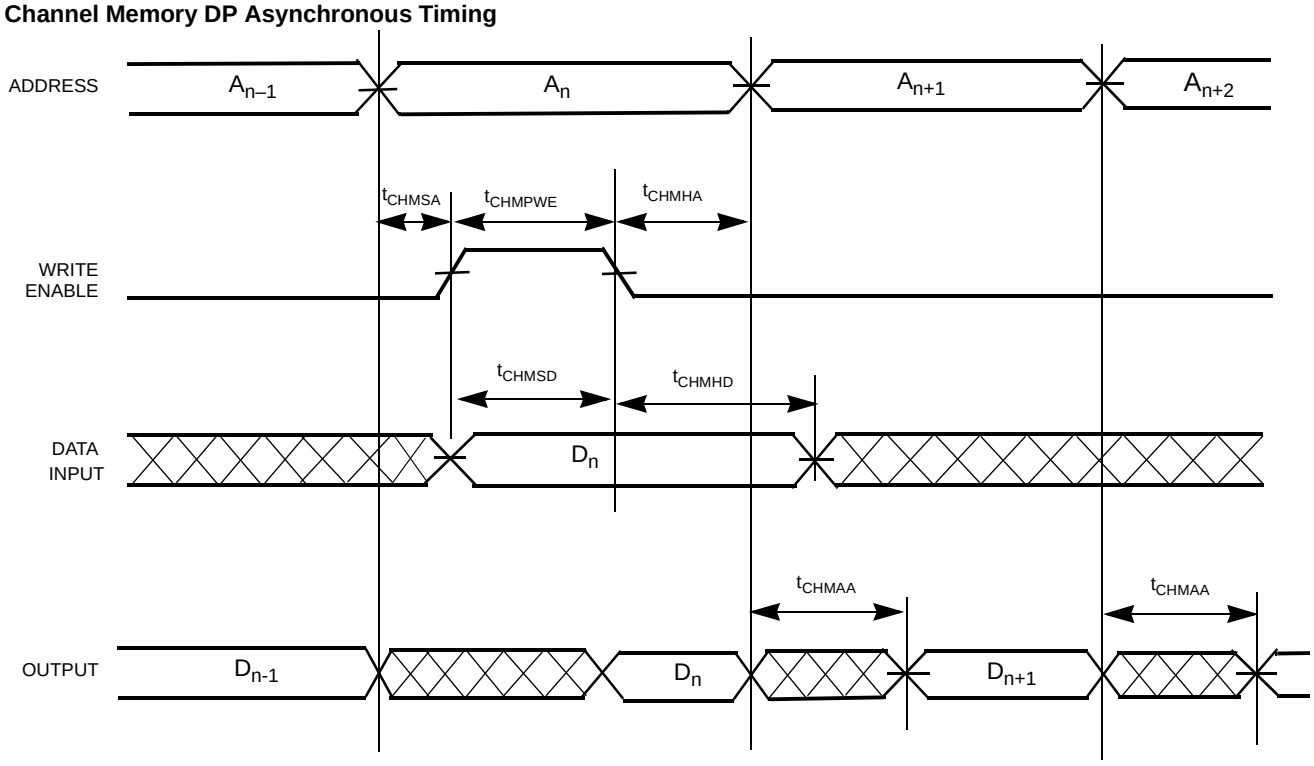
Asynchronous Reset/Preset



Output Enable/Disable

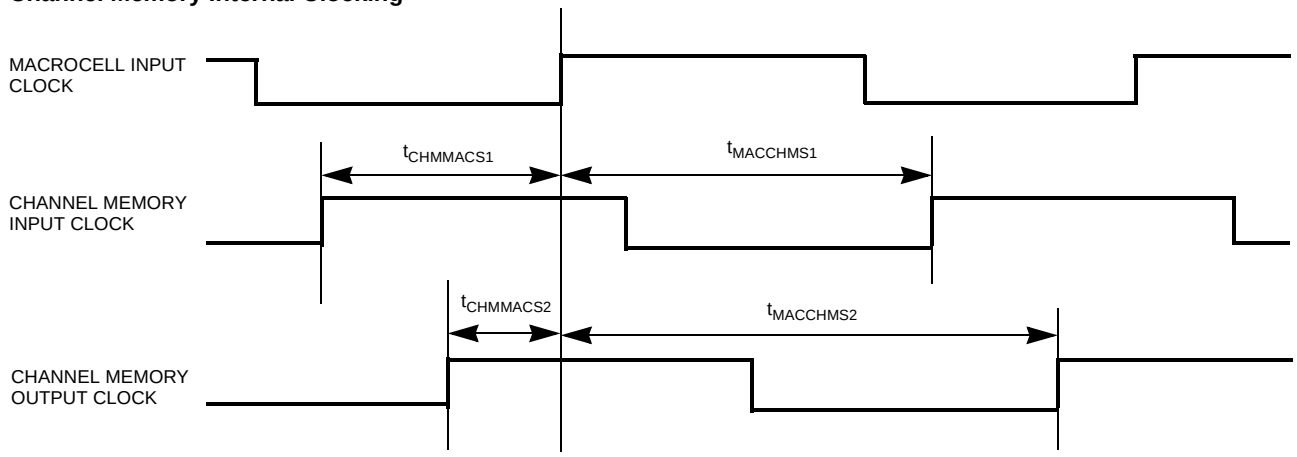


Channel Memory DP Asynchronous Timing

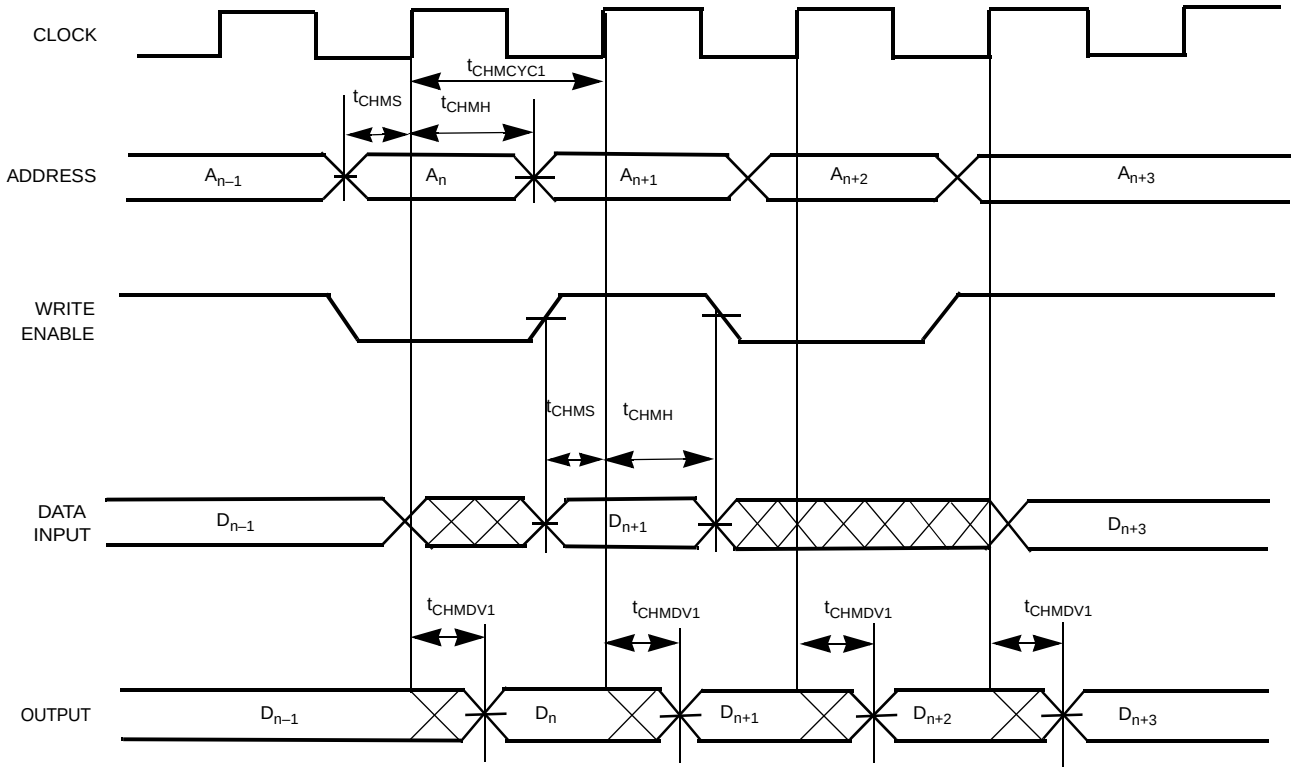


Switching Waveforms (continued)

Channel Memory Internal Clocking

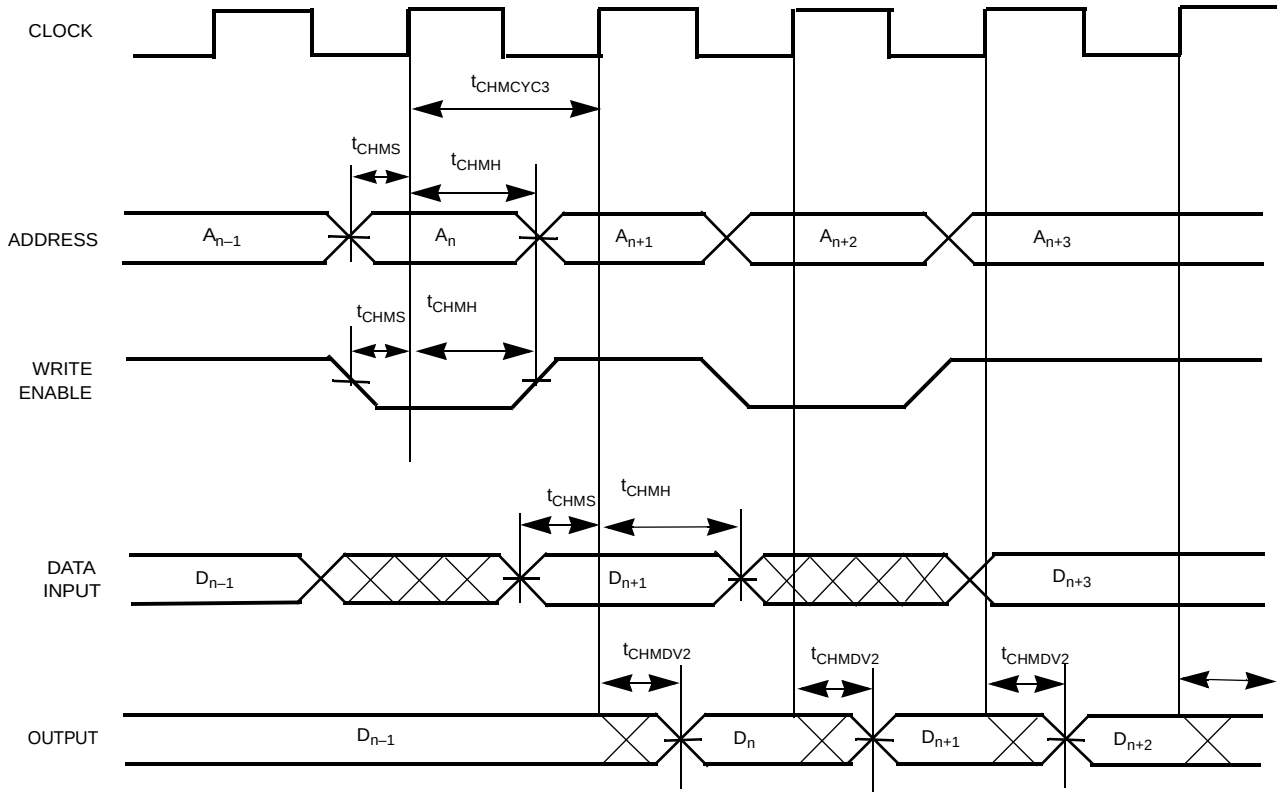


Channel Memory DP SRAM Flow Through R/W Timing

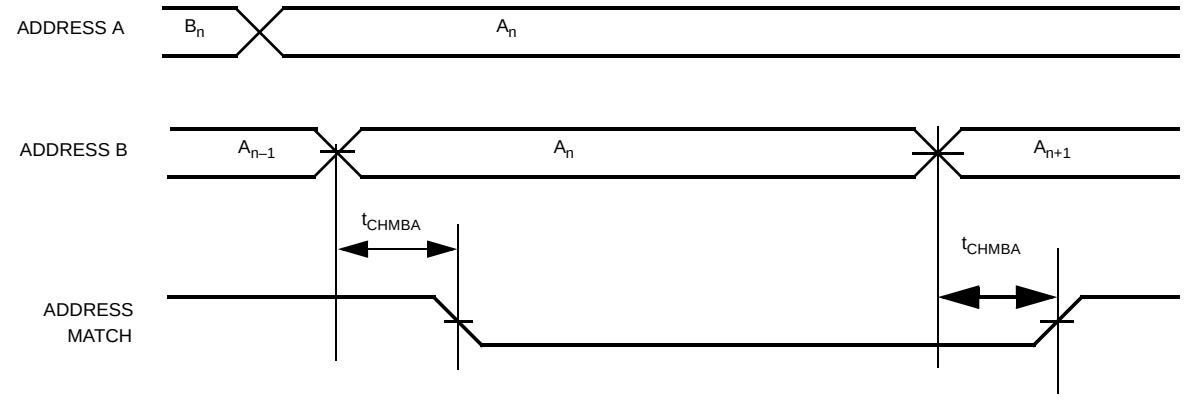


Switching Waveforms (continued)

Channel Memory DP SRAM Pipeline R/W Timing

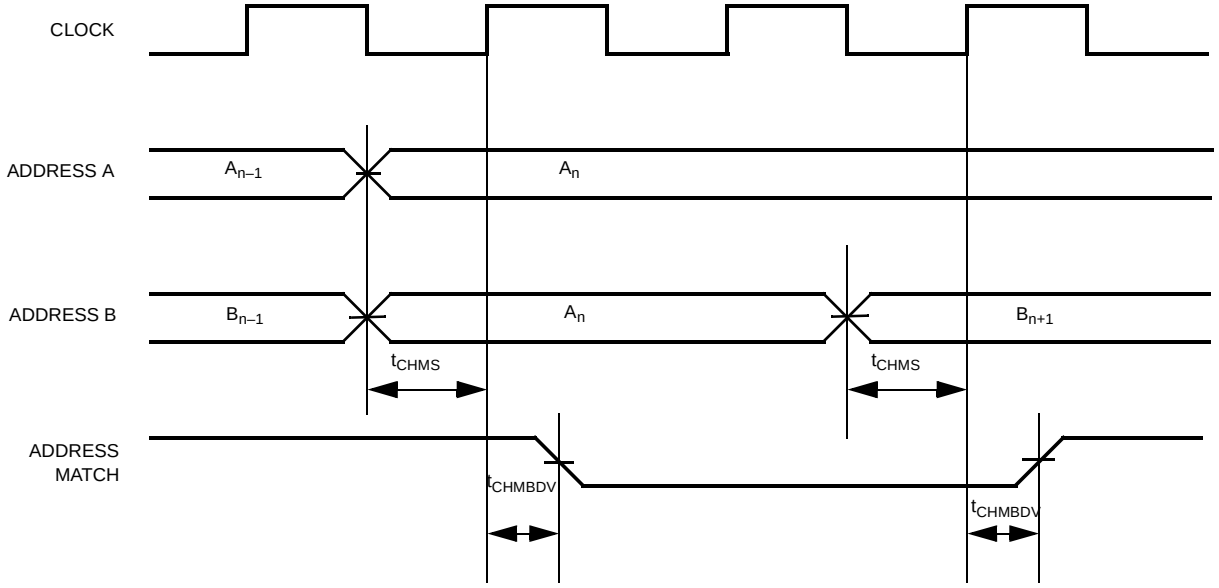


Dual-Port Asynchronous Address Match Busy Signal



Switching Waveforms (continued)

Dual-Port Synchronous Address Match Busy Signal



CY 38 100 V 484 - 125 BB C

Cypress Semiconductor ID

Family Type
38 = Quantum38K Family

Gate Density
30=30k Usable Gates
50=50k Usable Gates
100=100k Usable Gates

Operating Reference Voltage
V = 3.3V or 2.5V Supply Voltage

Pin Count
208 = 208 Leads
256 = 256 Balls
484 = 484 Balls

Speed
125 = 125 MHz 83 = 83 MHz

Package Type
N = Plastic Quad Flat Pack (PQFP)
NT = Thermally Enhanced Quad Flat Pack (EQFF
BB = Fine-Pitch Ball Grid Array (FBGA)
1.0-mm Lead Pitch

Operating Conditions
Commercial 0°C to +70°C
Industrial -40°C to +85°C

Quantum38K Part Numbers (Ordering Information)

Device	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
38K30	125	CY38030V208-125NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY38030V256-125BBC	BB256	256-Lead Fine Pitch Ball Grid Array	
		CY38030V208-125NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY38030V256-125BBI	BB256	256-Lead Fine Pitch Ball Grid Array	
	83	CY38030V208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY38030V256-83BBC	BB256	256-Lead Fine Pitch Ball Grid Array	
38K50	125	CY38050V208-125NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY38050V256-125BBC	BB256	256-Lead Fine Pitch Ball Grid Array	
		CY38050V484-125BBC	BB484	484-Lead Fine Pitch Ball Grid Array	
		CY38050V208-125NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY38050V256-125BBI	BB256	256-Lead Fine Pitch Ball Grid Array	
		CY38050V484-125BBI	BB484	484-Lead Fine Pitch Ball Grid Array	
	83	CY38050V208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY38050V256-83BBC	BB256	256-Lead Fine Pitch Ball Grid Array	
		CY38050V484-83BBC	BB484	484-Lead Fine Pitch Ball Grid Array	
38K100	125	CY38100V208-125NTC	NT208	208-Lead Enhanced Quad Flat Pack	Commercial
		CY38100V256-125BBC	BB256	256-Lead Fine Pitch Ball Grid Array	
		CY38100V484-125BBC	BB484	484-Lead Fine Pitch Ball Grid Array	
		CY38100V208-125NTI	NT208	208-Lead Enhanced Quad Flat Pack	Industrial
		CY38100V256-125BBI	BB256	256-Lead Fine Pitch Ball Grid Array	
		CY38100V484-125BBI	BB484	484-Lead Fine Pitch Ball Grid Array	
	83	CY38100V208-83NTC	NT208	208-Lead Enhanced Quad Flat Pack	Commercial
		CY38100V256-83BBC	BB256	256-Lead Fine Pitch Ball Grid Array	
		CY38100V484-83BBC	BB484	484-Lead Fine Pitch Ball Grid Array	

CPLD Boot EEPROM[11] Part Numbers (Ordering Information)

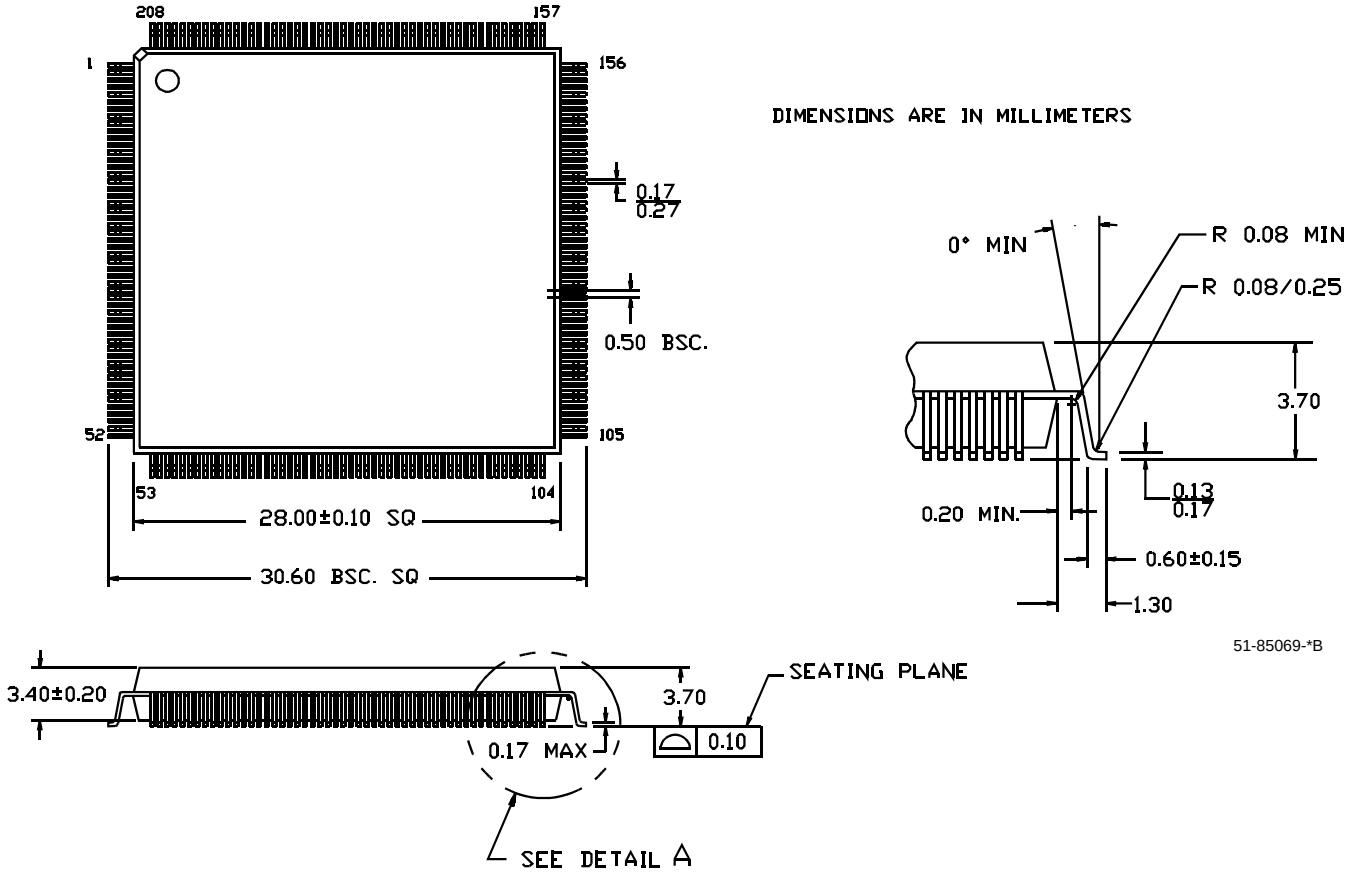
CPLD Boot EEPROM Density	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
1 Mbit	15	CY3LV010-10JC	20J	20-Lead Plastic Leaded Chip Carrier	Commercial
	10	CY3LV010-10JI	20J	20-Lead Plastic Leaded Chip Carrier	Industrial
512Kbit	15	CY3LV512-10JC	20J	20-Lead Plastic Leaded Chip Carrier	Commercial
	10	CY3LV512-10JI	20J	20-Lead Plastic Leaded Chip Carrier	Industrial

Recommended CPLD Boot EEPROM for Corresponding Quantum38K CPLDs

CPLD Device	Recommended CPLD Boot EEPROM	
	Cypress	Atmel
38K30	CY3LV512	AT17LV512
38K50	CY3LV512	AT17LV512
38K100	CY3LV010	AT17LV010

Package Diagrams

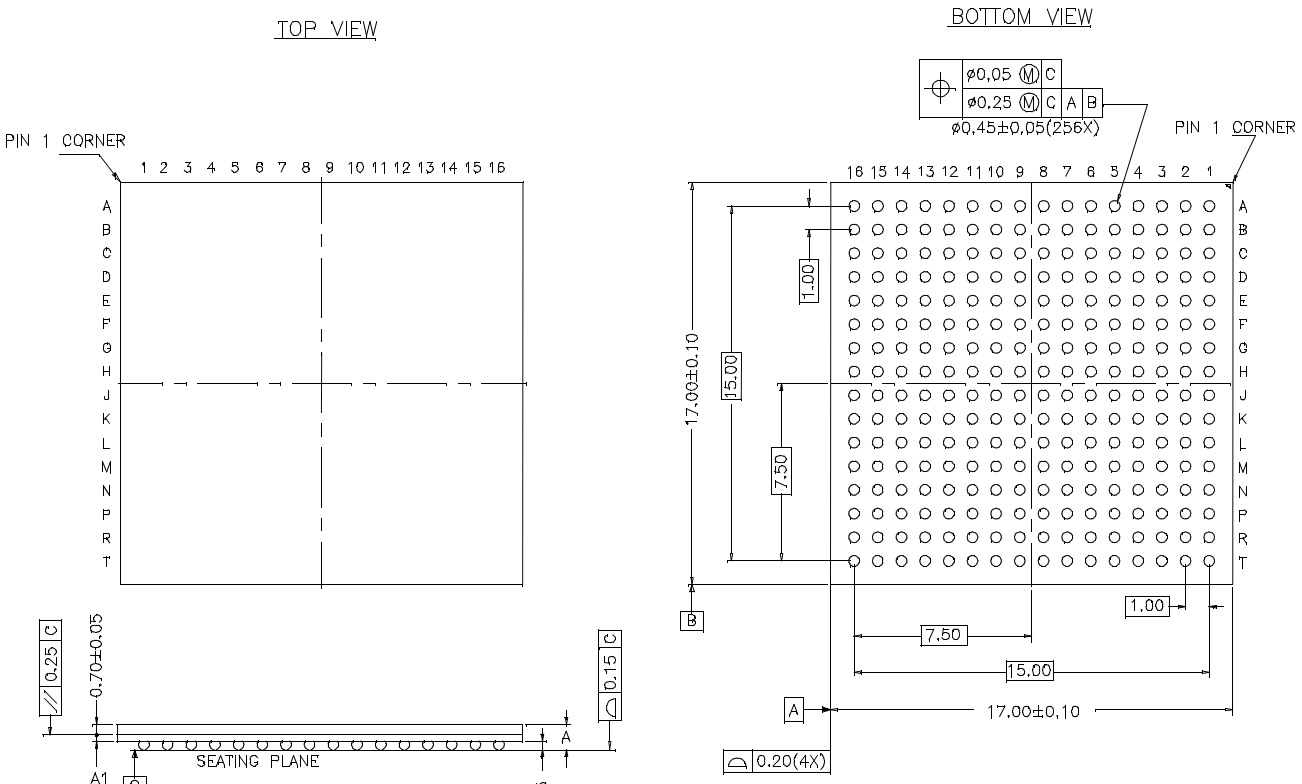
208-Lead Plastic Quad Flatpack (PQFP) N208
208-Lead Enhanced Quad Flatpack (EQFP) NT208



Note:
11. See the data sheet titled “CY3LV512/010 512K/1-Mbit CPLD Boot EEPROM” for detailed architectural and timing information.

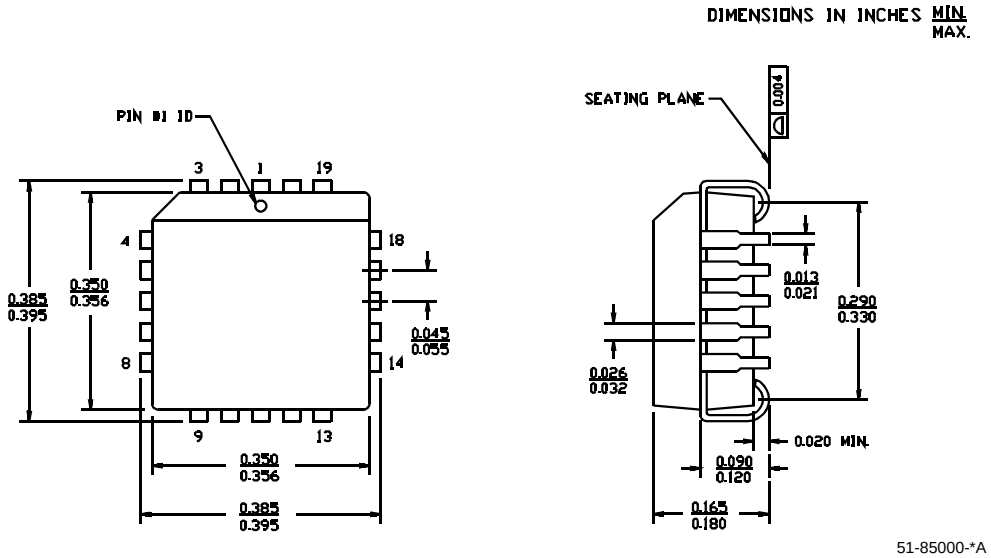
Package Diagrams (continued)

256-Ball FBGA (17 x 17 mm) BB256



A1	0.36	0.56
A	1.40 MAX.	1.60 MAX.

20-Lead Plastic Leaded Chip Carrier J61



Pin Tables

Table 2. Pin Definition Table

Pin Name	Function	Pin Description
CCLK	Output	Configuration Clock for serial interface with the external boot PROM
Config_Done	Output	Flag indicating that configuration is complete
Data	Input	Pin to receive configuration data from the external boot PROM
GCLK0-3	Input	Global Clock signals 0 through 3
CCE	Output	Chip select for the external boot PROM (active LOW)
GCTL0-3	Input	Global Control signals 0 through 3
GND	Ground	Ground
IO0	Input/Output	I/O for Bank 0
IO1	Input/Output	I/O for Bank 1
IO2	Input/Output	I/O for Bank 2
IO3	Input/Output	I/O for Bank 3
IO4	Input/Output	I/O for Bank 4
IO5	Input/Output	I/O for Bank 5
IO6	Input/Output	I/O for Bank 6
IO7	Input/Output	I/O for Bank 7
Reconfig	Input	Pin to start configuration of Quantum38K
Reset	Output	Reset signal to interface with the external boot PROM
TCLK	Input	JTAG Test Clock
TDI	Input	JTAG Test Data In
TDO	Output	JTAG Test Data Out
TMS	Input	JTAG Test Mode Select
V_{CC}	Power	Operating Voltage
V_{CCIO0}	Power	V_{CC} for I/O bank 0
V_{CCIO1}	Power	V_{CC} for I/O bank 1
V_{CCIO2}	Power	V_{CC} for I/O bank 2
V_{CCIO3}	Power	V_{CC} for I/O bank 3
V_{CCIO4}	Power	V_{CC} for I/O bank 4
V_{CCIO5}	Power	V_{CC} for I/O bank 5
V_{CCIO6}	Power	V_{CC} for I/O bank 6
V_{CCIO7}	Power	V_{CC} for I/O bank 7
V_{CCJTAG}	Power	V_{CC} for JTAG pins
V_{CCCNFG}	Power	V_{CC} for Configuration port

The following table identifies the bank assignments for the global clock and control signals for the Quantum38K devices. The bank assignments are the same for all densities and all packages.

Table 3. Global Signal Bank Assignments

Data sheet Pin Name	Bank Number
GCLK0	0
GCLK1	5
GCLK2	6
GCLK3	7
GCTL0	0
GCTL1	5
GCTL2	6
GCTL3	7

Table 4. 208 EQFP Pin Table

Pin	CY38030	CY38050	CY38100
1	GCTL0	GCTL0	GCTL0
2	GND	GND	GND
3	GCLK0	GCLK0	GCLK0
4	GND	GND	GND
5	IO0	IO0	IO0
6	IO0	IO0	IO0
7	IO0	IO0	IO0
8	IO0	IO0	IO0
9	IO0	IO0	IO0
10	IO0	IO0	IO0
11	V_{CCIO0}	V_{CCIO0}	V_{CCIO0}
12	IO0	IO0	IO0
13	IO0	IO0	IO0
14	IO0	IO0	IO0
15	IO0	IO0	IO0
16	IO0	IO0	IO0
17	IO0	IO0	IO0
18	IO0	IO0	IO0
19	IO0	IO0	IO0
20	V_{CCIO0}	V_{CCIO0}	V_{CCIO0}
21[12]	IO0	IO0	IO0
22[12]	IO0	IO0	IO0
23	V_{CC}	V_{CC}	V_{CC}
24	GND	GND	GND
25	NC	NC	V_{CC}
26	NC	NC	GND
27[12]	IO0	IO0	IO0
28	V_{CCIO0}	V_{CCIO0}	V_{CCIO0}
29	V_{CCIO1}	V_{CCIO1}	V_{CCIO1}
30[12]	IO1	IO1	IO1
31[12]	IO1	IO1	IO1
32[12]	IO1	IO1	IO1

Note:

12. Capacitance on these I/O pins meets the PCI spec (rev. 2.2), which requires IDSEL pin in a PCI design to have capacitance less than or equal to 8 pF. In the document titled “Quantum38K CPLD Family data sheet”, this spec is defined as C_{PCI}. All other I/O pins have a capacitance less than or equal to 10 pF.

Table 4. 208 EQFP Pin Table (continued)

Pin	CY38030	CY38050	CY38100
33	IO1	IO1	IO1
34	IO1	IO1	IO1
35	V_{CCIO1}	V_{CCIO1}	V_{CCIO1}
36	GND	GND	GND
37	IO1	IO1	IO1
38	IO1	IO1	IO1
39	IO1	IO1	IO1
40	IO1	IO1	IO1
41	IO1	IO1	IO1
42	IO1	IO1	IO1
43	IO1	IO1	IO1
44	IO1	IO1	IO1
45	V_{CC}	V_{CC}	V_{CC}
46	V_{CCIO1}	V_{CCIO1}	V_{CCIO1}
47	GND	GND	GND
48	IO1	IO1	IO1
49	IO1	IO1	IO1
50	IO1	IO1	IO1
51	IO1	IO1	IO1
52	V_{CCCNFG}	V_{CCCNFG}	V_{CCCNFG}
53	Data	Data	Data
54	Config_Done	Config_Done	Config_Done
55	Reset	Reset	Reset
56	Reconfig	Reconfig	Reconfig
57	CCE	CCE	CCE
58	CCLK	CCLK	CCLK
59	V_{CCCNFG}	V_{CCCNFG}	V_{CCCNFG}
60	V_{CCCNFG}	V_{CCCNFG}	V_{CCCNFG}
61	IO2	IO2	IO2
62	IO2	IO2	IO2
63	IO2	IO2	IO2
64	IO2	IO2	IO2
65	IO2	IO2	IO2
66	V_{CCIO2}	V_{CCIO2}	V_{CCIO2}
67	GND	GND	GND
68	IO2	IO2	IO2
69	IO2	IO2	IO2
70	IO2	IO2	IO2
71	IO2	IO2	IO2
72	IO2	IO2	IO2
73	GND	GND	GND
74	V_{CCIO2}	V_{CCIO2}	V_{CCIO2}
75	V_{CC}	V_{CC}	V_{CC}
76	GND	GND	GND
77	NC	NC	V_{CC}

Table 4. 208 EQFP Pin Table (continued)

Pin	CY38030	CY38050	CY38100
78	NC	NC	GND
79	IO2	IO2	IO2
80	IO2	IO2	IO2
81[12]	IO2	IO2	IO2
82[12]	IO2	IO2	IO2
83[12]	IO2	IO2	IO2
84	V_{CCIO2}	V_{CCIO2}	V_{CCIO2}
85	V_{CCIO3}	V_{CCIO3}	V_{CCIO3}
86[12]	IO3	IO3	IO3
87[12]	IO3	IO3	IO3
88[12]	IO3	IO3	IO3
89	V_{CCIO3}	V_{CCIO3}	V_{CCIO3}
90	GND	GND	GND
91	IO3	IO3	IO3
92	IO3	IO3	IO3
93	IO3	IO3	IO3
94	IO3	IO3	IO3
95	IO3	IO3	IO3
96	IO3	IO3	IO3
97	IO3	IO3	IO3
98	V_{CCIO3}	V_{CCIO3}	V_{CCIO3}
99	IO3	IO3	IO3
100	GND	GND	GND
101	IO3	IO3	IO3
102	IO3	IO3	IO3
103	IO3	IO3	IO3
104	IO3	IO3	IO3
105	IO4	IO4	IO4
106	IO4	IO4	IO4
107	IO4	IO4	IO4
108	IO4	IO4	IO4
109	IO4	IO4	IO4
110	IO4	IO4	IO4
111	V_{CCIO4}	V_{CCIO4}	V_{CCIO4}
112	GND	GND	GND
113	IO4	IO4	IO4
114	V_{CC}	V_{CC}	V_{CC}
115	IO4	IO4	IO4
116	IO4	IO4	IO4
117	IO4	IO4	IO4
118	IO4	IO4	IO4
119	IO4	IO4	IO4
120	IO4	IO4	IO4
121	IO4	IO4	IO4
122[12]	IO4	IO4	IO4

Table 4. 208 EQFP Pin Table (continued)

Pin	CY38030	CY38050	CY38100
123[12]	IO4	IO4	IO4
124	V_{CCIO4}	V_{CCIO4}	V_{CCIO4}
125	GND	GND	GND
126[12]	IO4	IO4	IO4
127	V_{CC}	V_{CC}	V_{CC}
128	GND	GND	GND
129	NC	NC	V_{CC}
130	NC	NC	GND
131	V_{CCIO4}	V_{CCIO4}	V_{CCIO4}
132	V_{CCIO5}	V_{CCIO5}	V_{CCIO5}
133[12]	IO5	IO5	IO5
134[12]	IO5	IO5	IO5
135[12]	IO5	IO5	IO5
136	IO5	IO5	IO5
137	IO5	IO5	IO5
138	V_{CCIO5}	V_{CCIO5}	V_{CCIO5}
139	IO5	IO5	IO5
140	IO5	IO5	IO5
141	IO5	IO5	IO5
142	IO5	IO5	IO5
143	IO5	IO5	IO5
144	IO5	IO5	IO5
145	IO5	IO5	IO5
146	IO5	IO5	IO5
147	IO5	IO5	IO5
148	V_{CCIO5}	V_{CCIO5}	V_{CCIO5}
149	IO5	IO5	IO5
150	IO5	IO5	IO5
151	IO5	IO5	IO5
152	GND	GND	GND
153	GCLK1	GCLK1	GCLK1
154	GND	GND	GND
155	GCTL1	GCTL1	GCTL1
156	TDO	TDO	TDO
157	TCLK	TCLK	TCLK
158	TDI	TDI	TDI
159	V_{CCJTAG}	V_{CCJTAG}	V_{CCJTAG}
160	GCLK2	GCLK2	GCLK2
161	GND	GND	GND
162	TMS	TMS	TMS
163	GCTL2	GCTL2	GCTL2
164	IO6	IO6	IO6
165	IO6	IO6	IO6
166	IO6	IO6	IO6
167	IO6	IO6	IO6

Table 4. 208 EQFP Pin Table (continued)

Pin	CY38030	CY38050	CY38100
168	IO6	IO6	IO6
169	V_{CCIO6}	V_{CCIO6}	V_{CCIO6}
170	IO6	IO6	IO6
171	IO6	IO6	IO6
172	IO6	IO6	IO6
173	IO6	IO6	IO6
174	IO6	IO6	IO6
175	IO6	IO6	IO6
176	IO6	IO6	IO6
177	GND	GND	GND
178	V_{CCIO6}	V_{CCIO6}	V_{CCIO6}
179	V_{CC}	V_{CC}	V_{CC}
180	GND	GND	GND
181	V_{CC}	V_{CC}	V_{CC}
182	GND	GND	GND
183[12]	IO6	IO6	IO6
184[12]	IO6	IO6	IO6
185[12]	IO6	IO6	IO6
186	V_{CCIO6}	V_{CCIO6}	V_{CCIO6}
187	V_{CCIO7}	V_{CCIO7}	V_{CCIO7}
188[12]	IO7	IO7	IO7
189[12]	IO7	IO7	IO7
190[12]	IO7	IO7	IO7
191	V_{CCIO7}	V_{CCIO7}	V_{CCIO7}
192	IO7	IO7	IO7
193	IO7	IO7	IO7
194	IO7	IO7	IO7
195	IO7	IO7	IO7
196	IO7	IO7	IO7
197	IO7	IO7	IO7
198	IO7	IO7	IO7
199	V_{CCIO7}	V_{CCIO7}	V_{CCIO7}
200	IO7	IO7	IO7
201	IO7	IO7	IO7
202	IO7	IO7	IO7
203	IO7	IO7	IO7
204	IO7	IO7	IO7
205	GND	GND	GND
206	GCLK3	GCLK3	GCLK3
207	GND	GND	GND
208	GCTL3	GCTL3	GCTL3

Table 5. 256 FBGA Pin Table

Pin	CY38030	CY38050	CY38100
A1	GND	GND	GND
A2	IO7	IO7	IO7
A3	IO7	IO7	IO7
A4	IO7	IO7	IO7
A5	IO7	IO7	IO7
A6	IO7	IO7	IO7
A7	NC	IO7	IO7
A8	IO6	IO6	IO6
A9	IO6	IO6	IO6
A10	IO6	IO6	IO6
A11	IO6	IO6	IO6
A12	IO6	IO6	IO6
A13	IO6	IO6	IO6
A14	IO6	IO6	IO6
A15	IO6	IO6	IO6
A16	GND	GND	GND
B1	IO0	IO0	IO0
B2	GND	GND	GND
B3	IO7	IO7	IO7
B4	IO7	IO7	IO7
B5	IO7	IO7	IO7
B6	V_{CCIO7}	V_{CCIO7}	V_{CCIO7}
B7	VCC	V_{CC}	V_{CC}
B8	IO7	IO7	IO7
B9	NC	IO6	IO6
B10	V_{CC}	V_{CC}	V_{CC}
B11	V_{CCIO6}	V_{CCIO6}	V_{CCIO6}
B12	IO6	IO6	IO6
B13	IO6	IO6	IO6
B14	IO6	IO6	IO6
B15	GND	GND	GND
B16	TDO	TDO	TDO
C1	IO0	IO0	IO0
C2	IO0	IO0	IO0
C3	GND	GND	GND
C4	IO7	IO7	IO7
C5	IO7	IO7	IO7
C6	V_{CCIO7}	V_{CCIO7}	V_{CCIO7}
C7	V_{CCIO7}	V_{CCIO7}	V_{CCIO7}
C8[12]	NC	IO7	IO7
C9[12]	IO6	IO6	IO6
C10	V_{CCIO6}	V_{CCIO6}	V_{CCIO6}
C11	V_{CCIO6}	V_{CCIO6}	V_{CCIO6}
C12	IO6	IO6	IO6

Table 5. 256 FBGA Pin Table (continued)

Pin	CY38030	CY38050	CY38100
C13	IO6	IO6	IO6
C14	GND	GND	GND
C15	TDI	TDI	TDI
C16	IO5	IO5	IO5
D1	IO0	IO0	IO0
D2	IO0	IO0	IO0
D3	IO0	IO0	IO0
D4	GND	GND	GND
D5	IO7	IO7	IO7
D6	IO7	IO7	IO7
D7	IO7	IO7	IO7
D8[12]	IO7	IO7	IO7
D9[12]	NC	IO6	IO6
D10	IO6	IO6	IO6
D11	IO6	IO6	IO6
D12	IO6	IO6	IO6
D13	GND	GND	GND
D14	TCLK	TCLK	TCLK
D15	IO5	IO5	IO5
D16	IO5	IO5	IO5
E1	IO0	IO0	IO0
E2	IO0	IO0	IO0
E3	IO0	IO0	IO0
E4	IO0	IO0	IO0
E5	IO7	IO7	IO7
E6	IO7	IO7	IO7
E7	IO7	IO7	IO7
E8[12]	IO7	IO7	IO7
E9[12]	IO6	IO6	IO6
E10	IO6	IO6	IO6
E11	IO6	IO6	IO6
E12	TMS	TMS	TMS
E13	IO5	IO5	IO5
E14	IO5	IO5	IO5
E15	IO5	IO5	IO5
E16	IO5	IO5	IO5
F1	IO0	IO0	IO0
F2	V_{CC}	V_{CC}	V_{CC}
F3	V_{CCIO0}	V_{CCIO0}	V_{CCIO0}
F4	IO0	IO0	IO0
F5	IO0	IO0	IO0
F6	IO7	IO7	IO7
F7	GCTL3	GCTL3	GCTL3
F8	GCLK3	GCLK3	GCLK3

Table 5. 256 FBGA Pin Table (continued)

Pin	CY38030	CY38050	CY38100
F9	GCTL2	GCTL2	GCTL2
F10	GCLK2	GCLK2	GCLK2
F11	IO5	IO5	IO5
F12	IO5	IO5	IO5
F13	IO5	IO5	IO5
F14	V_{CCIO5}	V_{CCIO5}	V_{CCIO5}
F15	V_{CCJTAG}	V_{CCJTAG}	V_{CCJTAG}
F16	IO5	IO5	IO5
G1	IO0	IO0	IO0
G2	NC	NC	V_{CC}
G3	V_{CCIO0}	V_{CCIO0}	V_{CCIO0}
G4	IO0	IO0	IO0
G5	IO0	IO0	IO0
G6	GCTL0	GCTL0	GCTL0
G7	GND	GND	GND
G8	GND	GND	GND
G9	GND	GND	GND
G10	GND	GND	GND
G11	GCTL1	GCTL1	GCTL1
G12	IO5	IO5	IO5
G13	IO5	IO5	IO5
G14	V_{CCIO5}	V_{CCIO5}	V_{CCIO5}
G15	NC	NC	VCC
G16	IO5	IO5	IO5
H1[12]	IO0	IO0	IO0
H2[12]	IO0	IO0	IO0
H3[12]	IO0	IO0	IO0
H4	IO0	IO0	IO0
H5	IO0	IO0	IO0
H6	GCLK0	GCLK0	GCLK0
H7	GND	GND	GND
H8	GND	GND	GND
H9	GND	GND	GND
H10	GND	GND	GND
H11	GCLK1	GCLK1	GCLK1
H12	IO5	IO5	IO5
H13	IO5	IO5	IO5
H14[12]	IO5	IO5	IO5
H15[12]	IO5	IO5	IO5
H16[12]	IO5	IO5	IO5
J1	IO1	IO1	IO1
J2	IO1	IO1	IO1
J3[12]	IO1	IO1	IO1
J4[12]	IO1	IO1	IO1

Table 5. 256 FBGA Pin Table (continued)

Pin	CY38030	CY38050	CY38100
J5[12]	IO1	IO1	IO1
J6	IO1	IO1	IO1
J7	GND	GND	GND
J8	GND	GND	GND
J9	GND	GND	GND
J10	GND	GND	GND
J11	IO4	IO4	IO4
J12[12]	IO4	IO4	IO4
J13[12]	IO4	IO4	IO4
J14[12]	IO4	IO4	IO4
J15	IO5	IO5	IO5
J16	IO5	IO5	IO5
K1	IO1	IO1	IO1
K2	V_{CC}	V_{CC}	V_{CC}
K3	V_{CCIO1}	V_{CCIO1}	V_{CCIO1}
K4	IO1	IO1	IO1
K5	IO1	IO1	IO1
K6	IO1	IO1	IO1
K7	GND	GND	GND
K8	GND	GND	GND
K9	GND	GND	GND
K10	GND	GND	GND
K11	IO4	IO4	IO4
K12	IO4	IO4	IO4
K13	IO4	IO4	IO4
K14	V_{CCIO4}	V_{CCIO4}	V_{CCIO4}
K15	V_{CC}	V_{CC}	V_{CC}
K16	IO4	IO4	IO4
L1	IO1	IO1	IO1
L2	NC	NC	V_{CC}
L3	V_{CCIO1}	V_{CCIO1}	V_{CCIO1}
L4	IO1	IO1	IO1
L5	V_{CCCNFG}	V_{CCCNFG}	V_{CCCNFG}
L6	Config_Done	Config_Done	Config_Done
L7	IO2	IO2	IO2
L8[12]	IO2	IO2	IO2
L9[12]	IO3	IO3	IO3
L10	IO3	IO3	IO3
L11	IO3	IO3	IO3
L12	IO4	IO4	IO4
L13	IO4	IO4	IO4
L14	V_{CCIO4}	V_{CCIO4}	V_{CCIO4}
L15	V_{CC}	V_{CC}	V_{CC}
L16	IO4	IO4	IO4

Table 5. 256 FBGA Pin Table (continued)

Pin	CY38030	CY38050	CY38100
M1	IO1	IO1	IO1
M2	IO1	IO1	IO1
M3	IO1	IO1	IO1
M4	Data	Data	Data
M5	Reconfig	Reconfig	Reconfig
M6	IO2	IO2	IO2
M7	IO2	IO2	IO2
M8[12]	IO2	IO2	IO2
M9[12]	IO3	IO3	IO3
M10	IO3	IO3	IO3
M11	IO3	IO3	IO3
M12	IO3	IO3	IO3
M13	IO4	IO4	IO4
M14	IO4	IO4	IO4
M15	IO4	IO4	IO4
M16	IO4	IO4	IO4
N1	IO1	IO1	IO1
N2	IO1	IO1	IO1
N3	IO1	IO1	IO1
N4	GND	GND	GND
N5	V_{CCCNFG}	V_{CCCNFG}	V_{CCCNFG}
N6	IO2	IO2	IO2
N7	IO2	IO2	IO2
N8[12]	IO2	IO2	IO2
N9[12]	IO3	IO3	IO3
N10	IO3	IO3	IO3
N11	IO3	IO3	IO3
N12	IO3	IO3	IO3
N13	GND	GND	GND
N14	IO4	IO4	IO4
N15	IO4	IO4	IO4
N16	IO4	IO4	IO4
P1	IO1	IO1	IO1
P2	IO1	IO1	IO1
P3	GND	GND	GND
P4	CCE	CCE	CCE
P5	IO2	IO2	IO2
P6	V_{CCIO2}	V_{CCIO2}	V_{CCIO2}
P7	V_{CCIO2}	V_{CCIO2}	V_{CCIO2}
P8	IO2	IO2	IO2
P9	IO2	IO2	IO2
P10	V_{CCIO3}	V_{CCIO3}	V_{CCIO3}
P11	V_{CCIO3}	V_{CCIO3}	V_{CCIO3}
P12	IO3	IO3	IO3

Table 5. 256 FBGA Pin Table (continued)

Pin	CY38030	CY38050	CY38100
P13	IO3	IO3	IO3
P14	GND	GND	GND
P15	IO4	IO4	IO4
P16	IO4	IO4	IO4
R1	IO1	IO1	IO1
R2	GND	GND	GND
R3	CCLK	CCLK	CCLK
R4	IO2	IO2	IO2
R5	IO2	IO2	IO2
R6	V_{CCCNFG}	V_{CCCNFG}	V_{CCCNFG}
R7	V_{CCIO2}	V_{CCIO2}	V_{CCIO2}
R8	IO2	IO2	IO2
R9	IO2	IO2	IO2
R10	V_{CC}	V_{CC}	V_{CC}
R11	V_{CCIO3}	V_{CCIO3}	V_{CCIO3}
R12	IO3	IO3	IO3
R13	IO3	IO3	IO3
R14	IO3	IO3	IO3
R15	GND	GND	GND
R16	IO4	IO4	IO4
T1	GND	GND	GND
T2	Reset	Reset	Reset
T3	IO2	IO2	IO2
T4	IO2	IO2	IO2
T5	IO2	IO2	IO2
T6	IO2	IO2	IO2
T7	NC	IO2	IO2
T8	IO2	IO2	IO2
T9	IO2	IO2	IO2
T10	NC	IO3	IO3
T11	IO3	IO3	IO3
T12	IO3	IO3	IO3
T13	IO3	IO3	IO3
T14	IO3	IO3	IO3
T15	IO3	IO3	IO3
T16	GND	GND	GND

Table 6. 484 FBGA Pin Table

Pin	CY38050	CY38100
A1	GND	GND
A2	GND	GND
A3	NC	NC
A4	NC	NC
A5	IO7	IO7

Table 6. 484 FBGA Pin Table (continued)

Pin	CY38050	CY38100
A6	IO7	IO7
A7	NC	IO7
A8	IO7	IO7
A9	IO7	IO7
A10	IO7	IO7

Table 6. 484 FBGA Pin Table (continued)

Pin	CY38050	CY38100
A11	GND	GND
A12	GND	GND
A13	IO6	IO6
A14	IO6	IO6
A15	IO6	IO6
A16	NC	IO6
A17	IO6	IO6
A18	IO6	IO6
A19	NC	NC
A20	NC	NC
A21	GND	GND
A22	GND	GND
B1	GND	GND
B2	GND	GND
B3	NC	NC
B4	V_{CCIO7}	V_{CCIO7}
B5	NC	IO7
B6	IO7	IO7
B7	NC	IO7
B8	IO7	IO7
B9	NC	NC
B10	IO7	IO7
B11	IO7	IO7
B12	IO6	IO6
B13	IO6	IO6
B14	NC	NC
B15	IO6	IO6
B16	NC	IO6
B17	IO6	IO6
B18	IO6	IO6
B19	V_{CCIO6}	V_{CCIO6}
B20	NC	NC
B21	GND	GND
B22	GND	GND
C1	NC	NC
C2	NC	NC
C3	NC	NC
C4	NC	IO7
C5	NC	IO7
C6	IO7	IO7
C7	NC	IO7
C8	IO7	IO7
C9	IO7	IO7
C10	IO7	IO7

Table 6. 484 FBGA Pin Table (continued)

Pin	CY38050	CY38100
C11	IO7	IO7
C12	IO6	IO6
C13	NC	IO6
C14	IO6	IO6
C15	IO6	IO6
C16	NC	IO6
C17	IO6	IO6
C18	IO6	IO6
C19	IO6	IO6
C20	NC	NC
C21	NC	NC
C22	NC	NC
D1	NC	NC
D2	V_{CCIO0}	V_{CCIO0}
D3	NC	NC
D4	GND	GND
D5	NC	IO7
D6	NC	IO7
D7	IO7	IO7
D8	IO7	IO7
D9	IO7	IO7
D10	NC	IO7
D11	IO6	IO6
D12	IO6	IO6
D13	IO6	IO6
D14	IO6	IO6
D15	IO6	IO6
D16	NC	IO6
D17	NC	IO6
D18	IO6	IO6
D19	GND	GND
D20	NC	NC
D21	V_{CCIO5}	V_{CCIO5}
D22	NC	NC
E1	NC	NC
E2	NC	NC
E3	NC	NC
E4	IO0	IO0
E5	GND	GND
E6	IO7	IO7
E7	IO7	IO7
E8	IO7	IO7
E9	V_{CCIO7}	V_{CCIO7}
E10	V_{CC}	V_{CC}

Table 6. 484 FBGA Pin Table (continued)

Pin	CY38050	CY38100
E11	IO7	IO7
E12	NC	IO6
E13	V_{CC}	V_{CC}
E14	V_{CCIO6}	V_{CCIO6}
E15	NC	IO6
E16	NC	IO6
E17	NC	IO6
E18	GND	GND
E19	TDO	TDO
E20	NC	NC
E21	NC	NC
E22	NC	NC
F1	NC	NC
F2	NC	IO0
F3	IO0	IO0
F4	IO0	IO0
F5	IO0	IO0
F6	GND	GND
F7	IO7	IO7
F8	IO7	IO7
F9	V_{CCIO7}	V_{CCIO7}
F10	V_{CCIO7}	V_{CCIO7}
F11[12]	IO7	IO7
F12[12]	IO6	IO6
F13	V_{CCIO6}	V_{CCIO6}
F14	V_{CCIO6}	V_{CCIO6}
F15	IO6	IO6
F16	NC	IO6
F17	GND	GND
F18	TDI	TDI
F19	IO5	IO5
F20	IO5	IO5
F21	NC	IO5
F22	NC	NC
G1	NC	NC
G2	IO0	IO0
G3	NC	IO0
G4	IO0	IO0
G5	IO0	IO0
G6	IO0	IO0
G7	GND	GND
G8	IO7	IO7
G9	NC	IO7
G10	IO7	IO7

Table 6. 484 FBGA Pin Table (continued)

Pin	CY38050	CY38100
G11[12]	IO7	IO7
G12[12]	IO6	IO6
G13	IO6	IO6
G14	IO6	IO6
G15	IO6	IO6
G16	GND	GND
G17	TCLK	TCLK
G18	IO5	IO5
G19	IO5	IO5
G20	IO5	IO5
G21	IO5	IO5
G22	NC	NC
H1	NC	NC
H2	IO0	IO0
H3	IO0	IO0
H4	IO0	IO0
H5	NC	IO0
H6	NC	IO0
H7	NC	IO0
H8	IO7	IO7
H9	IO7	IO7
H10	IO7	IO7
H11[12]	IO7	IO7
H12[12]	IO6	IO6
H13	IO6	IO6
H14	IO6	IO6
H15	TMS	TMS
H16	IO5	IO5
H17	IO5	IO5
H18	IO5	IO5
H19	IO5	IO5
H20	IO5	IO5
H21	IO5	IO5
H22	NC	NC
J1	NC	NC
J2	NC	NC
J3	NC	IO0
J4	NC	IO0
J5	NC	V_{CC}
J6	V_{CCIO0}	V_{CCIO0}
J7	IO0	IO0
J8	NC	IO0
J9	IO7	IO7
J10	GCTL3	GCTL3

Table 6. 484 FBGA Pin Table (continued)

Pin	CY38050	CY38100
J11	GCLK3	GCLK3
J12	GCTL2	GCTL2
J13	GCLK2	GCLK2
J14	IO5	IO5
J15	IO5	IO5
J16	IO5	IO5
J17	V_{CCIO5}	V_{CCIO5}
J18	V_{CCJTAG}	V_{CCJTAG}
J19	NC	IO5
J20	NC	IO5
J21	NC	NC
J22	NC	NC
K1	NC	NC
K2	IO0	IO0
K3	NC	IO0
K4	IO0	IO0
K5	V_{CC}	V_{CC}
K6	V_{CCIO0}	V_{CCIO0}
K7	IO0	IO0
K8	NC	IO0
K9	GCTL0	GCTL0
K10	GND	GND
K11	GND	GND
K12	GND	GND
K13	GND	GND
K14	GCTL1	GCTL1
K15	NC	IO5
K16	IO5	IO5
K17	V_{CCIO5}	V_{CCIO5}
K18	NC	V_{CC}
K19	NC	IO5
K20	NC	IO5
K21	NC	IO5
K22	NC	NC
L1	GND	GND
L2	IO0	IO0
L3	IO0	IO0
L4[12]	IO0	IO0
L5[12]	IO0	IO0
L6[12]	IO0	IO0
L7	IO0	IO0
L8	NC	IO0
L9	GCLK0	GCLK0
L10	GND	GND

Table 6. 484 FBGA Pin Table (continued)

Pin	CY38050	CY38100
L11	GND	GND
L12	GND	GND
L13	GND	GND
L14	GCLK1	GCLK1
L15	NC	IO5
L16	IO5	IO5
L17[12]	IO5	IO5
L18[12]	IO5	IO5
L19[12]	IO5	IO5
L20	IO5	IO5
L21	NC	IO5
L22	GND	GND
M1	GND	GND
M2	NC	IO1
M3	IO1	IO1
M4	IO1	IO1
M5	NC	IO1
M6[12]	IO1	IO1
M7[12]	IO1	IO1
M8[12]	IO1	IO1
M9	IO1	IO1
M10	GND	GND
M11	GND	GND
M12	GND	GND
M13	GND	GND
M14	IO4	IO4
M15[12]	IO4	IO4
M16[12]	IO4	IO4
M17[12]	IO4	IO4
M18	NC	IO5
M19	NC	IO5
M20	IO4	IO4
M21	IO4	IO4
M22	GND	GND
N1	NC	NC
N2	NC	IO1
N3	NC	IO1
N4	NC	IO1
N5	V_{CC}	V_{CC}
N6	V_{CCIO1}	V_{CCIO1}
N7	IO1	IO1
N8	NC	IO1
N9	NC	IO1
N10	GND	GND

Table 6. 484 FBGA Pin Table (continued)

Pin	CY38050	CY38100
N11	GND	GND
N12	GND	GND
N13	GND	GND
N14	NC	IO4
N15	IO4	IO4
N16	IO4	IO4
N17	V_{CCIO4}	V_{CCIO4}
N18	V_{CC}	V_{CC}
N19	NC	IO4
N20	NC	IO4
N21	NC	IO4
N22	NC	NC
P1	NC	NC
P2	NC	NC
P3	IO1	IO1
P4	NC	IO1
P5	V_{CC}	V_{CC}
P6	V_{CCIO1}	V_{CCIO1}
P7	NC	IO1
P8	V_{CCCNFG}	V_{CCCNFG}
P9	Config_Done	Config_Done
P10	IO2	IO2
P11[12]	IO2	IO2
P12[12]	IO3	IO3
P13	IO3	IO3
P14	IO3	IO3
P15	NC	IO4
P16	IO4	IO4
P17	V_{CCIO4}	V_{CCIO4}
P18	V_{CC}	V_{CC}
P19	NC	IO4
P20	NC	IO4
P21	NC	NC
P22	NC	NC
R1	NC	NC
R2	NC	IO1
R3	IO1	IO1
R4	IO1	IO1
R5	IO1	IO1
R6	IO1	IO1
R7	Data	Data
R8	Reconfig	Reconfig
R9	IO2	IO2
R10	IO2	IO2

Table 6. 484 FBGA Pin Table (continued)

Pin	CY38050	CY38100
R11[12]	IO2	IO2
R12[12]	IO3	IO3
R13	IO3	IO3
R14	IO3	IO3
R15	NC	IO3
R16	NC	IO4
R17	NC	IO4
R18	NC	IO4
R19	IO4	IO4
R20	IO4	IO4
R21	IO4	IO4
R22	NC	NC
T1	NC	NC
T2	IO1	IO1
T3	IO1	IO1
T4	IO1	IO1
T5	IO1	IO1
T6	IO1	IO1
T7	GND	GND
T8	V_{CCCNFG}	V_{CCCNFG}
T9	IO2	IO2
T10	IO2	IO2
T11[12]	IO2	IO2
T12[12]	IO3	IO3
T13	IO3	IO3
T14	IO3	IO3
T15	IO3	IO3
T16	GND	GND
T17	IO4	IO4
T18	IO4	IO4
T19	IO4	IO4
T20	IO4	IO4
T21	IO4	IO4
T22	NC	NC
U1	NC	NC
U2	IO1	IO1
U3	IO1	IO1
U4	IO1	IO1
U5	IO1	IO1
U6	GND	GND
U7	CCE	CCE
U8	IO2	IO2
U9	V_{CCIO2}	V_{CCIO2}
U10	V_{CCIO2}	V_{CCIO2}

Table 6. 484 FBGA Pin Table (continued)

Pin	CY38050	CY38100
U11	IO2	IO2
U12	IO2	IO2
U13	V_{CCIO3}	V_{CCIO3}
U14	V_{CCIO3}	V_{CCIO3}
U15	IO3	IO3
U16	IO3	IO3
U17	GND	GND
U18	IO4	IO4
U19	IO4	IO4
U20	IO4	IO4
U21	IO4	IO4
U22	NC	NC
V1	NC	NC
V2	NC	NC
V3	NC	NC
V4	NC	NC
V5	GND	GND
V6	CCLK	CCLK
V7	IO2	IO2
V8	NC	IO2
V9	V_{CCCNFG}	V_{CCCNFG}
V10	V_{CCIO2}	V_{CCIO2}
V11	IO2	IO2
V12	IO2	IO2
V13	NC	V_{CC}
V14	V_{CCIO3}	V_{CCIO3}
V15	IO3	IO3
V16	IO3	IO3
V17	IO3	IO3
V18	GND	GND
V19	NC	NC
V20	NC	NC
V21	NC	NC
V22	NC	NC
W1	NC	NC
W2	V_{CCIO1}	V_{CCIO1}
W3	NC	NC
W4	GND	GND
W5	Reset	Reset
W6	IO2	IO2
W7	NC	IO2
W8	IO2	IO2
W9	NC	IO2
W10	NC	IO2

Table 6. 484 FBGA Pin Table (continued)

Pin	CY38050	CY38100
W11	IO2	IO2
W12	IO2	IO2
W13	NC	IO3
W14	NC	IO3
W15	IO3	IO3
W16	IO3	IO3
W17	IO3	IO3
W18	NC	IO3
W19	GND	GND
W20	NC	NC
W21	V_{CCIO4}	V_{CCIO4}
W22	NC	NC
Y1	NC	NC
Y2	NC	NC
Y3	NC	NC
Y4	IO2	IO2
Y5	IO2	IO2
Y6	IO2	IO2
Y7	IO2	IO2
Y8	NC	IO2
Y9	NC	IO2
Y10	IO2	IO2
Y11	IO2	IO2
Y12	IO3	IO3
Y13	IO3	IO3
Y14	IO3	IO3
Y15	IO3	IO3
Y16	IO3	IO3
Y17	IO3	IO3
Y18	NC	IO3
Y19	NC	IO3
Y20	NC	NC
Y21	NC	NC
Y22	NC	NC
AA1	GND	GND
AA2	GND	GND
AA3	NC	NC
AA4	V_{CCIO2}	V_{CCIO2}
AA5	IO2	IO2
AA6	IO2	IO2
AA7	NC	IO2
AA8	IO2	IO2
AA9	NC	NC
AA10	NC	IO2

Table 6. 484 FBGA Pin Table (continued)

Pin	CY38050	CY38100
AA11	IO2	IO2
AA12	IO3	IO3
AA13	IO3	IO3
AA14	NC	NC
AA15	IO3	IO3
AA16	NC	IO3
AA17	NC	IO3
AA18	IO3	IO3
AA19	V_{CCIO3}	V_{CCIO3}
AA20	NC	NC
AA21	GND	GND
AA22	GND	GND
AB1	GND	GND
AB2	GND	GND
AB3	NC	NC
AB4	NC	NC
AB5	IO2	IO2
AB6	IO2	IO2
AB7	IO2	IO2
AB8	NC	IO2
AB9	NC	IO2
AB10	NC	IO2
AB11	GND	GND
AB12	GND	GND
AB13	IO3	IO3
AB14	IO3	IO3
AB15	IO3	IO3
AB16	NC	IO3
AB17	IO3	IO3
AB18	NC	IO3
AB19	NC	NC
AB20	NC	NC
AB21	GND	GND
AB22	GND	GND

Document History Page

Document Title: Quantum38K™ ISR™ CPLDs Designed for Migration Document Number: 38-03043				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106747	04/25/01	SZV	New Data Sheet Convert from Spec number 38-01058 to 38-03043
*A	108380	07/19/01	RN	Deleted 38K15 device from the data sheet. Deleted 144FBGA package from the data sheet. Changed ESD spec from “MIL-STD-883” to “JEDEC EIA./JESD22-A114-A“. Changed the two bin offerings for all devices from “83 MHz and 66 MHz” to “125 MHz and 83 MHz” respectively Changed the timing specs accordingly Changed the part ordering information accordingly Added paragraph about Quantum38K being CompactPCI hot swap Ready. Updated I/O standard Timing Delay Specs and changed the default I/O standard from 3.3V PCI to LVCMOS. Added Standby ICC Spec
*B	109680	09/25/01	RN	Removed revision ‘B’ from CY38K100 part number Removed errata from CY38K100 devices, as it is no longer applicable 208-pin package will now be “Thermally Enhanced Quad Flat Pack” (208-EQFP) instead of Plastic Quad Flat Pack (PQFP) for better heat dissipation and power management
*C	111959	12/21/01	RN	Combine with spec# 38-04042
*D	112947	04/23/02	RN	Updated pinouts for Quantum38K30 and Quantum38K50 packages Updated Standby current (ICC0) spec on page 13 Added a section titled “Family, Package and Density Migration in Quantum38K CPLDs” on page 10 Added slow slew rate timing delay adjustments to table on page 18 Added Table 3 on page 28 identifying bank assignments of global control/clock signals
*E	117519	09/17/02	OOR	Changed data sheet status from Preliminary to Final Added note #4 to DC Characteristics (p.12)
*F	122239	12/28/02	RBI	Power up requirements added to Operating Range Information
*G	125910	04/22/03	OOR	Added note to title page: “Use Delta39K CPLD For All New Designs”