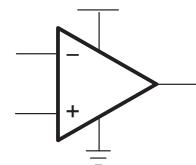


TLV2370, TLV2371, TLV2372, TLV2373, TLV2374, TLV2375 FAMILY OF 550- μ A/Ch 3-MHz RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS270D – MARCH 2001 – REVISED JANUARY 2005

- Rail-To-Rail Input/Output
- Wide Bandwidth . . . 3 MHz
- High Slew Rate . . . 2.4 V/ μ s
- Supply Voltage Range . . . 2.7 V to 16 V
- Supply Current . . . 550 μ A/Channel
- Low Power Shutdown Mode
 $I_{DD(SHDN)}$. . . 25 μ A/Channel
- Input Noise Voltage . . . 39 nV/ $\sqrt{\text{Hz}}$
- Input Bias Current . . . 1 pA
- Specified Temperature Range
–40°C to 125°C . . . Industrial Grade
- Ultrasmall Packaging
5 or 6 Pin SOT-23 (TLV2370/1)
8 or 10 Pin MSOP (TLV2372/3)

Operational Amplifier



description

The TLV237x single supply operational amplifiers provide rail-to-rail input and output capability. The TLV237x takes the minimum operating supply voltage down to 2.7 V over the extended industrial temperature range while adding the rail-to-rail output swing feature. The TLV237x also provides 3-MHz bandwidth from only 550 μ A. The maximum recommended supply voltage is 16 V, which allows the devices to be operated from (\pm 8 V supplies down to \pm 1.35 V) a variety of rechargeable cells.

The CMOS inputs enable use in high-impedance sensor interfaces, with the lower voltage operation making an ideal alternative for the TLC227x in battery-powered applications. The rail-to-rail input stage further increases its versatility. The TLV237x is the seventh member of a rapidly growing number of RRIO products available from TI, and it is the first to allow operation up to 16-V rails with good ac performance.

All members are available in PDIP and SOIC with the singles in the small SOT-23 package, duals in the MSOP, and quads in the TSSOP package.

The 2.7-V operation makes the TLV237x compatible with Li-Ion powered systems and the operating supply voltage range of many micro-power microcontrollers available today including TI's MSP430.

SELECTION OF SIGNAL AMPLIFIER PRODUCTS[†]

DEVICE	V _{DD} (V)	V _{IO} (μ V)	I _{Q/Ch} (μ A)	I _{IB} (pA)	GBW (MHz)	SR (V/ μ s)	SHUTDOWN	RAIL-TO-RAIL	SINGLES/DUALS/QUADS
TLV237x	2.7–16	500	550	1	3	2.4	Yes	I/O	S/D/Q
TLC227x	4–16	300	1100	1	2.2	3.6	—	O	D/Q
TLV27x	2.7–16	500	550	1	3	2.4	—	O	S/D/Q
TLC27x	3–16	1100	675	1	1.7	3.6	—	—	S/D/Q
TLV246x	2.7–6	150	550	1300	6.4	1.6	Yes	I/O	S/D/Q
TLV247x	2.7–6	250	600	2	2.8	1.5	Yes	I/O	S/D/Q
TLV244x	2.7–10	300	725	1	1.8	1.4	—	O	D/Q

[†] Typical values measured at 5 V, 25°C



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**TLV2370, TLV2371, TLV2372, TLV2373, TLV2374, TLV2375
FAMILY OF 550- μ A/Ch 3-MHz RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN**

SLOS270D – MARCH 2001 – REVISED JANUARY 2005

FAMILY PACKAGE TABLE(1)

DEVICE	NUMBER OF CHANNELS	PACKAGE TYPES					SHUTDOWN	UNIVERSAL EVM BOARD
		PDIP	SOIC	SOT-23	TSSOP	MSOP		
TLV2370	1	8	8	6	—	—	Yes	Refer to the EVM Selection Guide (Lit# SLOU060)
TLV2371	1	8	8	5	—	—	—	
TLV2372	2	8	8	—	—	8	—	
TLV2373	2	14	14	—	—	10	Yes	
TLV2374	4	14	14	—	14	—	—	
TLV2375	4	16	16	—	16	—	Yes	

TLV2370 and TLV2371 AVAILABLE OPTIONS(1)

TA	V _{IO} MAX AT 25°C	PACKAGED DEVICES				PLASTIC DIP (P)	
		SMALL OUTLINE (D)†	SOT-23		SYMBOL		
			(DBV)‡	(DBV)‡			
–40°C to 125°C	4.5 mV	TLV2370ID TLV2371ID	TLV2370IDBV TLV2371IDBV	VBFI VBGI	TLV2370IP TLV2371IP		

† This package is available taped and reeled. To order this packaging option, add an **R** suffix to the part number (e.g., TLV2370IDR).

‡ This package is only available taped and reeled. For standard quantities (3,000 pieces per reel), add an **R** suffix (e.g., TLV2370IDBVR). For smaller quantities (250 pieces per mini-reel), add a **T** suffix to the part number (e.g., TLV2370IDBVT).

TLV2372 AND TLV2373 AVAILABLE OPTIONS(1)

TA	V _{IO} MAX AT 25°C	PACKAGED DEVICES					PLASTIC DIP (N)	PLASTIC DIP (P)		
		SMALL OUTLINE (D)§	MSOP			SYMBOL				
			(DGK)§	SYMBOL	(DGS)§					
–40°C to 125°C	4.5 mV	TLV2372ID TLV2373ID	TLV2372IDGK —	APG —	— TLV2373IDGS	— API	— TLV2373IN	TLV2372IP —		

§ This package is available taped and reeled. To order this packaging option, add an **R** suffix to the part number (e.g., TLV2372IDR).

TLV2374 and TLV2375 AVAILABLE OPTIONS(1)

TA	V _{IO} MAX AT 25°C	PACKAGED DEVICES			TSSOP (PW)¶
		SMALL OUTLINE (D)¶	PLASTIC DIP (N)	SYMBOL	
–40°C to 125°C	4.5 mV	TLV2374ID TLV2375ID	TLV2374IN TLV2375IN	TLV2374IPW TLV2375IPW	

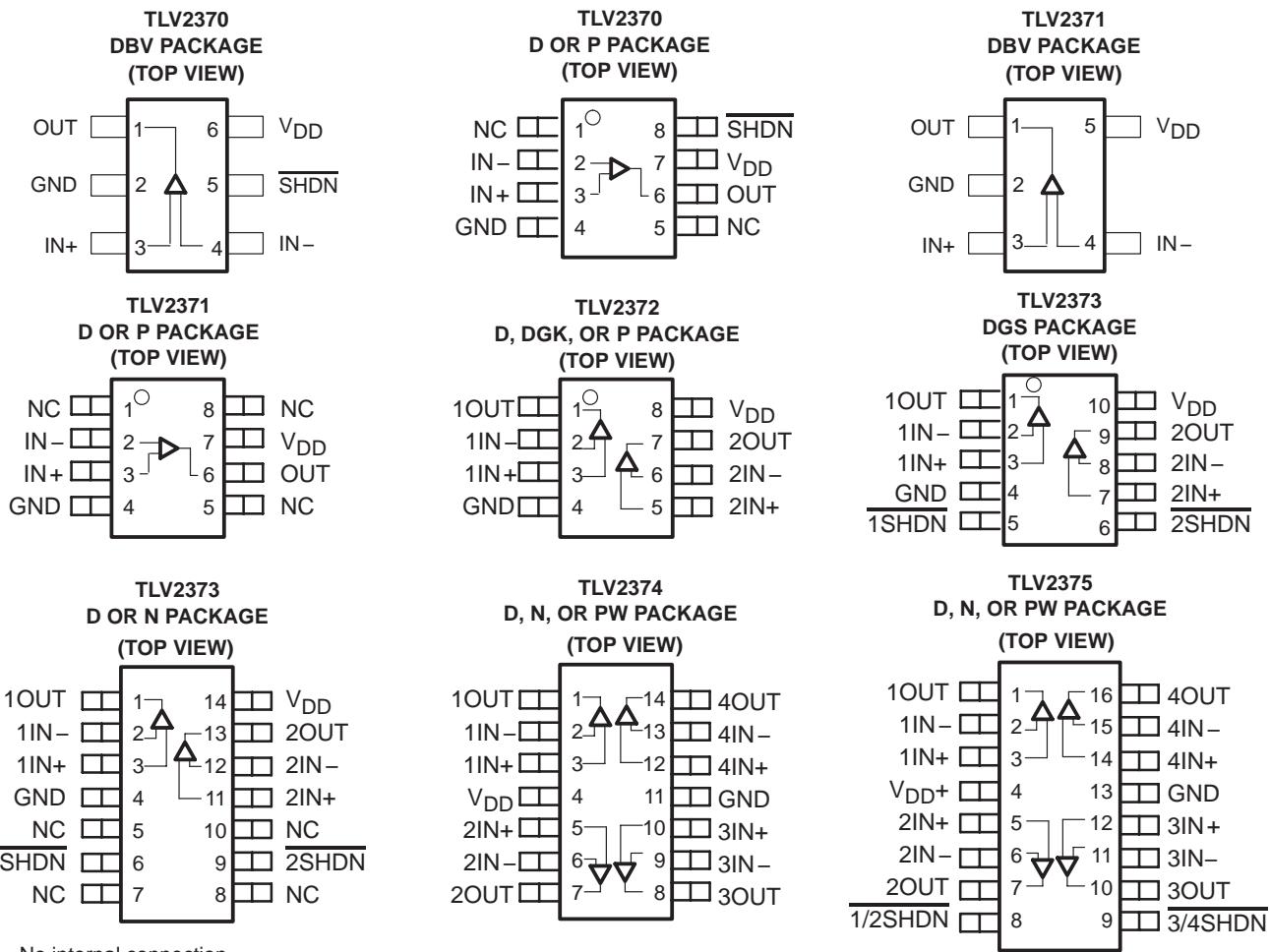
¶ This package is available taped and reeled. To order this packaging option, add an **R** suffix to the part number (e.g., TLV2374IDR).

1. For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

**TLV2370, TLV2371, TLV2372, TLV2373, TLV2374, TLV2375
FAMILY OF 550- μ A/Ch 3-MHz RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN**

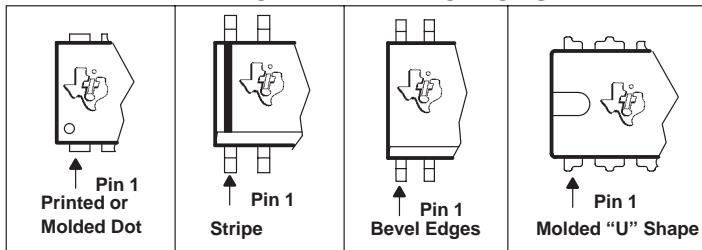
SLOS270D – MARCH 2001 – REVISED JANUARY 2005

TLV237x PACKAGE PINOUTS⁽¹⁾



NC – No internal connection

TYPICAL PIN 1 INDICATORS



NOTE: (1) If there is not a Pin 1 indicator, turn device to enable reading the symbol from the left to right. Pin 1 is at the lower left corner of the device.

**TLV2370, TLV2371, TLV2372, TLV2373, TLV2374, TLV2375
FAMILY OF 550- μ A/Ch 3-MHz RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN**

SLOS270D – MARCH 2001 – REVISED JANUARY 2005

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{DD} (see Note 1)	16.5 V
Differential input voltage, V_{ID}	$\pm V_{DD}$
Input voltage range, V_I (see Note 1)	–0.2 V to V_{DD} + 0.2 V
Input current range, I_I	± 10 mA
Output current range, I_O	± 100 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : I-suffix	–40°C to 125°C
Maximum junction temperature, T_J	150°C
Storage temperature range, T_{STG}	–65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltage values, except differential voltages, are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	$T_A \leq 25^\circ\text{C}$ POWER RATING
D (8)	38.3	176	710 mW
D (14)	26.9	122.3	1022 mW
D (16)	25.7	114.7	1090 mW
DBV (5)	55	324.1	385 mW
DBV (6)	55	294.3	425 mW
DGK (8)	54.23	259.96	481 mW
DGS (10)	54.1	257.71	485 mW
N (14, 16)	32	78	1600 mW
P (8)	41	104	1200 mW
PW (14)	29.3	173.6	720 mW
PW (16)	28.7	161.4	774 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}	Single supply	2.7	16	V
	Split supply	± 1.35	± 8	
Common-mode input voltage range, V_{ICR}		0	V_{DD}	V
Operating free-air temperature, T_A	I-suffix	–40	125	°C
Turnon voltage level, $V_{(ON)}$, relative to GND pin voltage			2	V
Turnoff voltage level, $V_{(OFF)}$, relative to GND pin voltage			0.8	V

**TLV2370, TLV2371, TLV2372, TLV2373, TLV2374, TLV2375
FAMILY OF 550- μ A/Ch 3-MHz RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN**

SLOS270D – MARCH 2001 – REVISED JANUARY 2005

electrical characteristics at specified free-air temperature, $V_{DD} = 2.7$ V, 5 V, and 15 V (unless otherwise noted)

dc performance

PARAMETER		TEST CONDITIONS		T _A	MIN	TYP	MAX	UNIT
V _{IO}	Input offset voltage	$V_{IC} = V_{DD}/2$, $R_S = 50 \Omega$	$V_O = V_{DD}/2$,	25°C		2	4.5	mV
				Full range			6	
αV_{IO}	Offset voltage drift			25°C		2		μ V/°C
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ to V_{DD} , $R_S = 50 \Omega$	$V_{DD} = 2.7$ V	25°C	50	68		dB
				Full range	49			
				25°C	56	70		
				Full range	54			
		$V_{IC} = 0$ to $V_{DD} - 1.35$ V, $R_S = 50 \Omega$	$V_{DD} = 5$ V	25°C	55	72		
				Full range	54			
				25°C	67	80		
				Full range	64			
		$V_{IC} = 0$ to V_{DD} , $R_S = 50 \Omega$	$V_{DD} = 15$ V	25°C	64	82		
				Full range	63			
				25°C	67	84		
				Full range	66			
AVD	Large-signal differential voltage amplification	$V_O(PP) = V_{DD}/2$, $R_L = 10$ k Ω	$V_{DD} = 2.7$ V	25°C	98	106		dB
				Full range	76			
				25°C	100	110		
				Full range	86			
		$V_{DD} = 5$ V	$V_{DD} = 15$ V	25°C	81	83		
				Full range	79			

input characteristics

PARAMETER		TEST CONDITIONS		T _A	MIN	TYP	MAX	UNIT
I _{IO}	Input offset current	$V_{DD} = 15$ V, $V_O = V_{DD}/2$	$V_{IC} = V_{DD}/2$,	25°C		1	60	pA
				70°C			100	
				125°C			1000	
I _{IB}	Input bias current			25°C	1	60		pA
				70°C			100	
				125°C			1000	
I _{i(d)}	Differential input resistance			25°C		1000		G Ω
C _{IC}	Common-mode input capacitance	$f = 21$ kHz		25°C		8		pF

**TLV2370, TLV2371, TLV2372, TLV2373, TLV2374, TLV2375
FAMILY OF 550- μ A/Ch 3-MHz RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN**

SLOS270D – MARCH 2001 – REVISED JANUARY 2005

electrical characteristics at specified free-air temperature, $V_{DD} = 2.7$ V, 5 V, and 15 V (unless otherwise noted) (continued)

output characteristics

PARAMETER	TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
VOH High-level output voltage	VIC = VDD/2, IOH = -1 mA	25°C	2.55	2.58		V
		Full range	2.48			
		25°C	4.9	4.93		
		Full range	4.85			
		25°C	14.92	14.96		
		Full range	14.9			
	VIC = VDD/2, IOH = -5 mA	25°C	1.9	2		
		Full range	1.6			
		25°C	4.6	4.68		
		Full range	4.5			
		25°C	14.7	14.8		
		Full range	14.6			
VOL Low-level output voltage	VIC = VDD/2, IOL = 1 mA	25°C	0.1	0.15		V
		Full range	0.22			
		25°C	0.05	0.1		
		Full range	0.15			
		25°C	0.05	0.08		
		Full range	0.1			
	VIC = VDD/2, IOL = 5 mA	25°C	0.52	0.7		
		Full range	1.1			
		25°C	0.28	0.4		
		Full range	0.5			
		25°C	0.19	0.3		
		Full range	0.35			
IO Output current	VDD = 2.7 V, VO = 0.5 V from rail	Positive rail	25°C	4		mA
		Negative rail	25°C	5		
	VDD = 5 V, VO = 0.5 V from rail	Positive rail	25°C	7		
		Negative rail	25°C	8		
	VDD = 15 V, VO = 0.5 V from rail	Positive rail	25°C	16		
		Negative rail	25°C	15		

power supply

PARAMETER	TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
IDD Supply current (per channel)	VO = VDD/2,	VDD = 2.7 V	25°C	470	560	μ A
		VDD = 5 V	25°C	550	660	
		VDD = 15 V	25°C	750	900	
		Full range			1200	
PSRR Supply voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	VDD = 2.7 V to 15 V, No load	VIC = VDD/2,	25°C	70	80	dB
			Full range	65		

**TLV2370, TLV2371, TLV2372, TLV2373, TLV2374, TLV2375
FAMILY OF 550- μ A/Ch 3-MHz RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN**

SLOS270D – MARCH 2001 – REVISED JANUARY 2005

electrical characteristics at specified free-air temperature, $V_{DD} = 2.7$ V, 5 V, and 15 V (unless otherwise noted) (continued)

dynamic performance

PARAMETER		TEST CONDITIONS		TA	MIN	TYP	MAX	UNIT
UGBW	Unity gain bandwidth	$R_L = 2$ k Ω , $C_L = 10$ pF	$V_{DD} = 2.7$ V	25°C	2.4			MHz
			$V_{DD} = 5$ V to 15 V	25°C	3			
SR	Slew rate at unity gain	$V_O(PP) = V_{DD}/2$, $C_L = 50$ pF, $R_L = 10$ k Ω	$V_{DD} = 2.7$ V	25°C	1.4	2		V/ μ s
				Full range	1			
			$V_{DD} = 5$ V	25°C	1.6	2.4		V/ μ s
				Full range	1.2			
		$V_{DD} = 15$ V	25°C	1.9	2.1			V/ μ s
				Full range	1.4			
ϕ_m	Phase margin	$R_L = 2$ k Ω ,	$C_L = 100$ pF	25°C	65°			
	Gain margin	$R_L = 2$ k Ω ,	$C_L = 10$ pF	25°C	18			dB
t_s	Settling time	$V_{DD} = 2.7$ V, $V_{O(STEP)PP} = 1$ V, $A_V = -1$, $C_L = 10$ pF, $R_L = 2$ k Ω	0.1%	25°C	2.9			μ s
		$V_{DD} = 5$ V, 15 V, $V_{O(STEP)PP} = 1$ V, $A_V = -1$, $C_L = 47$ pF, $R_L = 2$ k Ω	0.1%		2			

noise/distortion performance

PARAMETER		TEST CONDITIONS		TA	MIN	TYP	MAX	UNIT
THD + N	Total harmonic distortion plus noise	$V_{DD} = 2.7$ V, $V_O(PP) = V_{DD}/2$ V, $R_L = 2$ k Ω , $f = 10$ kHz	$A_V = 1$	25°C	0.02%			
			$A_V = 10$		0.05%			
			$A_V = 100$		0.18%			
		$V_{DD} = 5$ V, 15 V, $V_O(PP) = V_{DD}/2$ V, $R_L = 2$ k Ω , $f = 10$ kHz	$A_V = 1$	25°C	0.02%			
			$A_V = 10$		0.09%			
			$A_V = 100$		0.5%			
		$f = 1$ kHz		25°C	39			nV/ \sqrt Hz
					35			
V_n	Equivalent input noise voltage	$f = 10$ kHz		25°C	0.6			fA/ \sqrt Hz
I_n	Equivalent input noise current	$f = 1$ kHz		25°C				

shutdown characteristics

PARAMETER		TEST CONDITIONS		TA	MIN	TYP	MAX	UNIT
$I_{DD(SHDN)}$	Supply current in shutdown mode (TLV2370, TLV2371, TLV2372, TLV2373, TLV2374, TLV2375) (per channel)	$V_{DD} = 2.7$ V, 5 V, $SHDN = 0$ V	$25^\circ C$	25°C	25	30		μ A
			Full range		35			
		$V_{DD} = 15$ V, $SHDN = 0$ V	$25^\circ C$	25°C	40	45		μ A
			Full range		50			
$t_{(on)}$	Amplifier turnon time (see Note 2)	$R_L = 2$ k Ω	$25^\circ C$	25°C	0.8			μ s
$t_{(off)}$	Amplifier turnoff time (see Note 2)		$25^\circ C$	25°C	1			μ s

NOTE: Disable time and enable time are defined as the interval between application of the logic signal to the SHDN terminal and the point at which the supply current has reached one half of its final value.

**TLV2370, TLV2371, TLV2372, TLV2373, TLV2374, TLV2375
FAMILY OF 550- μ A/Ch 3-MHz RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN**

SLOS270D – MARCH 2001 – REVISED JANUARY 2005

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	vs Common-mode input voltage	1, 2, 3
CMRR	Common-mode rejection ratio	vs Frequency	4
	Input bias and offset current	vs Free-air temperature	5
V_{OL}	Low-level output voltage	vs Low-level output current	6, 8, 10
V_{OH}	High-level output voltage	vs High-level output current	7, 9, 11
$V_{O(PP)}$	Peak-to-peak output voltage	vs Frequency	12
I_{DD}	Supply current	vs Supply voltage	13
PSRR	Power supply rejection ratio	vs Frequency	14
A_{VD}	Differential voltage gain & phase	vs Frequency	15
	Gain-bandwidth product	vs Free-air temperature	16
SR	Slew rate	vs Supply voltage	17
		vs Free-air temperature	18
ϕ_m	Phase margin	vs Capacitive load	19
V_n	Equivalent input noise voltage	vs Frequency	20
		Voltage-follower large-signal pulse response	21, 22
		Voltage-follower small-signal pulse response	23
	Inverting large-signal response		24, 25
	Inverting small-signal response		26
	Crosstalk	vs Frequency	27
	Shutdown forward & reverse isolation	vs Frequency	28
$I_{DD(SHDN)}$	Shutdown supply current	vs Supply voltage	29
$I_{DD(SHDN)}$	Shutdown pin leakage current	vs Shutdown pin voltage	30
$I_{DD(SHDN)}$	Shutdown supply current/output voltage	vs Time	31, 32

TYPICAL CHARACTERISTICS

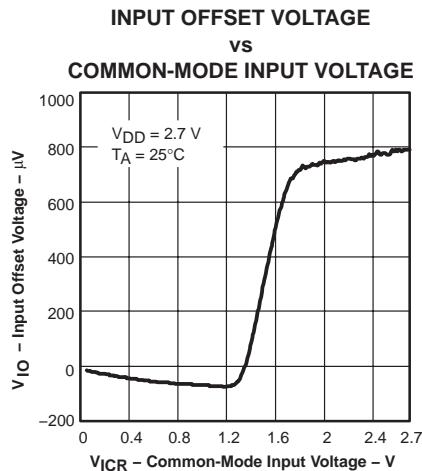


Figure 1

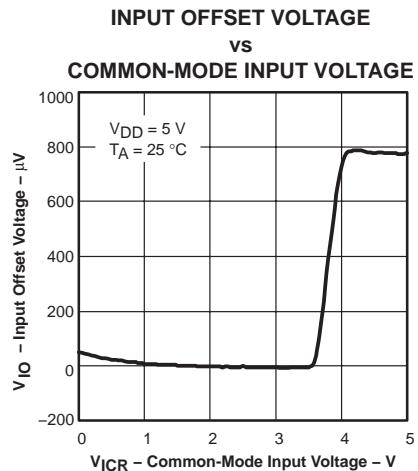


Figure 2

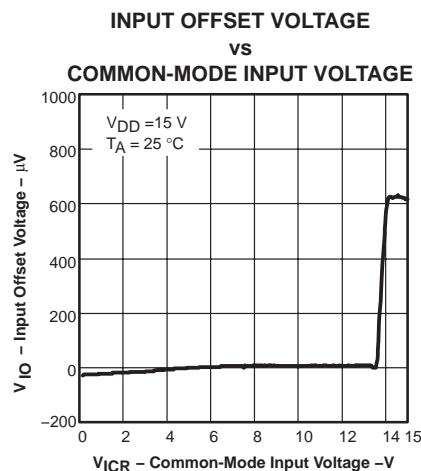


Figure 3

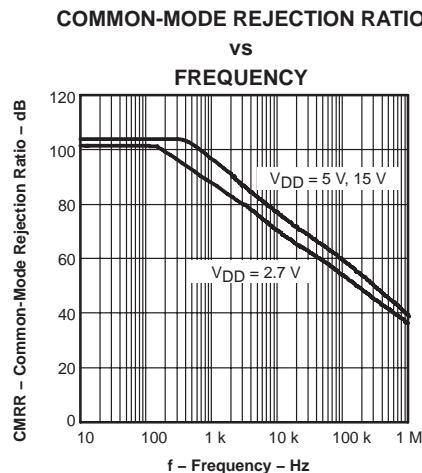


Figure 4

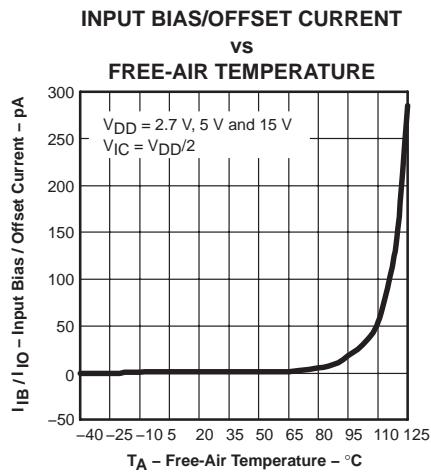


Figure 5

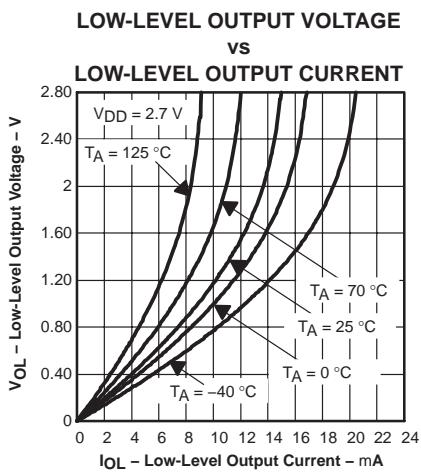


Figure 6

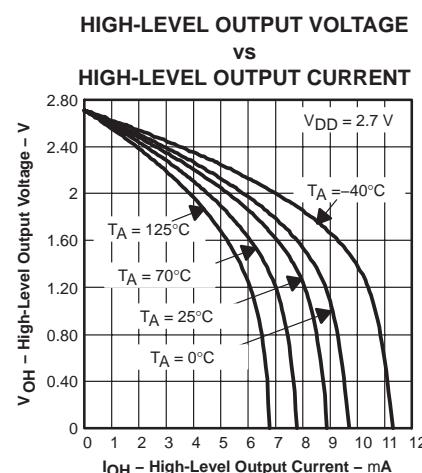


Figure 7

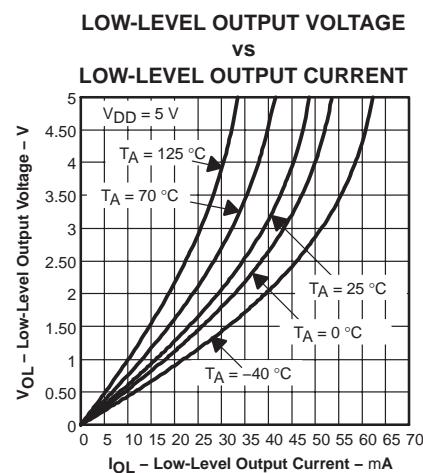


Figure 8

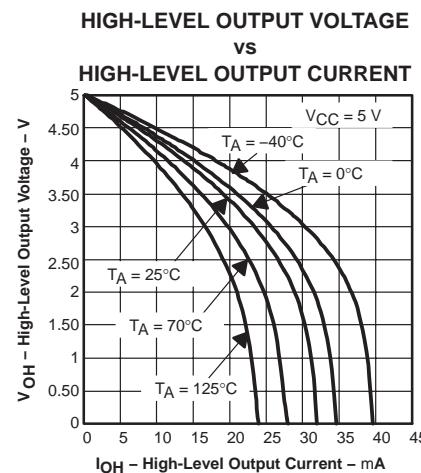
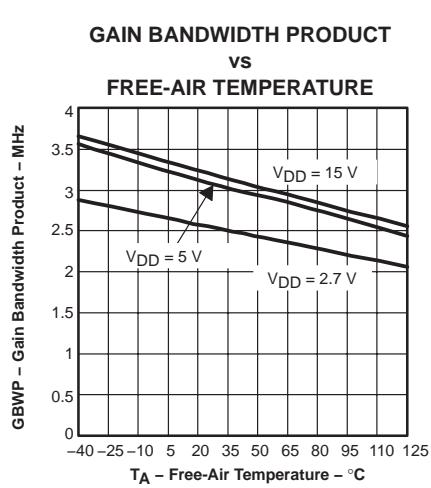
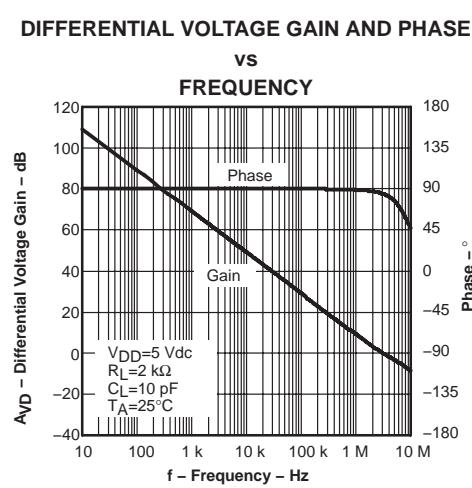
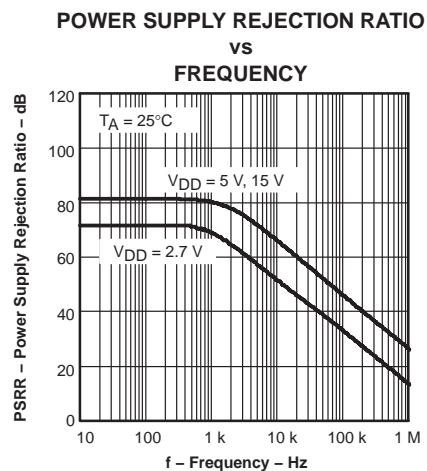
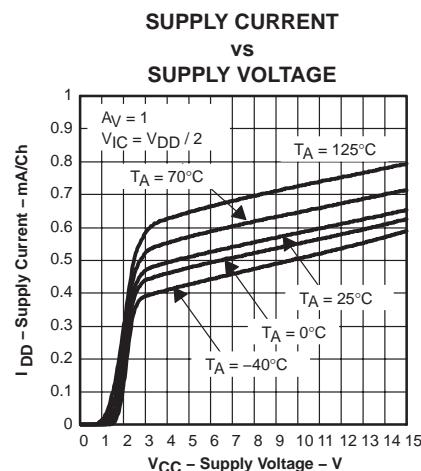
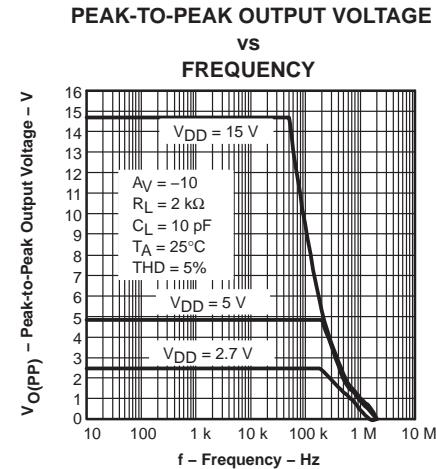
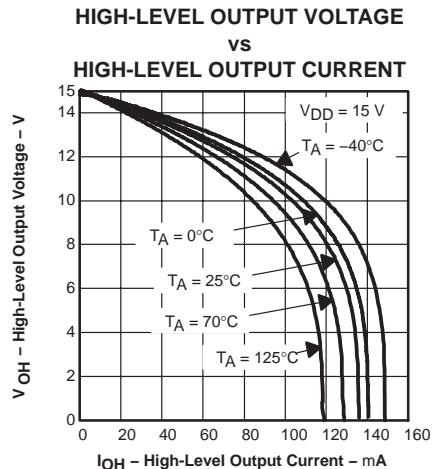
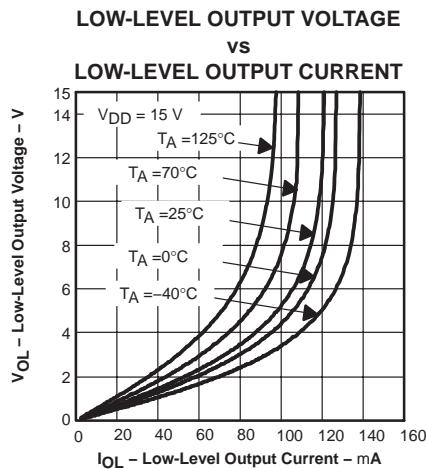


Figure 9

TLV2370, TLV2371, TLV2372, TLV2373, TLV2374, TLV2375 FAMILY OF 550- μ A/Ch 3-MHz RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS270D – MARCH 2001 – REVISED JANUARY 2005

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

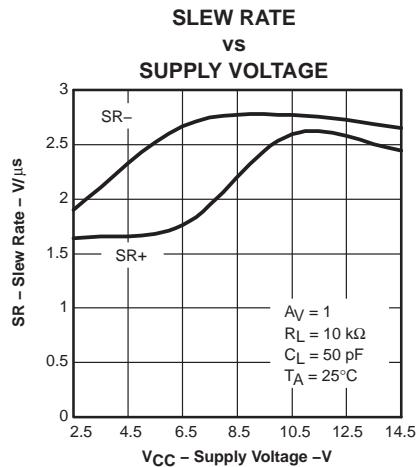


Figure 17

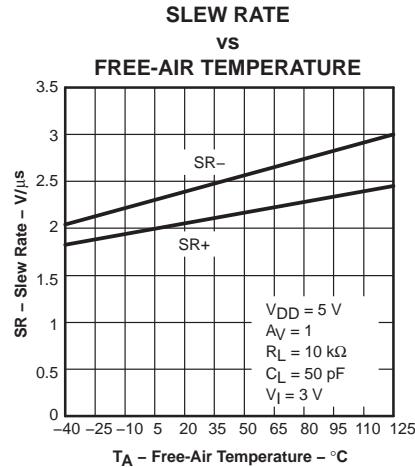


Figure 18

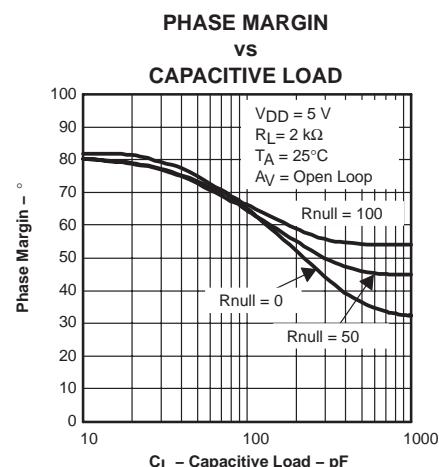


Figure 19

EQUIVALENT INPUT NOISE VOLTAGE

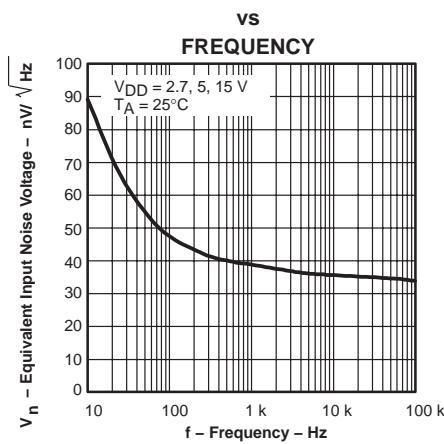


Figure 20

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

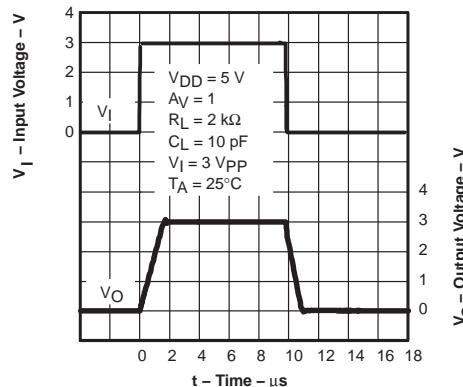


Figure 21

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

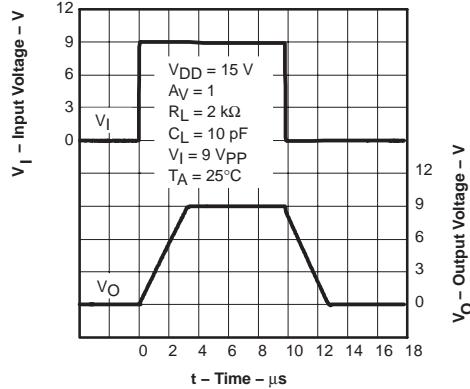


Figure 22

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

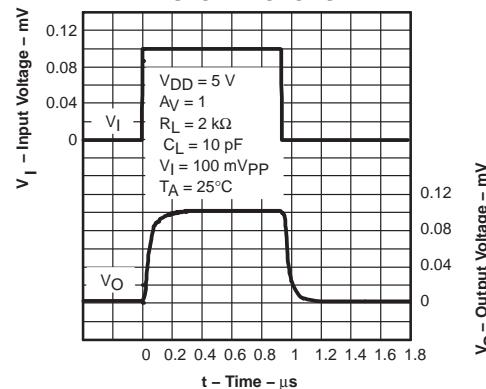


Figure 23

TLV2370, TLV2371, TLV2372, TLV2373, TLV2374, TLV2375 FAMILY OF 550- μ A/Ch 3-MHz RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS270D – MARCH 2001 – REVISED JANUARY 2005

TYPICAL CHARACTERISTICS

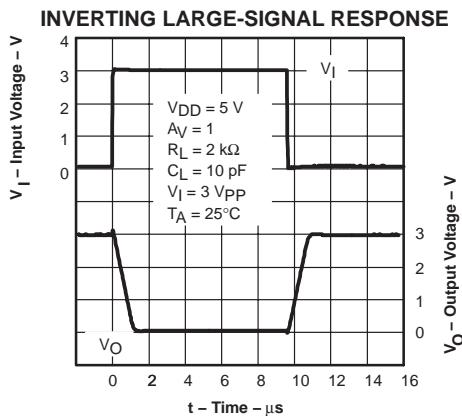


Figure 24

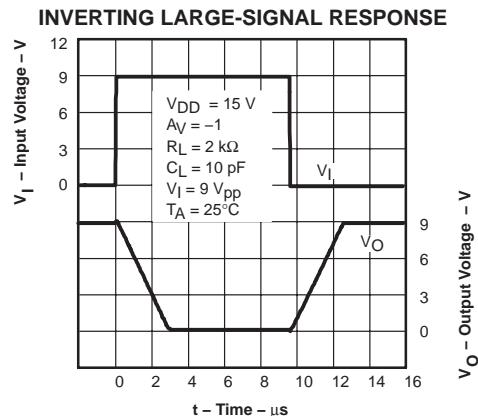


Figure 25

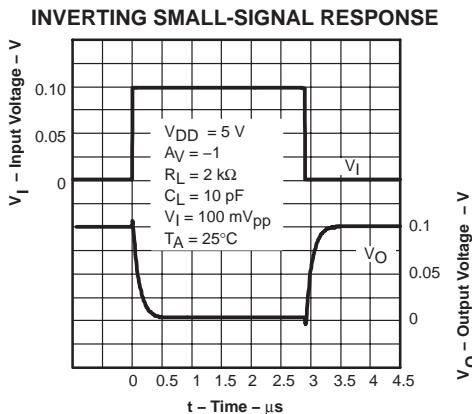


Figure 26

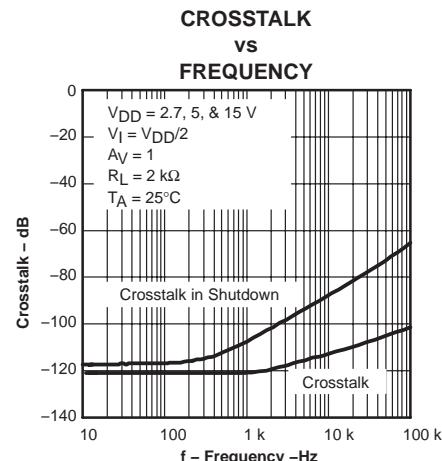


Figure 27

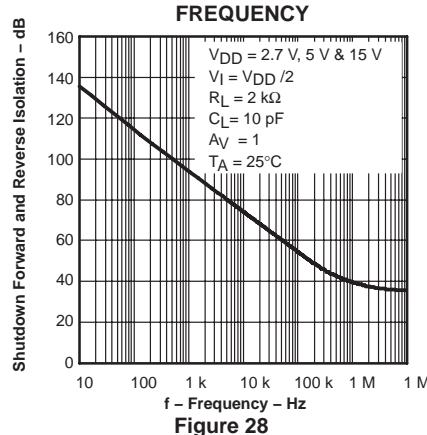


Figure 28

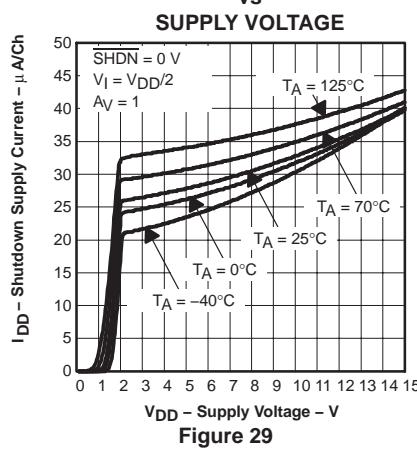


Figure 29

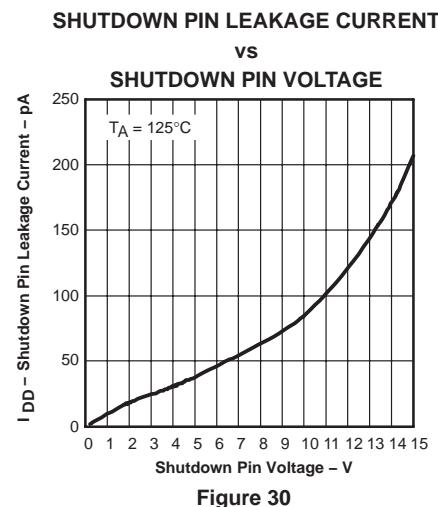


Figure 30

TYPICAL CHARACTERISTICS

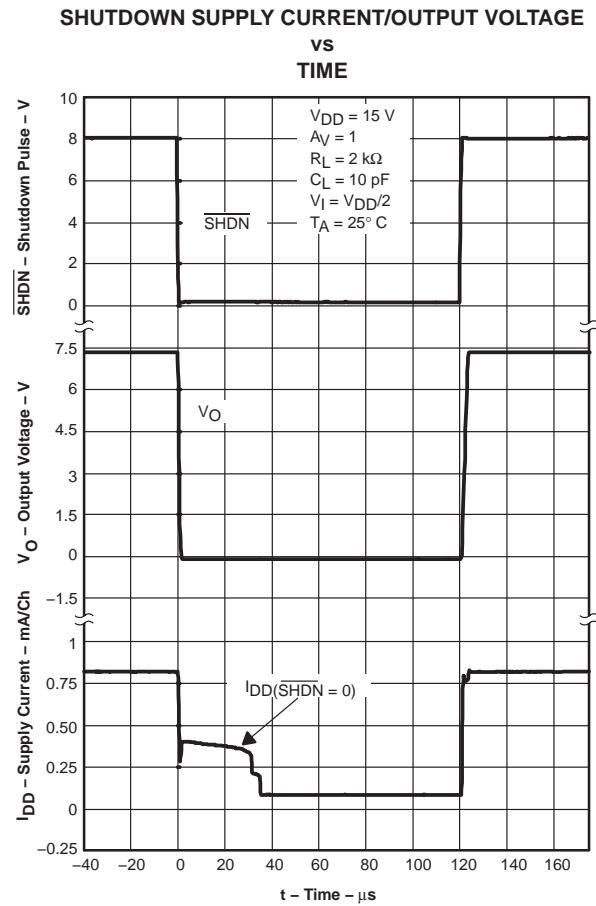


Figure 31

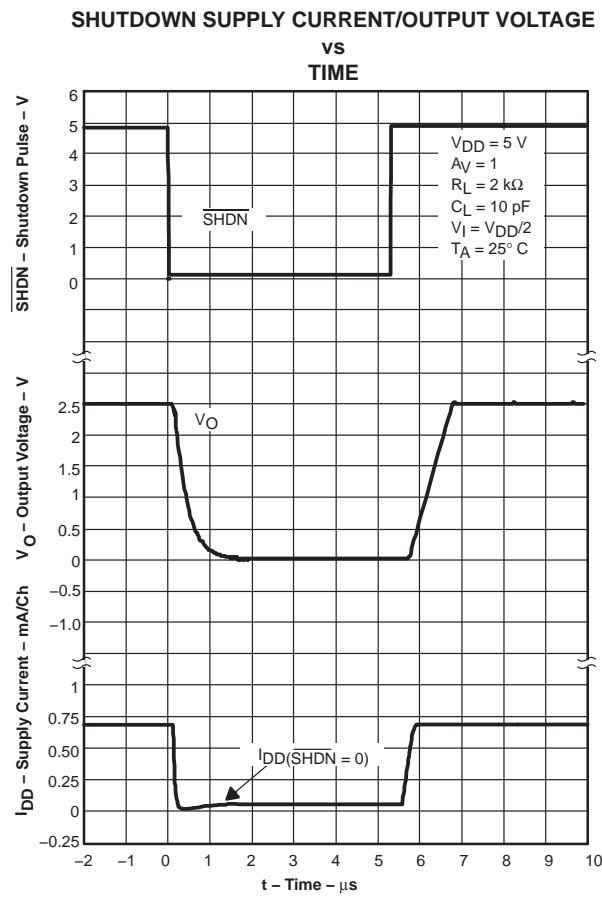


Figure 32

TLV2370, TLV2371, TLV2372, TLV2373, TLV2374, TLV2375 FAMILY OF 550- μ A/Ch 3-MHz RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS270D – MARCH 2001 – REVISED JANUARY 2005

APPLICATION INFORMATION

rail-to-rail input operation

The TLV237x input stage consists of two differential transistor pairs, NMOS and PMOS, that operate together to achieve rail-to-rail input operation. The transition point between these two pairs can be seen in Figure 1, Figure 2, and Figure 3 for a 2.7-V, 5-V, and 15-V supply. As the common-mode input voltage approaches the positive supply rail, the input pair switches from the PMOS differential pair to the NMOS differential pair. This transition occurs approximately 1.35 V from the positive rail and results in a change in offset voltage due to different device characteristics between the NMOS and PMOS pairs. If the input signal to the device is large enough to swing between both rails, this transition results in a reduction in common-mode rejection ratio (CMRR). If the input signal does not swing between both rails, it is best to bias the signal in the region where only one input pair is active. This is the region in Figure 1 through Figure 3 where the offset voltage varies slightly across the input range and optimal CMRR can be achieved. This has the greatest impact when operating from a 2.7-V supply voltage.

driving a capacitive load

When the amplifier is configured in this manner, capacitive loading directly on the output decreases the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series (R_{NULL}) with the output of the amplifier, as shown in Figure 33. A minimum value of $20\ \Omega$ should work well for most applications.

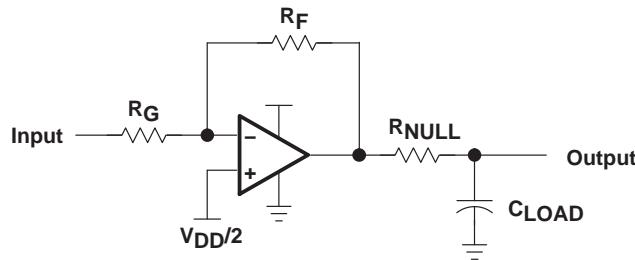


Figure 33. Driving a Capacitive Load

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

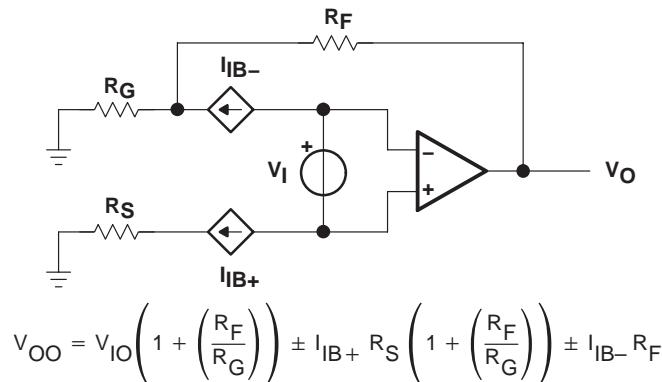


Figure 34. Output Offset Voltage Model

APPLICATION INFORMATION

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 35).

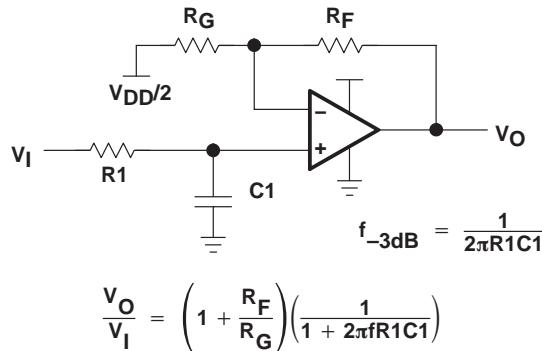


Figure 35. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

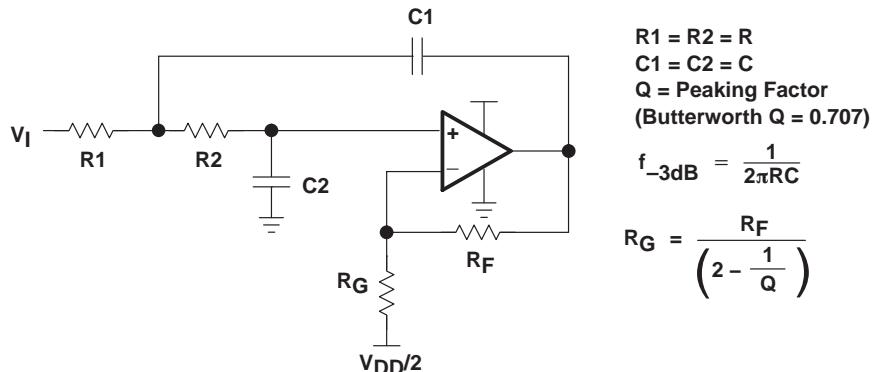


Figure 36. 2-Pole Low-Pass Sallen-Key Filter

TLV2370, TLV2371, TLV2372, TLV2373, TLV2374, TLV2375 FAMILY OF 550- μ A/Ch 3-MHz RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS270D – MARCH 2001 – REVISED JANUARY 2005

APPLICATION INFORMATION

circuit layout considerations

To achieve the levels of high performance of the TLV237x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- **Ground planes**—It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- **Proper power supply decoupling**—Use a 6.8- μ F tantalum capacitor in parallel with a 0.1- μ F ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1- μ F ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1- μ F capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- **Sockets**—Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- **Short trace runs/compact part placements**—Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This helps to minimize stray capacitance at the input of the amplifier.
- **Surface-mount passive components**—Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

shutdown function

Three members of the TLV237x family (TLV2370/3/5) have a shutdown terminal for conserving battery life in portable applications. When the shutdown terminal is tied low, the supply current is reduced to 25 μ A/channel, the amplifier is disabled, and the outputs are placed in a high impedance mode. To enable the amplifier, the shutdown terminal can either be left floating or pulled high. When the shutdown terminal is left floating, care should be taken to ensure that parasitic leakage current at the shutdown terminal does not inadvertently place the operational amplifier into shutdown.



WWW.TI.COM
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

APPLICATION INFORMATION

general power dissipation considerations

For a given θ_{JA} , the maximum power dissipation is shown in Figure 37 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of TLV237x IC (watts)

T_{MAX} = Absolute maximum junction temperature (150°C)

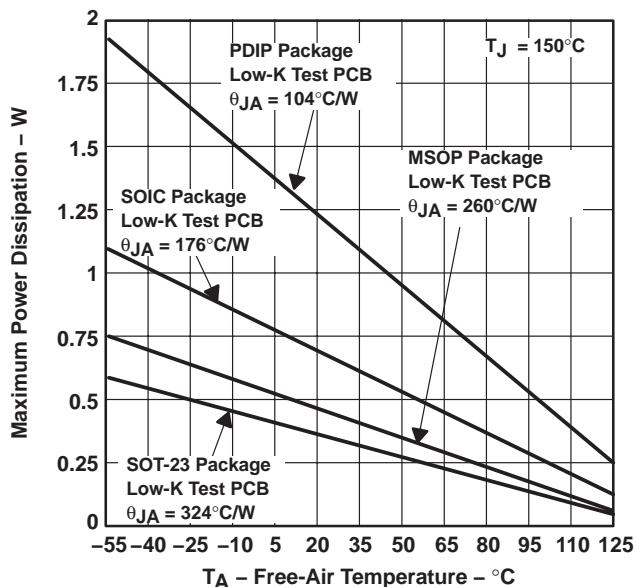
T_A = Free-ambient air temperature (°C)

θ_{JA} = $\theta_{JC} + \theta_{CA}$

θ_{JC} = Thermal coefficient from junction to case

θ_{CA} = Thermal coefficient from case to ambient air (°C/W)

**MAXIMUM POWER DISSIPATION
vs
FREE-AIR TEMPERATURE**



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 37. Maximum Power Dissipation vs Free-Air Temperature

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TLV2370ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2370IDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2370IDBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2370IDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2370IDBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2370IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2370IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2370IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2370IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV2370IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV2371ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2371IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2371IDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2371IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2371IDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2371IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2371IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2371IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2371IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	Call TI	N / A for Pkg Type
TLV2371IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	Call TI	N / A for Pkg Type
TLV2372ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2372IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2372IDGK	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2372IDGKG4	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2372IDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TLV2372IDGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2372IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2372IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2372IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV2372IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV2373ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2373IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2373IDGS	ACTIVE	MSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2373IDGSG4	ACTIVE	MSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2373IDGSR	ACTIVE	MSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2373IDGSRG4	ACTIVE	MSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2373IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2373IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2373IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV2373INE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV2374ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2374IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2374IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2374IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2374IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV2374INE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV2374IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2374IPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2374IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2374IPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2375D	PREVIEW	SOIC	D	16		TBD	Call TI	Call TI

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TLV2375DR	PREVIEW	SOIC	D	16		TBD	Call TI	Call TI
TLV2375ID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2375IDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2375IDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2375IDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2375IN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV2375INE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV2375IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2375IPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2375IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2375IPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

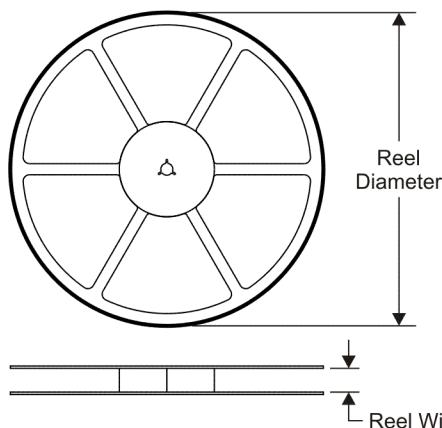
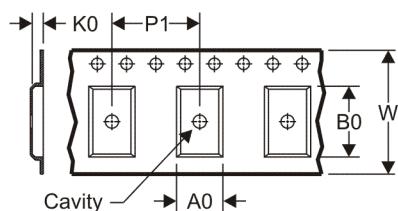
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV2371, TLV2372, TLV2374 :

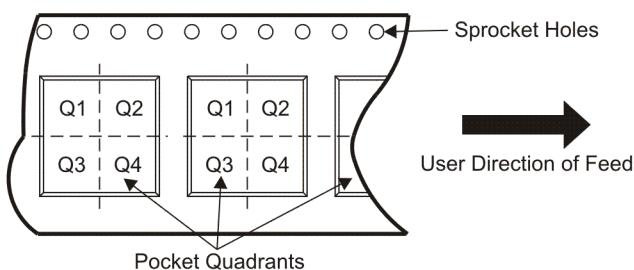
- Automotive: [TLV2371-Q1](#), [TLV2372-Q1](#), [TLV2374-Q1](#)
- Enhanced Product: [TLV2371-EP](#), [TLV2374-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

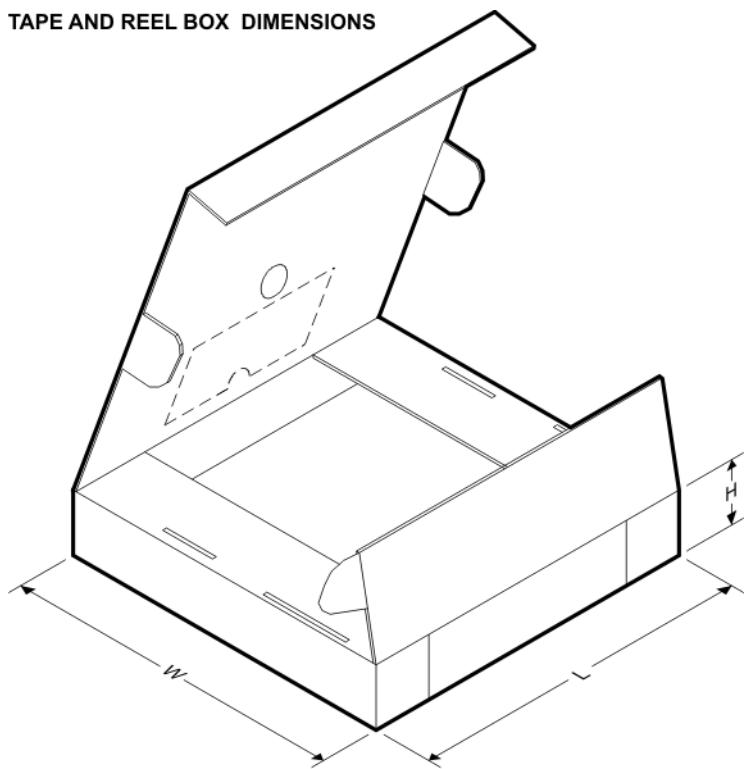
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2370IDBVR	SOT-23	DBV	6	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2370IDBVT	SOT-23	DBV	6	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2370IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2371IDBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2371IDBVT	SOT-23	DBV	5	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2371IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2372IDGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2372IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2373IDGSR	MSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2373IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2374IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2374IPWR	TSSOP	PW	14	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
TLV2375IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TLV2375IPWR	TSSOP	PW	16	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1

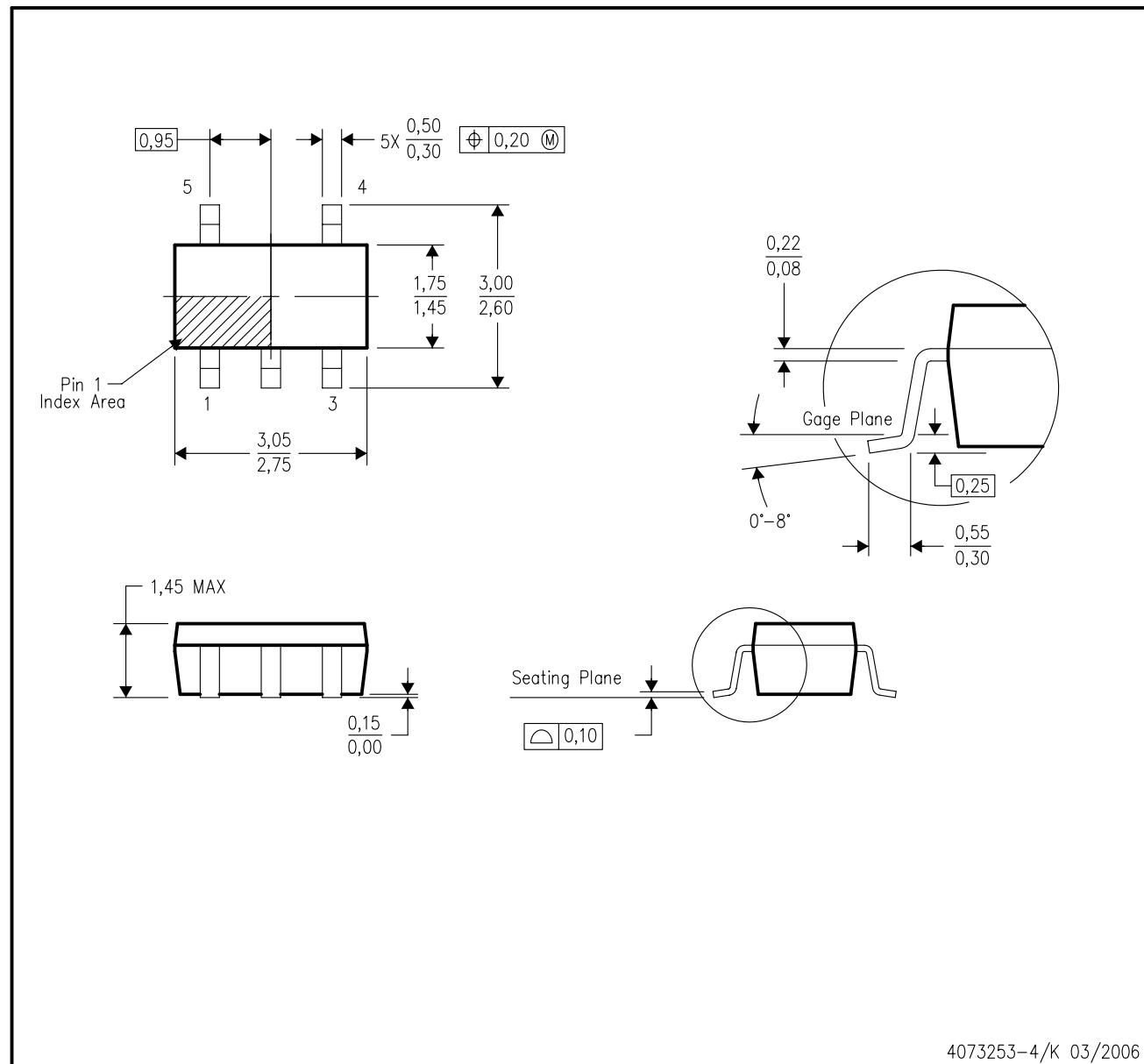
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2370IDBVR	SOT-23	DBV	6	3000	182.0	182.0	20.0
TLV2370IDBVT	SOT-23	DBV	6	250	182.0	182.0	20.0
TLV2370IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2371IDBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TLV2371IDBVT	SOT-23	DBV	5	250	182.0	182.0	20.0
TLV2371IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2372IDGKR	MSOP	DGK	8	2500	358.0	335.0	35.0
TLV2372IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2373IDGSR	MSOP	DGS	10	2500	358.0	335.0	35.0
TLV2373IDR	SOIC	D	14	2500	333.2	345.9	28.6
TLV2374IDR	SOIC	D	14	2500	333.2	345.9	28.6
TLV2374IPWR	TSSOP	PW	14	2000	346.0	346.0	29.0
TLV2375IDR	SOIC	D	16	2500	333.2	345.9	28.6
TLV2375IPWR	TSSOP	PW	16	2000	346.0	346.0	29.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



4073253-4/K 03/2006

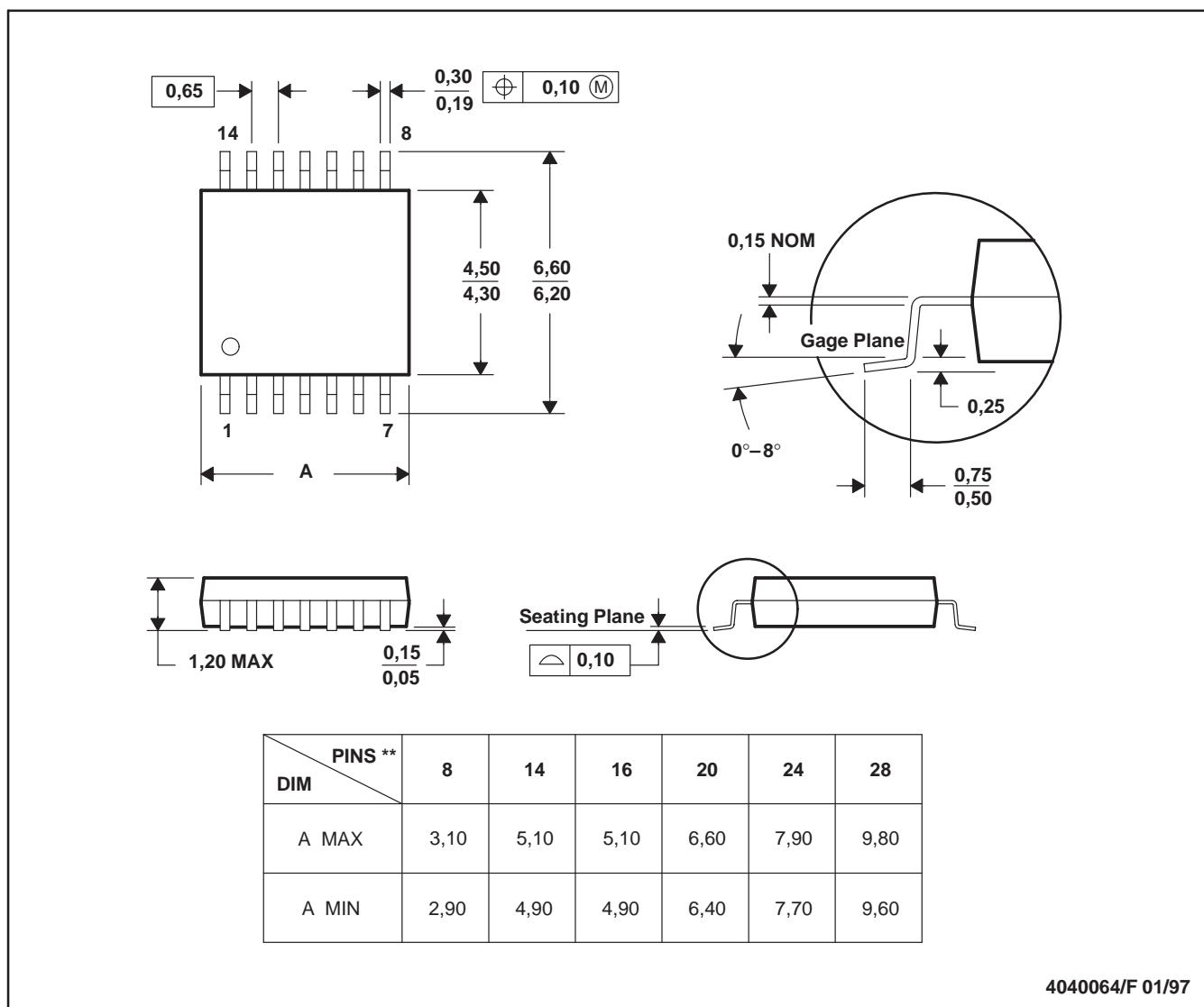
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- Falls within JEDEC MO-178 Variation AA.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN

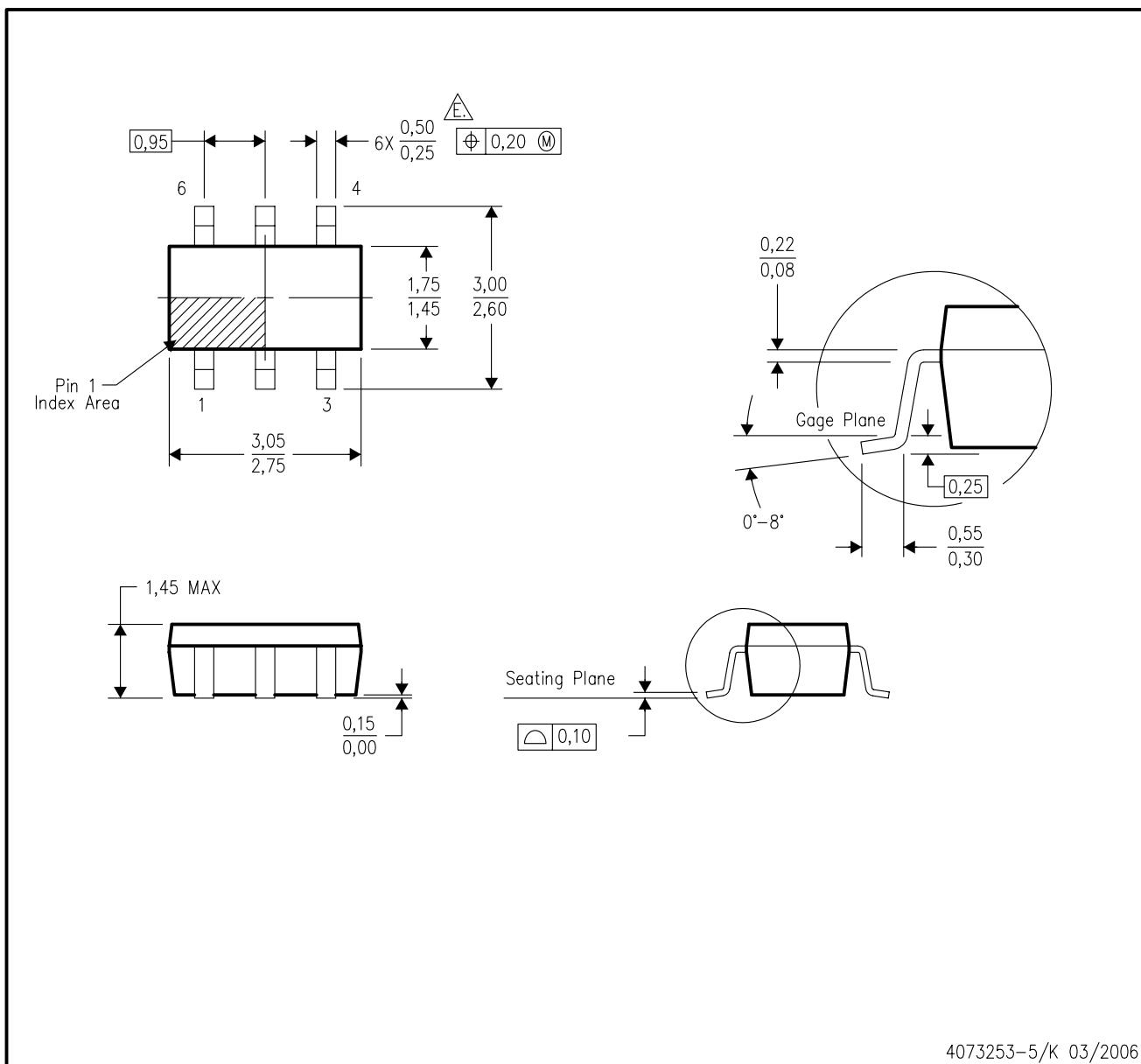


NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- Falls within JEDEC MO-153

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



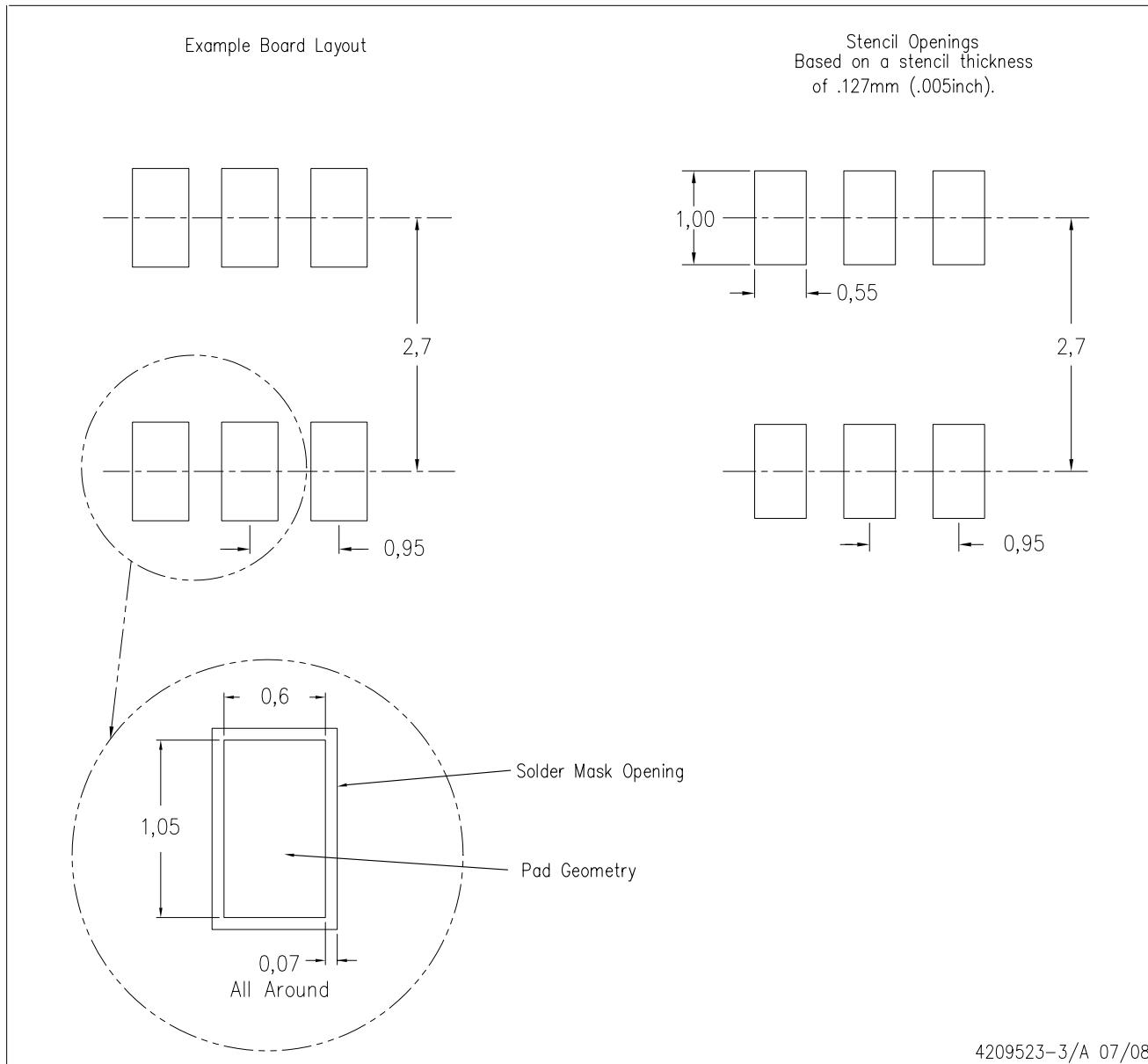
4073253-5/K 03/2006

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.

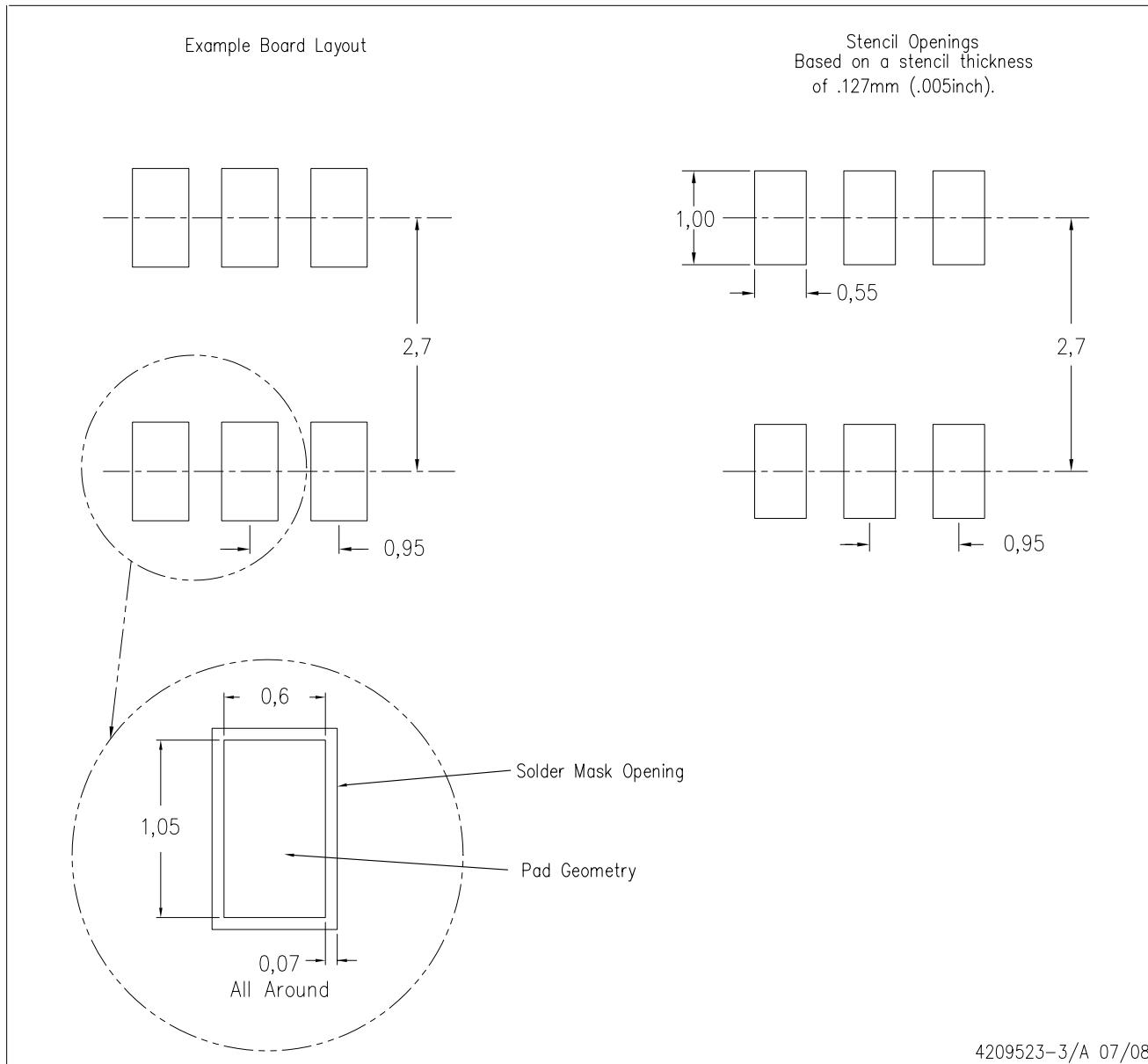
 Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6)



NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

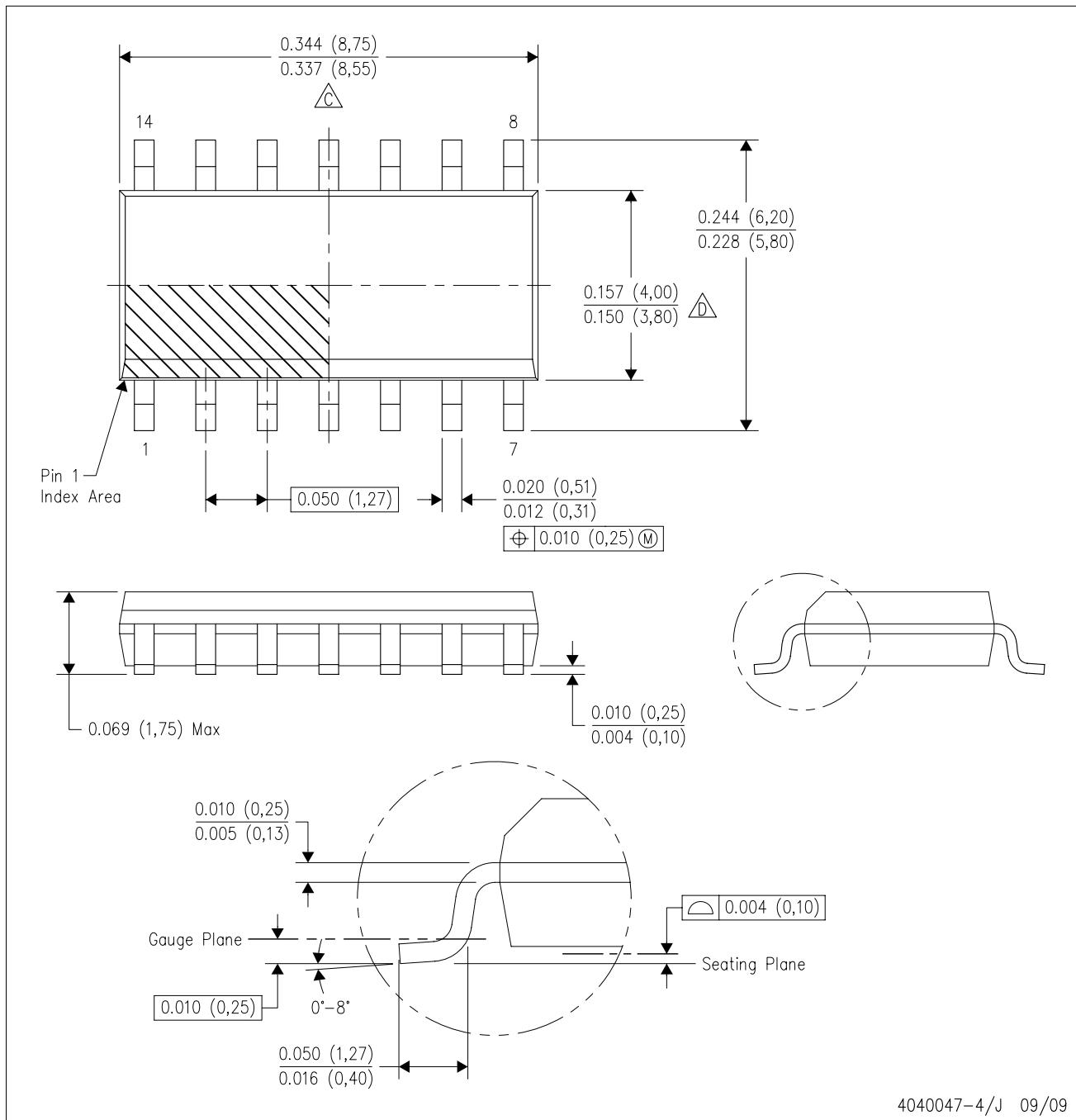
DBV (R-PDSO-G6)

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

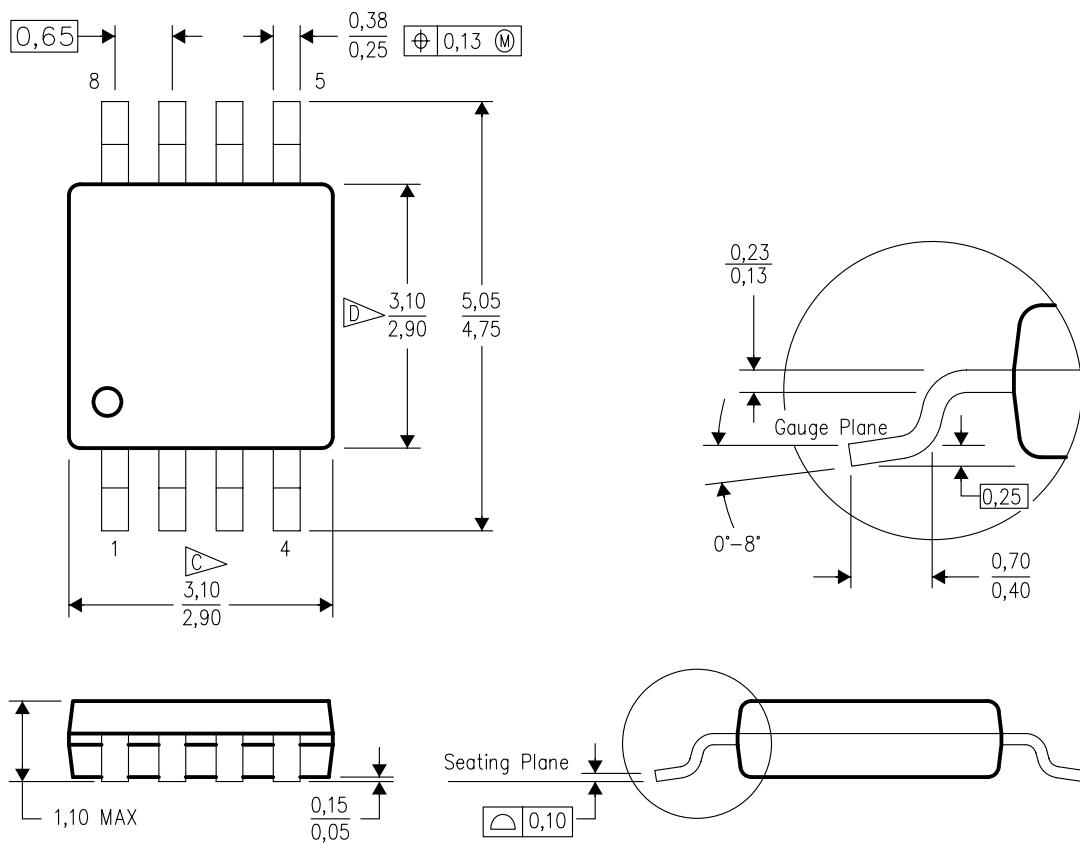
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.

D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.

E. Reference JEDEC MS-012 variation AB.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

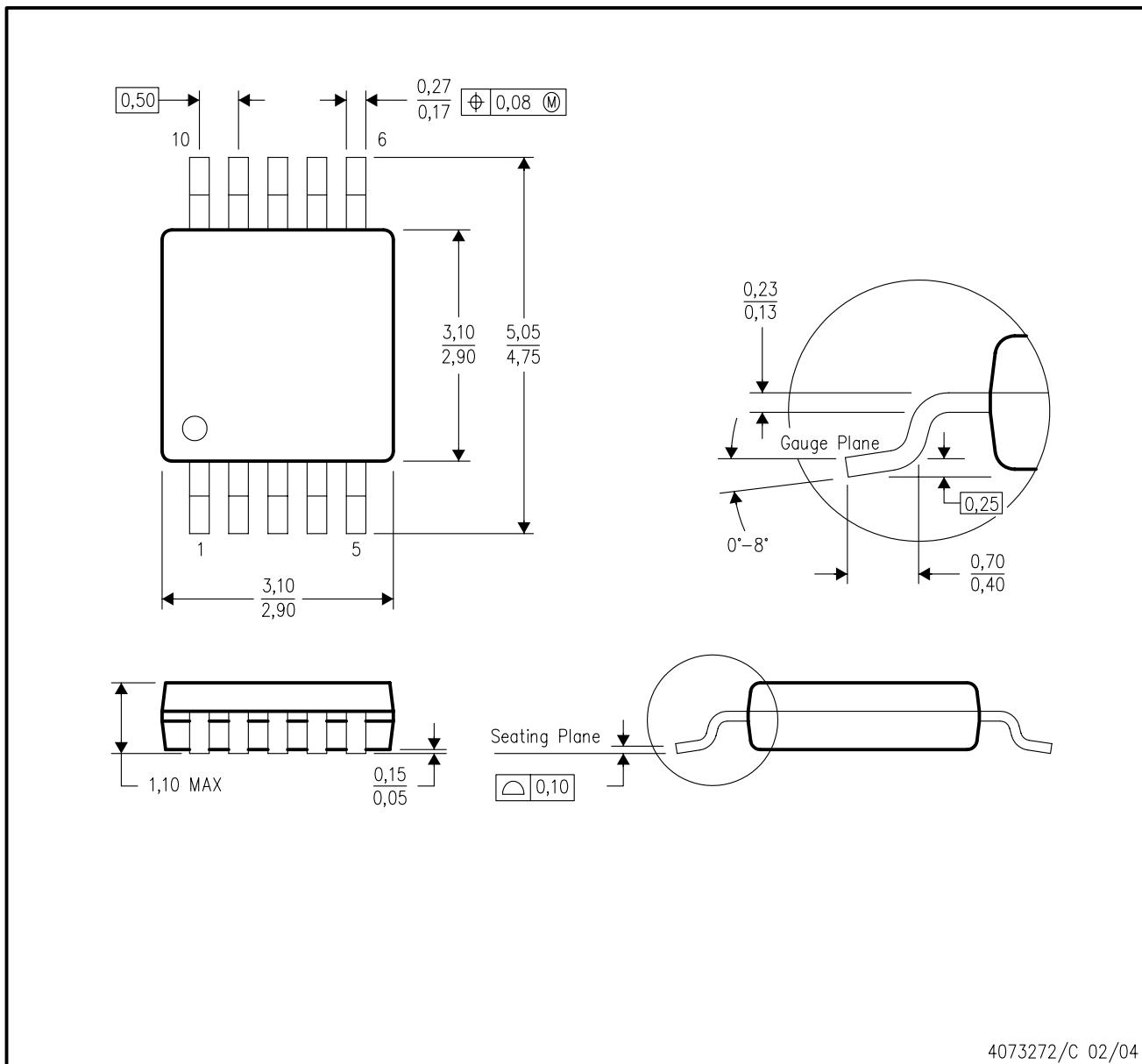
 Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.

 Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.

E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGS (S-PDSO-G10)

PLASTIC SMALL-OUTLINE PACKAGE



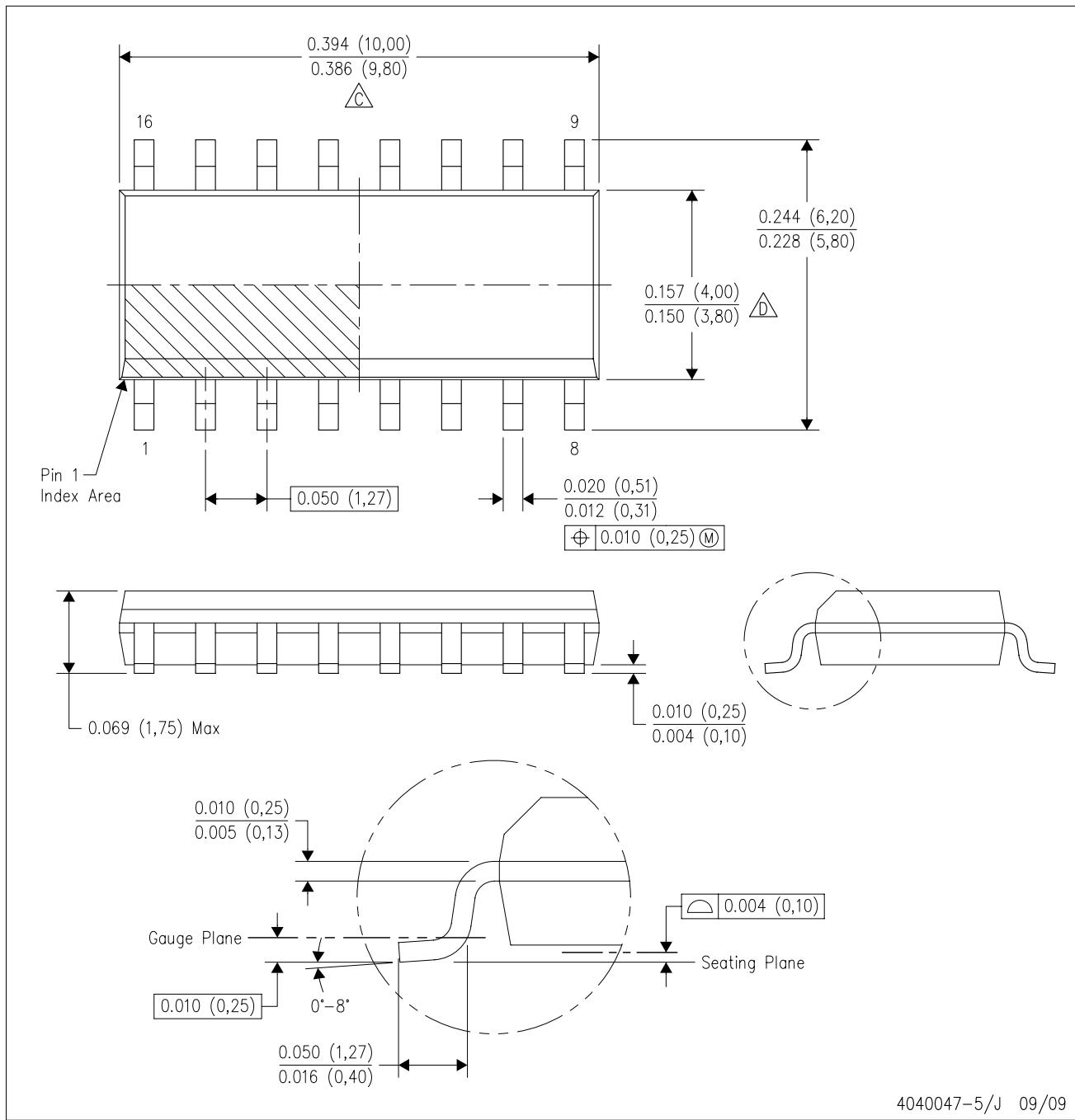
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Falls within JEDEC MO-187 variation BA.

4073272/C 02/04

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

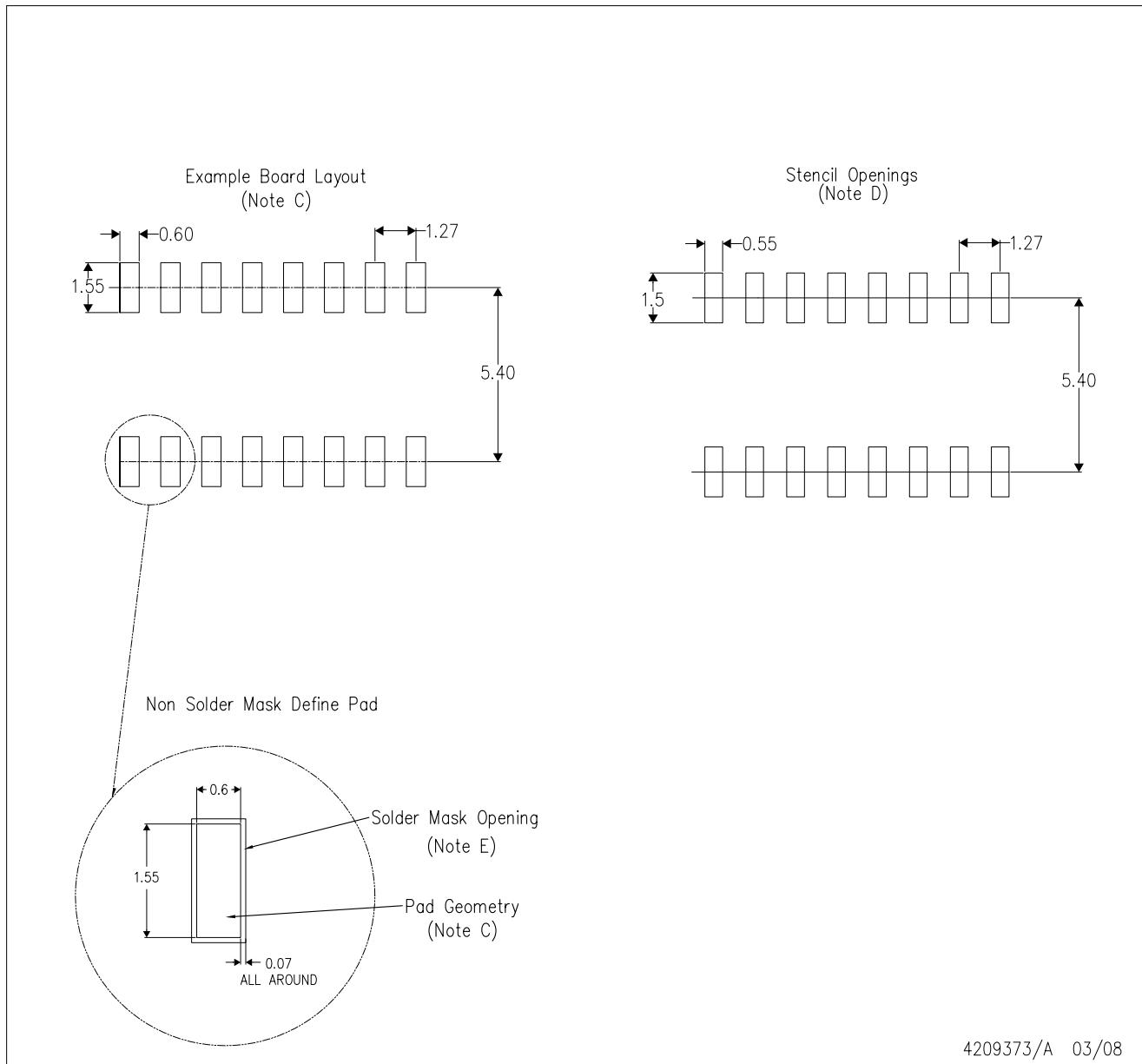
B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.

D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.

E. Reference JEDEC MS-012 variation AC.

D(R-PDSO-G16)

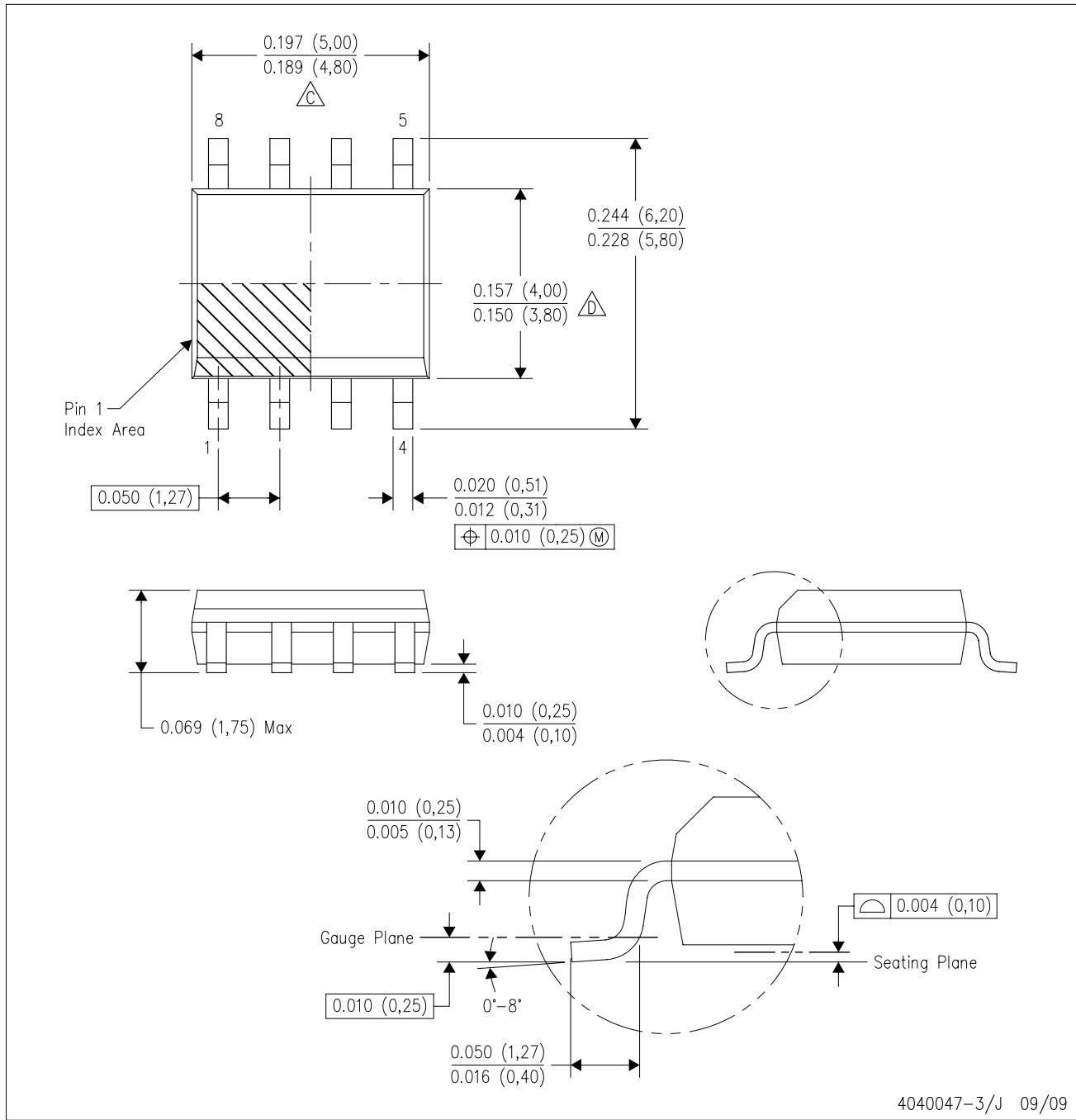


NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Refer to IPC7351 for alternate board design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-3/J 09/09

NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

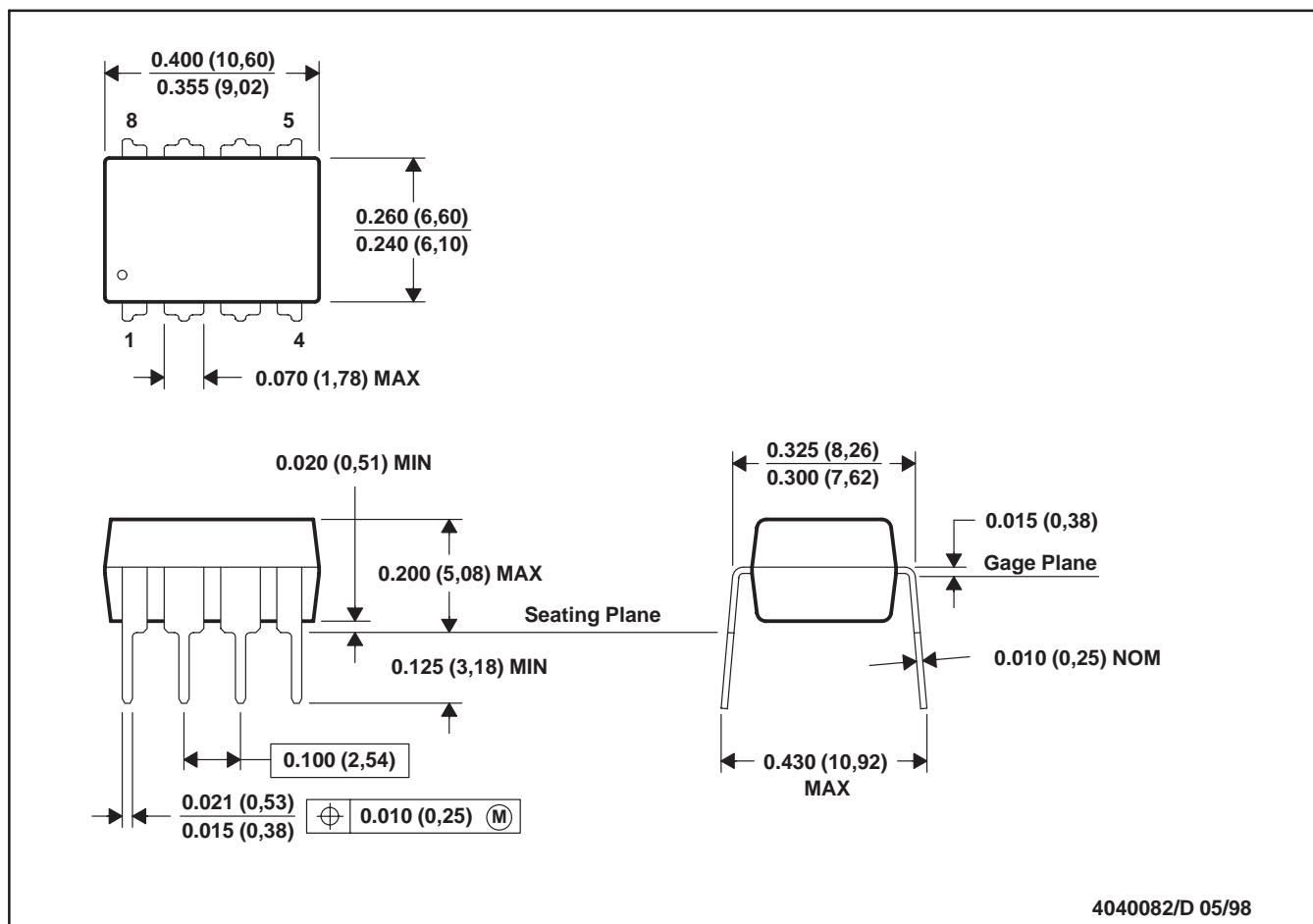
△C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.

△D Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.

E. Reference JEDEC MS-012 variation AA.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2009, Texas Instruments Incorporated