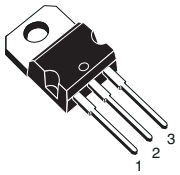
IRF640T

N-channel 200V - 0.15Ω - 15A - TO-220
MESH OVERLAY™ Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
IRF640T	200V	<0.16Ω	15A

- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitances



TO-220

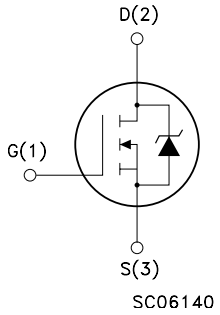
Description

This Power MOSFET is designed using the company's consolidated strip layout-based MESH OVERLAY™ process. This technology matches and improves the performances compared with standard parts from various sources.

Applications

- Switching application

Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
IRF640T	IRF640T	TO-220	Tube

Contents

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	200	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at T_C = 25°C	15	A
I_D	Drain current (continuous) at T_C=100°C	10	A
I_{DM}(1)	Drain current (pulsed)	60	A
P_{TOT}	Total dissipation at T_C = 25°C	90	W
	Derating factor	0.72	W/°C
dv/dt(2)	Peak diode recovery voltage slope	15	V/ns
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. Pulse width limited by safe operating area
2. I_{SD} ≤15A, di/dt ≤300A/µs, V_{DD} =80%$V_{(BR)DSS}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1.38	°C/W
$R_{thj\text{-}a}$	Thermal resistance junction-ambient max	62.5	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

Table 3. Avalanche data

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche curent, repetitive or not-repetitive (pulse width limited by Tj Max)	15	A
E_{AS}	Single pulse avalanche energy (starting Tj=25°C, Id=Iar, Vdd=50V)	110	mJ

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1mA, V_{GS}= 0	200			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating @125°C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10V, I_D= 7.5A		0.15	0.16	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} =8V, I_D = 7.5A		12		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25V, f=1 MHz, V_{GS}=0		800 165 26		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=160V, I_D = 15A V_{GS} =10V *(see Figure 14)*		24 4.4 11.6		nC nC nC

1. Pulsed: pulse duration=300µs, duty cycle 1.5%

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD}=100 V, I_D= 7.5A, R_G=4.7Ω, V_{GS}=10V *(see Figure 13)*		11.5 22		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	V_{DD} = 100 V, I_D = 7.5A, R_G = 4.7Ω, V_{GS} = 10V *(see Figure 13)*		19 11		ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				15	A
I_{SDM}(1)	Source-drain current (pulsed)				60	A
V_{SD}(2)	Forward on voltage	I_{SD}=15A, V_{GS}=0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}=15A, V_{DD}=50V di/dt = 100A/µs, *(see Figure 18)*		125 0.55 8.8		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}=15A, V_{DD}=50V di/dt = 100A/µs, Tj=150°C *(see Figure 18)*		148 0.73 9.9		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

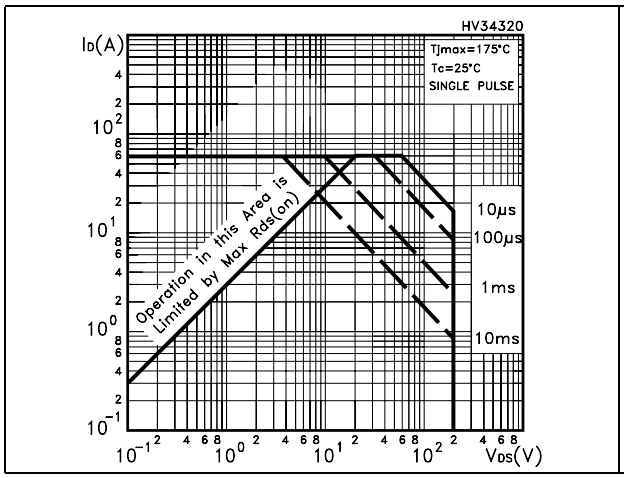


Figure 2. Thermal impedance

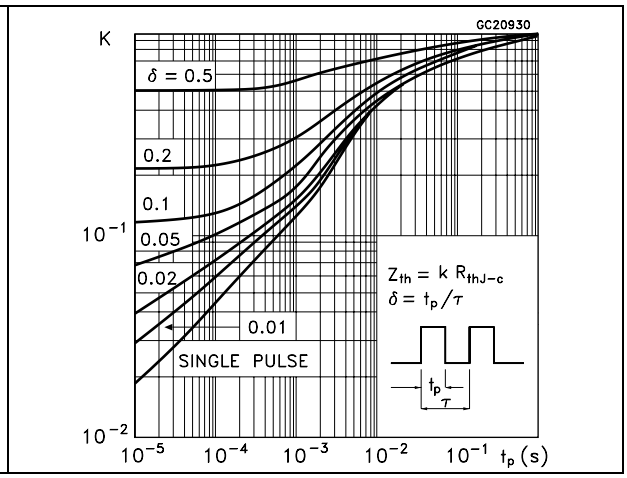


Figure 3. Output characteristics

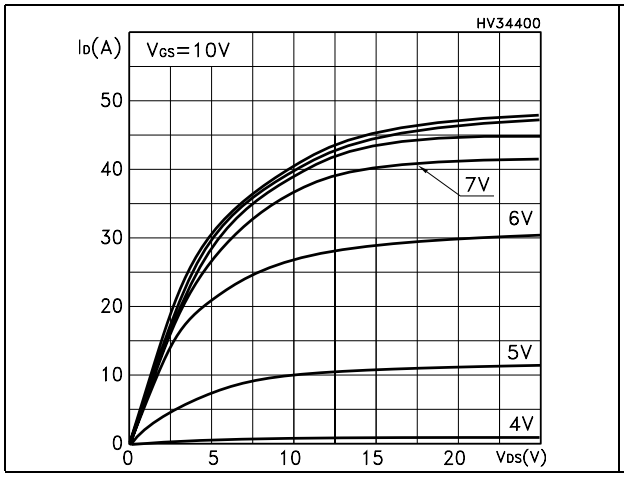


Figure 4. Transfer characteristics

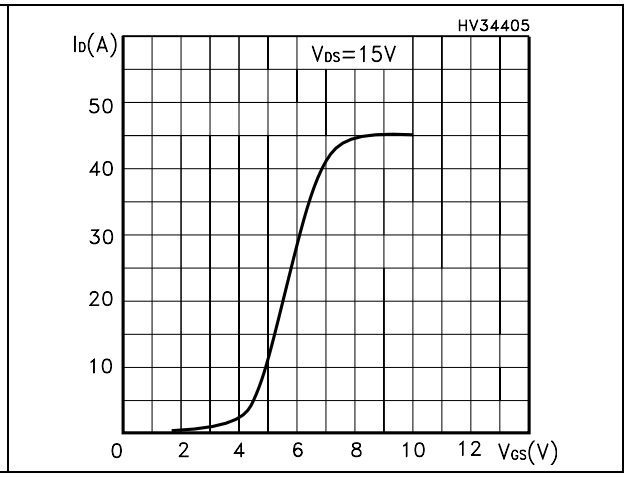


Figure 5. Static drain-source on resistance

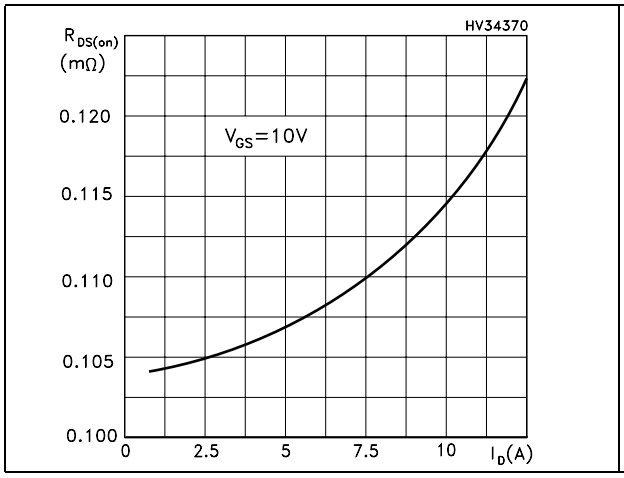


Figure 6. Normalized BV_{DSS} vs temperature

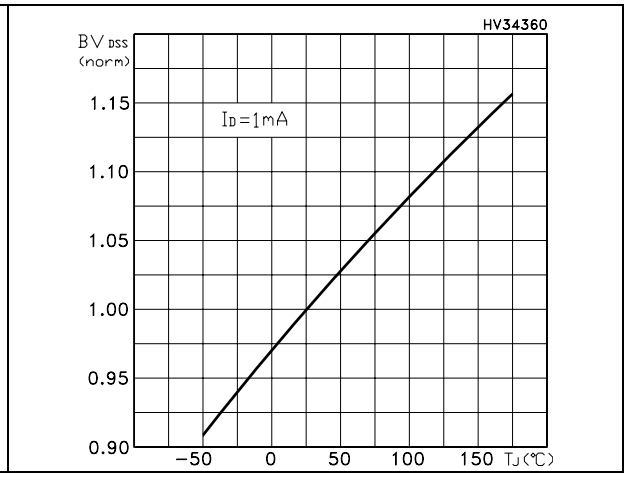


Figure 7. Gate charge vs gate-source voltage

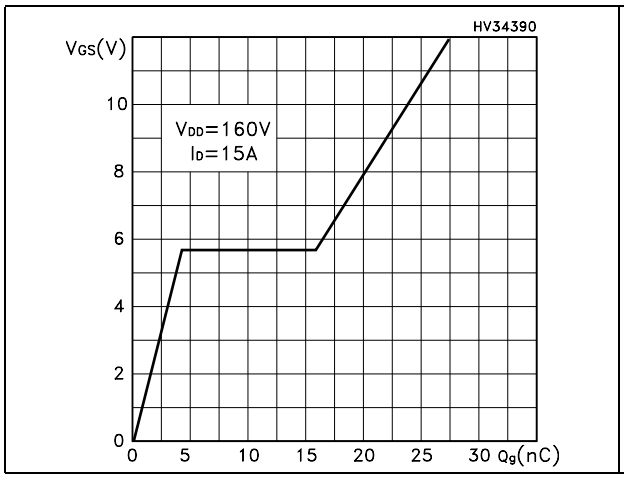


Figure 8. Capacitance variations

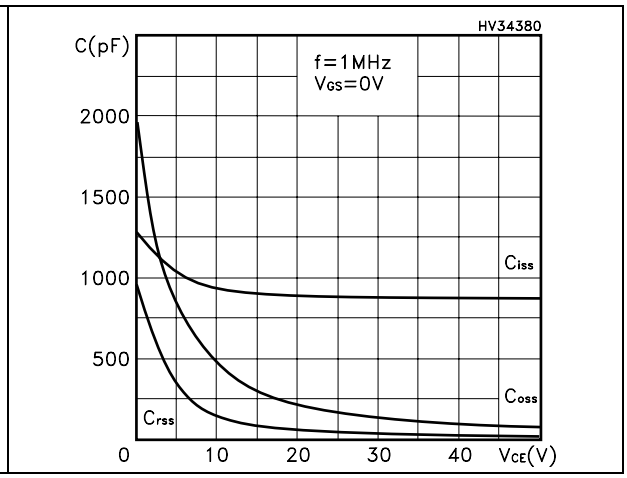


Figure 9. Normalized gate threshold voltage vs temperature

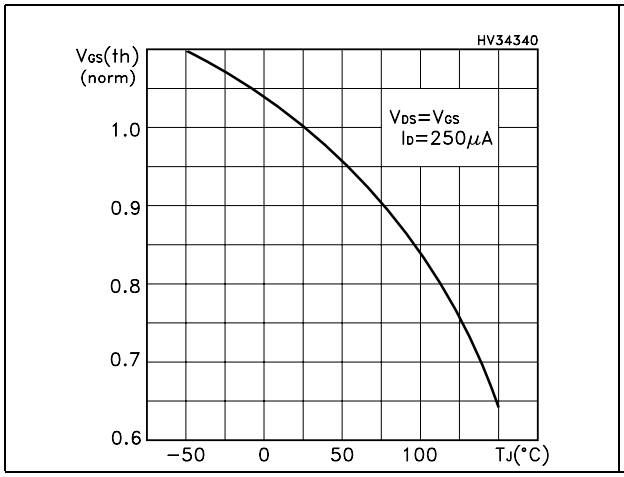


Figure 10. Normalized on resistance vs temperature

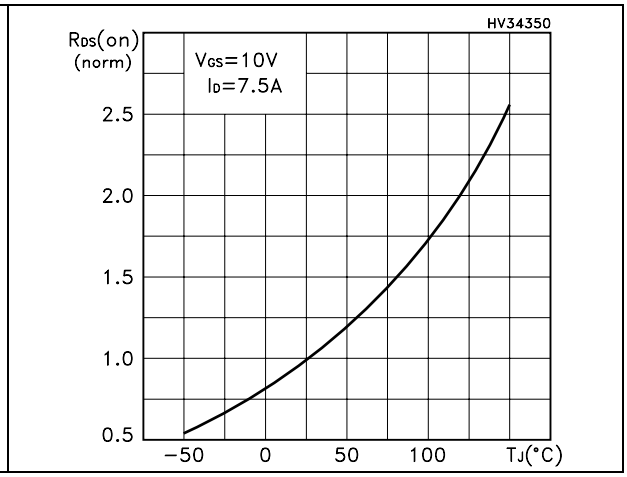


Figure 11. Source-drain forward characteristics

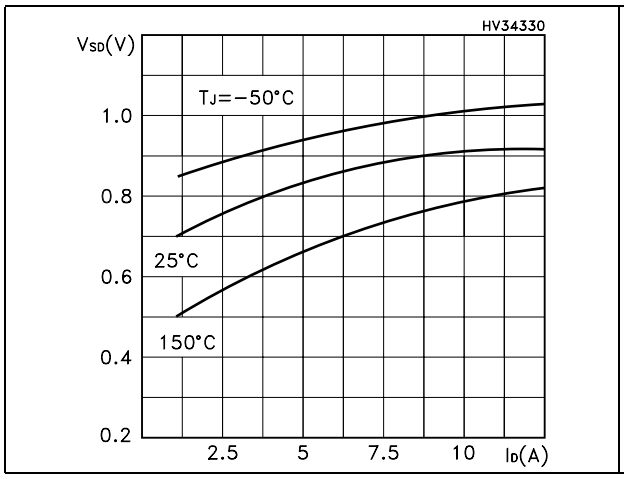
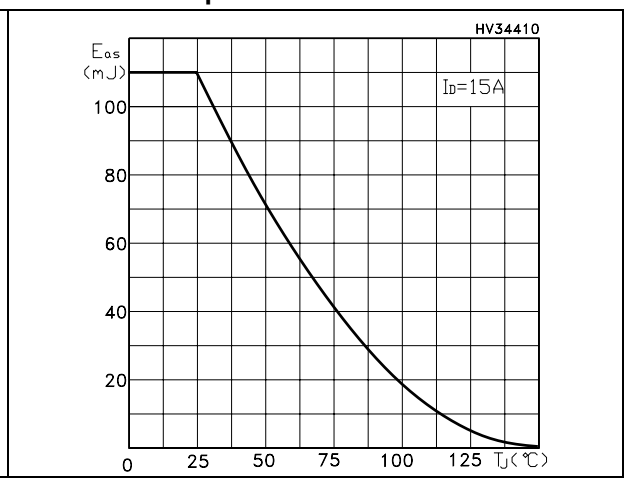


Figure 12. Maximum avalanche energy vs temperature



3 Test circuit

Figure 13. Switching times test circuit for resistive load

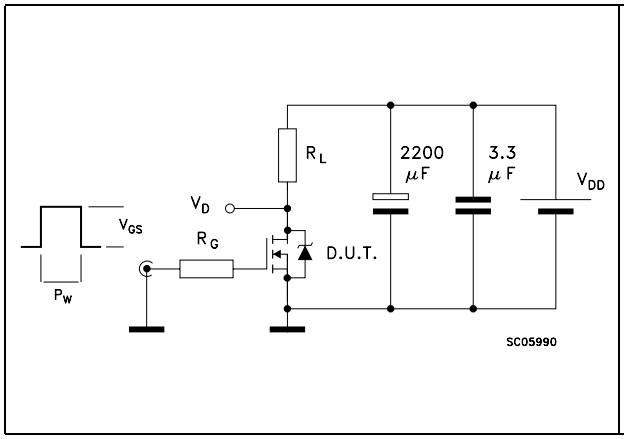


Figure 14. Gate charge test circuit

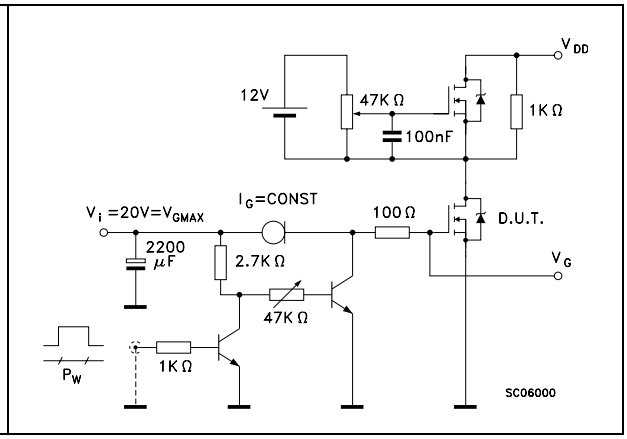


Figure 15. Test circuit for inductive load switching and diode recovery times

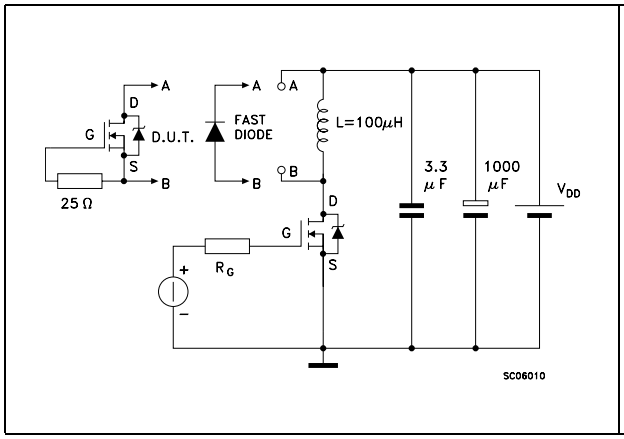


Figure 16. Unclamped Inductive load test circuit

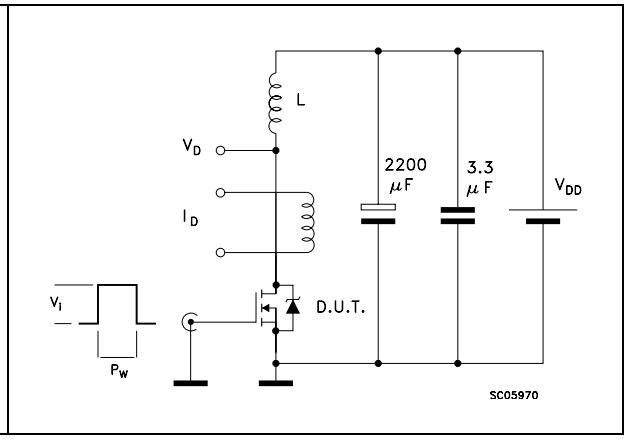


Figure 17. Unclamped inductive waveform

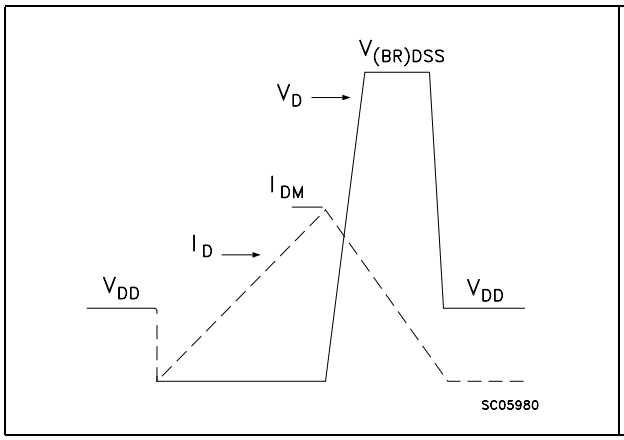
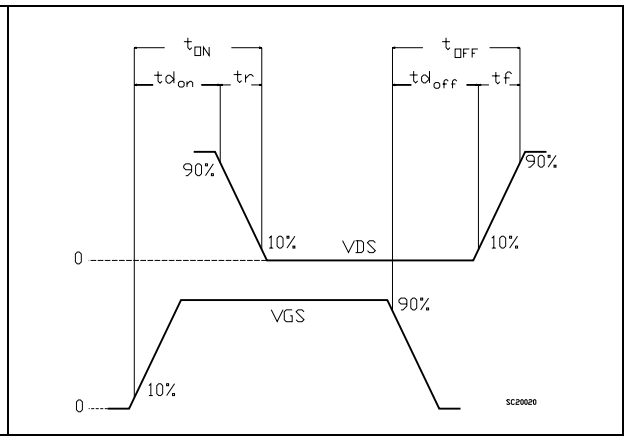


Figure 18. Switching time waveform

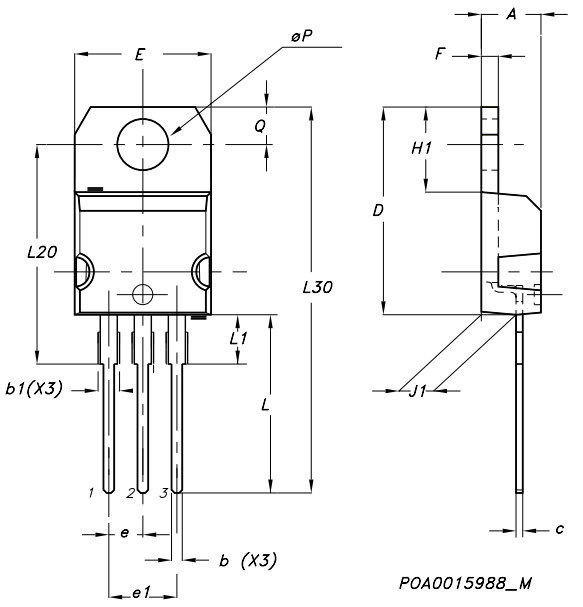


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



5 Revision history

Table 8. Revision history

Date	Revision	Changes
06-Oct-2006	1	First Release

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