



# PCA8576D

Automotive 40 x 4 LCD segment driver for low multiplex rates up to 1:4

Rev. 2 — 6 June 2013

Product data sheet

## 1. General description

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The PCA8576D is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments. It can be easily cascaded for larger LCD applications. The PCA8576D is compatible with most microcontrollers and communicates via the two-line bidirectional I<sup>2</sup>C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

## 2. Features and benefits

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- AEC-Q100 compliant for automotive applications
- Single chip LCD controller and driver
- Selectable backplane drive configuration: static or 2, 3, 4 backplane multiplexing
- Selectable display bias configuration: static,  $\frac{1}{2}$  or  $\frac{1}{3}$
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives:
  - ◆ Up to 20 7-segment numeric characters
  - ◆ Up to 10 14-segment alphanumeric characters
  - ◆ Any graphics of up to 160 elements
- 40 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- Independent supplies possible for LCD and logic voltages
- Wide power supply range: from 1.8 V to 5.5 V
- Wide logic LCD supply range:
  - ◆ From 2.5 V for low-threshold LCDs
  - ◆ Up to 6.5 V for high-threshold twisted nematic LCDs
- Low power consumption
- 400 kHz I<sup>2</sup>C-bus interface
- May be cascaded for large LCD applications (up to 2560 elements possible)
- No external components required
- Compatible with chip-on-glass and chip-on-board technology
- Manufactured in silicon gate CMOS process



### 3. Ordering information

### Table 1. Ordering information

| Type number | Package  |             |               |
|-------------|----------|-------------|---------------|
|             | Name     | Description | Version       |
| PCA8576DU   | bare die | 59 bumps    | PCA8576DU/2DA |

### 3.1 Ordering options

### Table 2. Ordering options

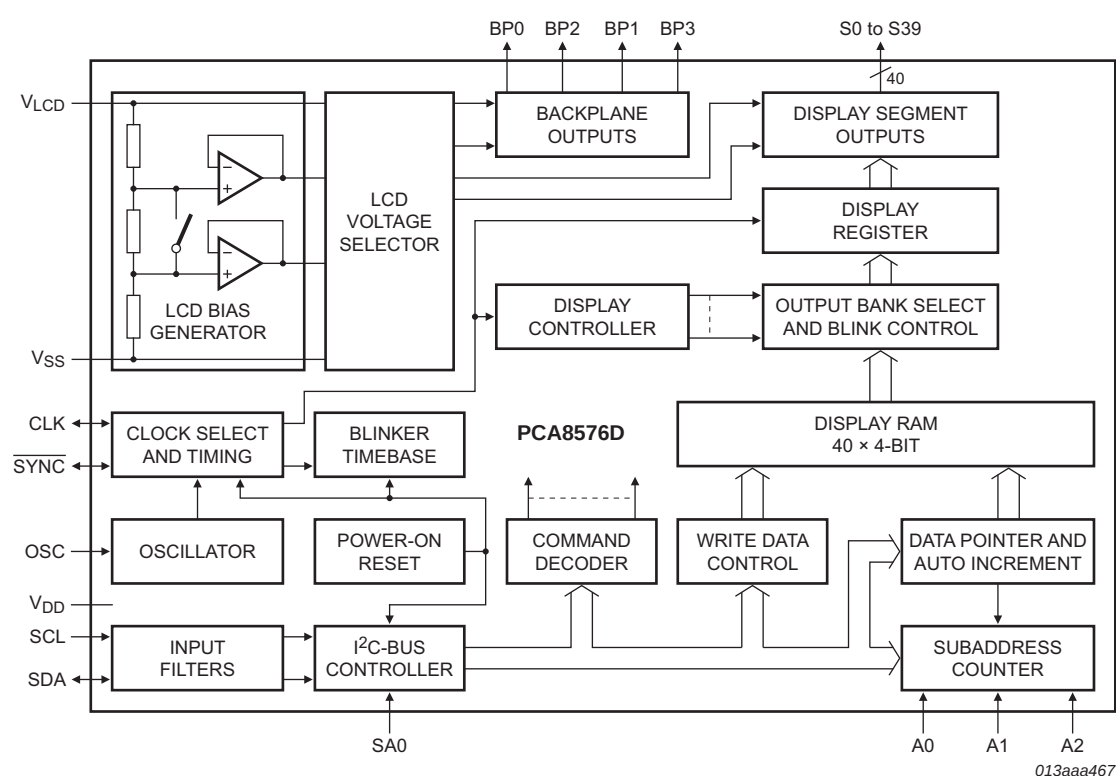
| Product type number | Sales item (12NC) | Orderable part number | IC revision | Delivery form            |
|---------------------|-------------------|-----------------------|-------------|--------------------------|
| PCA8576DU/2DA/Q2    | 935294883026      | PCA8576DU/2DA/Q2,0    | 1           | chips with bumps in tray |

## 4. Marking

### Table 3. Marking codes

| Product type number | Marking code |
|---------------------|--------------|
| PCA8576DU/2DA/Q2    | PC8576D-2    |

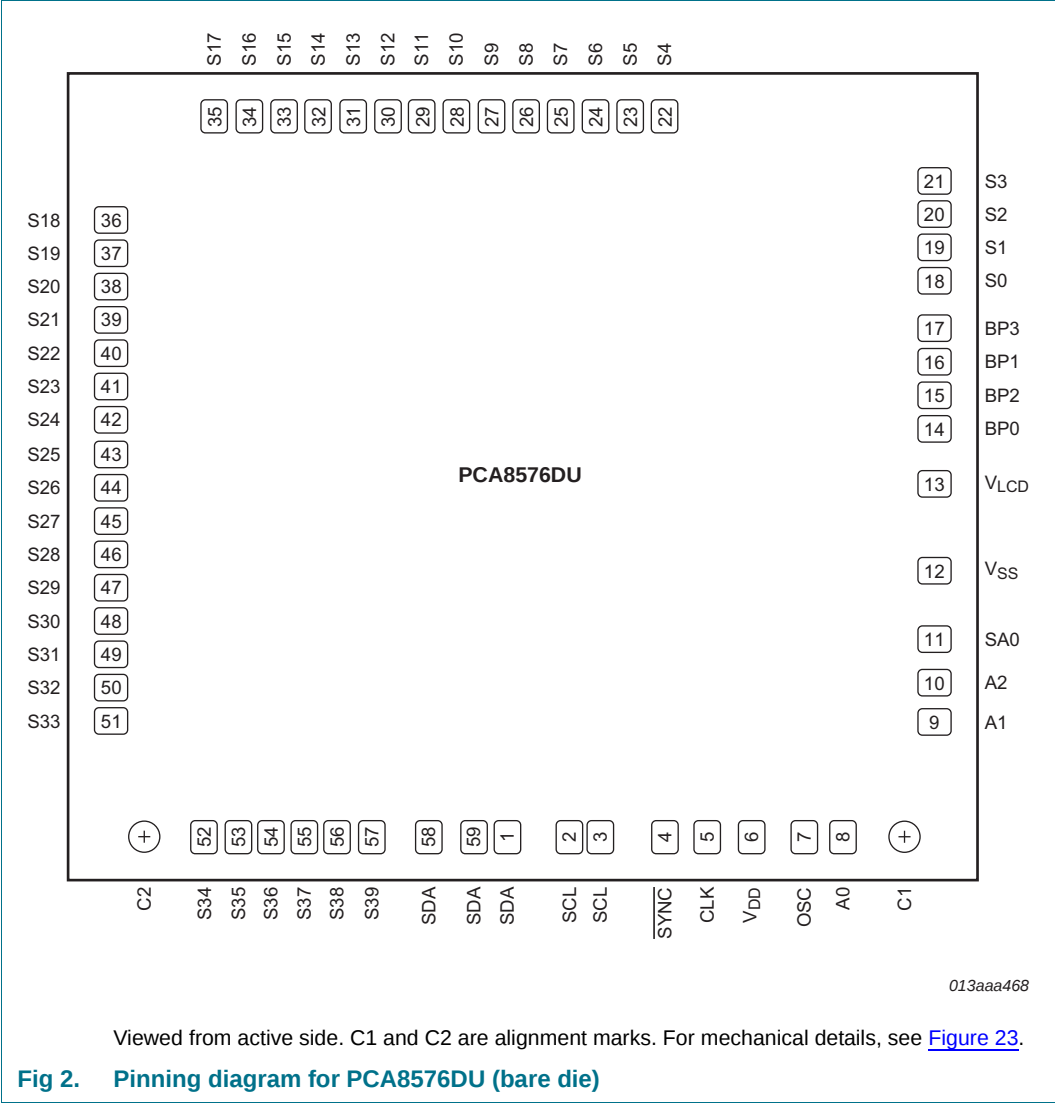
## 5. Block diagram



**Fig 1. Block diagram of PCA8576D**

6. Pinning information

6.1 Pinning



## 6.2 Pin description

Table 4. Pin description

| Symbol                | Pin<br>PCA8576DU  | Description                                       |
|-----------------------|-------------------|---------------------------------------------------|
| SDA                   | 1, 58, 59         | I <sup>2</sup> C-bus serial data input and output |
| SCL                   | 2, 3              | I <sup>2</sup> C-bus serial clock input           |
| CLK                   | 5                 | external clock input or output                    |
| V <sub>DD</sub>       | 6                 | supply voltage                                    |
| SYNC                  | 4                 | cascade synchronization input or output           |
| OSC                   | 7                 | internal oscillator enable input                  |
| A0 to A2              | 8 to 10           | subaddress inputs                                 |
| SA0                   | 11                | I <sup>2</sup> C-bus address input; bit 0         |
| V <sub>SS</sub>       | 12 <sup>[1]</sup> | ground supply voltage                             |
| V <sub>LCD</sub>      | 13                | LCD supply voltage                                |
| BP0, BP2, BP1,<br>BP3 | 14 to 17          | LCD backplane outputs                             |
| S0 to S39             | 18 to 57          | LCD segment outputs                               |

[1] The substrate (rear side of the die) is connected to V<sub>SS</sub> and should be electrically isolated.

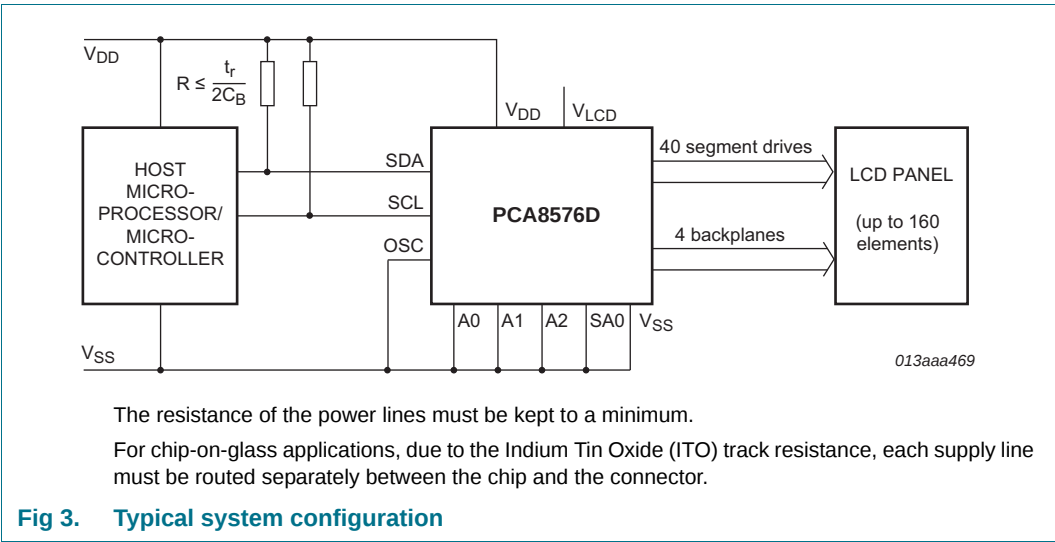
7. Functional description

The PCA8576D is a versatile peripheral device designed to interface any microcontroller with a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 40 segments.

The possible display configurations of the PCA8576D depend on the number of active backplane outputs required. A selection of display configurations is shown in Table 5. All of these configurations can be implemented in the typical system shown in Figure 3.

Table 5. Selection of possible display configurations

| Number of Backplanes | Icons | Digits/Characters |            | Dot matrix/Elements |
|----------------------|-------|-------------------|------------|---------------------|
|                      |       | 7-segment         | 14-segment |                     |
| 4                    | 160   | 20                | 10         | 160 (4 × 40)        |
| 3                    | 120   | 15                | 7          | 120 (3 × 40)        |
| 2                    | 80    | 10                | 5          | 80 (2 × 40)         |
| 1                    | 40    | 5                 | 2          | 40 (1 × 40)         |



The host microprocessor or microcontroller maintains the 2-line I<sup>2</sup>C-bus communication channel with the PCA8576D. The internal oscillator is enabled by connecting pin OSC to pin V<sub>SS</sub>. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V<sub>DD</sub>, V<sub>SS</sub> and V<sub>LCD</sub>) and the LCD panel chosen for the application.

## 7.1 Power-on reset

At power-on the PCA8576D resets to the following starting conditions:

- All backplane and segment outputs are set to  $V_{LCD}$
- The selected drive mode is: 1:4 multiplex with  $\frac{1}{3}$  bias
- Blinking is switched off
- Input and output bank selectors are reset
- The I<sup>2</sup>C-bus interface is initialized
- The data pointer and the subaddress counter are cleared (set to logic 0)
- The display is disabled (bit E = 0, see [Table 11](#))

Data transfers on the I<sup>2</sup>C-bus must be avoided for 1 ms following power-on to allow the reset action to complete.

## 7.2 LCD bias generator

Fractional LCD biasing voltages are obtained from an internal voltage divider consisting of three impedances connected in series between  $V_{LCD}$  and  $V_{SS}$ . The middle resistor can be bypassed to provide a  $\frac{1}{2}$  bias voltage level for the 1:2 multiplex configuration. The LCD voltage can be temperature compensated externally using the supply to pin  $V_{LCD}$ .

## 7.3 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the mode-set command (see [Table 11](#)) from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of  $V_{LCD}$  and the resulting discrimination ratios (D), are given in [Table 6](#).

**Table 6. Discrimination ratios**

| LCD drive mode | Number of: |        | LCD bias configuration | $\frac{V_{off(RMS)}}{V_{LCD}}$ | $\frac{V_{on(RMS)}}{V_{LCD}}$ | $D = \frac{V_{on(RMS)}}{V_{off(RMS)}}$ |
|----------------|------------|--------|------------------------|--------------------------------|-------------------------------|----------------------------------------|
|                | Backplanes | Levels |                        |                                |                               |                                        |
| static         | 1          | 2      | static                 | 0                              | 1                             | $\infty$                               |
| 1:2 multiplex  | 2          | 3      | $\frac{1}{2}$          | 0.354                          | 0.791                         | 2.236                                  |
| 1:2 multiplex  | 2          | 4      | $\frac{1}{3}$          | 0.333                          | 0.745                         | 2.236                                  |
| 1:3 multiplex  | 3          | 4      | $\frac{1}{3}$          | 0.333                          | 0.638                         | 1.915                                  |
| 1:4 multiplex  | 4          | 4      | $\frac{1}{3}$          | 0.333                          | 0.577                         | 1.732                                  |

A practical value for  $V_{LCD}$  is determined by equating  $V_{off(RMS)}$  with a defined LCD threshold voltage ( $V_{th}$ ), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode a suitable choice is  $V_{LCD} > 3V_{th}$ .

Multiplex drive modes of 1:3 and 1:4 with  $\frac{1}{2}$  bias are possible but the discrimination and hence the contrast ratios are smaller.

Bias is calculated by  $\frac{1}{1+a}$ , where the values for a are

a = 1 for  $\frac{1}{2}$  bias

$a = 2$  for  $\frac{1}{3}$  bias

The RMS on-state voltage ( $V_{on(RMS)}$ ) for the LCD is calculated with [Equation 1](#)

$$V_{on(RMS)} = V_{LCD} \sqrt{\frac{a^2 + 2a + n}{n \times (1 + a)^2}} \quad (1)$$

where the values for  $n$  are

$n = 1$  for static mode

$n = 2$  for 1:2 multiplex

$n = 3$  for 1:3 multiplex

$n = 4$  for 1:4 multiplex

The RMS off-state voltage ( $V_{off(RMS)}$ ) for the LCD is calculated with [Equation 2](#):

$$V_{off(RMS)} = V_{LCD} \sqrt{\frac{a^2 - 2a + n}{n \times (1 + a)^2}} \quad (2)$$

Discrimination is the ratio of  $V_{on(RMS)}$  to  $V_{off(RMS)}$  and is determined from [Equation 3](#):

$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{(a + 1)^2 + (n - 1)}{(a - 1)^2 + (n - 1)}} \quad (3)$$

Using [Equation 3](#), the discrimination for an LCD drive mode of 1:3 multiplex with

$\frac{1}{2}$  bias is  $\sqrt{3} = 1.732$  and the discrimination for an LCD drive mode of 1:4 multiplex with

$\frac{1}{2}$  bias is  $\frac{\sqrt{21}}{3} = 1.528$ .

The advantage of these LCD drive modes is a reduction of the LCD full scale voltage  $V_{LCD}$  as follows:

- 1:3 multiplex ( $\frac{1}{2}$  bias):  $V_{LCD} = \sqrt{6} \times V_{off(RMS)} = 2.449 V_{off(RMS)}$
- 1:4 multiplex ( $\frac{1}{2}$  bias):  $V_{LCD} = \left[ \frac{(4 \times \sqrt{3})}{3} \right] = 2.309 V_{off(RMS)}$

These compare with  $V_{LCD} = 3 V_{off(RMS)}$  when  $\frac{1}{3}$  bias is used.

It should be noted that  $V_{LCD}$  is sometimes referred as the LCD operating voltage.

### 7.3.1 Electro-optical performance

Suitable values for  $V_{on(RMS)}$  and  $V_{off(RMS)}$  are dependent on the LCD liquid used. The RMS voltage, at which a pixel will be switched on or off, determine the transmissibility of the pixel.

For any given liquid, there are two threshold values defined. One point is at 10 % relative transmission (at  $V_{low}$ ) and the other at 90 % relative transmission (at  $V_{high}$ ), see [Figure 4](#). For a good contrast performance, the following rules should be followed:

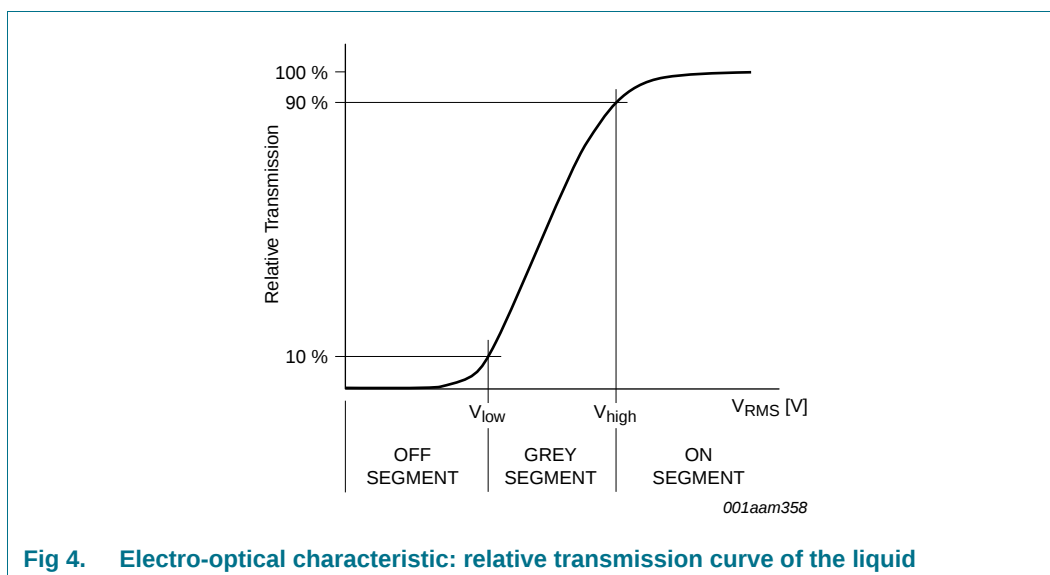
$$V_{on(RMS)} \geq V_{high} \quad (4)$$

$$V_{off(RMS)} \leq V_{low} \quad (5)$$

$V_{on(RMS)}$  and  $V_{off(RMS)}$  are properties of the display driver and are affected by the selection of  $a$ ,  $n$  (see [Equation 1](#) to [Equation 3](#)) and the  $V_{LCD}$  voltage.

$V_{th(off)}$  and  $V_{th(on)}$  are properties of the LCD liquid and can be provided by the module manufacturer.  $V_{th(off)}$  is sometimes just named  $V_{th}$ .  $V_{th(on)}$  is sometimes named saturation voltage  $V_{sat}$ .

It is important to match the module properties to those of the driver in order to achieve optimum performance.

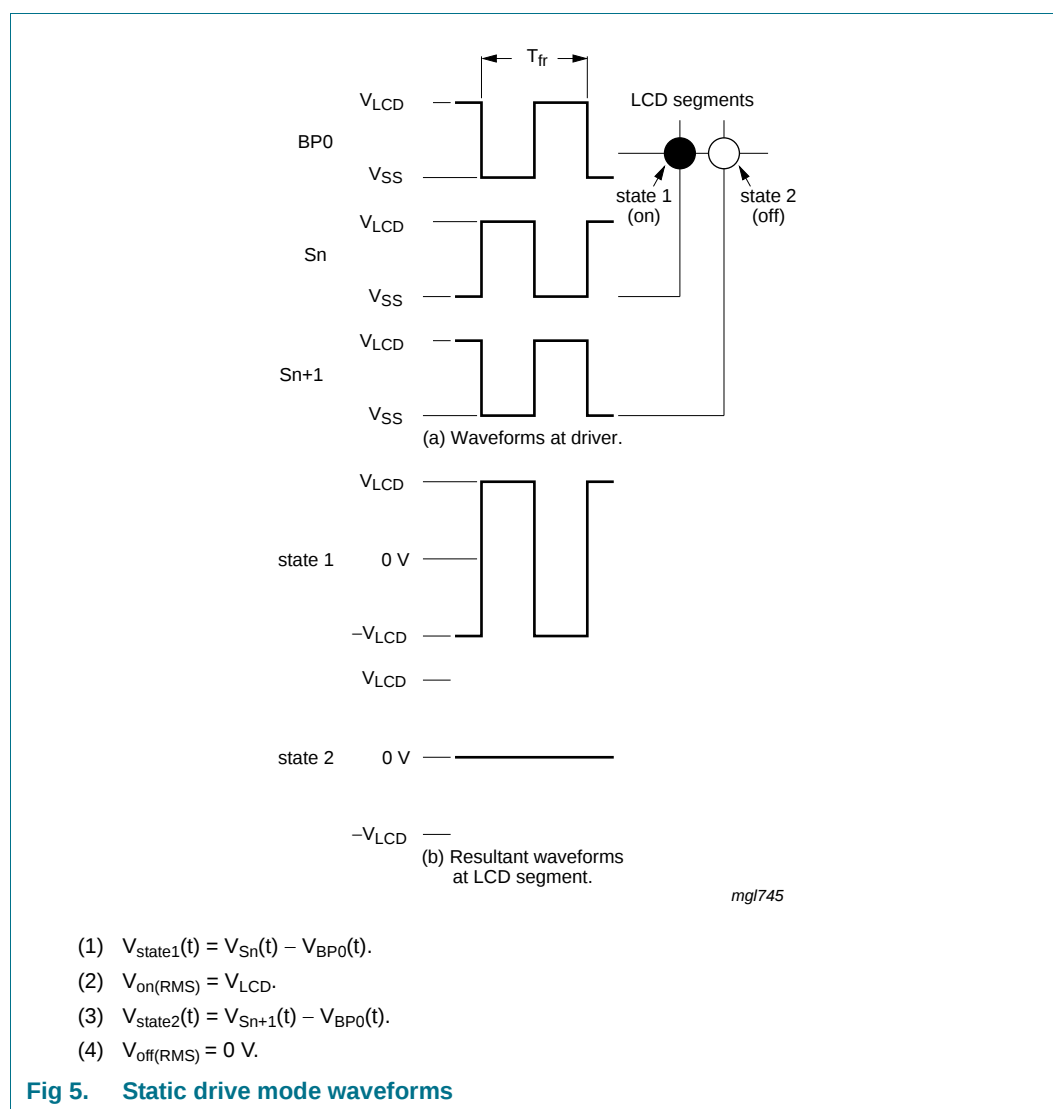


**Fig 4. Electro-optical characteristic: relative transmission curve of the liquid**

## 7.4 LCD drive mode waveforms

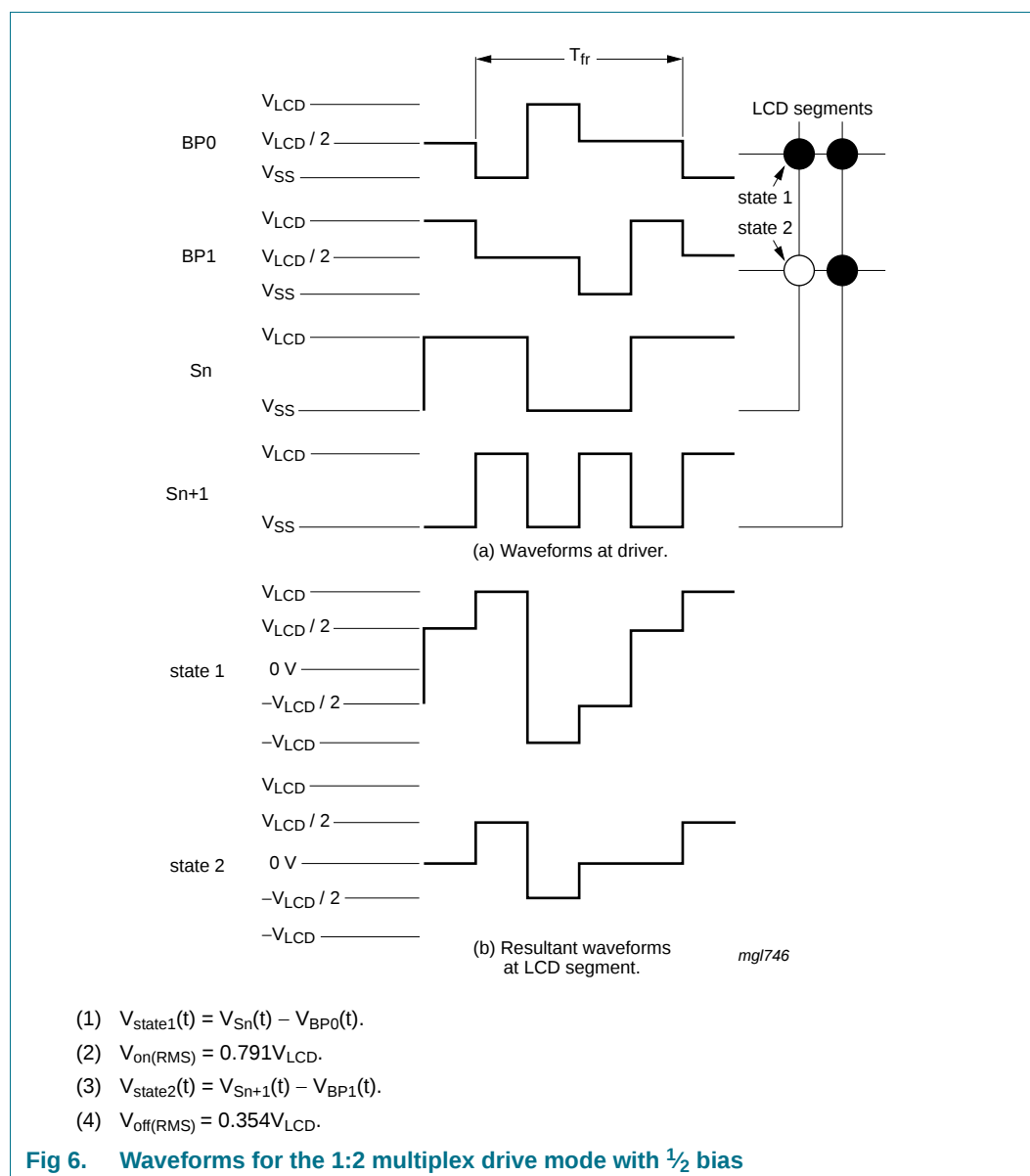
### 7.4.1 Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD. The backplane (BPn) and segment drive (Sn) waveforms for this mode are shown in [Figure 5](#).

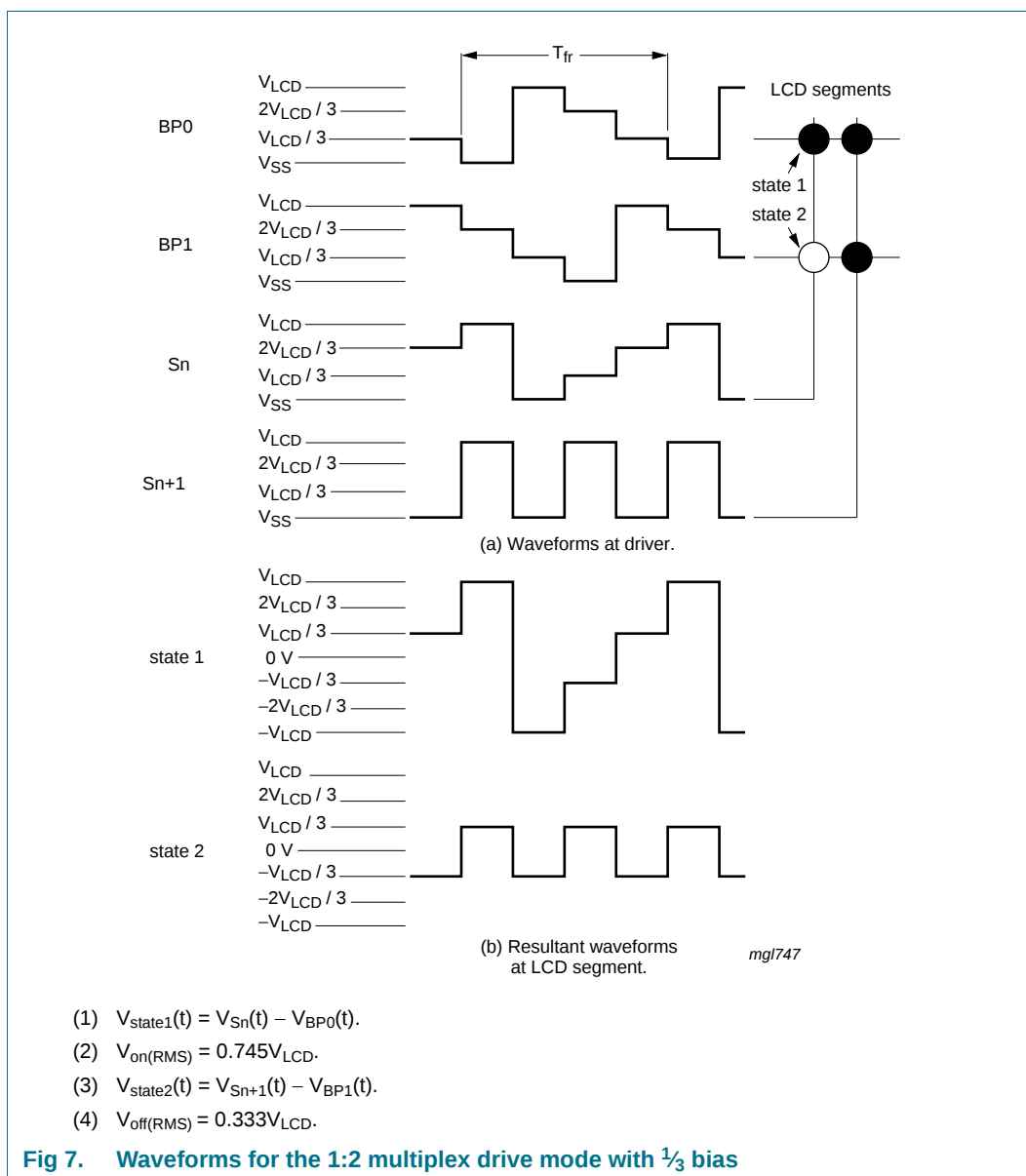


### 7.4.2 1:2 Multiplex drive mode

The 1:2 multiplex drive mode is used when two backplanes are provided in the LCD. This mode allows fractional LCD bias voltages of  $\frac{1}{2}$  bias or  $\frac{1}{3}$  bias as shown in [Figure 6](#) and [Figure 7](#).

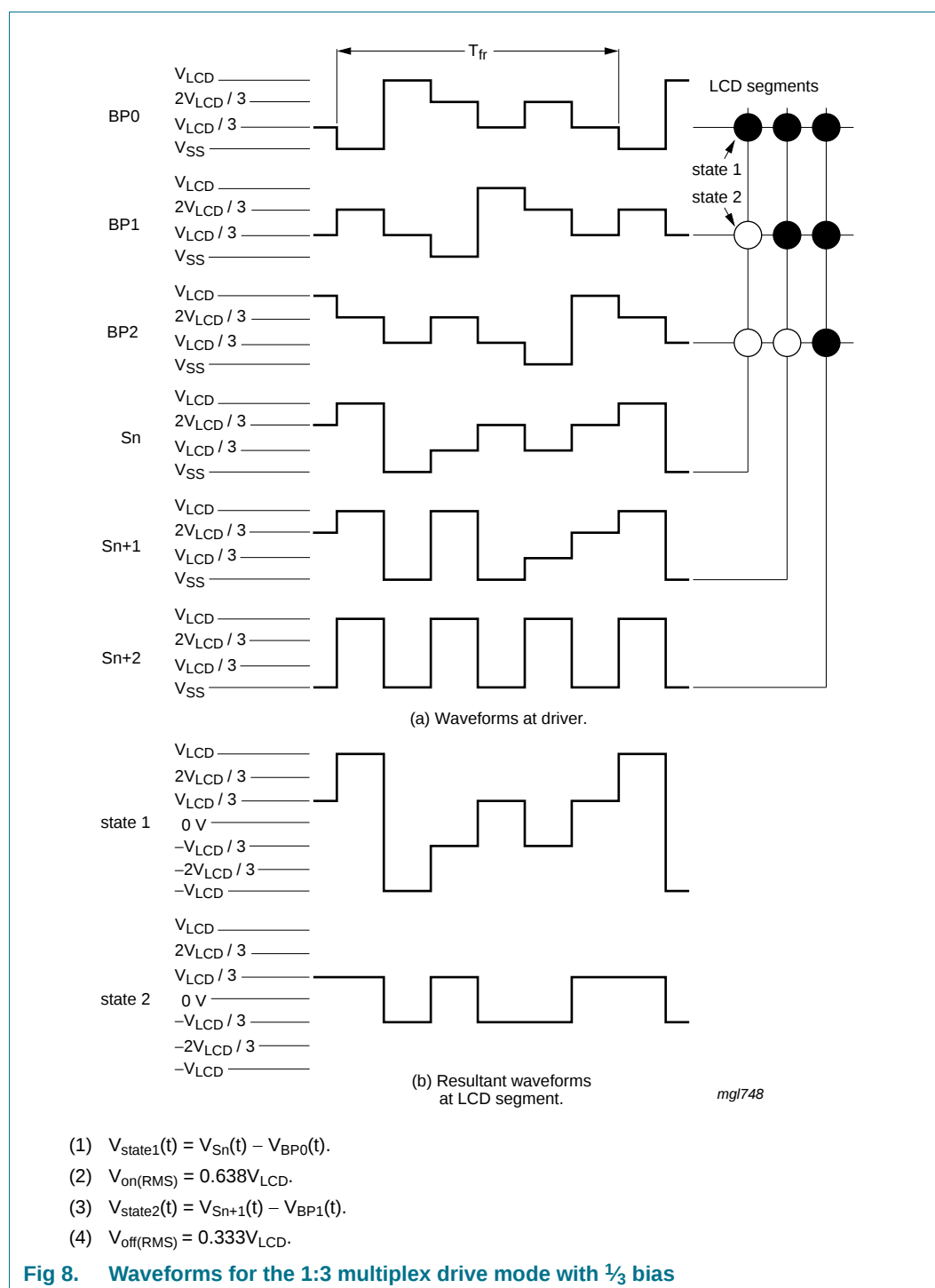


**Fig 6. Waveforms for the 1:2 multiplex drive mode with  $\frac{1}{2}$  bias**



### 7.4.3 1:3 Multiplex drive mode

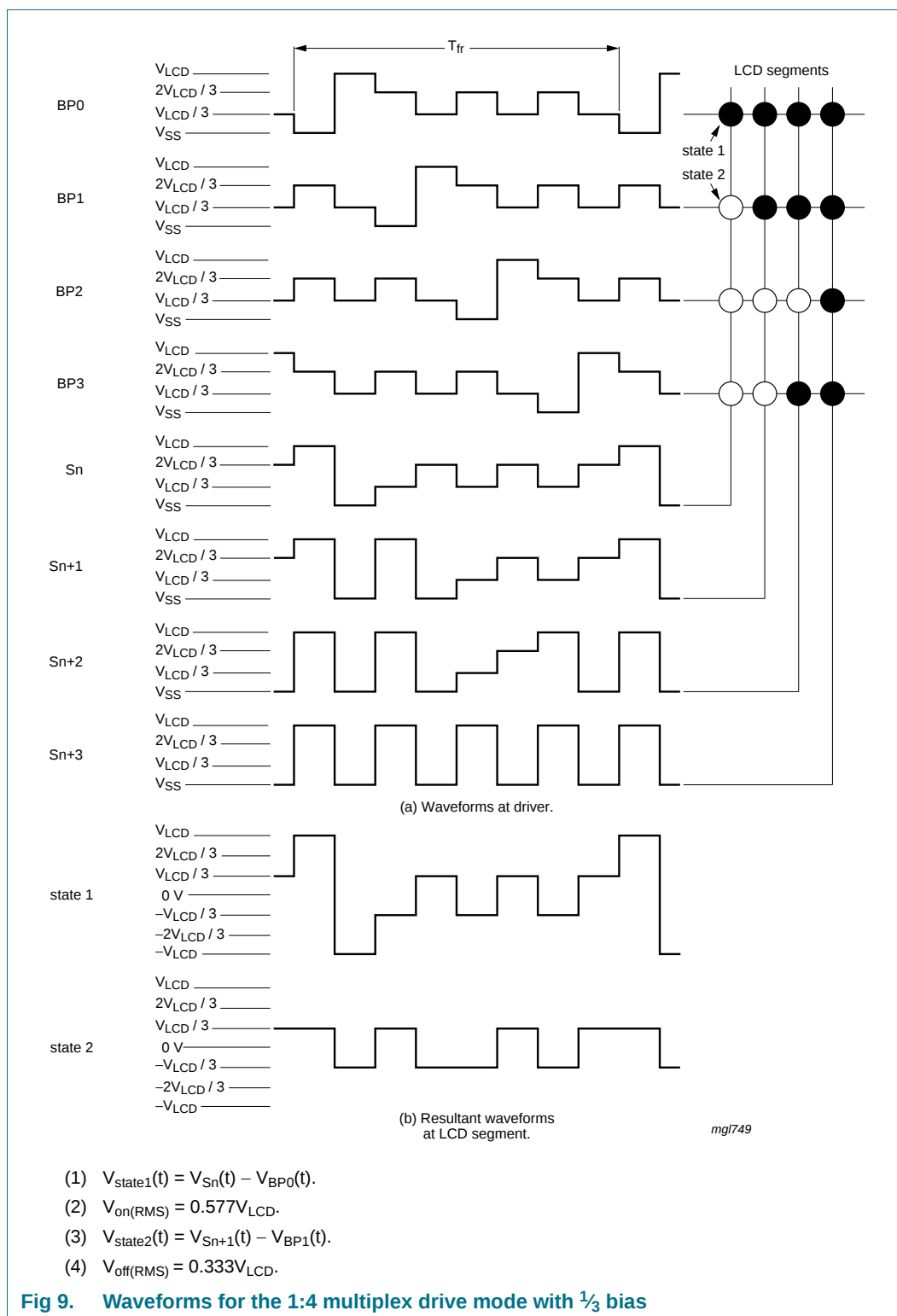
When three backplanes are provided in the LCD, the 1:3 multiplex drive mode applies (see [Figure 8](#)).



**Fig 8. Waveforms for the 1:3 multiplex drive mode with  $\frac{1}{3}$  bias**

#### 7.4.4 1:4 Multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies (see [Figure 9](#)).



## 7.5 Oscillator

### 7.5.1 Internal clock

The internal logic of the PCA8576D and its LCD drive signals are timed either by its internal oscillator or by an external clock. The internal oscillator is enabled by connecting pin OSC to pin V<sub>SS</sub>. If the internal oscillator is used, the output from pin CLK can be used as the clock signal for several PCA8576D in the system that are connected in cascade.

### 7.5.2 External clock

Pin CLK is enabled as an external clock input by connecting pin OSC to V<sub>DD</sub>.

The LCD frame signal frequency is determined by the clock frequency ( $f_{clk}$ ).

**Remark:** A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal.

## 7.6 Timing

The PCA8576D timing controls the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the correct timing relationship between each PCA8576D in the system is maintained by the synchronization signal at pin SYNC. The timing also generates the LCD frame signal whose frequency is derived from the clock frequency. The frame signal frequency is a fixed division of the clock frequency from either the internal or an external

$$\text{clock: } f_{fr} = \frac{f_{clk}}{24}.$$

## 7.7 Display register

The display register holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display register, the LCD segment outputs, and one column of the display RAM.

## 7.8 Segment outputs

The LCD drive section includes 40 segment outputs S0 to S39 which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data residing in the display register. When less than 40 segment outputs are required, the unused segment outputs should be left open-circuit.

## 7.9 Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which must be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required, the unused outputs can be left open-circuit.

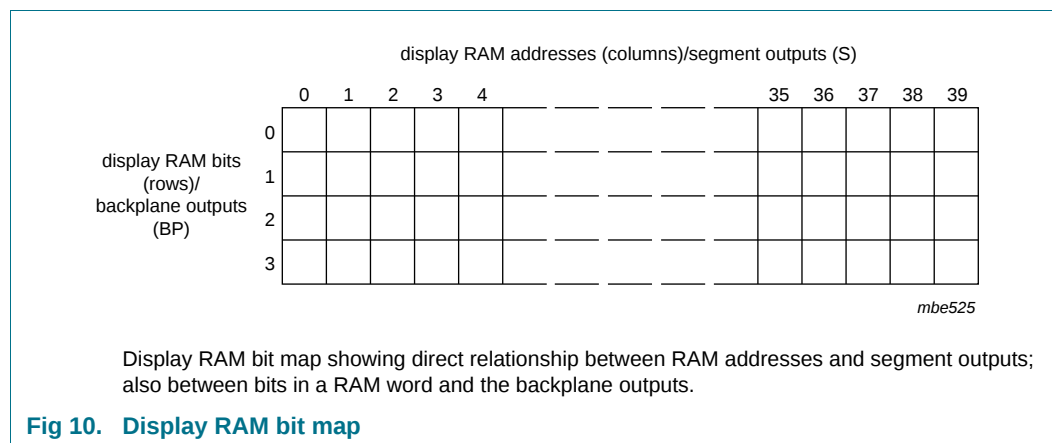
In the 1:3 multiplex drive mode, BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities.

In the 1:2 multiplex drive mode, BP0 and BP2, BP1 and BP3 all carry the same signals and may also be paired to increase the drive capabilities.

In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

## 7.10 Display RAM

The display RAM is a static  $40 \times 4$ -bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the on-state of the corresponding LCD element; similarly, a logic 0 indicates the off-state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The display RAM bit map [Figure 10](#) shows the rows 0 to 3 which correspond with the backplane outputs BP0 to BP3, and the columns 0 to 39 which correspond with the segment outputs S0 to S39. In multiplexed LCD applications the segment data of the first, second, third and fourth row of the display RAM are time-multiplexed with BP0, BP1, BP2 and BP3 respectively.



When display data is transmitted to the PCA8576D, the display bytes received are stored in the display RAM in accordance with the selected LCD drive mode. The data is stored as it arrives and does not wait for an acknowledge cycle as with the commands. Depending on the current multiplex drive mode, data is stored singularly, in pairs, triplets or quadruplets. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in [Figure 11](#); the RAM filling organization depicted applies equally to other LCD types.

| drive mode       | LCD segments | LCD backplanes | display RAM filling order                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | transmitted display byte |       |       |       |       |       |       |       |       |    |   |   |   |    |    |                                                                                                                                 |   |    |   |    |                                                                                                                                 |   |    |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |
|------------------|--------------|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|-------|-------|-------|-------|-------|-------|-------|-------|----|---|---|---|----|----|---------------------------------------------------------------------------------------------------------------------------------|---|----|---|----|---------------------------------------------------------------------------------------------------------------------------------|---|----|---|---|---------------------------------------------------------------------------------------------------------------------------------|---|---|---|---|---|---|---|----|---|---|---|---|---|---|---|---|---|---|---|---------------------------------------------------------------------------------------------------------------------------------|---|---|---|---|---|---|---|----|
| static           |              |                | <p>columns<br/>display RAM address/segment outputs (s)<br/>byte1</p> <table><tr><th>rows</th><th>n</th><th>n + 1</th><th>n + 2</th><th>n + 3</th><th>n + 4</th><th>n + 5</th><th>n + 6</th><th>n + 7</th></tr><tr><td>0</td><td>c</td><td>b</td><td>a</td><td>f</td><td>g</td><td>e</td><td>d</td><td>DP</td></tr><tr><td>1</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td></tr><tr><td>2</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td></tr><tr><td>3</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td></tr></table> | rows                     | n     | n + 1 | n + 2 | n + 3 | n + 4 | n + 5 | n + 6 | n + 7 | 0  | c | b | a | f  | g  | e                                                                                                                               | d | DP | 1 | x  | x                                                                                                                               | x | x  | x | x | x                                                                                                                               | x | 2 | x | x | x | x | x | x  | x | x | 3 | x | x | x | x | x | x | x | x | <p>MSB</p> <p>LSB</p> <table><tr><td>c</td><td>b</td><td>a</td><td>f</td><td>g</td><td>e</td><td>d</td><td>DP</td></tr></table> | c | b | a | f | g | e | d | DP |
| rows             | n            | n + 1          | n + 2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | n + 3                    | n + 4 | n + 5 | n + 6 | n + 7 |       |       |       |       |    |   |   |   |    |    |                                                                                                                                 |   |    |   |    |                                                                                                                                 |   |    |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |
| 0                | c            | b              | a                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | f                        | g     | e     | d     | DP    |       |       |       |       |    |   |   |   |    |    |                                                                                                                                 |   |    |   |    |                                                                                                                                 |   |    |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |
| 1                | x            | x              | x                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | x                        | x     | x     | x     | x     |       |       |       |       |    |   |   |   |    |    |                                                                                                                                 |   |    |   |    |                                                                                                                                 |   |    |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |
| 2                | x            | x              | x                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | x                        | x     | x     | x     | x     |       |       |       |       |    |   |   |   |    |    |                                                                                                                                 |   |    |   |    |                                                                                                                                 |   |    |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |
| 3                | x            | x              | x                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | x                        | x     | x     | x     | x     |       |       |       |       |    |   |   |   |    |    |                                                                                                                                 |   |    |   |    |                                                                                                                                 |   |    |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |
| c                | b            | a              | f                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | g                        | e     | d     | DP    |       |       |       |       |       |    |   |   |   |    |    |                                                                                                                                 |   |    |   |    |                                                                                                                                 |   |    |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |
| 1:2<br>multiplex |              |                | <p>columns<br/>display RAM address/segment outputs (s)<br/>byte1</p> <table><tr><th>rows</th><th>n</th><th>n + 1</th><th>n + 2</th><th>n + 3</th></tr><tr><td>0</td><td>a</td><td>f</td><td>e</td><td>d</td></tr><tr><td>1</td><td>b</td><td>g</td><td>c</td><td>DP</td></tr><tr><td>2</td><td>x</td><td>x</td><td>x</td><td>x</td></tr><tr><td>3</td><td>x</td><td>x</td><td>x</td><td>x</td></tr></table>                                                                                                                                                                                                                         | rows                     | n     | n + 1 | n + 2 | n + 3 | 0     | a     | f     | e     | d  | 1 | b | g | c  | DP | 2                                                                                                                               | x | x  | x | x  | 3                                                                                                                               | x | x  | x | x | <p>MSB</p> <p>LSB</p> <table><tr><td>a</td><td>b</td><td>f</td><td>g</td><td>e</td><td>c</td><td>d</td><td>DP</td></tr></table> | a | b | f | g | e | c | d | DP |   |   |   |   |   |   |   |   |   |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |
| rows             | n            | n + 1          | n + 2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | n + 3                    |       |       |       |       |       |       |       |       |    |   |   |   |    |    |                                                                                                                                 |   |    |   |    |                                                                                                                                 |   |    |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |
| 0                | a            | f              | e                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | d                        |       |       |       |       |       |       |       |       |    |   |   |   |    |    |                                                                                                                                 |   |    |   |    |                                                                                                                                 |   |    |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |
| 1                | b            | g              | c                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | DP                       |       |       |       |       |       |       |       |       |    |   |   |   |    |    |                                                                                                                                 |   |    |   |    |                                                                                                                                 |   |    |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |
| 2                | x            | x              | x                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | x                        |       |       |       |       |       |       |       |       |    |   |   |   |    |    |                                                                                                                                 |   |    |   |    |                                                                                                                                 |   |    |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |
| 3                | x            | x              | x                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | x                        |       |       |       |       |       |       |       |       |    |   |   |   |    |    |                                                                                                                                 |   |    |   |    |                                                                                                                                 |   |    |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |
| a                | b            | f              | g                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | e                        | c     | d     | DP    |       |       |       |       |       |    |   |   |   |    |    |                                                                                                                                 |   |    |   |    |                                                                                                                                 |   |    |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |
| 1:3<br>multiplex |              |                | <p>columns<br/>display RAM address/segment outputs (s)<br/>byte1</p> <table><tr><th>rows</th><th>n</th><th>n + 1</th><th>n + 2</th></tr><tr><td>0</td><td>b</td><td>a</td><td>f</td></tr><tr><td>1</td><td>DP</td><td>d</td><td>e</td></tr><tr><td>2</td><td>c</td><td>g</td><td>x</td></tr><tr><td>3</td><td>x</td><td>x</td><td>x</td></tr></table>                                                                                                                                                                                                                                                                               | rows                     | n     | n + 1 | n + 2 | 0     | b     | a     | f     | 1     | DP | d | e | 2 | c  | g  | x                                                                                                                               | 3 | x  | x | x  | <p>MSB</p> <p>LSB</p> <table><tr><td>b</td><td>DP</td><td>c</td><td>a</td><td>d</td><td>g</td><td>f</td><td>e</td></tr></table> | b | DP | c | a | d                                                                                                                               | g | f | e |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |
| rows             | n            | n + 1          | n + 2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                          |       |       |       |       |       |       |       |       |    |   |   |   |    |    |                                                                                                                                 |   |    |   |    |                                                                                                                                 |   |    |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |
| 0                | b            | a              | f                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                          |       |       |       |       |       |       |       |       |    |   |   |   |    |    |                                                                                                                                 |   |    |   |    |                                                                                                                                 |   |    |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |
| 1                | DP           | d              | e                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                          |       |       |       |       |       |       |       |       |    |   |   |   |    |    |                                                                                                                                 |   |    |   |    |                                                                                                                                 |   |    |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |
| 2                | c            | g              | x                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                          |       |       |       |       |       |       |       |       |    |   |   |   |    |    |                                                                                                                                 |   |    |   |    |                                                                                                                                 |   |    |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |
| 3                | x            | x              | x                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                          |       |       |       |       |       |       |       |       |    |   |   |   |    |    |                                                                                                                                 |   |    |   |    |                                                                                                                                 |   |    |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |
| b                | DP           | c              | a                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | d                        | g     | f     | e     |       |       |       |       |       |    |   |   |   |    |    |                                                                                                                                 |   |    |   |    |                                                                                                                                 |   |    |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |
| 1:4<br>multiplex |              |                | <p>columns<br/>display RAM address/segment outputs (s)<br/>byte1</p> <table><tr><th>rows</th><th>n</th><th>n + 1</th></tr><tr><td>0</td><td>a</td><td>f</td></tr><tr><td>1</td><td>c</td><td>e</td></tr><tr><td>2</td><td>b</td><td>g</td></tr><tr><td>3</td><td>DP</td><td>d</td></tr></table>                                                                                                                                                                                                                                                                                                                                     | rows                     | n     | n + 1 | 0     | a     | f     | 1     | c     | e     | 2  | b | g | 3 | DP | d  | <p>MSB</p> <p>LSB</p> <table><tr><td>a</td><td>c</td><td>b</td><td>DP</td><td>f</td><td>e</td><td>g</td><td>d</td></tr></table> | a | c  | b | DP | f                                                                                                                               | e | g  | d |   |                                                                                                                                 |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |
| rows             | n            | n + 1          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                          |       |       |       |       |       |       |       |       |    |   |   |   |    |    |                                                                                                                                 |   |    |   |    |                                                                                                                                 |   |    |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |
| 0                | a            | f              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                          |       |       |       |       |       |       |       |       |    |   |   |   |    |    |                                                                                                                                 |   |    |   |    |                                                                                                                                 |   |    |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |
| 1                | c            | e              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                          |       |       |       |       |       |       |       |       |    |   |   |   |    |    |                                                                                                                                 |   |    |   |    |                                                                                                                                 |   |    |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |
| 2                | b            | g              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                          |       |       |       |       |       |       |       |       |    |   |   |   |    |    |                                                                                                                                 |   |    |   |    |                                                                                                                                 |   |    |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |
| 3                | DP           | d              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                          |       |       |       |       |       |       |       |       |    |   |   |   |    |    |                                                                                                                                 |   |    |   |    |                                                                                                                                 |   |    |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |
| a                | c            | b              | DP                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | f                        | e     | g     | d     |       |       |       |       |       |    |   |   |   |    |    |                                                                                                                                 |   |    |   |    |                                                                                                                                 |   |    |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |                                                                                                                                 |   |   |   |   |   |   |   |    |

001aaJ646

x = data bit unchanged.

Fig 11. Relationship between LCD layout, drive mode, display RAM filling order and display data transmitted over the I<sup>2</sup>C-bus

The following applies to [Figure 11](#):

- In static drive mode the eight transmitted data bits are placed in row 0 as one byte.
- In 1:2 multiplex drive mode the eight transmitted data bits are placed in pairs into row 0 and 1 as two successive 4-bit RAM words.
- In 1:3 multiplex drive mode the eight bits are placed in triples into row 0, 1, and 2 as three successive 3-bit RAM words, with bit 3 of the third address left unchanged. It is not recommended to use this bit in a display because of the difficult addressing. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overwriting adjacent data because always full bytes are transmitted.
- In 1:4 multiplex drive mode, the eight transmitted data bits are placed in quadruples into row 0, 1, 2, and 3 as two successive 4-bit RAM words.

### 7.11 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer.

This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the load-data-pointer command (see [Section 7.17](#)).

Following this command, an arriving data byte is stored at the display RAM address indicated by the data pointer. The filling order is shown in [Figure 11](#).

After each byte is stored, the content of the data pointer is automatically incremented by a value dependent on the selected LCD drive mode:

After each byte is stored, the contents of the data pointer is automatically incremented by a value dependent on the selected LCD drive mode:

- In static drive mode by eight
- In 1:2 multiplex drive mode by four
- In 1:3 multiplex drive mode by three
- In 1:4 multiplex drive mode by two

If an I<sup>2</sup>C-bus data access is terminated early then the state of the data pointer is unknown. The data pointer should be re-written prior to further RAM accesses.

### 7.12 Subaddress counter

The storage of display data is determined by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter match with the hardware subaddress applied to A0, A1 and A2. The subaddress counter value is defined by the device-select command (see [Section 7.17](#)). If the contents of the subaddress counter and the hardware subaddress do not match then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are sent to the display RAM, automatic wrap-over to the next PCA8576D occurs when the last RAM address is exceeded.

Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character (such as during the 14<sup>th</sup> display data byte transmitted in 1:3 multiplex mode).

The hardware subaddress must not be changed while the device is being accessed on the I<sup>2</sup>C-bus interface.

### 7.13 Output bank selector

The output bank selector (see [Table 14](#)) selects one of the four rows per display RAM address for transfer to the display register. The actual row selected depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence.

- In 1:4 multiplex mode, all RAM addresses of row 0 are selected, these are followed by the contents of row 1, 2, and then 3
- In 1:3 multiplex mode, rows 0, 1, and 2 are selected sequentially
- In 1:2 multiplex mode, rows 0 and 1 are selected
- In static mode, row 0 is selected

The  $\overline{\text{SYNC}}$  signal resets these sequences to the following starting points: row 3 for 1:4 multiplex, row 2 for 1:3 multiplex, row 1 for 1:2 multiplex and row 0 for static mode.

The PCA8576D includes a RAM bank switching feature in the static and 1:2 multiplex drive modes. In the static drive mode, the bank-select command may request the contents of row 2 to be selected for display instead of the contents of row 0. In the 1:2 mode, the contents of rows 2 and 3 may be selected instead of rows 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it, once it is assembled.

### 7.14 Input bank selector

The input bank selector loads display data into the display RAM in accordance with the selected LCD drive configuration. Display data can be loaded in row 2 in static drive mode or in rows 2 and 3 in 1:2 multiplex drive mode by using the bank-select command. The input bank selector functions independently to the output bank selector.

### 7.15 Blinking

The PCA8576D has a very versatile display blinking capability. The whole display can blink at a frequency selected by the blink-select command (see [Table 15](#)). Each blink frequency is a fraction of the clock frequency; the ratio between the clock frequency and blink frequency depends on the blink mode selected (see [Table 7](#)).

An additional feature allows an arbitrary selection of LCD segments to blink in the static and 1:2 drive modes. This is implemented without any communication overheads by the output bank selector which alternates the displayed data between the data in the display RAM bank and the data in an alternative RAM bank at the blink frequency. This mode can also be implemented by the blink-select command (see [Table 15](#)).

In the 1:3 and 1:4 drive modes, where no alternative RAM bank is available, groups of LCD segments can blink selectively by changing the display RAM data at fixed time intervals.

The entire display can blink at a frequency other than the nominal blink frequency by sequentially resetting and setting the display enable bit E at the required rate using the mode-set command (see [Table 11](#)).

Table 7. Blinking frequencies<sup>[1]</sup>

| Blink mode | Normal operating mode ratio | Nominal blink frequency |
|------------|-----------------------------|-------------------------|
| off        | -                           | blinking off            |
| 1          | $\frac{f_{clk}}{768}$       | 2 Hz                    |
| 2          | $\frac{f_{clk}}{1536}$      | 1 Hz                    |
| 3          | $\frac{f_{clk}}{3072}$      | 0.5 Hz                  |

[1] Blink modes 1, 2 and 3 and the nominal blink frequencies 0.5 Hz, 1 Hz and 2 Hz correspond to an oscillator frequency ( $f_{clk}$ ) of 1536 Hz (see [Section 11](#)).

7.16 Characteristics of the I<sup>2</sup>C-bus

The I<sup>2</sup>C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial CLock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.16.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal (see [Figure 12](#)).

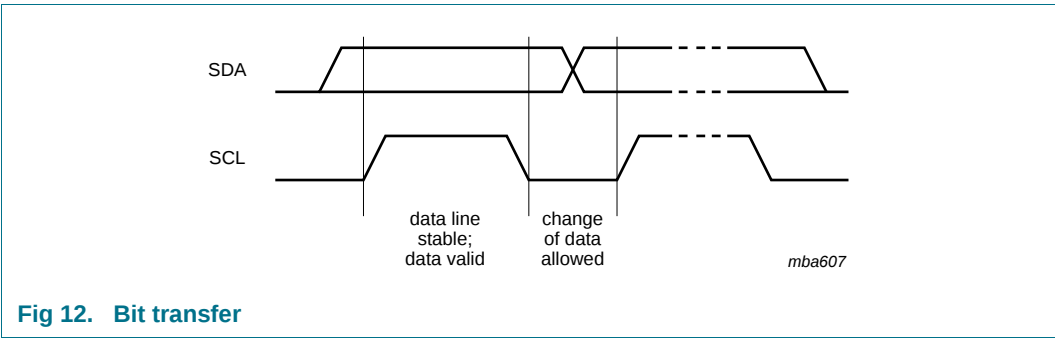


Fig 12. Bit transfer

### 7.16.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition - S.

A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition - P (see [Figure 13](#)).

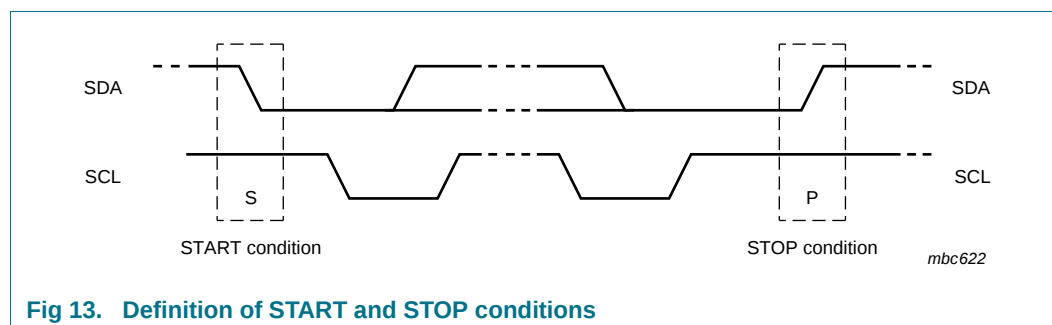


Fig 13. Definition of START and STOP conditions

### 7.16.3 System configuration

A device generating a message is a transmitter, a device receiving a message is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves (see [Figure 14](#)).

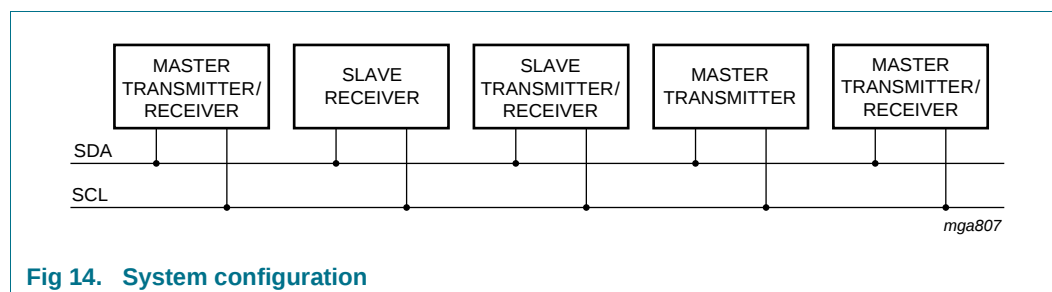


Fig 14. System configuration

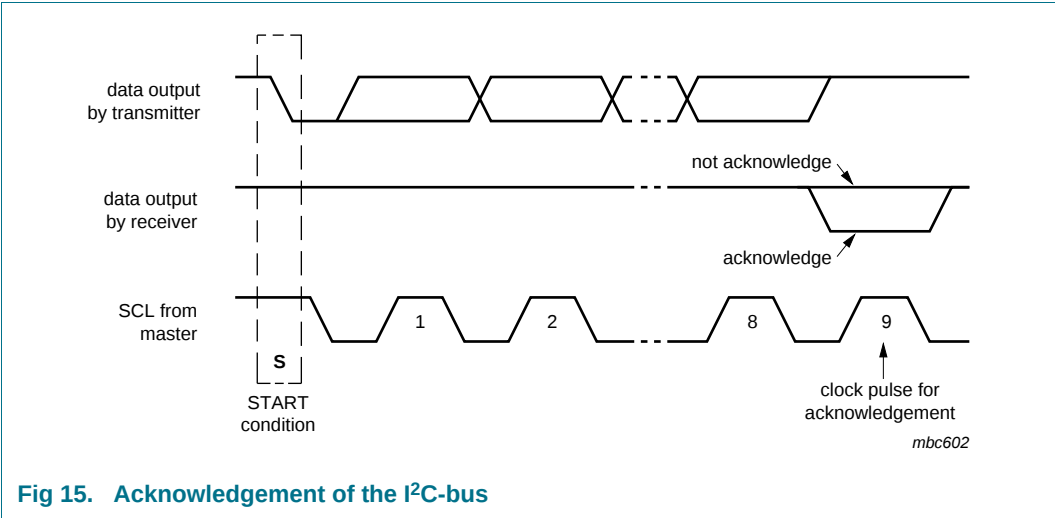
### 7.16.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge cycle.

- A slave receiver which is addressed must generate an acknowledge after the reception of each byte.
- Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).

- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I<sup>2</sup>C-bus is shown in [Figure 15](#).



**Fig 15. Acknowledgement of the I<sup>2</sup>C-bus**

### 7.16.5 I<sup>2</sup>C-bus controller

The PCA8576D acts as an I<sup>2</sup>C-bus slave receiver. It does not initiate I<sup>2</sup>C-bus transfers or transmit data to an I<sup>2</sup>C-bus master receiver. The only data output from the PCA8576D are the acknowledge signals of the selected devices. Device selection depends on the I<sup>2</sup>C-bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1 and A2 are normally tied to V<sub>SS</sub> which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are tied to V<sub>SS</sub> or V<sub>DD</sub> in accordance with a binary coding scheme such that no two devices with a common I<sup>2</sup>C-bus slave address have the same hardware subaddress.

### 7.16.6 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

### 7.16.7 I<sup>2</sup>C-bus protocol

Two I<sup>2</sup>C-bus slave addresses (0111 000 and 0111 001) are reserved for the PCA8576D.

The PCA8576D slave address is illustrated in [Table 8](#).

**Table 8. I<sup>2</sup>C slave address byte**

| Bit | Slave address |   |   |   |   |   |     | 0   |
|-----|---------------|---|---|---|---|---|-----|-----|
|     | 7             | 6 | 5 | 4 | 3 | 2 | 1   |     |
|     | MSB           |   |   |   |   |   |     | LSB |
|     | 0             | 1 | 1 | 1 | 0 | 0 | SA0 | R/W |

The least significant bit of the slave address that a PCA8576D will respond to is defined by the level tied to its SA0 input. The PCA8576D is a write-only device and will not respond to a read access. Having two reserved slave addresses allows the following on the same I<sup>2</sup>C-bus:

- Up to 16 PCA8576D for very large LCD applications
- The use of two types of LCD multiplex drive modes.

The I<sup>2</sup>C-bus protocol is shown in [Figure 16](#). The sequence is initiated with a START condition (S) from the I<sup>2</sup>C-bus master which is followed by one of two possible PCA8576D slave addresses available. All PCA8576D whose SA0 inputs correspond to bit 0 of the slave address respond by asserting an acknowledge in parallel. This I<sup>2</sup>C-bus transfer is ignored by all PCA8576D whose SA0 inputs are set to the alternative level.

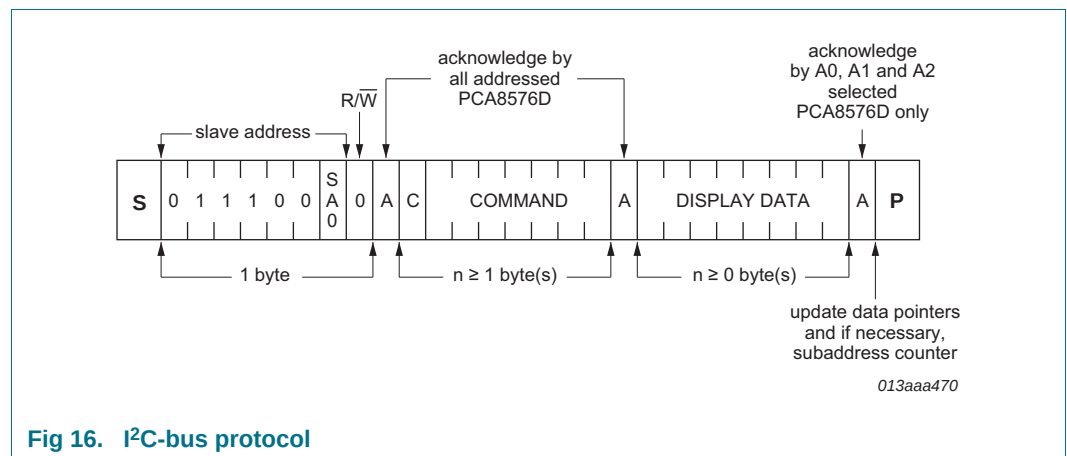


Fig 16. I<sup>2</sup>C-bus protocol

After an acknowledgement, one or more command bytes follow, that define the status of each addressed PCA8576D.

The last command byte sent is identified by resetting its most significant bit, continuation bit C, (see [Figure 17](#)). The command bytes are also acknowledged by all addressed PCA8576D on the bus.

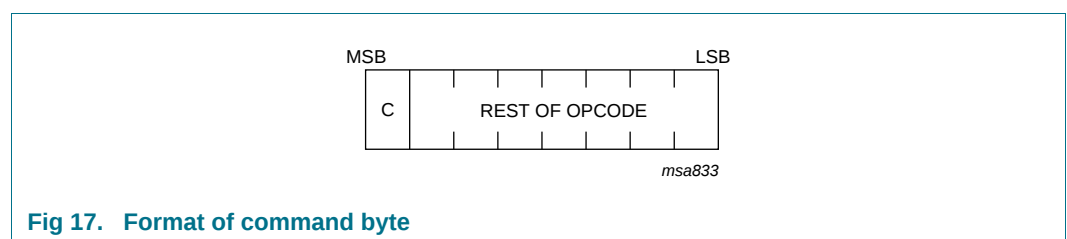


Fig 17. Format of command byte

After the last command byte, one or more display data bytes may follow. Display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data directed to the intended PCA8576D device.

An acknowledgement after each byte is asserted only by the PCA8576D that are addressed via address lines A0, A1 and A2. After the last display byte, the I<sup>2</sup>C-bus master asserts a STOP condition (P). Alternately a START may be asserted to restart an I<sup>2</sup>C-bus access.

## 7.17 Command decoder

The command decoder identifies command bytes that arrive on the I<sup>2</sup>C-bus. The commands available to the PCA8576D are defined in [Table 9](#).

**Table 9. Definition of PCA8576D commands**

| Command           | Operation Code |   |        |                     |   |        |         |   | Reference                |
|-------------------|----------------|---|--------|---------------------|---|--------|---------|---|--------------------------|
| Bit               | 7              | 6 | 5      | 4                   | 3 | 2      | 1       | 0 |                          |
| mode-set          | C              | 1 | 0      | <a href="#">[1]</a> | E | B      | M[1:0]  |   | <a href="#">Table 11</a> |
| load-data-pointer | C              | 0 | P[5:0] |                     |   |        |         |   | <a href="#">Table 12</a> |
| device-select     | C              | 1 | 1      | 0                   | 0 | A[2:0] |         |   | <a href="#">Table 13</a> |
| bank-select       | C              | 1 | 1      | 1                   | 1 | 0      | I       | O | <a href="#">Table 14</a> |
| blink-select      | C              | 1 | 1      | 1                   | 0 | AB     | BF[1:0] |   | <a href="#">Table 15</a> |

[1] Not used.

All available commands carry a continuation bit C in their most significant bit position as shown in [Figure 17](#). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If this bit is reset, it indicates that the command byte is the last in the transfer. Further bytes will be regarded as display data (see [Table 10](#)).

**Table 10. C bit description**

| Bit | Symbol | Value | Description                                                                   |
|-----|--------|-------|-------------------------------------------------------------------------------|
| 7   | C      |       | <b>continue bit</b>                                                           |
|     |        | 0     | last control byte in the transfer; next byte will be regarded as display data |
|     |        | 1     | control bytes continue; next byte will be a command too                       |

**Table 11. Mode-set command bit description**

| Bit    | Symbol | Value                  | Description                                       |
|--------|--------|------------------------|---------------------------------------------------|
| 7      | C      | 0, 1                   | see <a href="#">Table 10</a>                      |
| 6 to 5 | -      | 10                     | fixed value                                       |
| 4      | -      | -                      | unused                                            |
| 3      | E      |                        | <b>display status</b> <a href="#">[1]</a>         |
|        |        | 0 <a href="#">[2]</a>  | disabled (blank) <a href="#">[3]</a>              |
|        |        | 1                      | enabled                                           |
| 2      | B      |                        | <b>LCD bias configuration</b> <a href="#">[4]</a> |
|        |        | 0 <a href="#">[2]</a>  | $\frac{1}{3}$ bias                                |
|        |        | 1                      | $\frac{1}{2}$ bias                                |
| 1 to 0 | M[1:0] |                        | <b>LCD drive mode selection</b>                   |
|        |        | 01                     | static; BP0                                       |
|        |        | 10                     | 1:2 multiplex; BP0, BP1                           |
|        |        | 11                     | 1:3 multiplex; BP0, BP1, BP2                      |
|        |        | 00 <a href="#">[2]</a> | 1:4 multiplex; BP0, BP1, BP2, BP3                 |

[1] The possibility to disable the display allows implementation of blinking under external control.

[2] Default value.

[3] The display is disabled by setting all backplane and segment outputs to V<sub>LCD</sub>.

[4] Not applicable for static drive mode.

**Table 12. Load-data-pointer command bit description**

| Bit    | Symbol | Value                           | Description                                                                                               |
|--------|--------|---------------------------------|-----------------------------------------------------------------------------------------------------------|
| 7      | C      | 0, 1                            | see <a href="#">Table 10</a>                                                                              |
| 6      | -      | 0                               | fixed value                                                                                               |
| 5 to 0 | P[5:0] | 000000 <sup>[1]</sup> to 100111 | 6 bit binary value, 0 to 39; transferred to the data pointer to define one of forty display RAM addresses |

[1] Default value.

**Table 13. Device-select command bit description**

| Bit    | Symbol | Value                     | Description                                                                                                    |
|--------|--------|---------------------------|----------------------------------------------------------------------------------------------------------------|
| 7      | C      | 0, 1                      | see <a href="#">Table 10</a>                                                                                   |
| 6 to 3 | -      | 1100                      | fixed value                                                                                                    |
| 2 to 0 | A[2:0] | 000 <sup>[1]</sup> to 111 | 3 bit binary value, 0 to 7; transferred to the subaddress counter to define one of eight hardware subaddresses |

[1] Default value.

**Table 14. Bank-select command bit description**

| Bit    | Symbol | Value            | Description                                                    |                              |
|--------|--------|------------------|----------------------------------------------------------------|------------------------------|
|        |        |                  | Static                                                         | 1:2 multiplex <sup>[1]</sup> |
| 7      | C      | 0, 1             | see <a href="#">Table 10</a>                                   |                              |
| 6 to 2 | -      | 11110            | fixed value                                                    |                              |
| 1      | I      |                  | <b>input bank selection</b> ; storage of arriving display data |                              |
|        |        | 0 <sup>[2]</sup> | RAM bit 0                                                      | RAM bits 0 and 1             |
|        |        | 1                | RAM bit 2                                                      | RAM bits 2 and 3             |
| 0      | O      |                  | <b>output bank selection</b> ; retrieval of LCD display data   |                              |
|        |        | 0 <sup>[2]</sup> | RAM bit 0                                                      | RAM bits 0 and 1             |
|        |        | 1                | RAM bit 2                                                      | RAM bits 2 and 3             |

[1] The bank-select command has no effect in 1:3 and 1:4 multiplex drive modes.

[2] Default value.

**Table 15. Blink-select command bit description**

| Bit    | Symbol  | Value             | Description                                |
|--------|---------|-------------------|--------------------------------------------|
| 7      | C       | 0, 1              | see <a href="#">Table 10</a>               |
| 6 to 3 | -       | 1110              | fixed value                                |
| 2      | AB      |                   | <b>blink mode selection</b>                |
|        |         | 0 <sup>[1]</sup>  | normal blinking <sup>[2]</sup>             |
|        |         | 1                 | alternate RAM bank blinking <sup>[3]</sup> |
| 1 to 0 | BF[1:0] |                   | <b>blink frequency selection</b>           |
|        |         | 00 <sup>[1]</sup> | off                                        |
|        |         | 01                | 1                                          |
|        |         | 10                | 2                                          |
|        |         | 11                | 3                                          |

[1] Default value.

[2] Normal blinking is assumed when the LCD multiplex drive modes 1:3 or 1:4 are selected.

[3] Alternate RAM bank blinking does not apply in 1:3 and 1:4 multiplex drive modes.

## 7.18 Display controller

The display controller executes the commands identified by the command decoder. It contains the device's status registers and coordinates their effects. The display controller is also responsible for loading display data into the display RAM in the correct filling order.

8. Internal circuitry

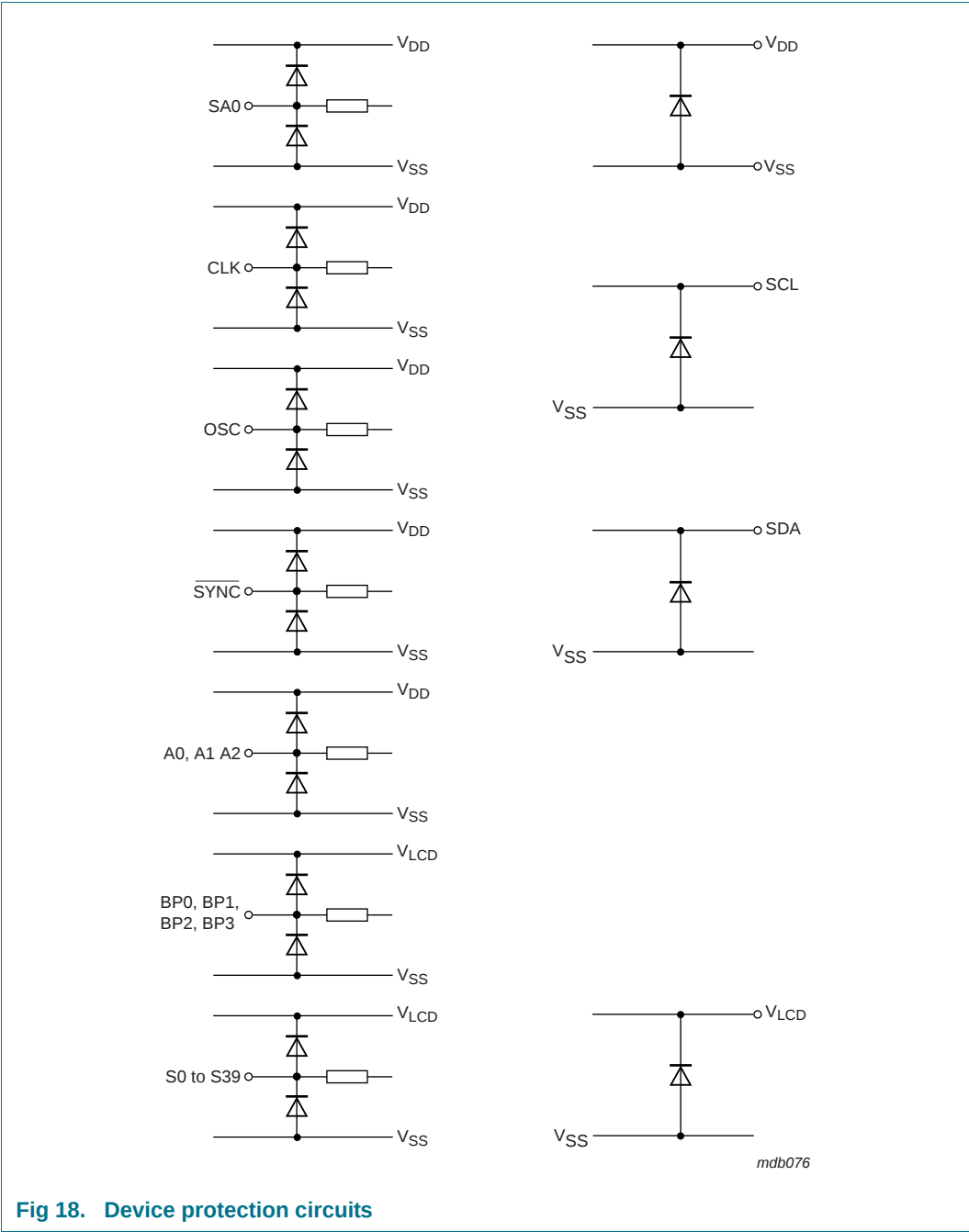


Fig 18. Device protection circuits

## 9. Limiting values

### CAUTION



Static voltages across the liquid crystal display can build up when the LCD supply voltage ( $V_{LCD}$ ) is on while the IC supply voltage ( $V_{DD}$ ) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts,  $V_{LCD}$  and  $V_{DD}$  must be applied or removed together.

**Table 16. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol        | Parameter                       | Conditions                                                  | Min     | Max   | Unit |
|---------------|---------------------------------|-------------------------------------------------------------|---------|-------|------|
| $V_{DD}$      | supply voltage                  |                                                             | -0.5    | +6.5  | V    |
| $V_{LCD}$     | LCD supply voltage              |                                                             | -0.5    | +7.5  | V    |
| $V_I$         | input voltage                   | on each of the pins CLK, SDA, SCL, SYNC, SA0, OSC, A0 to A2 | -0.5    | +6.5  | V    |
| $V_O$         | output voltage                  | on each of the pins S0 to S39, BP0 to BP3                   | -0.5    | +7.5  | V    |
| $I_I$         | input current                   |                                                             | -10     | +10   | mA   |
| $I_O$         | output current                  |                                                             | -10     | +10   | mA   |
| $I_{DD}$      | supply current                  |                                                             | -50     | +50   | mA   |
| $I_{DD(LCD)}$ | LCD supply current              |                                                             | -50     | +50   | mA   |
| $I_{SS}$      | ground supply current           |                                                             | -50     | +50   | mA   |
| $P_{tot}$     | total power dissipation         |                                                             | -       | 400   | mW   |
| $P_O$         | output power                    |                                                             | -       | 100   | mW   |
| $V_{ESD}$     | electrostatic discharge voltage | HBM                                                         | [1] -   | ±5000 | V    |
|               |                                 | MM                                                          | [2] -   | ±200  | V    |
| $I_{lu}$      | latch-up current                |                                                             | [3] -   | 100   | mA   |
| $T_{stg}$     | storage temperature             |                                                             | [4] -65 | +150  | °C   |
| $T_{amb}$     | ambient temperature             | operating device                                            | -40     | +85   | °C   |

[1] Pass level; Human Body Model (HBM) according to [Ref. 6 "JESD22-A114"](#).

[2] Pass level; Machine Model (MM), according to [Ref. 7 "JESD22-A115"](#).

[3] Pass level; latch-up testing according to [Ref. 8 "JESD78"](#) at maximum ambient temperature ( $T_{amb(max)}$ ).

[4] According to the store and transport requirements (see [Ref. 11 "UM10569"](#)) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

## 10. Static characteristics

**Table 17. Static characteristics**

$V_{DD} = 1.8\text{ V to }5.5\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $V_{LCD} = 2.5\text{ V to }6.5\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

| Symbol               | Parameter                            | Conditions                                                                                          | Min                | Typ | Max                | Unit |
|----------------------|--------------------------------------|-----------------------------------------------------------------------------------------------------|--------------------|-----|--------------------|------|
| Supplies             |                                      |                                                                                                     |                    |     |                    |      |
| V <sub>DD</sub>      | supply voltage                       |                                                                                                     | 1.8                | -   | 5.5                | V    |
| V <sub>LCD</sub>     | LCD supply voltage                   | [1]                                                                                                 | 2.5                | -   | 6.5                | V    |
| I <sub>DD</sub>      | supply current                       | f <sub>clk(ext)</sub> = 1536 Hz [2]                                                                 | -                  | 3.5 | 7                  | μA   |
|                      |                                      | V <sub>DD</sub> = 3.0 V;<br>T <sub>amb</sub> = 25 °C                                                | -                  | 2.7 | -                  | μA   |
| I <sub>DD(LCD)</sub> | LCD supply current                   | f <sub>clk(ext)</sub> = 1536 Hz [2]                                                                 | -                  | 18  | 25                 | μA   |
|                      |                                      | V <sub>LCD</sub> = 3.0 V;<br>T <sub>amb</sub> = 25 °C                                               | -                  | 13  | -                  | μA   |
| Logic[3]             |                                      |                                                                                                     |                    |     |                    |      |
| V <sub>P(POR)</sub>  | power-on reset supply voltage        |                                                                                                     | 1.0                | 1.3 | 1.6                | V    |
| V <sub>IL</sub>      | LOW-level input voltage              | on pins CLK, $\overline{\text{SYNC}}$ ,<br>OSC, A0 to A2, SA0,<br>SCL, SDA                          | V <sub>SS</sub>    | -   | 0.3V <sub>DD</sub> | V    |
| V <sub>IH</sub>      | HIGH-level input voltage             | on pins CLK, $\overline{\text{SYNC}}$ ,<br>OSC, A0 to A2, SA0,<br>SCL, SDA [4][5]                   | 0.7V <sub>DD</sub> | -   | V <sub>DD</sub>    | V    |
| I <sub>OL</sub>      | LOW-level output current             | output sink current;<br>V <sub>OL</sub> = 0.4 V; V <sub>DD</sub> = 5 V                              |                    |     |                    |      |
|                      |                                      | on pins CLK and $\overline{\text{SYNC}}$                                                            | 1                  | -   | -                  | mA   |
|                      |                                      | on pin SDA                                                                                          | 3                  | -   | -                  | mA   |
| I <sub>OH(CLK)</sub> | HIGH-level output current on pin CLK | output source current;<br>V <sub>OH</sub> = 4.6 V; V <sub>DD</sub> = 5 V                            | 1                  | -   | -                  | mA   |
| I <sub>L</sub>       | leakage current                      | V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub> ;<br>on pins CLK, SCL, SDA,<br>A0 to A2 and SA0 | −1                 | -   | +1                 | μA   |
| I <sub>L(OSC)</sub>  | leakage current on pin OSC           | V <sub>I</sub> = V <sub>DD</sub>                                                                    | −1                 | -   | +1                 | μA   |
| C <sub>I</sub>       | input capacitance                    | [6]                                                                                                 | -                  | -   | 7                  | pF   |
| LCD outputs          |                                      |                                                                                                     |                    |     |                    |      |
| ΔV <sub>O</sub>      | output voltage variation             | on pins BP0 to BP3 and<br>S0 to S39                                                                 | −100               | -   | +100               | mV   |
| R <sub>O</sub>       | output resistance                    | V <sub>LCD</sub> = 5 V [7]                                                                          |                    |     |                    |      |
|                      |                                      | on pins BP0 to BP3                                                                                  | -                  | 1.5 | -                  | kΩ   |
|                      |                                      | on pins S0 to S39                                                                                   | -                  | 6.0 | -                  | kΩ   |

[1]  $V_{LCD} > 3\text{ V}$  for  $\frac{1}{3}$  bias.

[2] LCD outputs are open-circuit; inputs at  $V_{SS}$  or  $V_{DD}$ ; external clock with 50 % duty factor; I<sup>2</sup>C-bus inactive.

[3] The I<sup>2</sup>C-bus interface of PCA8576D is 5 V tolerant.

[4] When tested, I<sup>2</sup>C pins SCL and SDA have no diode to  $V_{DD}$  and may be driven to the  $V_I$  limiting values given in Table 16.

[5] Propagation delay of driver between clock (CLK) and LCD driving signals.

[6] Periodically sampled, not 100 % tested.

[7] Outputs measured one at a time.

## 11. Dynamic characteristics

**Table 18. Dynamic characteristics**

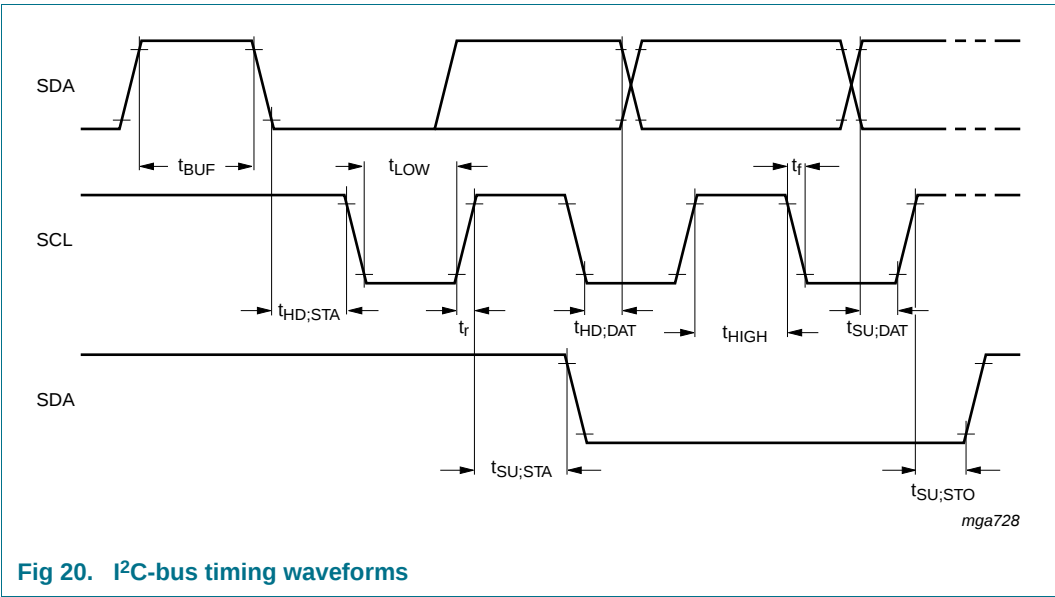
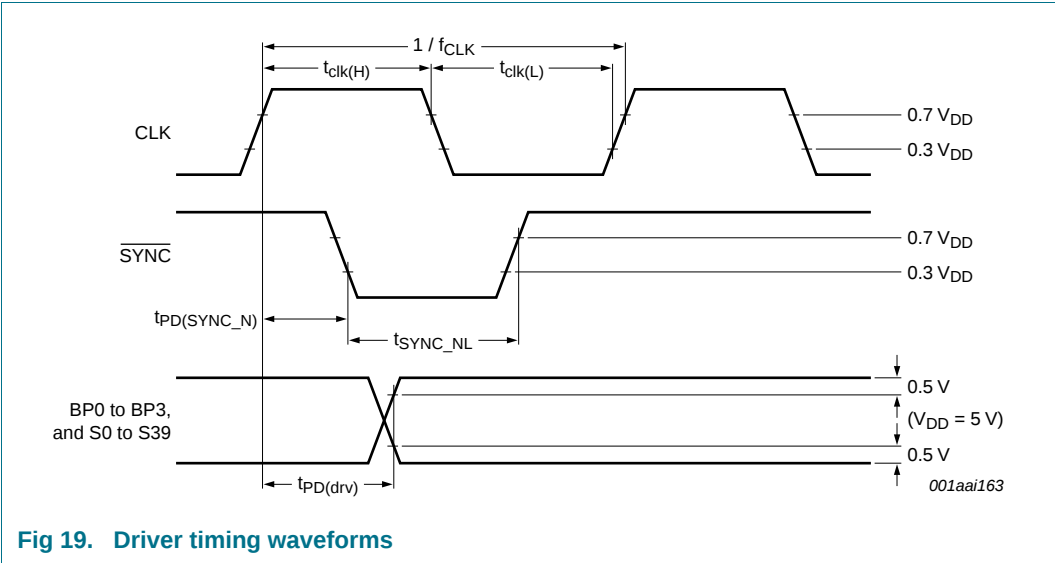
$V_{DD} = 1.8\text{ V to }5.5\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $V_{LCD} = 2.5\text{ V to }6.5\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

| Symbol                       | Parameter                                        | Conditions                  | Min  | Typ  | Max  | Unit          |
|------------------------------|--------------------------------------------------|-----------------------------|------|------|------|---------------|
| <b>Clock</b>                 |                                                  |                             |      |      |      |               |
| $f_{clk(int)}$               | internal clock frequency                         | [1]                         | 1440 | 1850 | 2640 | Hz            |
| $f_{clk(ext)}$               | external clock frequency                         |                             | 960  | -    | 2640 | Hz            |
| $t_{clk(H)}$                 | HIGH-level clock time                            |                             | 60   | -    | -    | $\mu\text{s}$ |
| $t_{clk(L)}$                 | LOW-level clock time                             |                             | 60   | -    | -    | $\mu\text{s}$ |
| <b>Synchronization</b>       |                                                  |                             |      |      |      |               |
| $t_{PD(SYNC\_N)}$            | $\overline{\text{SYNC}}$ propagation delay       |                             | -    | 30   | -    | ns            |
| $t_{SYNC\_NL}$               | $\overline{\text{SYNC}}$ LOW time                |                             | 1    | -    | -    | $\mu\text{s}$ |
| $t_{PD(drv)}$                | driver propagation delay                         | $V_{LCD} = 5\text{ V}$ [2]  | -    | -    | 30   | $\mu\text{s}$ |
| <b>I<sup>2</sup>C-bus[3]</b> |                                                  |                             |      |      |      |               |
| <b>Pin SCL</b>               |                                                  |                             |      |      |      |               |
| $f_{SCL}$                    | SCL clock frequency                              |                             | -    | -    | 400  | kHz           |
| $t_{LOW}$                    | LOW period of the SCL clock                      |                             | 1.3  | -    | -    | $\mu\text{s}$ |
| $t_{HIGH}$                   | HIGH period of the SCL clock                     |                             | 0.6  | -    | -    | $\mu\text{s}$ |
| <b>Pin SDA</b>               |                                                  |                             |      |      |      |               |
| $t_{SU,DAT}$                 | data set-up time                                 |                             | 100  | -    | -    | ns            |
| $t_{HD,DAT}$                 | data hold time                                   |                             | 0    | -    | -    | ns            |
| <b>Pins SCL and SDA</b>      |                                                  |                             |      |      |      |               |
| $t_{BUF}$                    | bus free time between a STOP and START condition |                             | 1.3  | -    | -    | $\mu\text{s}$ |
| $t_{SU,STO}$                 | set-up time for STOP condition                   |                             | 0.6  | -    | -    | $\mu\text{s}$ |
| $t_{HD,STA}$                 | hold time (repeated) START condition             |                             | 0.6  | -    | -    | $\mu\text{s}$ |
| $t_{SU,STA}$                 | set-up time for a repeated START condition       |                             | 0.6  | -    | -    | $\mu\text{s}$ |
| $t_r$                        | rise time of both SDA and SCL signals            | $f_{SCL} = 400\text{ kHz}$  | -    | -    | 0.3  | $\mu\text{s}$ |
|                              |                                                  | $f_{SCL} < 125\text{ kHz}$  | -    | -    | 1.0  | $\mu\text{s}$ |
| $t_f$                        | fall time of both SDA and SCL signals            |                             | -    | -    | 0.3  | $\mu\text{s}$ |
| $C_b$                        | capacitive load for each bus line                |                             | -    | -    | 400  | pF            |
| $t_{w(spike)}$               | spike pulse width                                | on the I <sup>2</sup> C-bus | -    | -    | 50   | ns            |

[1] Typical output duty factor: 50 % measured at the CLK output pin.

[2] Not tested in production.

[3] All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to  $V_{IL}$  and  $V_{IH}$  with an input voltage swing of  $V_{SS}$  to  $V_{DD}$ .



## 12. Application information

### 12.1 Cascaded operation

In large display configurations, up to 16 PCA8576D can be differentiated on the same I<sup>2</sup>C-bus by using the 3-bit hardware subaddresses (A0, A1 and A2) and the programmable I<sup>2</sup>C-bus slave address (SA0).

**Table 19. Addressing cascaded PCA8576D**

| Cluster | Bit SA0 | Pin A2 | Pin A1 | Pin A0 | Device |
|---------|---------|--------|--------|--------|--------|
| 1       | 0       | 0      | 0      | 0      | 0      |
|         |         | 0      | 0      | 1      | 1      |
|         |         | 0      | 1      | 0      | 2      |
|         |         | 0      | 1      | 1      | 3      |
|         |         | 1      | 0      | 0      | 4      |
|         |         | 1      | 0      | 1      | 5      |
|         |         | 1      | 1      | 0      | 6      |
|         |         | 1      | 1      | 1      | 7      |
| 2       | 1       | 0      | 0      | 0      | 8      |
|         |         | 0      | 0      | 1      | 9      |
|         |         | 0      | 1      | 0      | 10     |
|         |         | 0      | 1      | 1      | 11     |
|         |         | 1      | 0      | 0      | 12     |
|         |         | 1      | 0      | 1      | 13     |
|         |         | 1      | 1      | 0      | 14     |
|         |         | 1      | 1      | 1      | 15     |

The PCA8576D connected in cascade are synchronized to allow the backplane signals from only one device in the cascade to be shared. This arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other cascaded PCA8576D contribute additional segment outputs but their backplane outputs are left open-circuit (see [Figure 21](#)).

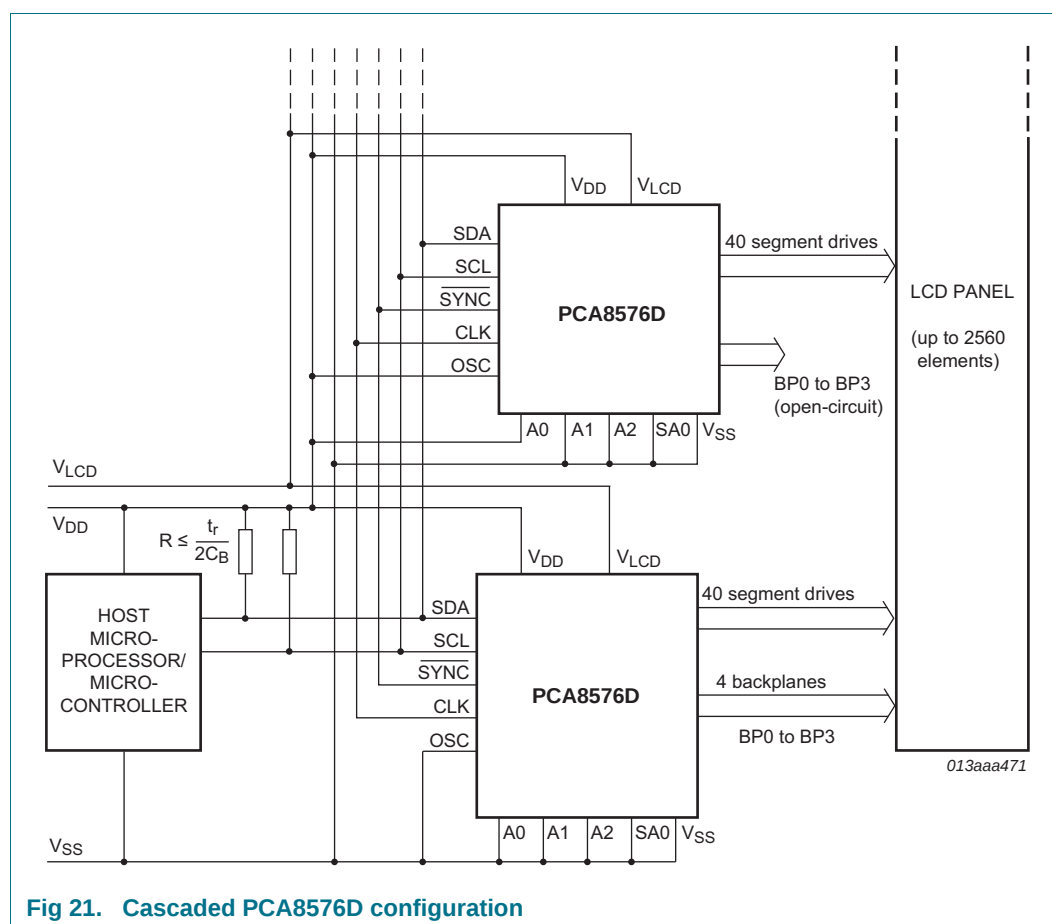
All PCA8576D connected in cascade are correctly synchronized by the  $\overline{\text{SYNC}}$  signal. This synchronization is guaranteed after the power-on reset. The only time that  $\overline{\text{SYNC}}$  is likely to be needed is if synchronization is lost accidentally, for example, by noise in adverse electrical environments, or if the LCD multiplex drive mode is changed in an application using several cascaded PCA8576D, as the drive mode cannot be changed on all of the cascaded devices simultaneously.  $\overline{\text{SYNC}}$  can be either an input or an output signal; a  $\overline{\text{SYNC}}$  output is implemented as an open-drain driver with an internal pull-up resistor. The PCA8576D asserts  $\overline{\text{SYNC}}$  at the start of its last active backplane signal and monitors the  $\overline{\text{SYNC}}$  line at all other times. If cascade synchronization is lost, it is restored by the first PCA8576D to assert  $\overline{\text{SYNC}}$ . The timing relationship between the backplane waveforms and the  $\overline{\text{SYNC}}$  signal for each LCD drive mode is shown in [Figure 22](#).

The contact resistance between the  $\overline{\text{SYNC}}$  on each cascaded device must be controlled. If the resistance is too high, the device is not able to synchronize properly; this is particularly applicable to chip-on-glass applications. The maximum  $\overline{\text{SYNC}}$  contact resistance allowed for the number of devices in cascade is given in [Table 20](#).

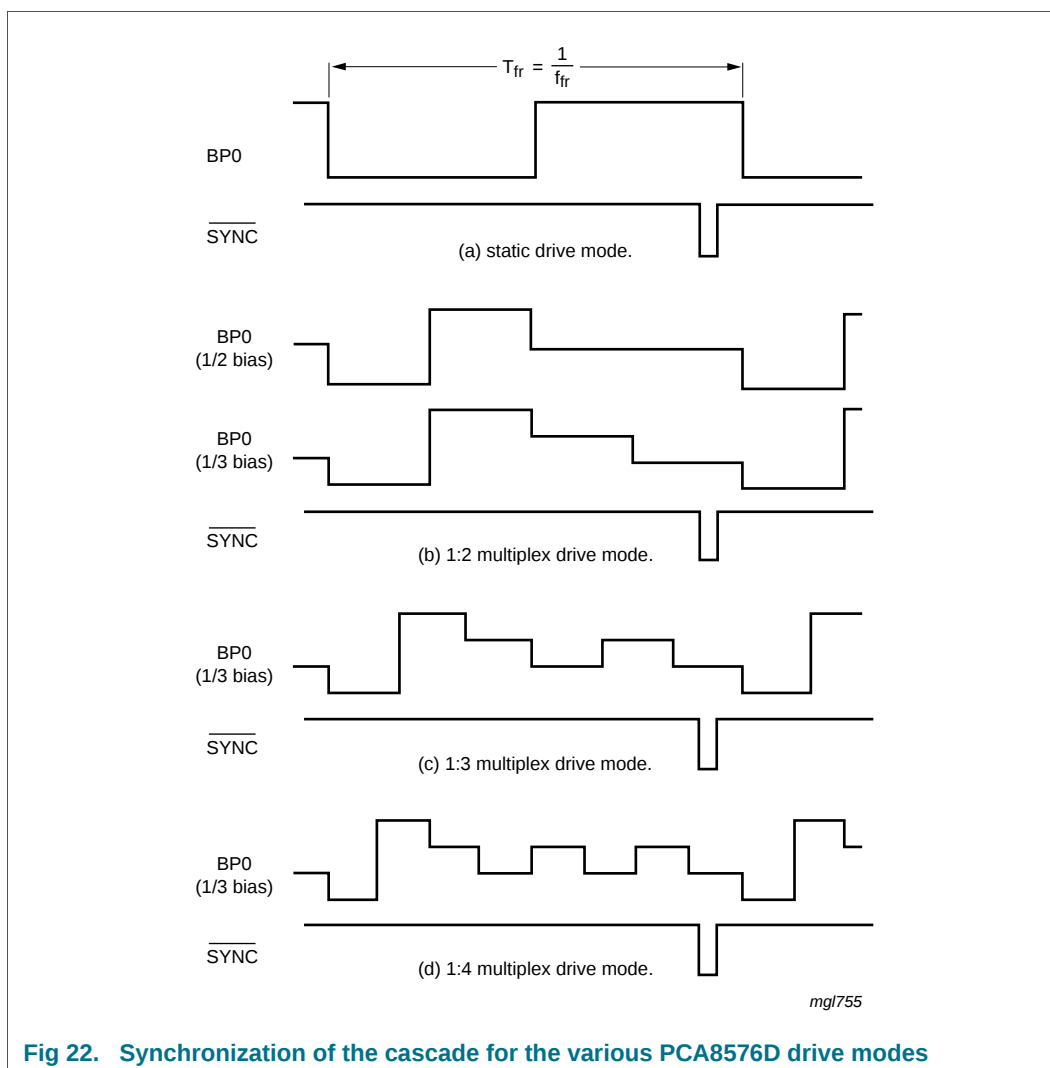
**Table 20.**  $\overline{\text{SYNC}}$  contact resistance

| Number of devices | Maximum contact resistance |
|-------------------|----------------------------|
| 2                 | 6 k $\Omega$               |
| 3 to 5            | 2.2 k $\Omega$             |
| 6 to 10           | 1.2 k $\Omega$             |
| 10 to 16          | 700 $\Omega$               |

The PCA8576D can be cascaded with the PCA8534A. This allows optimal drive selection for a given number of pixels to display. [Figure 19](#) and [Figure 20](#) show the timing of the synchronization signals.



**Fig 21.** Cascaded PCA8576D configuration



## 12.2 RAM writing in 1:3 multiplex drive mode

In 1:3 multiplex drive mode, the RAM is written as shown in [Table 21](#) (see [Figure 11](#) as well).

**Table 21. Standard RAM filling in 1:3 multiplex drive mode**

Assumption: BP2/S2, BP2/S5, BP2/S8 etc. are not connected to any elements on the display.

| Display RAM bits (rows)/backplane outputs (BPn) | Display RAM addresses (columns)/segment outputs (Sn) |    |    |    |    |    |    |    |    |    |   |
|-------------------------------------------------|------------------------------------------------------|----|----|----|----|----|----|----|----|----|---|
|                                                 | 0                                                    | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | : |
| 0                                               | a7                                                   | a4 | a1 | b7 | b4 | b1 | c7 | c4 | c1 | d7 | : |
| 1                                               | a6                                                   | a3 | a0 | b6 | b3 | b0 | c6 | c3 | c0 | d6 | : |
| 2                                               | a5                                                   | a2 | -  | b5 | b2 | -  | c5 | c2 | -  | d5 | : |
| 3                                               | -                                                    | -  | -  | -  | -  | -  | -  | -  | -  | -  | : |

If the bit at position BP2/S2 would be written by a second byte transmitted, then the mapping of the segment bits would change as illustrated in [Table 22](#).

**Table 22. Continuous RAM filling by rewriting in 1:3 multiplex drive mode**

Assumption: BP2/S2, BP2/S5, BP2/S8 etc. are connected to elements on the display.

| Display RAM bits (rows)/backplane outputs (BPn) | Display RAM addresses (columns)/segment outputs (Sn) |    |       |    |       |    |       |    |       |    |   |
|-------------------------------------------------|------------------------------------------------------|----|-------|----|-------|----|-------|----|-------|----|---|
|                                                 | 0                                                    | 1  | 2     | 3  | 4     | 5  | 6     | 7  | 8     | 9  | : |
| 0                                               | a7                                                   | a4 | a1/b7 | b4 | b1/c7 | c4 | c1/d7 | d4 | d1/e7 | e4 | : |
| 1                                               | a6                                                   | a3 | a0/b6 | b3 | b0/c6 | c3 | c0/d6 | d3 | d0/e6 | e3 | : |
| 2                                               | a5                                                   | a2 | b5    | b2 | c5    | c2 | d5    | d2 | e5    | e2 | : |
| 3                                               | -                                                    | -  | -     | -  | -     | -  | -     | -  | -     | -  | : |

In the case described in [Table 22](#) the RAM has to be written entirely and BP2/S2, BP2/S5, BP2/S8 etc. have to be connected to elements on the display. This can be achieved by a combination of writing and rewriting the RAM like follows:

- In the first write to the RAM, bits a7 to a0 are written.
- In the second write, bits b7 to b0 are written, overwriting bits a1 and a0 with bits b7 and b6.
- In the third write, bits c7 to c0 are written, overwriting bits b1 and b0 with bits c7 and c6.

Depending on the method of writing to the RAM (standard or continuous filling by rewriting), some elements remain unused or can be used, but it has to be considered in the module layout process as well as in the driver software design.

## 13. Test information

### 13.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

14. Bare die outline

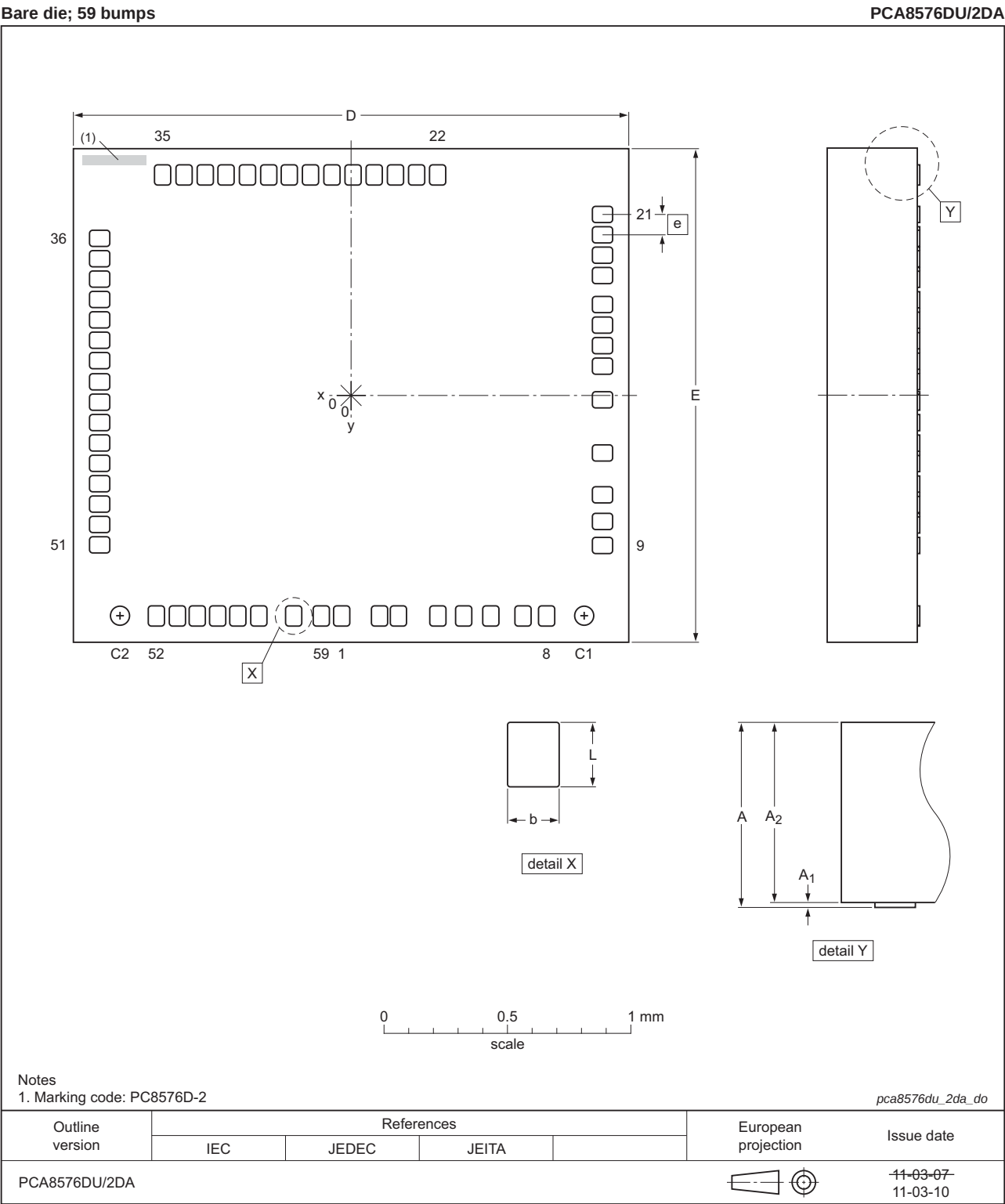


Fig 23. Bare die outline PCA8576DU/2DA/2 (for dimensions see Table 23)

**Table 23. Dimensions of PCA8576DU**

Original dimensions are in mm.

| Unit (mm) | A    | A <sub>1</sub> | A <sub>2</sub> | b     | D   | E   | e <sup>[1]</sup> | L     |
|-----------|------|----------------|----------------|-------|-----|-----|------------------|-------|
| max       | -    | -              | -              | -     | -   | -   | -                | -     |
| nom       | 0.40 | 0.015          | 0.381          | 0.052 | 2.2 | 2.0 | -                | 0.077 |
| min       | -    | -              | -              | -     | -   | -   | 0.072            | -     |

[1] Dimension not drawn to scale.

**Table 24. Bump location for PCA8576DU**All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip (see [Figure 2](#) and [Figure 23](#)).

| Symbol           | Bump | X (μm)  | Y (μm) | Description                                   |
|------------------|------|---------|--------|-----------------------------------------------|
| SDA              | 1    | -34.38  | -876.6 | I <sup>2</sup> C-bus serial data input/output |
| SCL              | 2    | 109.53  | -876.6 | I <sup>2</sup> C-bus serial clock input       |
| SCL              | 3    | 181.53  | -876.6 |                                               |
| SYNC             | 4    | 365.58  | -876.6 | cascade synchronization input/output          |
| CLK              | 5    | 469.08  | -876.6 | external clock input/output                   |
| V <sub>DD</sub>  | 6    | 577.08  | -876.6 | supply voltage                                |
| OSC              | 7    | 740.88  | -876.6 | internal oscillator enable input              |
| A0               | 8    | 835.83  | -876.6 | subaddress inputs                             |
| A1               | 9    | 1005.48 | -630.9 |                                               |
| A2               | 10   | 1005.48 | -513.9 |                                               |
| SA0              | 11   | 1005.48 | -396.9 | I <sup>2</sup> C-bus address input; bit 0     |
| V <sub>SS</sub>  | 12   | 1005.48 | -221.4 | ground supply voltage                         |
| V <sub>LCD</sub> | 13   | 1005.48 | 10.71  | LCD supply voltage                            |
| BP0              | 14   | 1005.48 | 156.51 | LCD backplane outputs                         |
| BP2              | 15   | 1005.48 | 232.74 |                                               |
| BP1              | 16   | 1005.48 | 308.97 |                                               |
| BP3              | 17   | 1005.48 | 385.2  |                                               |
| S0               | 18   | 1005.48 | 493.2  | LCD segment outputs                           |
| S1               | 19   | 1005.48 | 565.2  |                                               |
| S2               | 20   | 1005.48 | 637.2  |                                               |
| S3               | 21   | 1005.48 | 709.2  |                                               |
| S4               | 22   | 347.22  | 876.6  | LCD segment outputs                           |
| S5               | 23   | 263.97  | 876.6  |                                               |
| S6               | 24   | 180.72  | 876.6  |                                               |
| S7               | 25   | 97.47   | 876.6  |                                               |
| S8               | 26   | 14.22   | 876.6  |                                               |
| S9               | 27   | -69.03  | 876.6  |                                               |
| S10              | 28   | -152.28 | 876.6  |                                               |
| S11              | 29   | -235.53 | 876.6  |                                               |
| S12              | 30   | -318.78 | 876.6  |                                               |

**Table 24. Bump location for PCA8576DU ...continued**

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip (see [Figure 2](#) and [Figure 23](#)).

| Symbol | Bump | X (μm)  | Y (μm) | Description                                   |
|--------|------|---------|--------|-----------------------------------------------|
| S13    | 31   | -402.03 | 876.6  |                                               |
| S14    | 32   | -485.28 | 876.6  |                                               |
| S15    | 33   | -568.53 | 876.6  |                                               |
| S16    | 34   | -651.78 | 876.6  |                                               |
| S17    | 35   | -735.03 | 876.6  |                                               |
| S18    | 36   | -1005.5 | 625.59 |                                               |
| S19    | 37   | -1005.5 | 541.62 |                                               |
| S20    | 38   | -1005.5 | 458.19 |                                               |
| S21    | 39   | -1005.5 | 374.76 |                                               |
| S22    | 40   | -1005.5 | 291.33 |                                               |
| S23    | 41   | -1005.5 | 207.9  |                                               |
| S24    | 42   | -1005.5 | 124.47 |                                               |
| S25    | 43   | -1005.5 | 41.04  |                                               |
| S26    | 44   | -1005.5 | -42.39 |                                               |
| S27    | 45   | -1005.5 | -125.8 |                                               |
| S28    | 46   | -1005.5 | -209.3 |                                               |
| S29    | 47   | -1005.5 | -292.7 |                                               |
| S30    | 48   | -1005.5 | -376.1 |                                               |
| S31    | 49   | -1005.5 | -459.5 |                                               |
| S32    | 50   | -1005.5 | -543   |                                               |
| S33    | 51   | -1005.5 | -625.6 |                                               |
| S34    | 52   | -735.03 | -876.6 |                                               |
| S35    | 53   | -663.03 | -876.6 |                                               |
| S36    | 54   | -591.03 | -876.6 |                                               |
| S37    | 55   | -519.03 | -876.6 |                                               |
| S38    | 56   | -447.03 | -876.6 |                                               |
| S39    | 57   | -375.03 | -876.6 | LCD segment outputs                           |
| SDA    | 58   | -196.38 | -876.6 | I <sup>2</sup> C-bus serial data input/output |
| SDA    | 59   | -106.38 | -876.6 |                                               |

**Table 25. Alignment marks**

All x/y coordinates represent the position of the center of each alignment mark with respect to the center (x/y = 0) of the chip (see [Figure 2](#) and [Figure 23](#)).

| Symbol | X (μm)  | Y (μm) |
|--------|---------|--------|
| C1     | 930.42  | -870.3 |
| C2     | -829.98 | -870.3 |

## 15. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

## 16. Packing information

### 16.1 Tray information

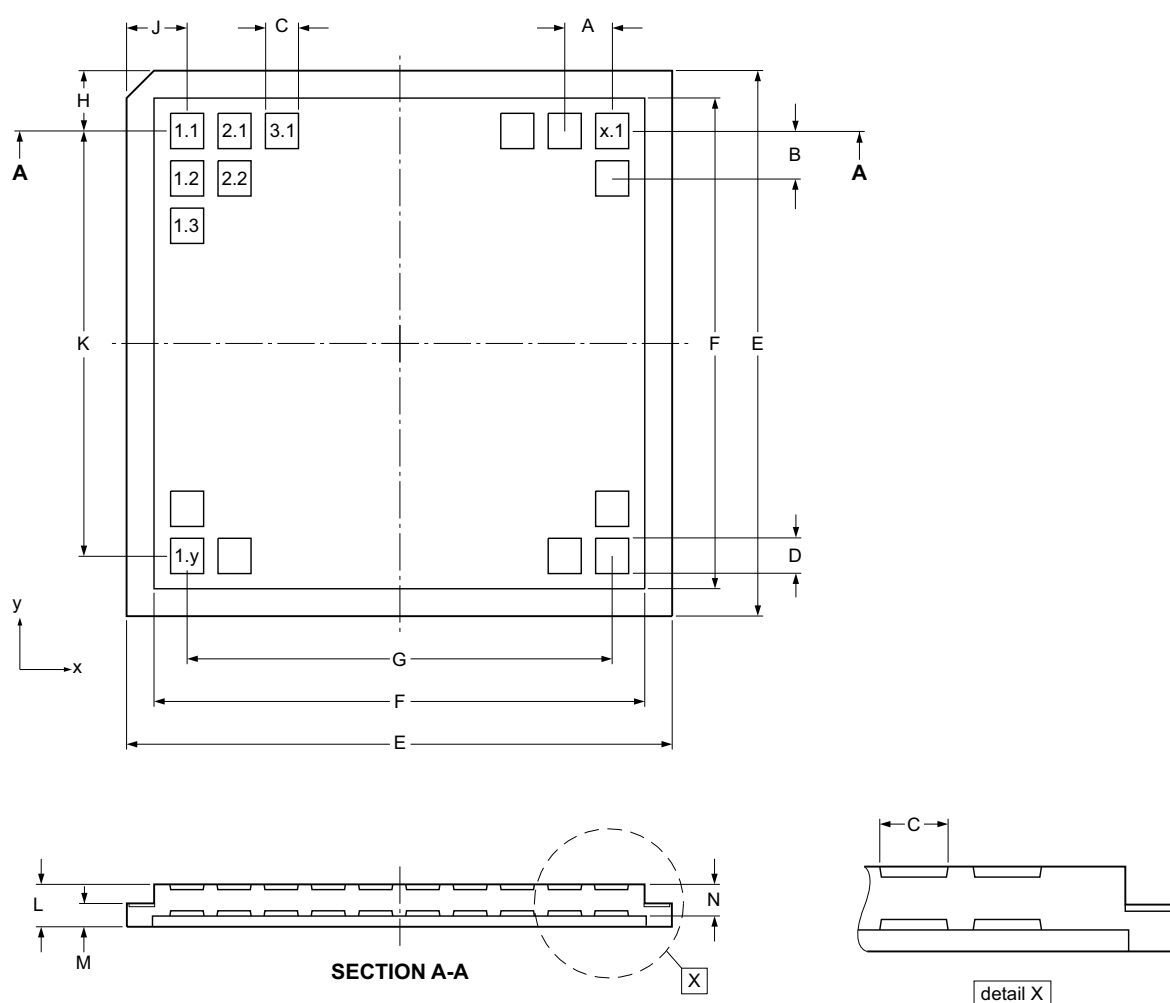
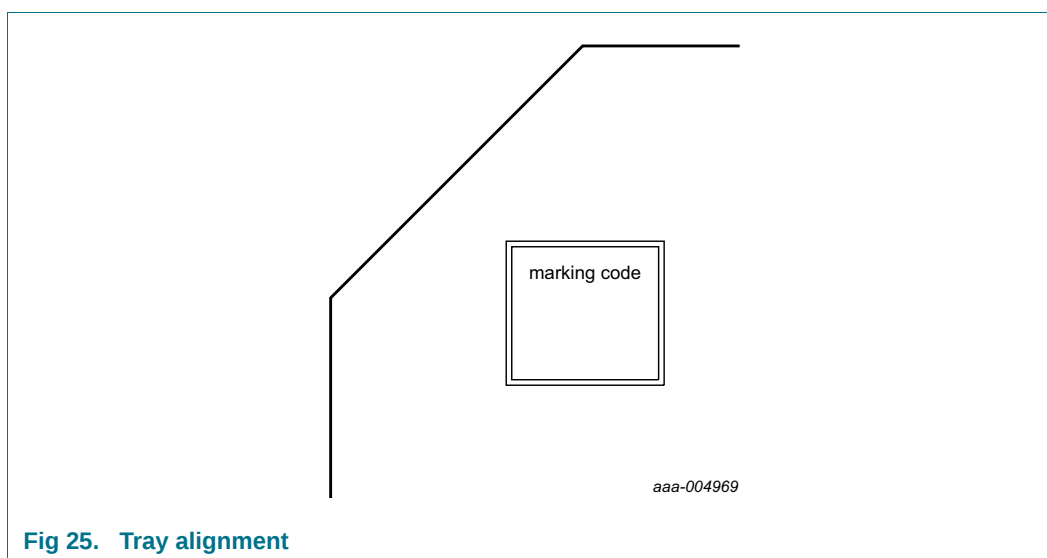


Fig 24. Tray details

**Table 26. Description of tray details**Tray details are shown in [Figure 24](#).

| Tray details      |     |      |      |      |       |      |     |             |      |      |      |      |      |
|-------------------|-----|------|------|------|-------|------|-----|-------------|------|------|------|------|------|
| Dimensions        |     |      |      |      |       |      |     |             |      |      |      |      |      |
| A                 | B   | C    | D    | E    | F     | G    | H   | J           | K    | L    | M    | N    | Unit |
| 3.6               | 3.6 | 2.36 | 2.11 | 50.8 | 45.72 | 39.6 | 5.6 | 5.6         | 39.6 | 3.96 | 2.18 | 2.49 | mm   |
| Number of pockets |     |      |      |      |       |      |     |             |      |      |      |      |      |
| x direction       |     |      |      |      |       |      |     | y direction |      |      |      |      |      |
| 12                |     |      |      |      |       |      |     | 12          |      |      |      |      |      |

**Fig 25. Tray alignment**

## 17. Abbreviations

**Table 27. Abbreviations**

| Acronym | Description                             |
|---------|-----------------------------------------|
| CMOS    | Complementary Metal-Oxide Semiconductor |
| HBM     | Human Body Model                        |
| ITO     | Indium Tin Oxide                        |
| LCD     | Liquid Crystal Display                  |
| LSB     | Least Significant Bit                   |
| MM      | Machine Model                           |
| MSB     | Most Significant Bit                    |
| PCB     | Printed Circuit Board                   |
| RAM     | Random Access Memory                    |
| RMS     | Root Mean Square                        |
| SCL     | Serial CLock line                       |
| SDA     | Serial DATa line                        |

## 18. References

- [1] **AN10170** — Design guidelines for COG modules with NXP monochrome LCD drivers
- [2] **AN10706** — Handling bare die
- [3] **IEC 60134** — Rating systems for electronic tubes and valves and analogous semiconductor devices
- [4] **IEC 61340-5** — Protection of electronic devices from electrostatic phenomena
- [5] **IPC/JEDEC J-STD-020D** — Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
- [6] **JESD22-A114** — Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
- [7] **JESD22-A115** — Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)
- [8] **JESD78** — IC Latch-Up Test
- [9] **JESD625-A** — Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices
- [10] **UM10204** — I<sup>2</sup>C-bus specification and user manual
- [11] **UM10569** — Store and transport requirements

## 19. Revision history

**Table 28. Revision history**

| Document ID    | Release date                                                                                                                                                                                                                                      | Data sheet status  | Change notice | Supersedes   |
|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|---------------|--------------|
| PCA8576D v.2   | 20130606                                                                                                                                                                                                                                          | Product data sheet | -             | PCA8576D v.1 |
| Modifications: | <ul style="list-style-type: none"> <li>Added improved I<sub>DD</sub> and I<sub>DD(LCD)</sub> values (<a href="#">Table 17</a>)</li> <li>Improved description of bit E</li> <li>Changed tray information (<a href="#">Section 16.1</a>)</li> </ul> |                    |               |              |
| PCA8576D v.1   | 20110404                                                                                                                                                                                                                                          | Product data sheet | -             | -            |

## 20. Legal information

### 20.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition                                                                            |
|-----------------------------------|-------------------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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