PRELIMINARY PRODUCT INFORMATION

MOS INTEGRATED CIRCUIT

μPD789462, 789464, 789466, 789467

8-BIT SINGLE-CHIP MICROCONTROLLER

The μPD789462, 789464, 789466, and 789467 are μPD789467 Subseries (designed for remote controller with on-chip LCD) products in the 78K/0S Series.

In addition to an 8-bit CPU, the μPD789462, 789464, 789466, and 789467 incorporate a variety of hardware supporting an on-chip LCD remote controller, such as an LCD controller/driver, A/D converter, key return signal detector, and a timer with a carrier generator enabling output of waveforms for infrared remote control.

A flash memory version, the μPD78F9468, which can operate in the same voltage range as the mask ROM versions, and various development tools are also under development.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD789327, 789467 Subseries User's Manual: To be prepared
78K/0S Series User's Manual Instructions: U11047E

FEATURES

- ROM and RAM capacities

Item / Part Number	Program Memory (ROM)	Data Memory		Package
		Internal High-Speed RAM	LCD Display RAM	
μPD789462	4 KB	256 bytes	23 bytes	52-pin plastic LQFP (10 × 10)
μPD789464	8 KB			
μPD789466	16 KB	512 bytes		
μPD789467	24 KB			

- Variable minimum instruction execution time: High speed (0.4 μs: @5.0 MHz operation with main system clock), low speed (1.6 μs: @5.0 MHz operation with main system clock), and ultra low speed (122 μs: @32.768 kHz operation with subsystem clock)
- I/O ports: 18
- 8-bit resolution A/D converter: 1 channel
- LCD controller/driver (On-chip voltage amplifier)
  Segment signals: 23
  Common signals: 4
- Timer: 4 channels
- On-chip power-on clear circuit (POC) (mask option)
- Supply voltage: V_{DD} = 1.8 to 5.5 V

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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APPLICATIONS

Remote-control devices, healthcare equipment, etc.

ORDERING INFORMATION

Part Number	Package
μPD789462GB-×××-8ET	52-pin plastic LQFP (10 × 10)
μPD789464GB-×××-8ET	52-pin plastic LQFP (10 × 10)
μPD789466GB-×××-8ET	52-pin plastic LQFP (10 × 10)
μPD789467GB-×××-8ET	52-pin plastic LQFP (10 × 10)

Remark ××× indicates ROM code suffix.

78K/0S SERIES LINEUP

The products in the 78K/0S Series are listed below. The names enclosed in boxes are subseries names.

Products in mass production

Products under development

Y subseries products support SMB.

78K/0S Series

Small-scale package, general-purpose applications

44-pin	μPD789046	μPD789026 with internal subsystem clock
42/44-pin	μPD789026	μPD789014 with enhanced timer and expanded ROM, RAM
28-pin	μPD789014	On-chip UART. Capable of low-voltage (1.8 V) operation

Small-scale package, general-purpose applications + A/D

44-pin	μPD789177	PD789177Y	μPD789167 with enhanced A/D converter
44-pin	μPD789167	PD789167Y	μPD789104A with enhanced timer
30-pin	μPD789156		μPD789146 with enhanced A/D converter
30-pin	μPD789146		μPD789104A with EEPROM
30-pin	μPD789134A		μPD789124A with enhanced A/D converter
30-pin	μPD789124A		RC oscillation version of the μPD789104A
30-pin	μPD789114A		μPD789104A with enhanced A/D converter
30-pin	μPD789104A		μPD789026 with added A/D and multiplier

Inverter control

44-pin	μPD789842	On-chip inverter controller and UART

LCD drive

80-pin	μPD789417A	μPD789407A with enhanced A/D converter
80-pin	μPD789407A	μPD789456 with enhanced I/O
64-pin	μPD789456	μPD789446 with enhanced A/D converter
64-pin	μPD789446	RC oscillation version of the μPD789426
64-pin	μPD789436	μPD789426 with enhanced A/D converter
64-pin	μPD789426	μPD789306 with A/D converter
64-pin	μPD789316	RC oscillation version of the μPD789306
64-pin	μPD789306	Basic subseries for LCD drive

Dot LCD drive

144-pin	μPD789835	Segment/common outputs: 96
88-pin	μPD789830	Segment: 40, common: 16

ASSP

52-pin	μPD789467	μPD789327 with A/D converter
52 -pin	μPD789327	For remote-controller. On-chip LCD controller/driver.
44-pin	μPD789800	For PC keyboard, on-chip USB function
44-pin	μPD789840	For key pad, on-chip POC
20-pin	μPD789861	RC oscillation version of the μPD789860
20-pin	μPD789860	For keyless entry, on-chip POC and key return circuit

The major functional differences among the subseries are listed below.

Subseries Name \ Function		ROM Capacity	Timer				8-Bit A/D	10-Bit A/D	Serial Interface	I/O	V_{DD} Min. Value	Remarks
			8-Bit	16-Bit	Watch	WDT						
Small-scale package, general-purpose applications	μPD789046	16 K	1 ch	1 ch	1 ch	1 ch	–	–	1 ch (UART: 1 ch)	34	1.8 V	–
	μPD789026	4 K to 16 K			–							
	μPD789014	2 K to 4 K	2 ch	–						22		
Small-scale package, general-purpose applications + A/D	μPD789177	16 K to 24 K	3 ch	1 ch	1 ch		–	8 ch	1 ch (UART: 1 ch)	31		–
	μPD789167						8 ch	–				
	μPD789156	8 K to 16 K	1 ch		–		–	4 ch		20		On-chip EEPROM
	μPD789146						4 ch	–				
	μPD789134A	2 K to 8 K					–	4 ch				RC oscillation version
	μPD789124A						4 ch	–				
	μPD789114A						–	4 ch				–
	μPD789104A						4 ch	–				
Inverter control	μPD789842	8 K to 16 K	3 ch	**Note**	1 ch	1 ch	8 ch	–	1 ch (UART: 1 ch)	30	4.0 V	–
LCD drive	μPD789417A	12 K to 24 K	3 ch	1 ch	1 ch	1 ch	–	7 ch	1 ch (UART: 1 ch)	43	1.8 V	–
	μPD789407A						7 ch	–				
	μPD789456	12 K to 16 K	2 ch				–	6 ch		30		
	μPD789446						6 ch	–				
	μPD789436						–	6 ch		40		
	μPD789426						6 ch	–				
	μPD789316	8 K to 16 K					–		2 ch (UART: 1 ch)	23		RC oscillation version
	μPD789306											–
Dot LCD drive	μPD789835	24 K to 60 K	6 ch	–	1 ch	1 ch	3 ch	–	1 ch (UART: 1 ch)	28	1.8 V	–
	μPD789830	24 K	1 ch	1 ch			–			30	2.7 V	
ASSP	μPD789467	4 K to 24 K	2 ch	–	1 ch	1 ch	1 ch	–	–	18	1.8 V	On-chip LCD
	μPD789327						–		1 ch	21		
	μPD789800	8 K			–		–		2 ch (USB: 1 ch)	31	4.0 V	–
	μPD789840						4 ch		1 ch	29	2.8 V	
	μPD789861	4 K					–		–	14	1.8 V	RC oscillation version, on-chip EEPROM
	μPD789860											On-chip EEPROM

Note 10-bit timer: 1 channel

OVERVIEW OF FUNCTIONS

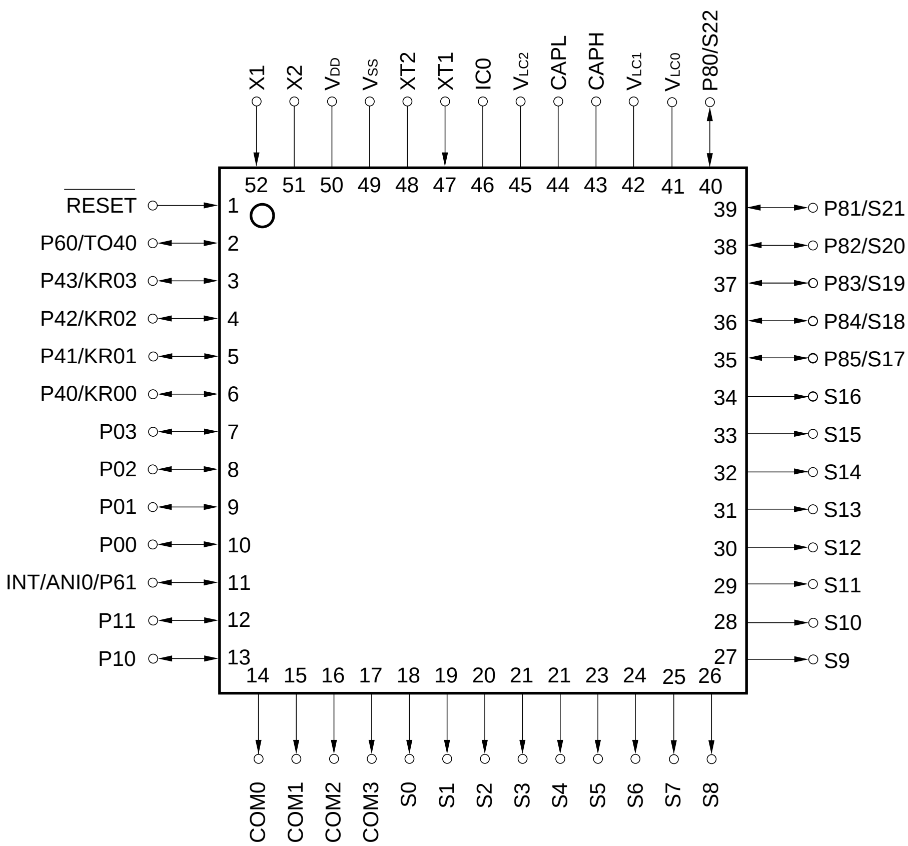
Item		μPD789462	μPD789464	μPD789466	μPD789467
Internal memory	ROM	4 KB	8 KB	16 KB	24 KB
	High-speed RAM	256 bytes		512 bytes	
	LCD display RAM	23 bytes			
Main system clock (oscillation frequency)		Ceramic/crystal oscillation (1.0 to 5.0 MHz)			
Subsystem clock (oscillation frequency)		Crystal oscillation (32.768 kHz)			
Minimum instruction execution time		0.4 μs/1.6 μs (@5.0 MHz operation with main system clock)			
		122 μs (@32.768 kHz operation with subsystem clock)			
General-purpose registers		8 bits × 8 registers			
Instruction set		• 16-bit operations • Bit manipulation (set, reset, test) etc.			
I/O ports		Total: 18 (including pins shared with LCD) CMOS I/O: 12 CMOS input: 6			
Timers		• 8-bit timer: 2 channels • Watch timer: 1 channel • Watchdog timer: 1 channel			
Timer outputs		1			
A/D converter		8-bit resolution × 1 channel			
LCD controller/driver		• Segment signal outputs: 23 • Common signal outputs: 4			
Vectored interrupt sources	Maskable	Internal: 6, External: 2			
	Non-maskable	Internal: 1			
Reset		• Reset by $\overline{\text{RESET}}$ signal input • Internal reset by watchdog timer • Reset via power-on-clear circuit			
Supply voltage		V_{DD} = 1.8 to 5.5 V			
Operating ambient temperature		T_A = –40 to +85°C			
Package		52-pin plastic LQFP (10 × 10)			

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

52-pin plastic LQFP (10 × 10)

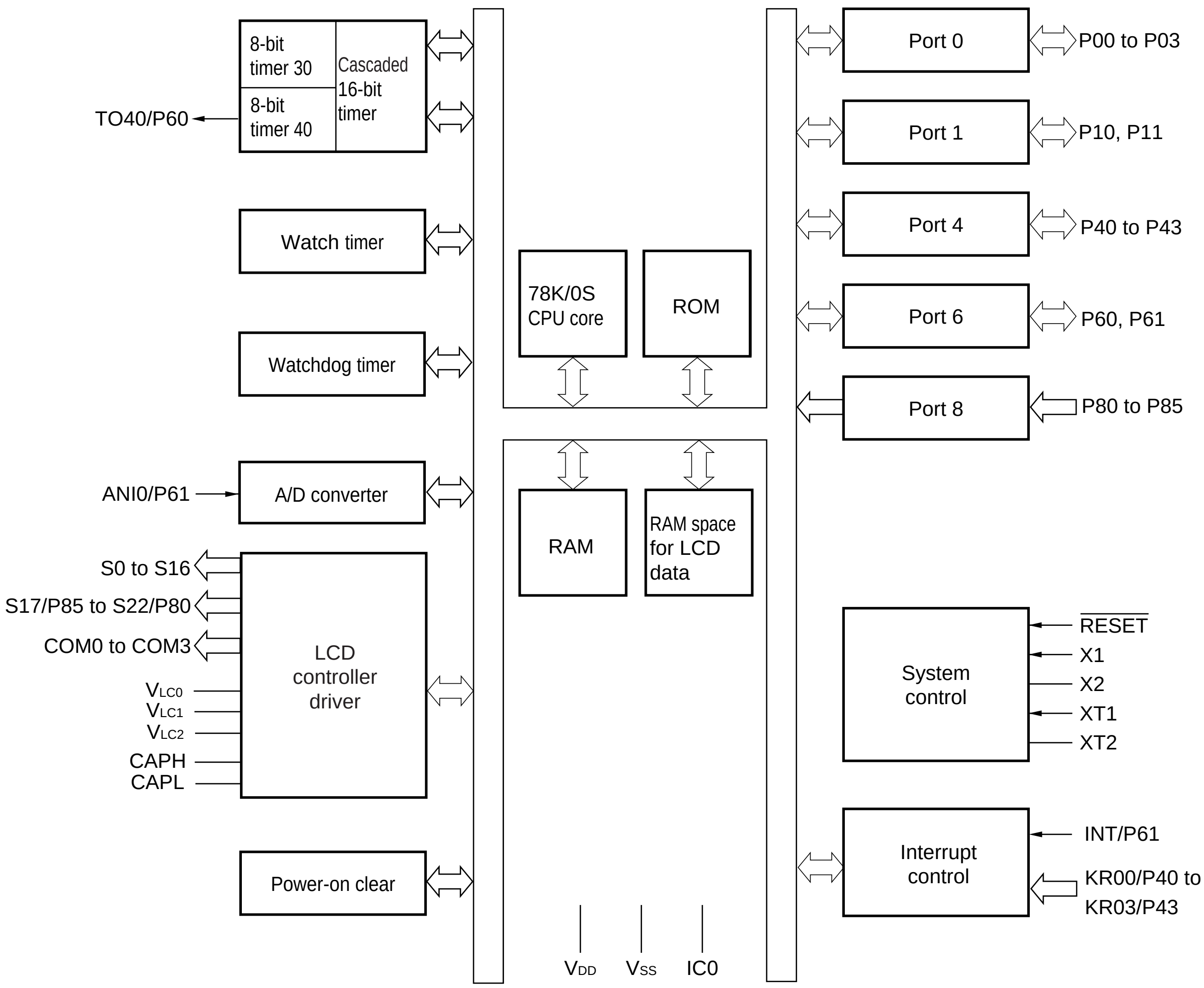
μPD789462GB-×××-8ET, μPD789464GB-×××-8ET, μPD789466GB-×××-8ET, μPD789467GB-×××-8ET



Caution Connect the IC0 (Internally Connected) pin directly to V_{SS}.

ANI0:	Analog Input	$\overline{\text{RESET}}$:	Reset
CAPH, CAPL:	LCD Power Supply Capacitance Control	S0 to S22:	Segment Output
COM0 to COM3:	Common Output	TO40:	Timer Output
IC0:	Internally Connected	V_{DD}:	Power Supply
INT:	Interrupt from Peripherals	V_{LC0} to V_{LC2}:	Power Supply for LCD
KR00 to KR03:	Key Return	V_{SS}:	Ground
P00 to P03:	Port 0	X1, X2:	Crystal (Main system clock)
P10, P11:	Port 1	XT1, XT2:	Crystal (Subsystem clock)
P40 to P43:	Port 4		
P60, P61:	Port 6		
P80 to P85:	Port 8		

2. BLOCK DIAGRAM



Remark Internal ROM and RAM capacities vary depending on the product.

3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P03	I/O	Port 0. 4-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, on-chip pull-up resistors can be specified for the whole port using pull-up resistor option register 0 (PU0).	Input	–
P10, P11	I/O	Port 1. 2-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, on-chip pull-up resistors can be specified for the whole port using pull-up resistor option register 0 (PU0).	Input	–
P40 to P43	I/O	Port 4. 4-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, on-chip pull-up resistors can be specified for the whole port using pull-up resistor option register 0 (PU0), or key return mode register 00 (KRM00).	Input	KR00 to KR03
P60	I/O	Port 6. 2-bit I/O port. Input/output can be specified in 1-bit units.	Input	TO40
P61				INT/ANI0
P80 to P85	Input	Port 8. 6-bit Input port.	Input	S22 to S17

3.2 Non-Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
INT	Input	External interrupt input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.	Input	P61/ANI0
KR00 to KR03	Input	Key return signal detection	Input	P40 to P43
TO40	Output	8-bit timer 40 output	Input	P60
ANI0	Input	A/D converter analog input	Input	P61/INT
S0 to S16	Output	LCD controller/driver segment signal outputs	Low-level output	–
S17 to S22			Input	P85 to P80
COM0 to COM3	Output	LCD controller/driver common signal outputs	Low-level output	–
V_{LC0} to V_{LC2}	–	LCD drive voltage	–	–
CAPH, CAPL	–	Voltage amplifier capacitor for LCD drive connection pins	–	–
X1	Input	Connecting crystal resonator for main system clock oscillation	–	–
X2	–		–	–
XT1	Input	Connecting crystal resonator for subsystem clock oscillation	–	–
XT2	–		–	–
$\overline{\text{RESET}}$	Input	System reset input	Input	–
V_{DD}	–	Positive power supply	–	–
V_{SS}	–	Ground potential	–	–
IC0	–	Internally connected. Connect directly to V_{SS}.	–	–

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The I/O circuit type of each pin and recommended connection of unused pins is shown in Table 3-1.
For the input/output circuit configuration of each type, refer to Figure 3-1.

Table 3-1. Types of Pin I/O Circuits and Recommended Connection of Unused Pins

Pin Name	I/O Circuit Type	I/O	Recommend Connection of Unused Pins
P00 to P03	5-A	I/O	Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P10, P11			
P40/KR00 to P43/KR03	8-A		
P60/TO40	5		
P61/INT/ANI0	33		Input: Independently connect to V_{SS} via a resistor. Output: Leave open.
P80/S22 to P85/S17	17-G		Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
S0 to S16	17-D	Output	Leave open.
COM0 to COM3	18-B		
CAPH, CAPL	–	–	
V_{LC0} to V_{LC2}			
XT1		Input	Connect to V_{SS}.
XT2		–	Leave open.
$\overline{\text{RESET}}$	2	Input	–
IC0	–	–	Connect directly to V_{SS}.

Figure 3-1. I/O Circuit Types (1/2)

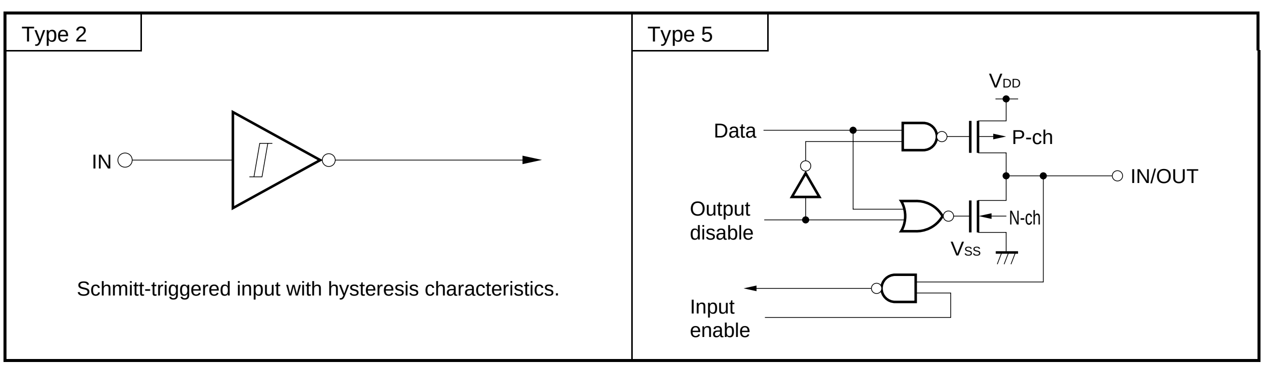
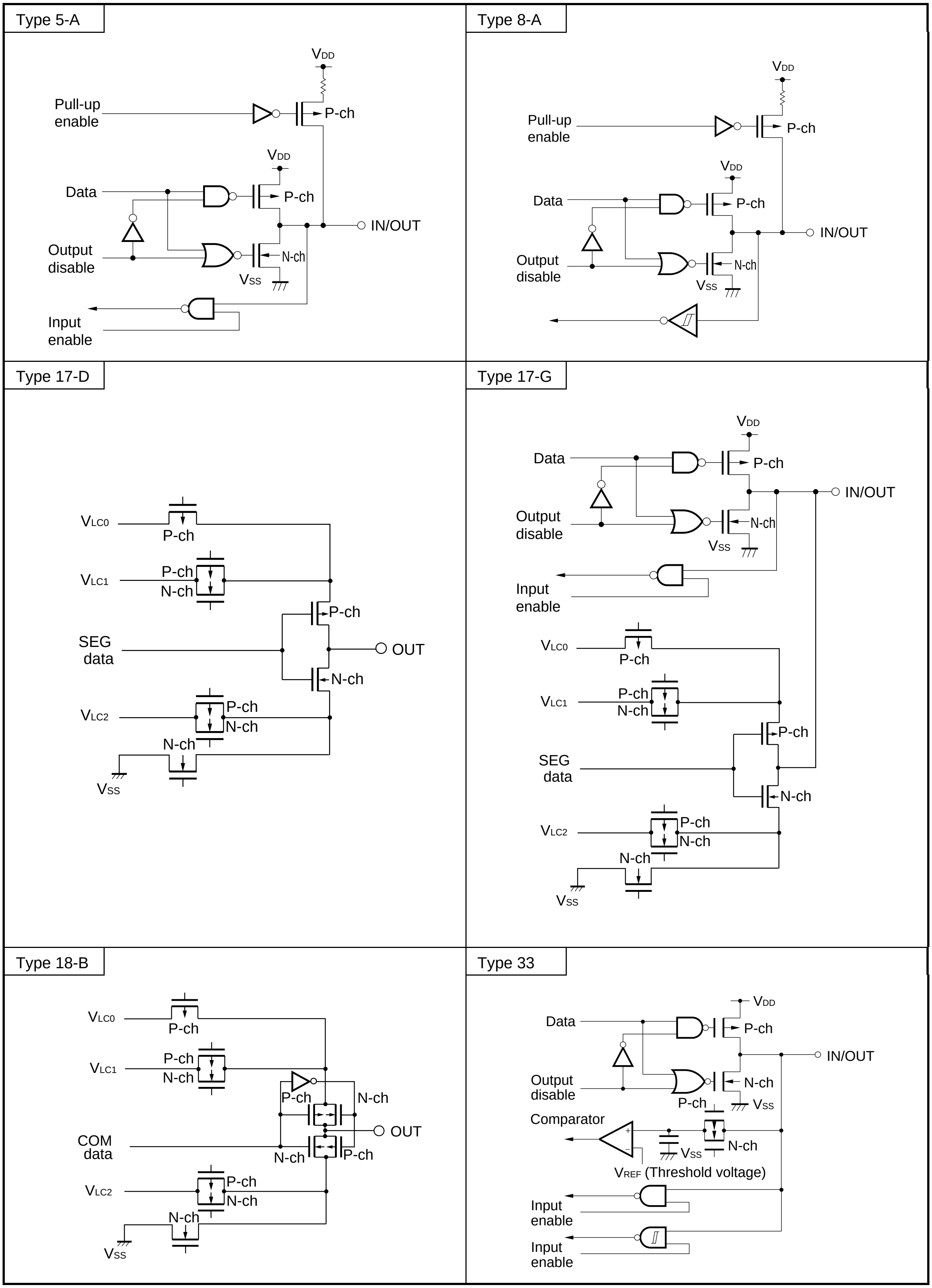


Figure 3-1. I/O Circuit Types (2/2)

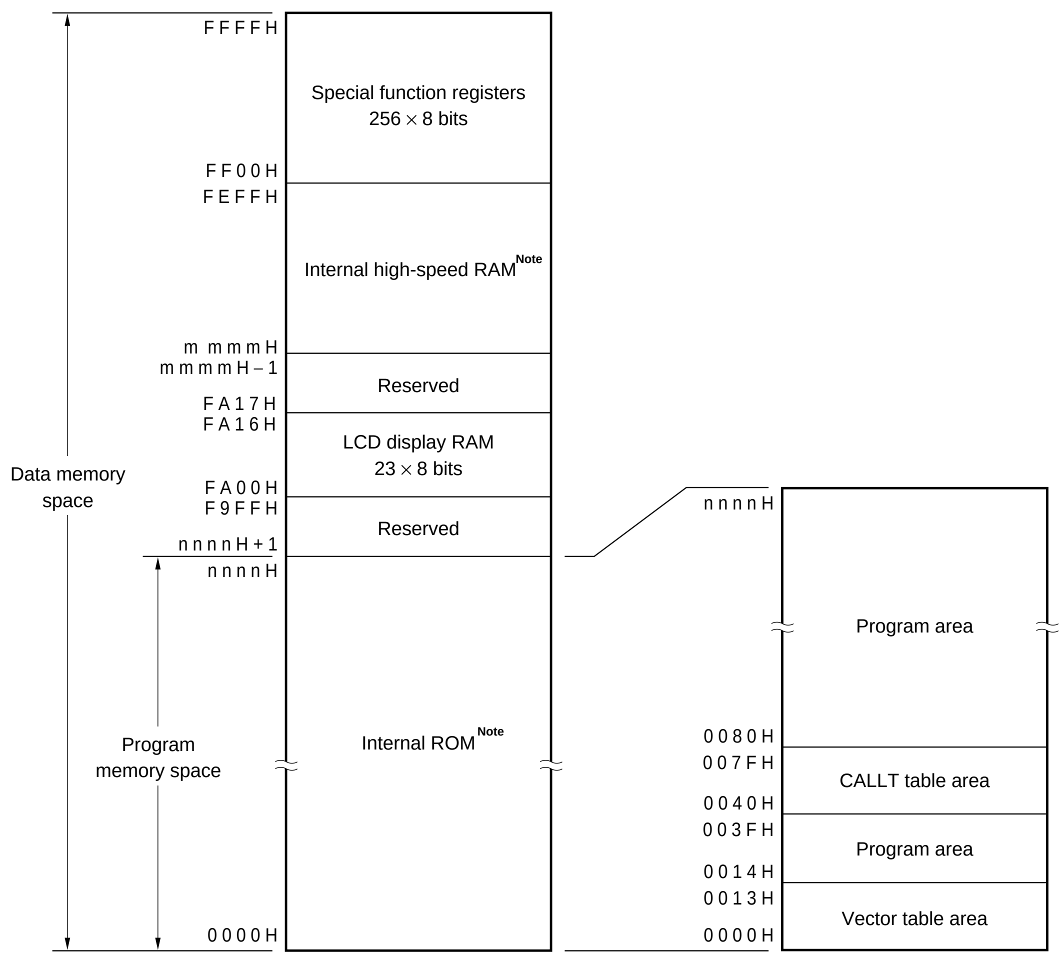


4. CPU ARCHITECTURE

4.1 Memory Space

The μPD789462, 789464, 789466, and 789467 are provided with 64 KB of accessible memory space. Figure 4-1 shows the memory map.

Figure 4-1. Memory Map



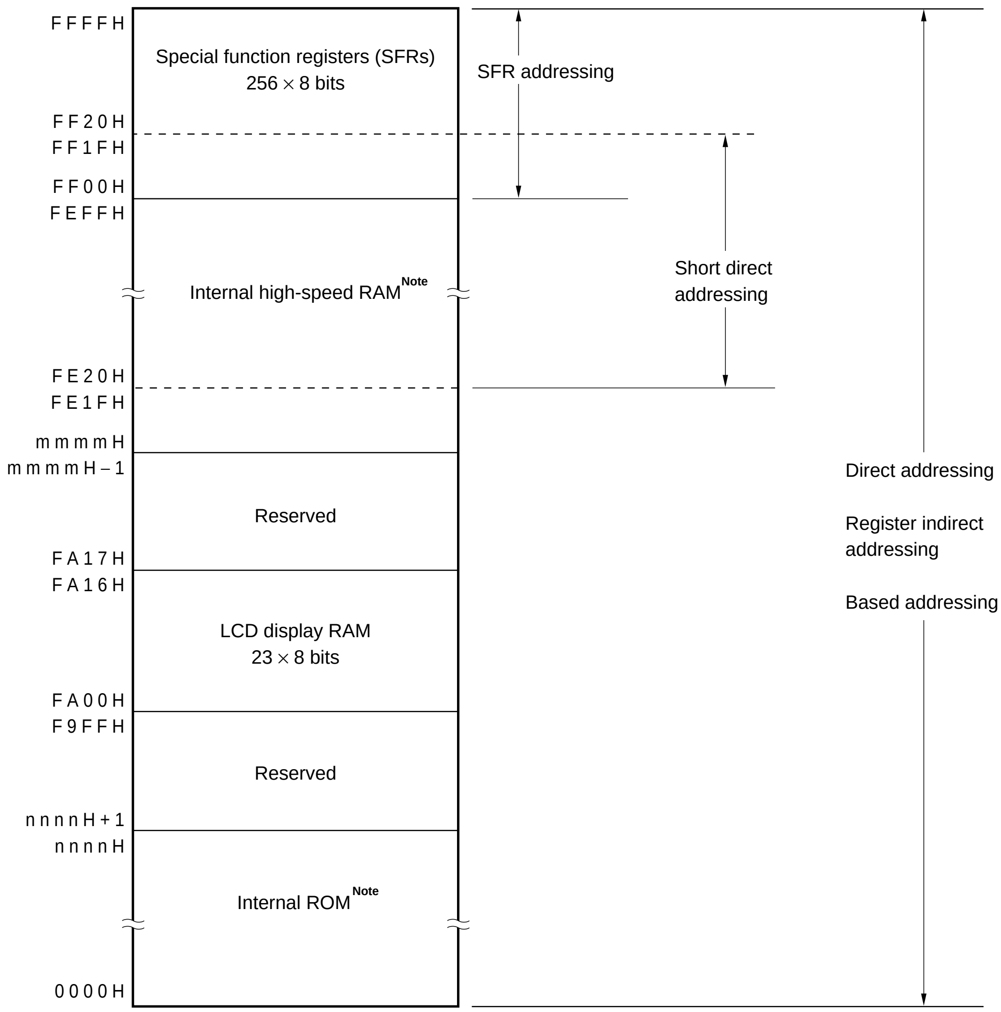
Note Internal ROM and internal high-speed RAM capacities vary depending on the product (see the table below).

Part Number	Last Address of Internal ROM nnnnH	Start Address of Internal High-Speed RAM mmmmH
μPD789462	0FFFH	FE00H
μPD789464	1FFFH	
μPD789466	3FFFH	FD00H
μPD789467	5FFFH	

4.2 Data Memory Addressing

The μPD789462, 789464, 789466, and 789467 are provided with a variety of addressing modes to improve the operability of the memory. In the area that incorporates data memory (FD00H to FFFFH) in particular, specific addressing modes that correspond to the particular functions of an area, such as the special function registers (SFRs), are available. Figure 4-2 shows the data memory addressing modes.

Figure 4-2. Data Memory Addressing Modes



Note Internal ROM and internal high-speed RAM capacities vary depending on the product (see the table below).

Part Number	Last Address of Internal ROM nnnnH	Start Address of Internal High-speed RAM mmmmH
μPD789462	0FFFH	FE00H
μPD789464	1FFFH	
μPD789466	3FFFH	FD00H
μPD789467	5FFFH	

4.3 Processor Registers

4.3.1 Control registers

(1) Program counter (PC)

The PC is a 16-bit register that holds the address information of the next program to be executed.

Figure 4-3. Program Counter Configuration

	15															0
PC	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0

(2) Program status word (PSW)

The PSW is an 8-bit register that indicates the status of the CPU according to the results of instruction execution.

Figure 4-4. Program Status Word Configuration

7							0
IE	Z	0	AC	0	0	1	CY

(a) Interrupt enable flag (IE)

This flag controls the interrupt request acknowledgement of the CPU.

(b) Zero flag (Z)

This flag is set (1) if the result of an operation is zero; otherwise it is reset (0).

(c) Auxiliary carry flag (AC)

AC is set (1) if the result of the operation has a carry from bit 3 or a borrow at bit 3; otherwise it is reset (0).

(d) Carry flag (CY)

CY is used to indicate whether an overflow or underflow has occurred during the execution of a subtract or add instruction.

(3) Stack pointer (SP)

The SP is a 16-bit register that holds the start address of the stack area. Only the internal RAM area (FD00H to FEFFH) can be specified as the stack area.

Figure 4-5. Stack Pointer Configuration

	15															0
SP	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0

Caution $\overline{\text{RESET}}$ input makes the SP contents undefined, so be sure to initialize the SP before instruction execution.

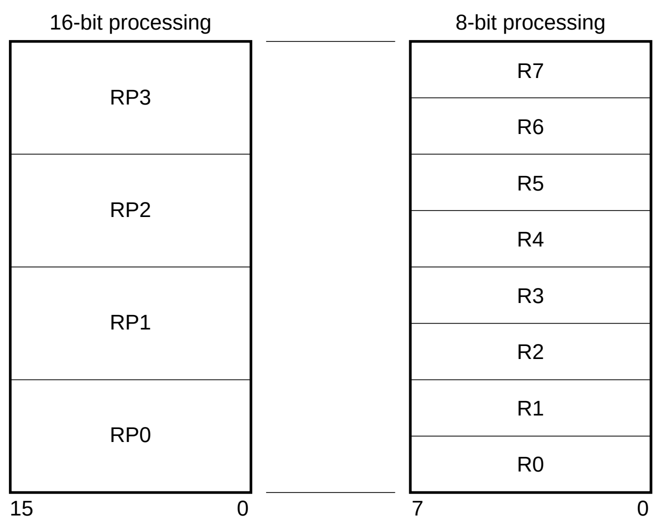
4.3.2 General-purpose registers

The μPD78F9468 has eight 8-bit general-purpose registers (X, A, C, B, E, D, L, and H).

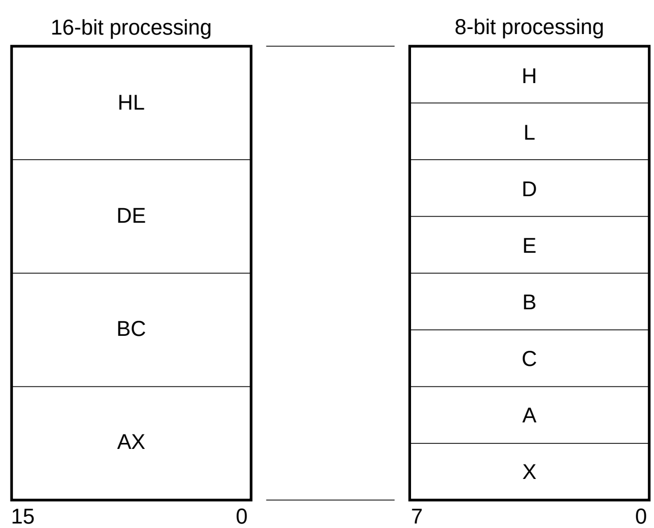
These registers can be used either singly as 8-bit registers or in pairs as 16-bit registers (AX, BC, DE, and HL), and can be described in terms of function names (X, A, C, B, E, D, L, H, AX, BC, DE, and HL) and absolute names (R0 to R7 and RP0 to RP3).

Figure 4-6. General-Purpose Register Configuration

(a) Absolute register names



(b) Functional register names



4.3.3 Special function registers (SFRs)

Special function registers are used as peripheral hardware mode registers and control registers, and are mapped in the 256-byte space from FF00H to FFFFH.

Note that the bit number of a bit name that is a reserved word in the RA78K0S and defined under the header file “sfrbit.h” in the CC78K0S appears enclosed inside < > in the register formats. Refer to the register formats in **5. PERIPHERAL HARDWARE FUNCTIONS**.

Table 4-1. Special Function Registers (1/2)

Address	Special Function Register (SFR) Name	Symbol	R/W	Bit Unit for Manipulation			After Reset
				1 Bit	8 Bits	16 Bits	
FF00H	Port 0	P0	R/W	√	√	–	00H
FF01H	Port 1	P1		√	√	–	
FF03H	port 4	P4		√	√	–	
FF05H	Port 6	P6		√	√	–	
FF08H	Port 8	P8		√	√	–	
FF15H	A/D conversion result register	ADCR0	R	–	√	–	Undefined
FF20H	Port mode register 0	PM0	R/W	√	√	–	FFH
FF21H	Port mode register 1	PM1		√	√	–	
FF24H	Port mode register 4	PM4		√	√	–	
FF26H	Port mode register 6	PM6		√	√	–	
FF42H	Watchdog timer clock selection resister	WDCS		–	√	–	00H
FF4AH	Watch timer mode control register	WTM		√	√	–	
FF58H	Port function register 8	PF8		√	√	–	
FF63H	8-bit compare register 30	CR30	W	–	√	–	Undefined
FF64H	8-bit timer counter 30	TM30	R	–	√	–	00H
FF65H	8-bit timer mode control register 30	TMC30	R/W	√	√	–	
FF66H	8-bit compare register 40	CR40	W	–	√	–	Undefined
FF67H	8-bit H width compare register 40	CRH40		–	√	–	
FF68H	8-bit timer counter 40	TM40	R	–	√	–	00H
FF69H	8-bit timer mode control register 40	TMC40	R/W	√	√	–	
FF6AH	Carrier generator output control register 40	TCA40	W	–	√	–	
FF80H	A/D converter mode register 0	ADM0	R/W	√	√	–	
FF84H	A/D input selection register 0	ADS0		√	√	–	
FFB0H	LCD display mode register 0	LCDM0		√	√	–	
FFB2H	LCD clock control register 0	LCDC0		√	√	–	
FFB3H	LCD voltage amplification control register 0	LCDVA0		√	√	–	

Table 4-1. Special Function Registers (2/2)

Address	Special Function Register (SFR) Name	Symbol	R/W	Bit Unit for Manipulation			After Reset
				1 Bit	8 Bits	16 Bits	
FFE0H	Interrupt request flag register 0	IF0	R/W	√	√	–	00H
FFE4H	Interrupt mask flag register 0	MK0		√	√	–	FFH
FFECH	External interrupt mode register 0	INTM0		–	√	–	00H
FFF0H	Subclock oscillation mode register	SCKM		√	√	–	
FFF2H	Subclock control register	CSS		√	√	–	
FFF5H	Key return mode register 00	KRM00		√	√	–	
FFF7H	Pull-up resistor option register 0	PU0		√	√	–	
FFF9H	Watchdog timer mode register	WDTM		√	√	–	
FFFAH	Oscillation stabilization time selection register	OSTS		–	√	–	04H
FFFBH	Processor clock control register	PCC		√	√	–	02H

5. PERIPHERAL HARDWARE FUNCTIONS

5.1 Ports

5.1.1 Port functions

Various kinds of control operations are possible using the ports provided in the μPD789462, 789464, 789466, and 789467. These ports are illustrated in Figure 5-1 and their functions are listed in Table 5-1.

A number of alternate functions are also provided, except for those ports functioning as digital I/O ports. Refer to **3. PIN FUNCTIONS** for details of the alternate function pins.

Figure 5-1. Ports

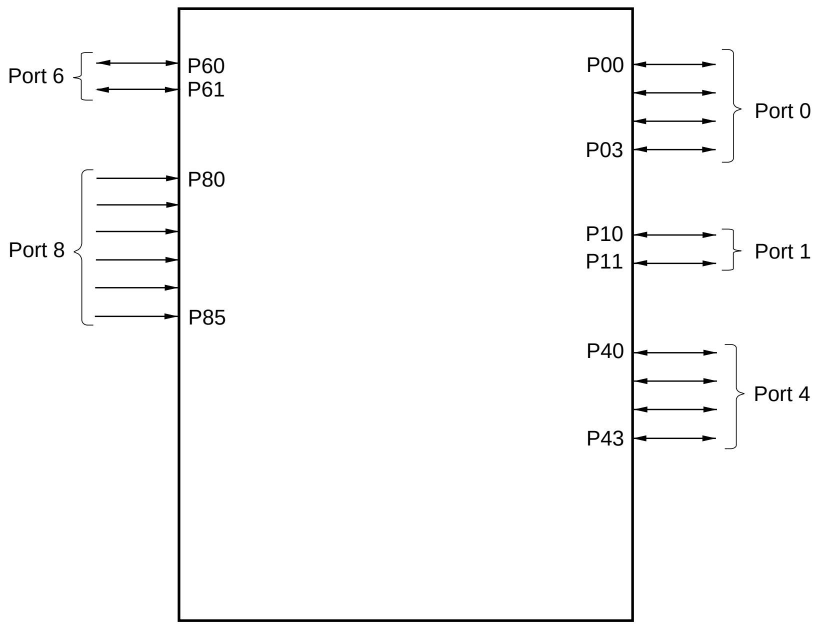


Table 5-1. Port Functions

Port Name	Pin Name	Function
Port 0	P00 to P03	I/O port. Input and output can be specified in 1-bit units. When used as an input port, on-chip pull-up resistors can be specified using pull-up resistor option register 0 (PU0).
Port 1	P10, P11	I/O port. Input and output can be specified in 1-bit units. When used as an input port, on-chip pull-up resistors can be specified using pull-up resistor option register 0 (PU0).
Port 4	P40 to P43	I/O port. Input and output can be specified in 1-bit units. When used as an input port, on-chip pull-up resistors can be specified using pull-up resistor option register 0 (PU0), or key return mode register 00 (KRM00).
Port 6	P60, P61	I/O port. Input and output can be specified in 1-bit units.
Port 8	P80 to P85	Input port

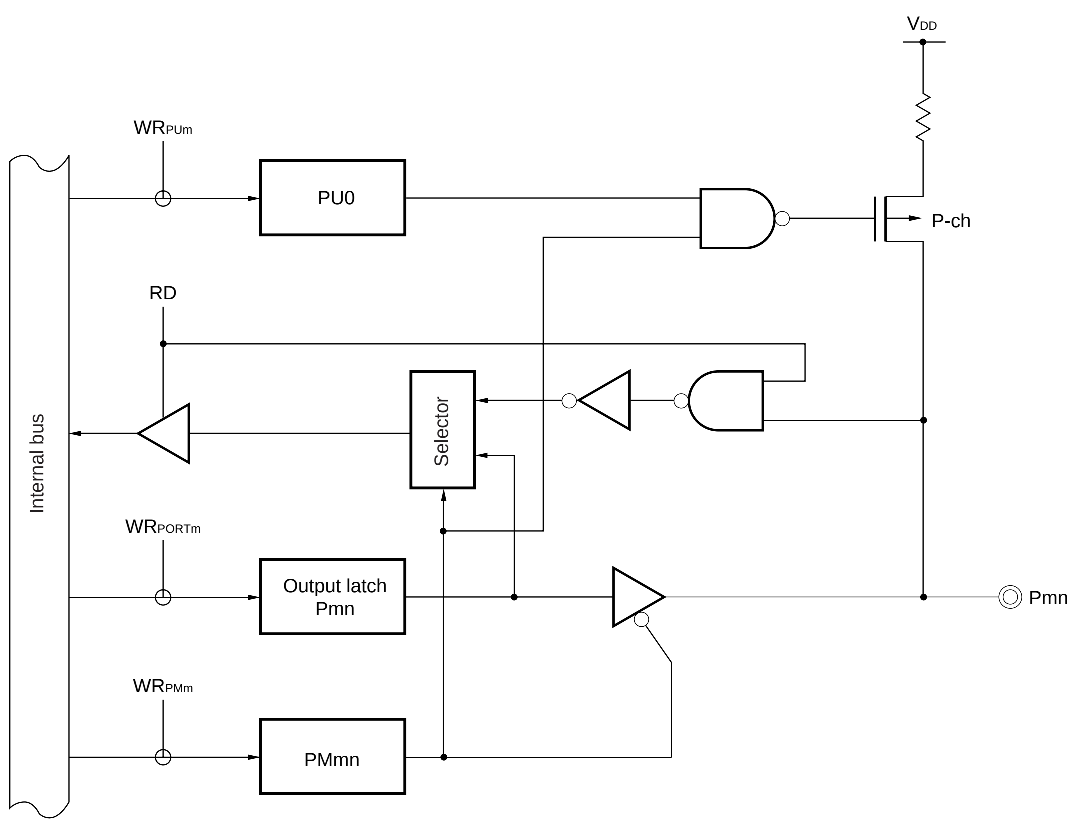
5.1.2 Port configuration

The ports consist of the following hardware.

Table 5-2. Port Configuration

Item	Configuration
Control registers	Port mode registers (PMm: m = 0, 1, 4, 6) Pull-up resistor option register 0 (PU0) Port function register 8 (PF8)
Ports	Total: 18 (CMOS I/O: 12, CMOS input: 6 (including pins shared with LCD))
Pull-up resistors	Total: 10 (software control: 10)

Figure 5-2. Basic Configuration of CMOS Port



Caution Figure 5-2 shows the basic configuration of a CMOS I/O port. This configuration differs depending on the functions of alternate function pins. Also, on-chip pull-up resistors can be connected to port 4 by means of a setting in key return mode register 00 (KRM00).

Remark PU0: Pull-up resistor option register 0
PMmn: Bit n of port mode register m (m = 0, 1, 4, 6, n = 0 to 3)
Pmn: Bit n of port m
RD: Port read signal
WR: Port write signal

5.1.3 Port function control registers

The ports are controlled by the following three types of registers.

- Port mode registers (PM0, PM1, PM4, PM6)
- Pull-up resistor option register 0 (PU0)
- Port function register 8 (PF8)

(1) Port mode registers (PM0, PM1, PM4, PM6)

Input and output can be specified in 1-bit units.

These registers can be set using a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets these registers to FFH.

When using the port pins as their alternate functions, set the output latch as shown in Table 5-3.

Caution Because P61 functions alternately as an external interrupt input, when the output level changes after the output mode of the port function is specified, the interrupt request flag will be inadvertently set. Therefore, be sure to preset the interrupt mask flag (PMK0) before using the port in output mode.

Figure 5-3. Port Mode Register Format

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM0	1	1	1	1	PM03	PM02	PM01	PM00	FF20H	FFH	R/W
PM1	1	1	1	1	1	1	PM11	PM10	FF21H	FFH	R/W
PM4	1	1	1	1	PM43	PM42	PM41	PM40	FF24H	FFH	R/W
PM6	1	1	1	1	1	1	PM61	PM60	FF26H	FFH	R/W

PMmn	Pmn pin input/output mode selection (m = 0, 1, 4, 6, n = 0 to 3)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Table 5-3. Port Mode Registers and Output Latch Settings When Using Alternate Functions

Pin Name	Alternate Function		PM××	P××
	Name	I/O		
P40 to P43	KR00 to KR03	Input	1	×
P60	TO40	Output	0	0
P61	INT/ANI0	Input	1	×

Remark ×: don't care
PM××: Port mode register
P××: Port output latch

(2) Pull-up resistor option register 0 (PU0)

This register sets whether to use on-chip pull-up resistors for ports 0, 1, and 4. An on-chip pull-up resistor can be used only for those bits set to the input mode of a port for which the use of the on-chip pull-up resistor has been specified using PU0.

For those bits set to the output mode, on-chip pull-up resistors cannot be used, regardless of the setting of PU0. This also applies to alternate-function pins used as output pins.

PU0 is set using a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets this register to 00H.

Figure 5-4. Format of Pull-up Resistor Option Register 0

Symbol	7	6	5	<4>	3	2	<1>	<0>	Address	After reset	R/W
PU0	0	0	0	PU04	0	0	PU01	PU00	FFF7H	00H	R/W

PU0m	Port m on-chip pull-up resistor selection (m = 0, 1, 4)
0	An on-chip pull-up resistor is not connected
1	An on-chip pull-up resistor is connected

Caution Always set bits 2, 3, and 5 to 7 to 0.

(3) Port function register 8 (PF8)

This register sets the port function of port 8 in 1-bit units.

The pins of port 8 are selected as either LCD segment signal outputs or general-purpose port pins according to the setting of PF8.

PF8 can be set using a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets this register to 00H.

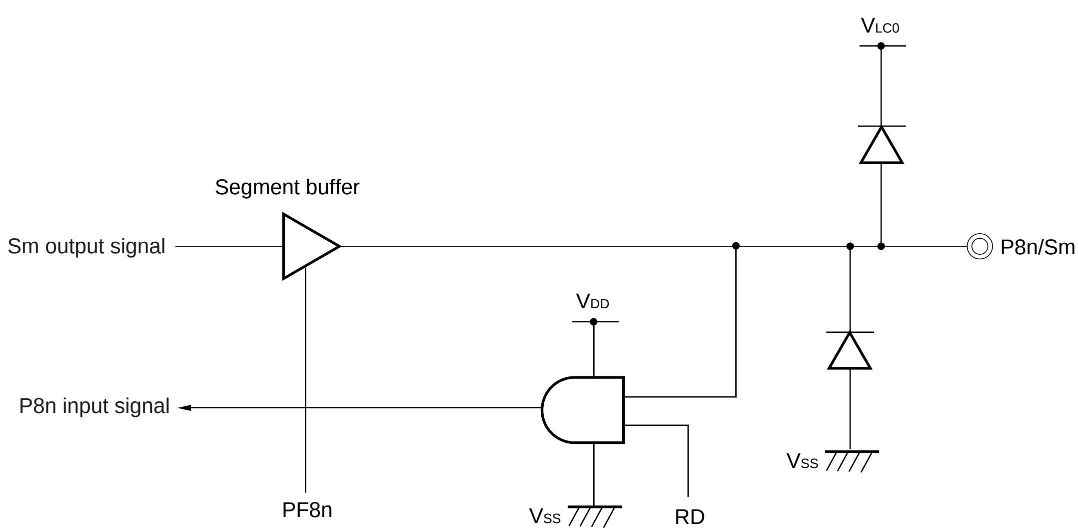
Figure 5-5. Format of Port Function Register 8

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PF8	0	0	PF85	PF84	PF83	PF82	PF81	PF80	FF58H	00H	R/W

PF8n	P8n port function (n = 0 to 5)
0	Operates as a general-purpose port
1	Operates as an LCD segment signal output

Caution When port 8 pins are used as LCD segment pins, observe the following restrictions (because an ESD protection circuit for the LCD pins is connected to the V_{LC0} side).

- **When all of pins P80 to P85 are used as general-purpose port pins: Use the pins in the range of V_{DD} = 1.8 to 5.5 V.**
- **When any one of pins P80 to P85 is used as an LCD segment pin:**
  In V_{LC0} = 3.0 V mode (GAIN = 1)... Use the pin(s) in the range of V_{DD} = 1.8 to 3.0 V.
  In V_{LC0} = 4.5 V mode (GAIN = 0)... Use the pin(s) in the range of V_{DD} = 1.8 to 4.5 V.



Remark Sm: LCD segment output (m = 22 to 17)
P8n: Bit n of port 8 (n = 0 to 5)
PF8n: Bit n of port function register 8 (n = 0 to 5)
RD: Read signal of port 8n

5.2 Clock Generator

5.2.1 Clock generator function

The clock generator generates the clock pulse to be supplied to the CPU and peripheral hardware.
There are two types of system clock oscillators:

- Main system clock oscillator (ceramic/crystal resonator)
  This circuit generates a frequency of 1.0 to 5.0 MHz. Oscillation can be stopped by executing the STOP instruction or by means of a processor clock control register (PCC) setting.
- Subsystem clock oscillator
  This circuit generates a frequency of 32.768 kHz. Oscillation can be stopped using the subclock oscillation mode register (SCKM).

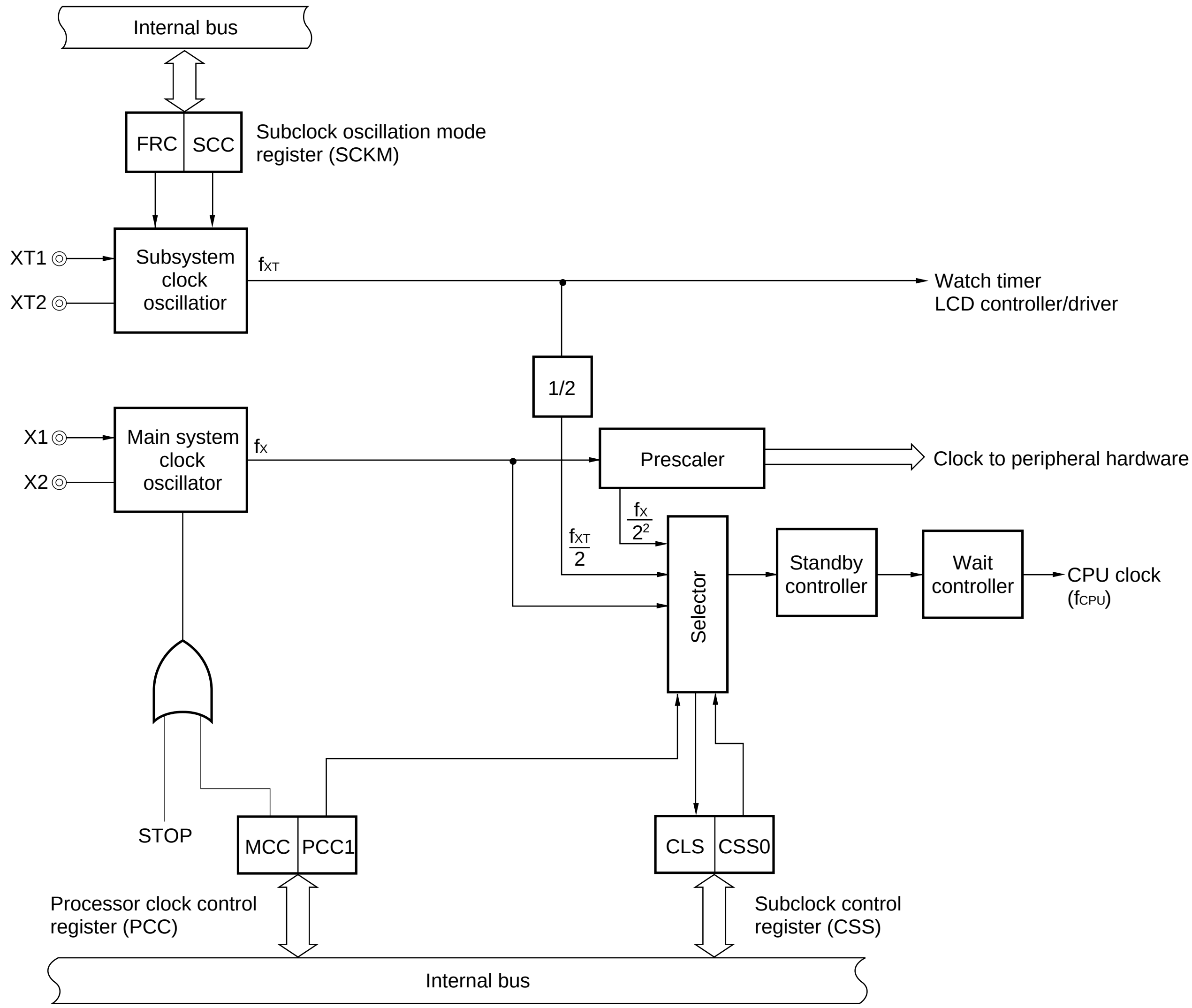
5.2.2 Clock generator configuration

The clock generator consists of the following hardware.

Table 5-4. Clock Generator Configuration

Item	Configuration
Control registers	Processor clock control register (PCC) Subclock oscillation mode register (SCKM) Subclock control register (CSS)
Oscillators	Main system clock oscillator Subsystem clock oscillator

Figure 5-6. Clock Generator Block Diagram



5.2.3 Clock generator control registers

The clock generator is controlled by the following three registers.

- Processor clock control register (PCC)
- Subclock oscillation mode register (SCKM)
- Subclock control register (CSS)

(1) Processor clock control register (PCC)

This register is used to select the CPU clock and set the frequency division ratio.

PCC is set using a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets this register to 02H.

Figure 5-7. Format of Processor Clock Control Register

Symbol	<7>	6	5	4	3	2	1	0	Address	After reset	R/W
PCC	MCC	0	0	0	0	0	PCC1	0	FFFBH	02H	R/W

MCC	Main system clock oscillator operation control
0	Operation enabled
1	Operation stopped

CSS0	PCC1	CPU clock (f_{CPU}) selection[Note]	Minimum instruction execution time: $2f_{CPU}$
0	0	f_X (0.2 μs)	0.4 μs
0	1	$f_X/2^2$ (0.8 μs)	1.6 μs
1	×	$f_{XT}/2$ (61 μs)	122 μs

Note The CPU clock is selected by a combination of flag settings in the PCC and CSS registers (refer to **5.2.3 (3) Subclock control register (CSS)**).

Cautions 1. Always set bits 0 and 2 to 6 to 0.

2. MCC can be set only when the subsystem clock is selected as the CPU clock. Setting MCC to 1 while the main system clock is operating is invalid.

Remarks 1. f_X: Main system clock oscillation frequency

2. f_{XT}: Subsystem clock oscillation frequency

3. The parenthesized values apply to operation at f_X = 5.0 MHz or f_{XT} = 32.768 kHz.

4. ×: don’t care

(2) Subclock oscillation mode register (SCKM)

This register is used to select a feedback resistor for the subsystem clock and control the oscillation of the clock.

SCKM is set using a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets this register to 00H.

Figure 5-8. Format of Subclock Oscillation Mode Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
SCKM	0	0	0	0	0	0	FRC	SCC	FFF0H	00H	R/W

FRC	Feedback resistor selection
0	An on-chip feedback resistor is used
1	An on-chip feedback resistor is not used

SCC	Control of subsystem clock oscillator operation
0	Operation enabled
1	Operation stopped

Caution Always set bits 2 to 7 to 0.

(3) Subclock control register (CSS)

This register is used to specify whether the main system or subsystem clock oscillator is selected and to indicate the operating status of the CPU clock.

CSS is set using a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets this register to 00H.

Figure 5-9. Format of Subclock Control Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
CSS	0	0	CLS	CSS0	0	0	0	0	FFF2H	00H	R/W[Note]

CLS	CPU clock operating status
0	Operating on the output of the (divided) main system clock
1	Operating on the output of the subsystem clock

CSS0	Selection of main system clock or subsystem clock oscillator
0	Main system clock oscillator (divided) output
1	Subsystem clock oscillator output

Note Bit 5 is read-only.

Caution Always set bits 0 to 3, 6, and 7 to 0.

5.3 8-Bit Timer 30, 40

5.3.1 Functions of 8-bit timer 30, 40

The 8-bit timer in the μPD789462, 789464, 789466, and 789467 has 2 channels (timer 30 and timer 40). The operation modes in the following table are possible by means of mode register settings.

Table 5-5. List of Modes

Mode \ Channel	Timer 30	Timer 40
8-bit timer mode (discrete mode)	√	√
16-bit timer mode (cascade connection mode)	√	
Carrier generator mode	√	
PWM output mode	–	√

(1) 8-bit timer mode (discrete mode)

The timer can be used for the following functions in this mode.

- 8-bit resolution interval timer
- 8-bit resolution square wave output (timer 40 only)

(2) 16-bit timer mode (cascade connection mode)

These timers can be used for 16-bit timer operations via a cascade connection.
The timer can be used for the following functions in this mode.

- 16-bit resolution interval timer
- 16-bit resolution square wave output

(3) Carrier generator mode

In this mode the carrier clock generated by timer 40 is output in the cycle set by timer 30.

(4) PWM output mode

In this mode, a pulse with an arbitrary duty ratio, which is set by timer 40, is output.

5.3.2 Configuration of 8-bit timer 30, 40

8-bit timers 30 and 40 consist of the following hardware.

Table 5-6. Configuration of 8-Bit Timer 30, 40

Item	Configuration
Timer counter	8 bits × 2 (TM30, TM40)
Registers	Compare registers: 8 bits × 3 (CR30, CR40, CRH40)
Timer outputs	1 (TO40)
Control registers	8-bit timer mode control register 30 (TMC30) 8-bit timer mode control register 40 (TMC40) Carrier generator output control register 40 (TCA40) Port mode register 6 (PM6)

Figure 5-10. Block Diagram of Timer 30

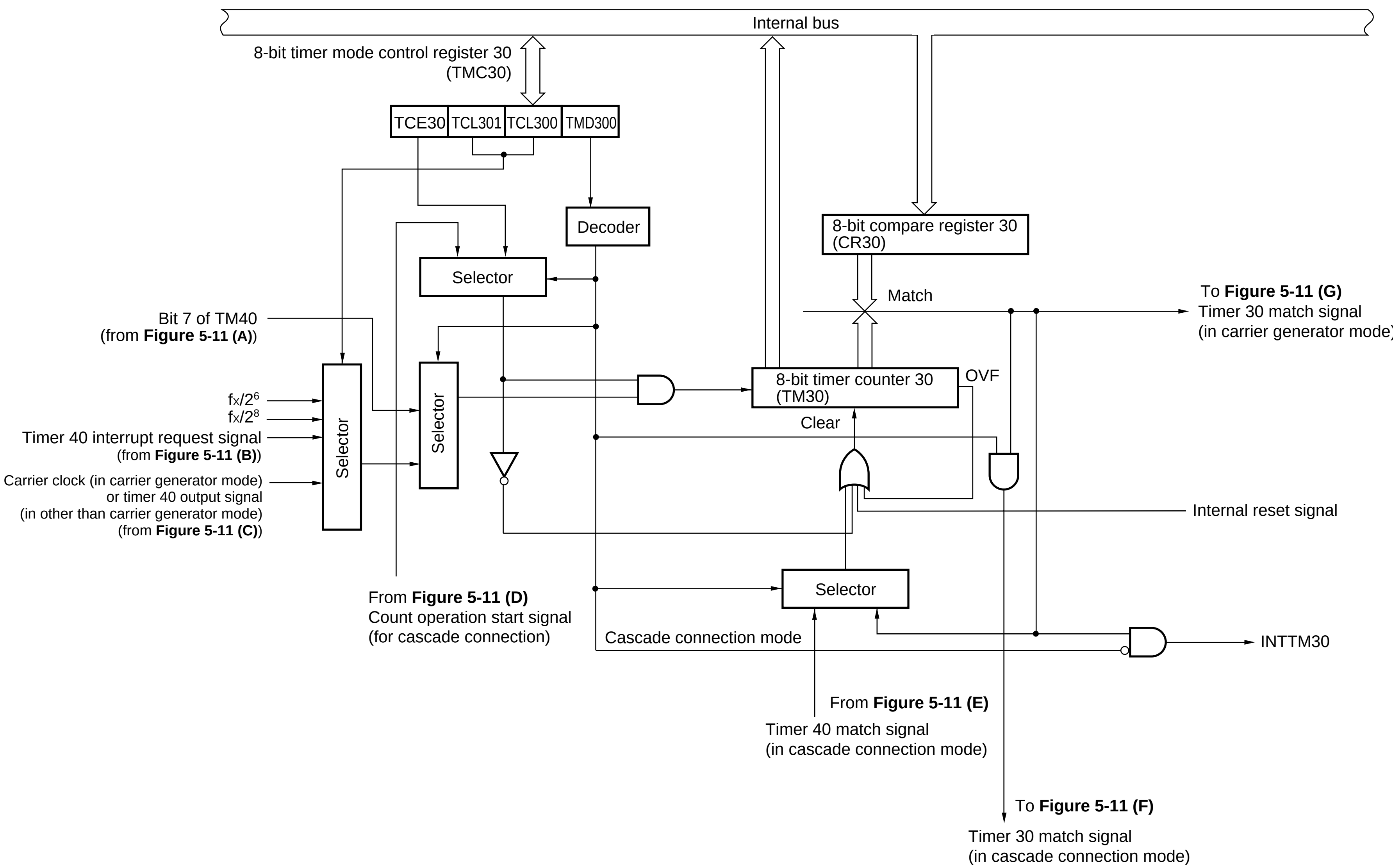
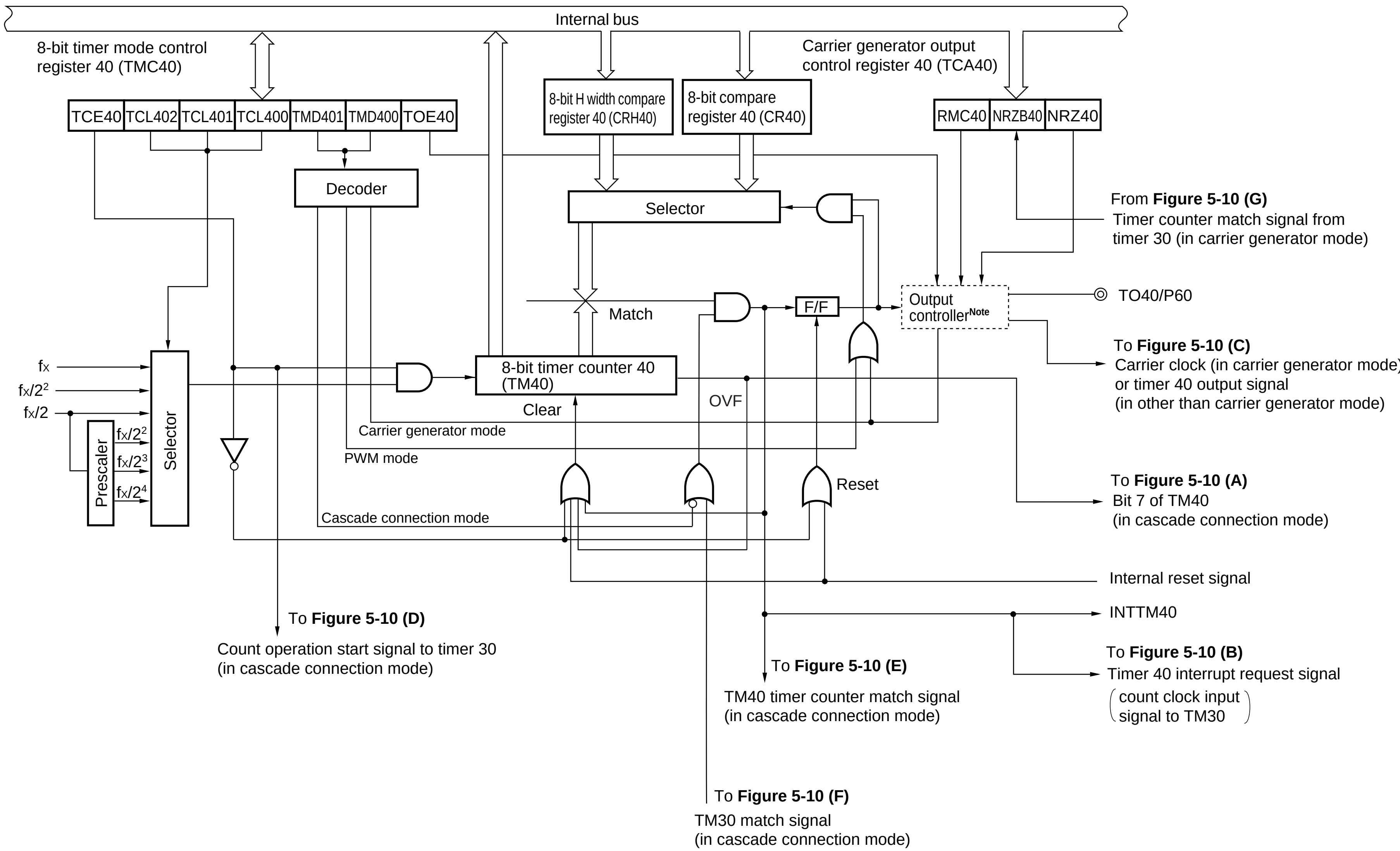
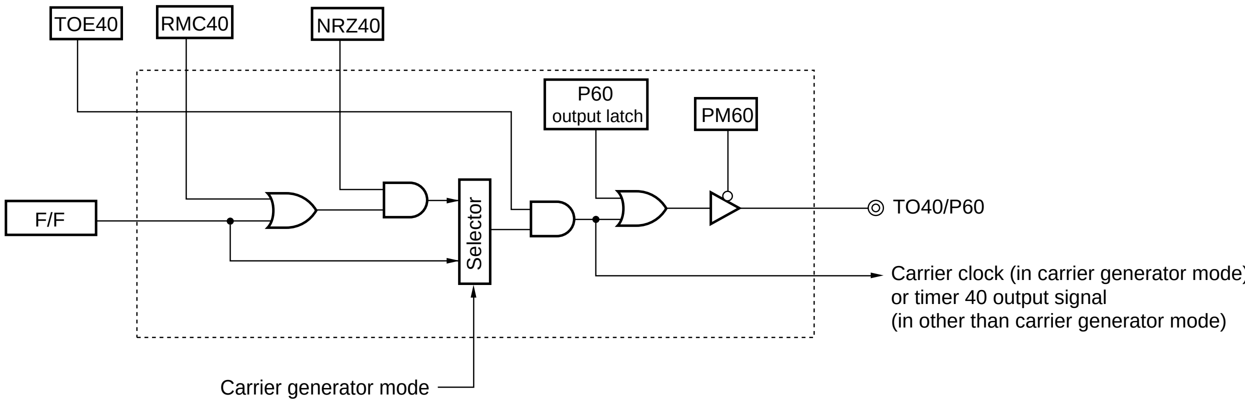


Figure 5-11. Block Diagram of Timer 40



Note Refer to **Figure 5-12** for details.

Figure 5-12. Block Diagram of Output Controller (Timer 40)



(1) 8-bit compare register 30 (CR30)

A value specified in CR30 is compared with the count value in 8-bit timer counter 30 (TM30), and if they match, an interrupt request (INTTM30) is generated.

CR30 is set using an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input makes this register undefined.

Caution CR30 cannot be used in carrier generator mode or PWM output mode.

(2) 8-bit compare register 40 (CR40)

A value specified in CR40 is compared with the count value in 8-bit timer counter 40 (TM40), and if they match, an interrupt request (INTTM40) is generated. When operating as a 16-bit timer in cascade connection with TM30, an interrupt request (INTTM40) is only generated if both CR30 and TM30, and CR40 and TM40 match simultaneously (INTTM30 is not issued).

CR40 is set using an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input makes this register undefined.

(3) 8-bit H width compare register (CRH40)

In carrier generator mode or PWM output mode, a timer output high-level width can be set by writing a value to CRH40.

CRH40 is set using an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input makes this register undefined.

(4) 8-bit timer counter 30, 40 (TM30, TM40)

These are 8-bit registers for counting the count pulses.

TM30 and TM40 can be read with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets these registers to 00H.

The conditions under which TM30 and TM40 are cleared to 00H are listed below.

(a) Discrete mode

(i) TM30

- Upon a reset
- When TCE30 (bit 7 of 8-bit timer mode control register 30 (TMC30)) is cleared to 0
- Upon a match between TM30 and CR30
- If the TM30 count value overflows

(ii) TM40

- Upon a reset
- When TCE40 (bit 7 of 8-bit timer mode control register 40 (TMC40)) is cleared to 0
- Upon a match between TM40 and CR40
- If the TM40 count value overflows

(b) Cascade connection mode (TM30 and TM40 cleared to 00H simultaneously)

- Upon a reset
- When the TCE40 flag is cleared to 0
- Upon a simultaneous match between TM30 and CR30, and TM40 and CR40
- If the TM30 and TM40 count values overflow simultaneously

(c) Carrier generator/PWM output mode (TM40 only)

- Upon a reset
- When the TCE40 flag is cleared to 0
- Upon a match between TM40 and CR40
- Upon a match between TM40 and CRH40
- If the TM40 count value overflows

5.3.3 8-bit timer 30, 40 control registers

8-bit timers 30 and 40 are controlled by the following 4 registers.

- 8-bit timer mode control register 30 (TMC30)
- 8-bit timer mode control register 40 (TMC40)
- Carrier generator output control register 40 (TCA40)
- Port mode register 6 (PM6)

(1) 8-bit timer mode control register 30 (TMC30)

This register is used to control the timer 30 count clock and operation mode settings.

TMC30 is set using a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets this register to 00H.

Figure 5-13. Format of 8-Bit Timer Mode Control Register 30

Symbol	<7>	6	5	4	3	2	1	0	Address	After reset	R/W
TMC30	TCE30	0	0	TCL301	TCL300	0	TMD300	0	FF65H	00H	R/W

TCE30	TM30 count control operation[Note 1]
0	TM30 count value cleared and operation stopped
1	Count operation starts

TCL301	TCL300	Timer 30 count clock selection
0	0	$f_X/2^6$ (78.1 kHz)
0	1	$f_X/2^8$ (19.5 kHz)
1	0	Timer 40 match signal
1	1	Carrier clock (in carrier generator mode) or timer 40 output signal (in other than carrier generator mode)

TMD300	TMD401	TMD400	Timer 30, timer 40 operation mode selection[Note 2]
0	0	0	Discrete mode
1	0	1	Cascade connection mode
0	1	1	Carrier generator mode
0	1	0	PWM output mode
Other than above			Setting prohibited

Notes 1. The TCE30 setting will be ignored in cascade mode because in this case the count operation is controlled by TCE40 (bit 7 of TMC40).

2. The operation mode selection is made using a combination of TMC30 and TMC40 register settings.

Caution In cascade connection mode, the timer 40 output signal is forcibly selected for the count clock.

Remarks 1. f_X: Main system clock oscillation frequency

2. The parenthesized values apply to operation at f_X = 5.0 MHz

(2) 8-bit timer mode control register 40 (TMC40)

This register is used to control the timer 40 count clock and operation mode settings.

TMC40 is set using a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets this register to 00H.

Figure 5-14. Format of 8-Bit Timer Mode Control Register 40

Symbol	<7>	6	5	4	3	2	1	<0>	Address	After reset	R/W
TMC40	TCE40	0	TCL402	TCL401	TCL400	TMD401	TMD400	TOE40	FF69H	00H	R/W

TCE40	TM40 count control operation[Note 1]
0	TM40 count value cleared and operation stopped (in cascade connection mode, the count value of TM30 is cleared at the same time)
1	Count operation starts (in cascade connection mode, the count operation of TM30 starts at the same time)

TCL402	TCL401	TCL400	Timer 40 count clock selection
0	0	0	f_X (5 MHz)
0	0	1	$f_X/2^2$ (1.25 MHz)
0	1	0	$f_X/2$ (2.5 MHz)
0	1	1	$f_X/2^2$ (1.25 MHz)
1	0	0	$f_X/2^3$ (625 kHz)
1	0	1	$f_X/2^4$ (313 kHz)
Other than above			Setting prohibited

TMD300	TMD401	TMD400	Timer 30, timer 40 operation mode selection[Note 2]
0	0	0	Discrete mode
1	0	1	Cascade connection mode
0	1	1	Carrier generator mode
0	1	0	PWM output mode
Other than above			Setting prohibited

TOE40	Timer output control
0	Output disabled (port mode)
1	Output enabled

Notes 1. The TCE30 setting will be ignored in cascade mode because in this case the count operation is controlled by TCE40 (bit 7 of TMC40).

2. The operation mode selection is made using a combination of TMC30 and TMC40 register settings.

Remarks 1. f_X: Main system clock oscillation frequency

2. The parenthesized values apply to operation at f_X = 5.0 MHz

(3) Carrier generator output control register 40 (TCA40)

This register is used to set the timer output data in the carrier generator mode.

TCA40 is set using an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets this register to 00H.

Figure 5-15. Format of Carrier Generator Output Control Register 40

Symbol	7	6	5	4	3	<2>	<1>	<0>	Address	After reset	R/W
TCA40	0	0	0	0	0	RMC40	NRZB40	NRZ40	FF6AH	00H	W

RMC40	Remote controller output control
0	When NRZ40 = 1, a carrier pulse is output to the TO40/P60 pin
1	When NRZ40 = 1, a high level is output to the TO40/P60 pin

NRZB40	This bit stores the data that NRZ40 will output next. Data is transferred to NRZ40 upon the generation of a timer 30 match signal.

NRZ40	No return, zero data
0	A low level is output (the carrier clock is stopped)
1	A carrier pulse or high level is output

Caution TCA40 cannot be set using a 1-bit memory manipulation instruction.
Be sure to use an 8-bit memory manipulation instruction.

(4) Port mode register 6 (PM6)

This register is used to set port 6 to input or output in 1-bit units.

When the TO40/P60 pin is used as a timer output, set the PM60 and P60 output latches to 0.

PM6 is set using a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets this register to FFH.

Figure 5-16. Format of Port Mode Register 6

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM6	1	1	1	1	1	1	PM61	PM60	FF26H	FFH	R/W

PM6n	Input/output mode of pin P6n (n = 0, 1)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

5.4 Watch Timer

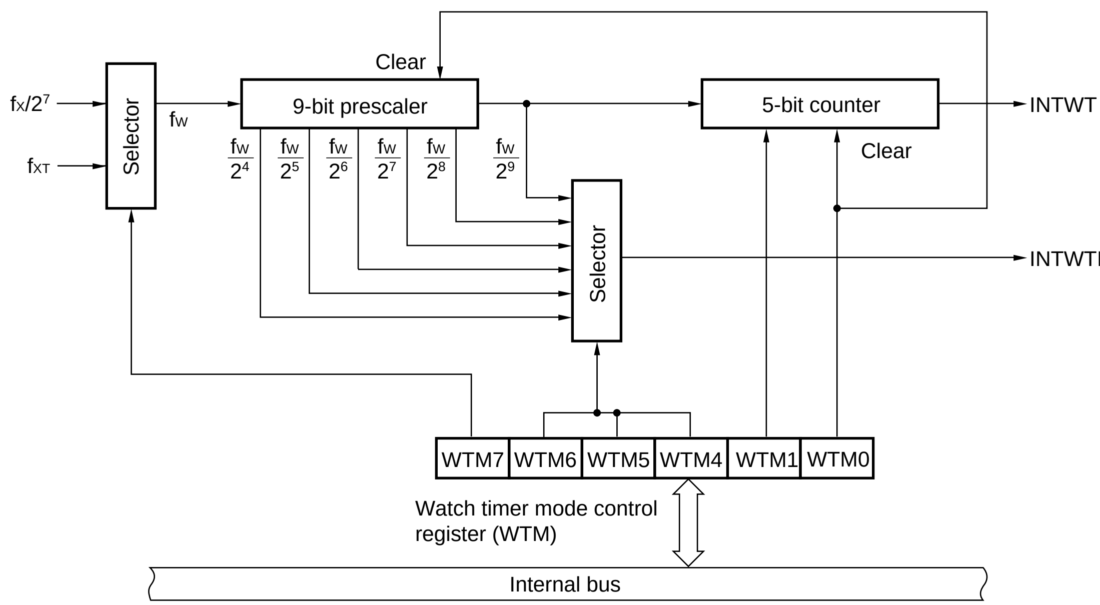
5.4.1 Watch timer functions

The watch timer has the following functions.

- Watch timer
- Interval timer

The watch and interval timers can be used at the same time.
Figure 5-17 shows a block diagram of the watch timer.

Figure 5-17. Watch Timer Block Diagram



(1) Watch timer

An interrupt request (INTWT) is generated at 0.5-second intervals using the 4.19 MHz main system clock or 32.768 kHz subsystem clock.

Caution When the main system clock is operating at 5.0 MHz, it cannot be used to generate a 0.5-second interval. In this case, the subsystem clock, which operates at 32.768 kHz, should be used instead.

(2) Interval timer

The interval timer is used to generate an interrupt request (INTWTI) at preset intervals.

Table 5-7. Interval Time of Interval Timer

Interval Time	At f_X = 5.0 MHz Operation	At f_X = 4.19 MHz Operation	At f_{XT} = 32.768 kHz Operation
$2^4 \times 1/f_W$	409.6 μs	488 μs	488 μs
$2^5 \times 1/f_W$	819.2 μs	977 μs	977 μs
$2^6 \times 1/f_W$	1.64 ms	1.95 ms	1.95 ms
$2^7 \times 1/f_W$	3.28 ms	3.91 ms	3.91 ms
$2^8 \times 1/f_W$	6.55 ms	7.81 ms	7.81 ms
$2^9 \times 1/f_W$	13.1 ms	15.6 ms	15.6 ms

Remarks 1. f_W: Watch timer clock frequency ($f_X/2^7$ or f_{XT})

2. f_X: Main system clock oscillation frequency

3. f_{XT}: Subsystem clock oscillation frequency

5.4.2 Watch timer configuration

The watch timer consists of the following hardware.

Table 5-8. Watch Timer Configuration

Item	Configuration
Counter	5 bits × 1
Prescaler	9 bits × 1
Control register	Watch timer mode control register (WTM)

5.4.3 Watch timer control register

The following register controls the watch timer.

- Watch timer mode control register (WTM)

(1) Watch timer mode control register (WTM)

This register is used to enable/disable the count clock and operation of the watch timer and set the interval time of the prescaler and operation control of the 5-bit counter.

WTM is set using a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets this register to 00H.

Figure 5-18. Format of Watch Timer Mode Control Register

Symbol	7	6	5	4	3	2	<1>	<0>	Address	After reset	R/W
WTM	WTM7	WTM6	WTM5	WTM4	0	0	WTM1	WTM0	FF4AH	00H	R/W

WTM7	Watch timer count clock (f_W) selection
0	$f_X/2^7$ (39.1 kHz)
1	f_{XT} (32.768 kHz)

WTM6	WTM5	WTM4	Prescaler interval time selection
0	0	0	$2^4/f_W$
0	0	1	$2^5/f_W$
0	1	0	$2^6/f_W$
0	1	1	$2^7/f_W$
1	0	0	$2^8/f_W$
1	0	1	$2^9/f_W$
Other than above			Setting prohibited

WTM1	5-bit counter operation control
0	Cleared after operation stopped
1	Start

WTM0	Watch timer operation enable
0	Operation stopped (both prescaler and timer cleared)
1	Operation enabled

Remarks 1. f_W: Watch timer clock frequency ($f_X/2^7$ or f_{XT})

2. f_X: Main system clock oscillation frequency

3. f_{XT}: Subsystem clock oscillation frequency

4. The parenthesized values apply to operation at f_X = 5.0 MHz or f_{XT} = 32.768 kHz.

5.5 Watchdog Timer

5.5.1 Watchdog timer functions

The watchdog timer has the following functions.

(1) Watchdog timer

The watchdog timer is used to detect a program runaway. If a runaway is detected, either a non-maskable interrupt or the $\overline{\text{RESET}}$ signal can be generated.

(2) Interval timer

The interval timer is used to generate interrupts at preset intervals.

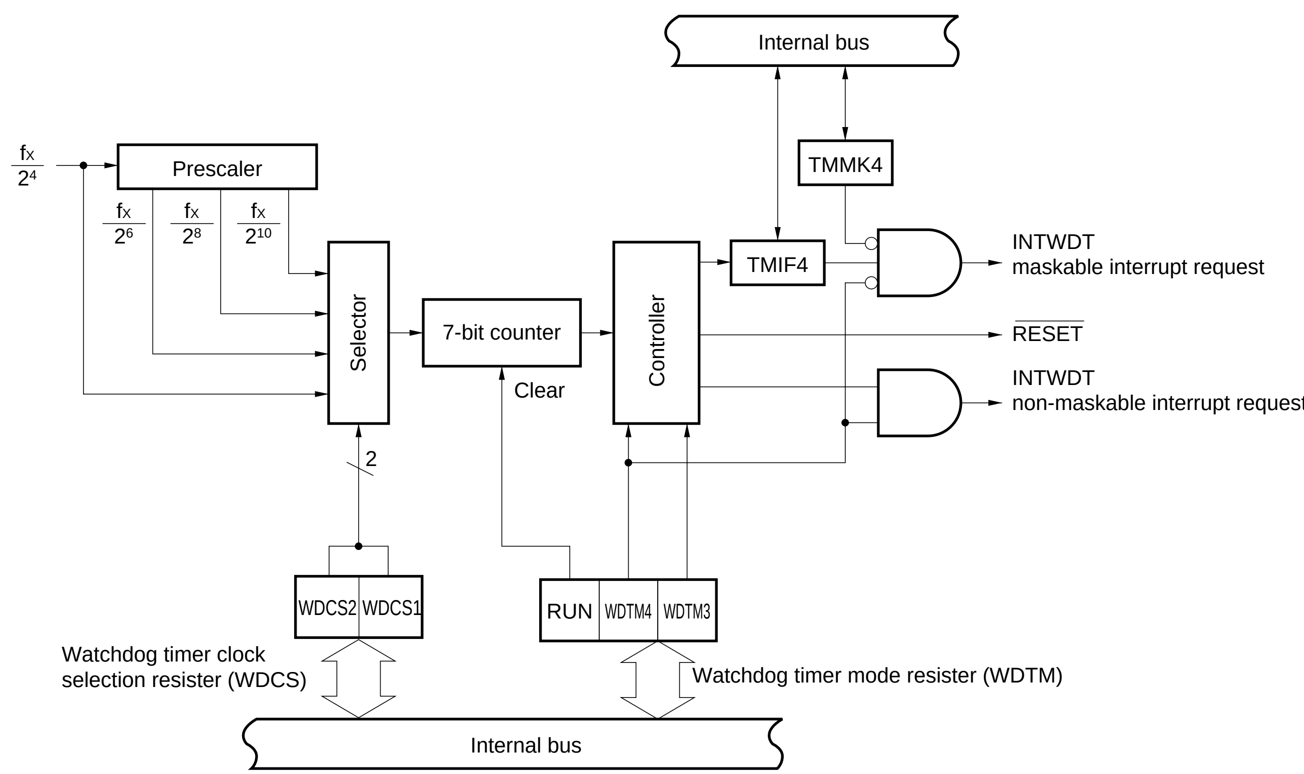
5.5.2 Watchdog timer configuration

The watchdog timer consists of the following hardware.

Table 5-9. Watchdog Timer Configuration

Item	Configuration
Control register	Watchdog timer clock selection resister (WDCS) Watchdog timer mode register (WDTM)

Figure 5-19. Watchdog Timer Block Diagram



5.5.3 Watchdog timer control register

The watchdog timer is controlled by the following registers.

- Watchdog timer clock selection resister (WDCS)
- Watchdog timer mode register (WDTM)

(1) Watchdog timer clock selection register (WDCS)

This register is used to set the count clock of the watchdog timer.

WDCS is set using an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets this register to 00H.

Figure 5-20. Format of Watchdog Timer Clock Selection Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
WDCS	0	0	0	0	0	WDCS2	WDCS1	0	FF42H	00H	R/W

WDCS2	WDCS1	Wachdog timer count clock selection	Interval time
0	0	$f_X/2^4$ (312.5 kHz)	$2^{11}/f_X$ (410 μs)
0	1	$f_X/2^6$ (78.1 kHz)	$2^{13}/f_X$ (1.64 ms)
1	0	$f_X/2^8$ (19.5 kHz)	$2^{15}/f_X$ (6.55 ms)
1	1	$f_X/2^{10}$ (4.88 kHz)	$2^{17}/f_X$ (26.2 ms)
Other than above		Setting prohibited	

Remarks 1. fx: System clock oscillation frequency

2. The parenthesized values apply to operation at fx = 5.0 MHz.

(2) Watchdog timer mode register (WDTM)

This register is used to set the watchdog timer operation mode and whether to enable or disable counting.
WDTM is set using a 1-bit or 8-bit memory manipulation instruction.
$\overline{\text{RESET}}$ input sets this register to 00H.

Figure 5-21. Format of Watchdog Timer Mode Register

Symbol	<7>	6	5	4	3	2	1	0	Address	After reset	R/W
WDTM	RUN	0	0	WDTM4	WDTM3	0	0	0	FFF9H	00H	R/W

RUN	Watchdog timer operation selection[Note 1]
0	Counting stopped
1	Counter cleared and counting starts

WDTM4	WDTM3	Watchdog timer operation mode selection[Note 2]
0	0	Operation stopped
0	1	Interval timer mode (when an overflow occurs, a maskable interrupt is generated)[Note 3]
1	0	Watchdog timer mode 1 (when an overflow occurs, a non-maskable interrupt is generated)
1	1	Watchdog timer mode 2 (when an overflow occurs, a reset operation is activated)

Notes 1. Once RUN is set (1), it is impossible to clear it (0) by software. Consequently, once counting begins, it cannot be stopped by any means other than $\overline{\text{RESET}}$ input.

2. Once WDTM3 and WDTM4 are set (1), it is impossible to clear them (0) by software.

3. The interval timer starts operating as soon as RUN is set to 1.

Cautions 1. When RUN is set to 1, and the watchdog timer is cleared, the actual overflow time will be up to 0.8% shorter than the time specified by the watchdog timer clock selection register.

2. To use watchdog timer mode 1 or 2, be sure to set WDTM4 to 1 after confirming that WDTIF (bit 0 of interrupt request flag 0 (IF0)) has been set to 0. If WDTIF is 1, selecting watchdog timer mode 1 or 2 causes a non-maskable interrupt to be generated the instant rewriting ends.

5.6 A/D Converter

5.6.1 A/D converter function

The A/D converter converts analog inputs into digital values with 8-bit resolution and is configured so as to enable control of one analog input channel (ANI0).

An A/D conversion operation can only be started via a software start.

A/D conversion is repeated, with an interrupt request (INTAD0) generated at the completion of each A/D conversion operation.

Caution A/D conversion is stopped in the STOP mode.

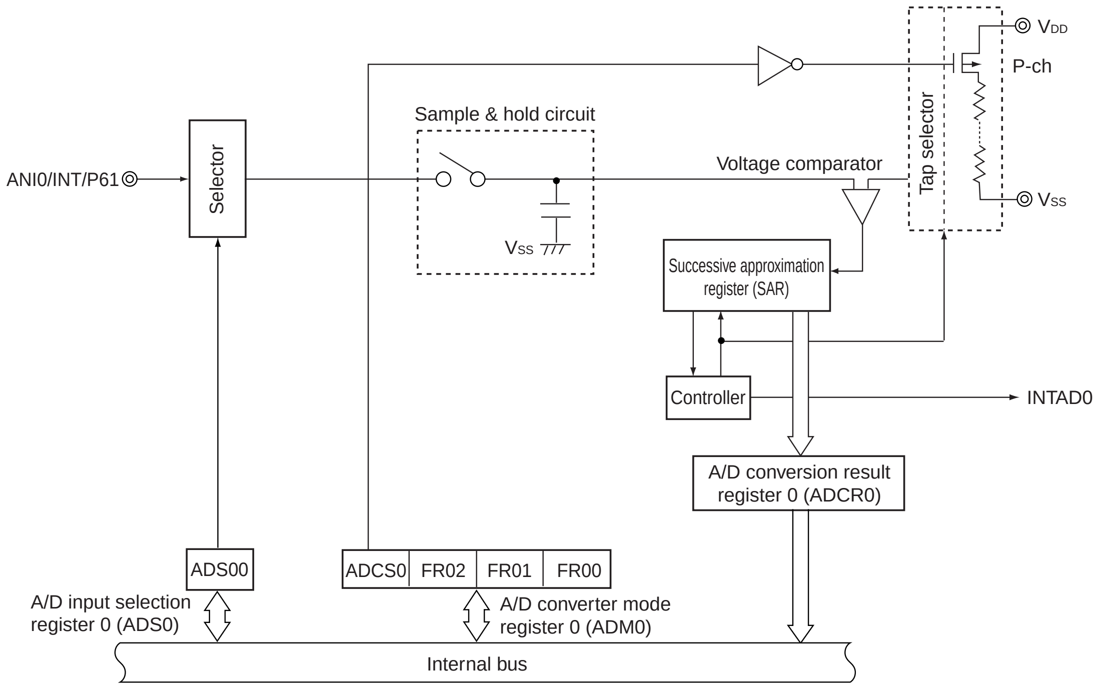
5.6.2 A/D converter configuration

The A/D converter consists of the following hardware.

Table 5-10. A/D Converter Configuration

Item	Configuration
Analog inputs	1 channel (ANI0)
Registers	Successive approximation register (SAR) A/D conversion result register 0 (ADCR0)
Control registers	A/D converter mode register 0 (ADM0) A/D input selection register 0 (ADS0)

Figure 5-22. A/D Converter Block Diagram



(1) Successive approximation register (SAR)

The SAR holds the result of comparing an analog input voltage and a voltage at a voltage tap (comparison voltage), received from the series resistor string, starting from the most significant bit (MSB).

Upon receiving all the bits down to the least significant bit (LSB) (end of A/D conversion), the SAR transfers its contents to A/D conversion result register.

(2) A/D conversion result register 0 (ADCR0)

ADCR0 holds the result of A/D conversion. Each time A/D conversion ends, the conversion result in the successive approximation register is loaded into ADCR0.

ADCR0 can be read with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input makes this register undefined.

(3) Sample-and-hold circuit

The sample-and-hold circuit samples consecutive analog inputs from the input circuit, one by one, and sends them to the voltage comparator. The sampled analog input voltage is held during A/D conversion.

(4) Voltage comparator

The voltage comparator compares an analog input with the voltage output by the series resistor string.

(5) Series resistor string

The series resistor string is configured between V_{DD} and V_{SS}. It generates the reference voltages against which analog inputs are compared.

(6) ANI0 pin

The ANI0 pin is a 1-channel analog input pin for the A/D converter. It is used to receive the analog signals for A/D conversion.

5.6.3 A/D converter control registers

The following two registers are used to control the A/D converter.

- A/D converter mode register 0 (ADM0)
- A/D input selection register 0 (ADS0)

(1) A/D converter mode register 0 (ADM0)

ADM0 is used to set the conversion time for analog inputs to be A/D converted and to start and stop A/D conversion.

ADM0 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets ADM0 to 00H.

Figure 5-23. Format of A/D Converter Mode Register 0

Symbol	<7>	6	5	4	3	2	1	0	Address	After reset	R/W
ADM0	ADCS0	0	FR02	FR01	FR00	0	0	0	FF80H	00H	R/W

ADCS0	A/D conversion control
0	A/D conversion stopped
1	A/D conversion enabled

FR02	FR01	FR00	A/D conversion time selection[Note 1]
0	0	0	72/fx (14.4 μs)
0	0	1	60/fx (setting prohibited[Note 2])
0	1	0	48/fx (setting prohibited[Note 2])
1	0	0	144/fx (28.8 μs)
1	0	1	120/fx (24 μs)
1	1	0	96/fx (19.2 μs)
Other than above			Setting prohibited

Notes 1. The specifications of FR02, FR01, and FR00 must be such that the A/D conversion time is at least 14 μs.

2. These bit combinations must not be used, as the A/D conversion time will fall below 14 μs.

Cautions 1. The result of conversion performed immediately after bit 7 (ADCS0) is set is undefined.

2. The result of conversion performed after the ADCS0 is cleared may become undefined. When reading the result of conversion, read it during A/D conversion. If reading the result of conversion after stopping A/D conversion, stop A/D conversion and then read the result between completion of A/D conversion and starting the next A/D conversion.

3. Always set bits 0 to 2 and bit 6 to 0.

Remarks 1. fx: Main system clock oscillation frequency

2. The parenthesized values apply to operation at fx = 5.0 MHz.

(2) A/D input selection register 0 (ADS0)

ADS0 specifies the port used to input the analog voltage to be A/D converted.

ADS0 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets ADS0 to 00H.

Figure 5-24. Format of A/D Input Selection Register 0

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
ADS0	0	0	0	0	0	0	0	ADS00	FF84H	00H	R/W

ADS00	Port function of P61
0	Operates as P61(general-purpose port pin) or INT (external interrupt pin)
1	Operates as ANI0 (analog input pin). External interrupts are prohibited.

Caution　Always set bits 1 to 7 to 0.

5.7 LCD Controller/Driver

5.7.1 LCD controller/driver functions

The LCD controller/driver incorporated in the μPD78F9468 has the following features.

(1) Segment and common signals based on the automatic reading of the display data memory can be automatically output
(2) Four types of frame frequencies are selectable
(3) 23 segment signal outputs (S0 to S22), 4 common signal outputs (COM0 to COM3)
(4) Operation with the subsystem clock is possible
(5) A voltage amplifier is incorporated

The maximum number of displayable pixels is shown in Table 5-11 below.

Table 5-11. Maximum Number of Display Pixels

Bias Method	Time Division	Common Signals Used	Maximum Number of Display Pixels
1/3	4	COM0 to COM3	92 (23 segments × 4 commons)[Note]

Note The LCD panel of the figure 8. consists of 11 rows with 2 segments per row.

5.7.2 LCD controller/driver configuration

The LCD controller/driver consists of the following hardware.

Table 5-12. Configuration of LCD Controller/Driver

Item	Configuration
Display outputs	Segment signals: 23 Common signals: 4
Control registers	LCD display mode register 0 (LCDM0) LCD clock control register 0 (LCDC0) LCD voltage amplification control register 0 (LCDVA0) Port function register 8 (PF8)

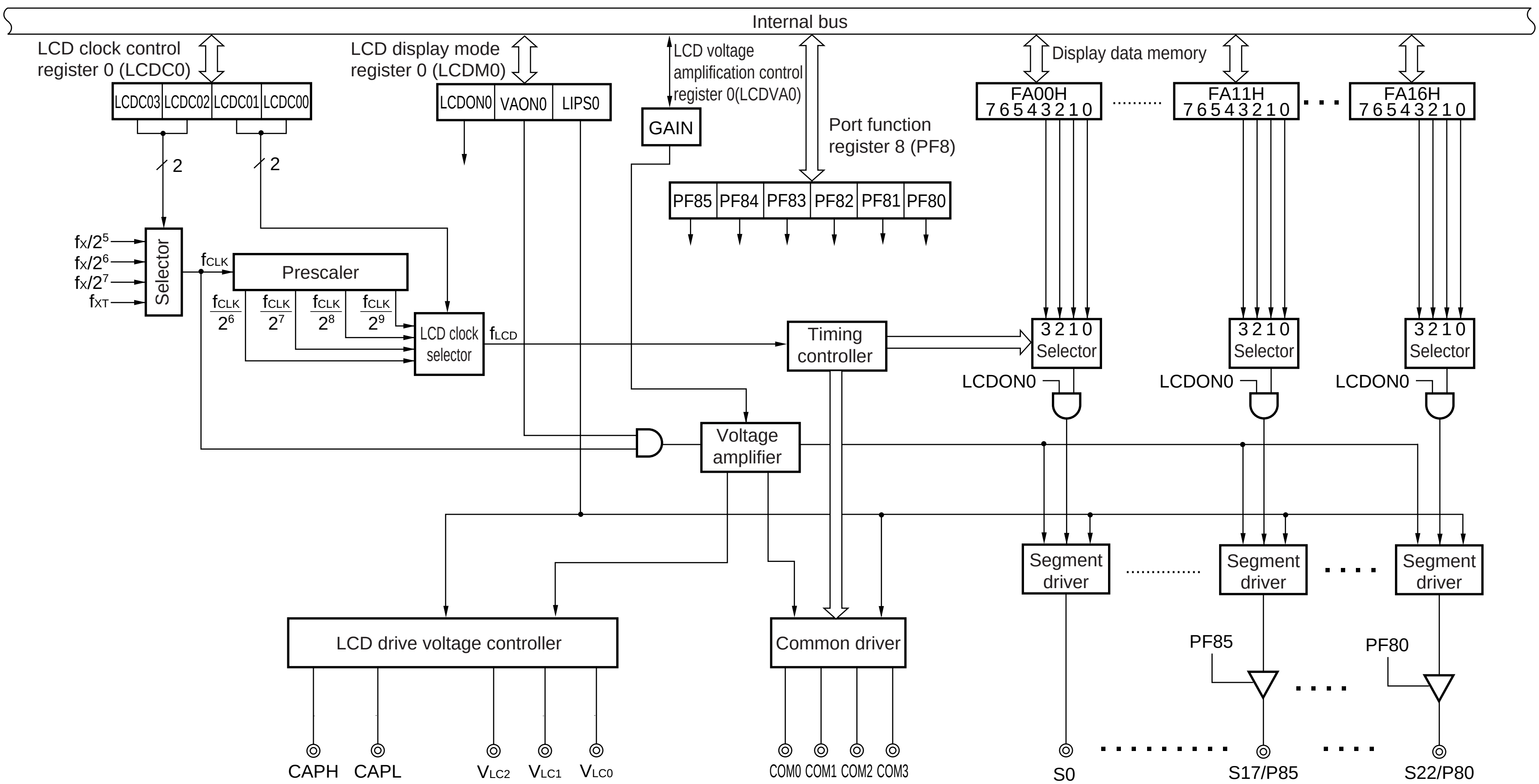
The correspondence with the LCD display RAM is shown in Figure 5-25 below.

Figure 5-25. Correspondence with LCD Display RAM

Address	Bit 7	6	5	4	3	2	1	0	Segment
FA16H	0	0	0	0					→ S22
FA15H	0	0	0	0					→ S21
FA14H	0	0	0	0					→ S20
FA13H	0	0	0	0					→ S19
FA12H	0	0	0	0					→ S18
FA11H	0	0	0	0					→ S17
FA10H	0	0	0	0					→ S16
FA0FH	0	0	0	0					→ S15
FA0EH	0	0	0	0					→ S14
FA0DH	0	0	0	0					→ S13
FA0CH	0	0	0	0					→ S12
FA0BH	0	0	0	0					→ S11
FA0AH	0	0	0	0					→ S10
FA09H	0	0	0	0					→ S9
FA08H	0	0	0	0					→ S8
FA07H	0	0	0	0					→ S7
FA06H	0	0	0	0					→ S6
FA05H	0	0	0	0					→ S5
FA04H	0	0	0	0					→ S4
FA03H	0	0	0	0					→ S3
FA02H	0	0	0	0					→ S2
FA01H	0	0	0	0					→ S1
FA00H	0	0	0	0					→ S0
				Common	↑ COM3	↑ COM2	↑ COM1	↑ COM0	

Remark Bits 4 to 7 are fixed to 0.

Figure 5-26. LCD Controller/Driver Block Diagram



5.7.3 LCD controller/driver control registers

The LCD controller/driver is controlled by the following four registers.

- LCD display mode register 0 (LCDM0)
- LCD clock control register 0 (LCDC0)
- LCD voltage amplification control register 0 (LCDVA0)
- Port function register 8 (PF8)

(1) LCD display mode register 0 (LCDM0)

This register is used to enable/disable operation, and set the operation mode and the supply of power for LCD drive.

LCDM0 is set using a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets this register to 00H.

Figure 5-27. Format of LCD Display Mode Register 0

Symbol	<7>	<6>	5	<4>	3	2	1	0	Address	After reset	R/W
LCDM0	LCDON0	VAON0	0	LIPS0	0	0	0	0	FFB0H	00H	R/W

LCDON0	LCD display enable/disable
0	Display off (all segment outputs are unselected for signal output)
1	Display on

VAON0	LCD controller/driver operation mode Note
0	No internal voltage amplification
1	Internal voltage amplification enabled

LIPS0	Supply of power for LCD drive Note
0	Power not supplied for LCD drive
1	Power supplied for LCD drive

Note To reduce power consumption when the LCD display is not being used, set VAON0 and LIPS0 to 0.

Cautions 1. Always set bits 0 to 3 and 5 to 0.

2. To manipulate VAON0, follow the procedure described below.

A. When stopping voltage amplification after turning the LCD display off:

1) Turn off the LCD display by setting LCDON0 to 0.

2) Set all segment buffers and common buffers to output-disabled by setting LIPS0 to 0.

3) Stop voltage amplification by setting VAON0 to 0.

B. When stopping voltage amplification while the LCD display is on:

Setting is prohibited. Be sure to stop voltage amplification after turning off the LCD display.

C. When turning on the LCD display after voltage amplification has been stopped:

1) Wait about 500 ms after starting voltage amplification by setting VAON0 to 1.

2) Set all segment buffers and common buffers to a non-display output state by setting LIPS0 to 1.

3) Turn on the LCD display by setting LCDON0 to 1.

(2) LCD clock control register (LCDC0)

This register is used to set the internal and LCD clocks. The frame frequency is determined by the number of LCD clock time divisions.

LCDC0 is set using a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets this register to 00H.

Figure 5-28. Format of LCD Clock Control Register 0

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
LCDC0	0	0	0	0	LCDC03	LCDC02	LCDC01	LCDC00	FFB2H	00H	R/W

LCDC03	LCDC02	Internal clock (f_{CLK}) selection[Note]
0	0	f_{XT} (32.768 kHz)
0	1	$f_X/2^5$ (156.3 kHz)
1	0	$f_X/2^6$ (78.1 kHz)
1	1	$f_X/2^7$ (39.1 kHz)

LCDC01	LCDC00	LCD clock (f_{LCD}) selection
0	0	$f_{CLK}/2^6$
0	1	$f_{CLK}/2^7$
1	0	$f_{CLK}/2^8$
1	1	$f_{CLK}/2^9$

Note Select a clock of at least 32 kHz for the internal clock (f_{CLK}).

Remarks 1. f_X: Main system clock oscillation frequency

2. f_{XT}: Subsystem clock oscillation frequency

3. The parenthesized values apply to operation at f_X = 5.0 MHz or f_{XT} = 32.768 kHz

Cautions 1. Always set bits 4 to 7 to 0.

2. Be sure to change the LCDC0 setting after setting VAON0 to 0.

Examples of the frame frequencies when the internal clock (f_{CLK}) is connected to f_{XT} (32.768 kHz) are shown in Table 5-13 below.

Caution Set the frame frequency to 128 Hz or below.

Table 5-13. Frame Frequency (Hz)

LCD Clock (f_{LCD}) / Time Divisions	$f_{XT}/2^9$ (64 Hz)	$f_{XT}/2^8$ (128 Hz)	$f_{XT}/2^7$ (256 Hz)	$f_{XT}/2^6$ (512 Hz)
4	16	32	64	128

(3) LCD voltage amplification control register 0 (LCDVA0)

This register is used to select the voltage amplification level when the voltage amplifier is operating.

LCDVA0 is set using a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets this register to 00H.

Figure 5-29. Format of LCD Voltage Amplification Control Register 0

Symbol	7	6	5	4	3	2	1	<0>	Address	After reset	R/W
LCDVA0	0	0	0	0	0	0	0	GAIN	FFB3H	00H	R/W

GAIN	Selection of voltage amplification level[Note]
0	1.5 times (when using a 4.5 V specification panel)
1	1.0 times (when using a 3 V specification panel)

Note Switch the level based on the specification of the panel used.

Caution Be sure to change the LCDVA0 setting after setting VAON0 to 0.

(4) Port function register 8 (PF8)

This register is used to select whether S17/P85 to S22/P80 are used as LCD segment signal outputs or general-purpose ports.

PF8 is set using a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets this register to 00H.

Figure 5-30. Format of Port Function Register 8

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PF8	0	0	PF85	PF84	PF83	PF82	PF81	PF80	FF58H	00H	R/W

PF8n	Port function of P8n (n = 0 to 5)
0	Operates as a general-purpose port
1	Operates as an LCD segment signal output

6. INTERRUPT FUNCTION

6.1 Interrupt Types

Two types of interrupts are supported.

(1) Non-maskable interrupts

Non-maskable interrupt requests are acknowledged unconditionally, i.e. even when interrupts are disabled. These interrupts take precedence over all other interrupts and are not subject to interrupt priority control.
A non-maskable interrupt causes the generation of the standby release signal.
An interrupt from the watchdog timer is the only non-maskable interrupt source.

(2) Maskable interrupts

Maskable interrupts are subject to mask control. If two or more maskable interrupts occur simultaneously, the default priority listed in Table 6-1 applies.
A maskable interrupt causes the generation of the standby release signal.
There are maskable interrupts from 2 external and 6 internal sources.

6.2 Interrupt Sources and Configuration

There are a total of 9 maskable and non-maskable interrupt sources (see **Table 6-1**).

Table 6-1. Interrupt Sources

Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Non-maskable	–	INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer mode selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTAD0	Signal indicating end of A/D conversion	Internal	0008H	(B)
	3	INTWT	Watch timer interrupt		000AH	
	4	INTTM30	Generation of 8-bit timer 30 match signal		000CH	
	5	INTTM40	Generation of 8-bit timer 40 match signal		000EH	
	6	INTKR00	Key return signal detection	External	0010H	(C)
	7	INTWTI	Watch timer interval timer interrupt	Internal	0012H	(B)

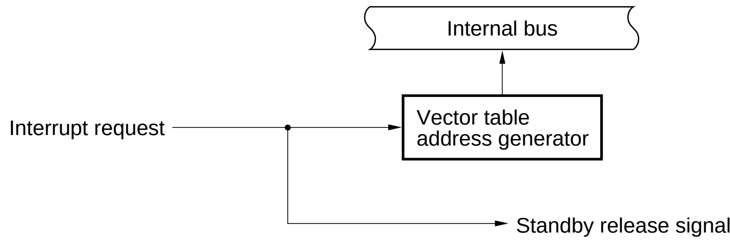
Notes 1. Default priority is the priority order when more than one maskable interrupt request is generated at the same time. 0 is the highest priority and 7 is the lowest.

2. Basic configuration types (A), (B), and (C) correspond to (A), (B), and (C) in **Figure 6-1**.

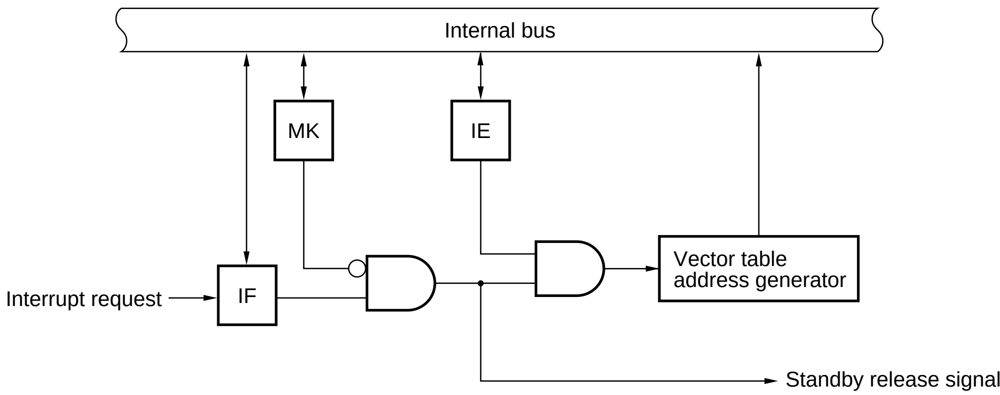
Remark Only one of the two watchdog timer interrupt sources (INTWDT), non-maskable or maskable (internal), can be selected.

Figure 6-1. Basic Configuration of Interrupt Function

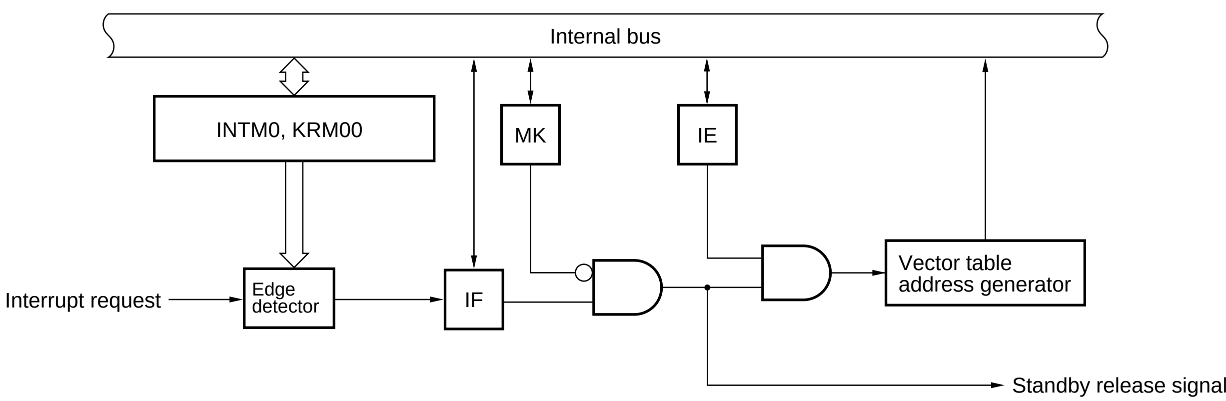
(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt



INTM0: External interrupt mode register 0
KRM00: Key return mode register 00
IF: Interrupt request flag
IE: Interrupt enable flag
MK: Interrupt mask flag

6.3 Interrupt Function Control Registers

Interrupts are controlled by the following five registers.

- Interrupt request flag register 0 (IF0)
- Interrupt mask flag register 0 (MK0)
- External interrupt mode register 0 (INTM0)
- Program status word (PSW)
- Key return mode register 00 (KRM00)

Table 6-2 lists the interrupt requests and the corresponding interrupt request and interrupt mask flags.

Table 6-2. Interrupt Request Signals and Corresponding Flags

Interrupt Request Signal	Interrupt Request Flag	Interrupt Mask Flag
INTWDT	WDTIF	WDTMK
INTP0	PIF0	PMK0
INTAD0	ADIF0	ADMK0
INTWT	WTIF	WTMK
INTTM30	TMIF30	TMMK30
INTTM40	TMIF40	TMMK40
INTKR00	KRIF00	KRMK00
INTWTI	WTIIF	WTIMK

(1) Interrupt request flag register 0 (IF0)

An interrupt request flag is set (1) when the corresponding interrupt request is generated, or when an instruction is executed. It is cleared (0) when the interrupt request is acknowledged, when the $\overline{\text{RESET}}$ signal is input, or when an instruction is executed.

IF0 is set using a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets this register to 00H.

Figure 6-2. Format of Interrupt Request Flag Register 0

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After reset	R/W
IF0	WTIIF	KRIF00	TMIF40	TMIF30	WTIF	ADIF0	PIF0	WDTIF	FFE0H	00H	R/W

××IF×	Interrupt request flag
0	No interrupt request signal generated
1	An interrupt request signal is generated and an interrupt request made

Cautions 1. The WDTIF flag can be read/written only when the watchdog timer is being used as an interval timer. It must be cleared to 0 if the watchdog timer is used in watchdog timer mode 1 or 2.

2. Because P61 functions alternately as an external interrupt, when the output level changes after the output mode of the port function is specified, the interrupt request flag will be inadvertently set. Therefore, be sure to preset the interrupt mask flag (PMK0) before using the port in output mode.

(2) Interrupt mask flag register 0 (MK0)

Interrupt mask flags are used to enable and disable the corresponding maskable interrupts.

MK0 is set using a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets this register to FFH.

Figure 6-3. Format of Interrupt Mask Flag Register 0

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After reset	R/W
MK0	WTIMK	KRMK00	TMMK40	TMMK30	WTMK	ADMK0	PMK0	WDTMK	FFE4H	FFH	R/W

××MK	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Cautions 1. When the watchdog timer is being used in watchdog timer mode 1 or 2, any attempt to read the WDTMK flag results in an undefined value being detected.

2. Because P61 functions alternately as an external interrupt, when the output level changes after the output mode of the port function is specified, the interrupt request flag will be inadvertently set. Therefore, be sure to preset the interrupt mask flag (PMK0) before using the port in output mode.

(3) External interrupt mode register 0 (INTM0)

This register is used to specify the valid edge for INTP0.

INTM0 is set using an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets this register to 00H.

Figure 6-4. Format of External Interrupt Mode Register 0

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
INTM0	0	0	0	0	ES01	ES00	0	0	FFECH	00H	R/W

ES01	ES00	INTP0 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

Cautions 1. Always set bits 0, 1, and 4 to 7 to 0.

2. Before setting INTM0, set (1) the interrupt mask flag (PMK0) to disable interrupts. To enable interrupts, clear (0) the interrupt request flag (PIF0), then clear (0) the interrupt mask flag (PMK0).

(4) Program status word (PSW)

The program status word is used to hold the instruction execution results and the current status of the interrupt requests. The IE flag, used to enable and disable maskable interrupts, is mapped to the PSW.

The PSW can be read and written in 8-bit units, as well as in 1-bit units by using bit manipulation instructions and dedicated instructions (EI and DI). When a vectored interrupt is acknowledged, the PSW is automatically saved to the stack, and the IE flag is reset (0).

$\overline{\text{RESET}}$ input sets the PSW to 02H.

Figure 6-5. Program Status Word Configuration

Symbol	7	6	5	4	3	2	1	0	After reset
PSW	IE	Z	0	AC	0	0	1	CY	02H

Used in the execution of ordinary instructions

IE	Interrupt acknowledgement enable/disable
0	Disabled
1	Enabled

(5) Key return mode register 00 (KRM00)

This register is used to set the pin that is to detect the key return signal (rising edge of port 4).
KRM00 is set using a 1-bit or 8-bit memory manipulation instruction.
RESET input sets this register to 00H.

Figure 6-6. Format of Key Return Mode Register 00

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
KRM00	0	0	0	0	0	0	0	KRM000	FFF5H	00H	R/W

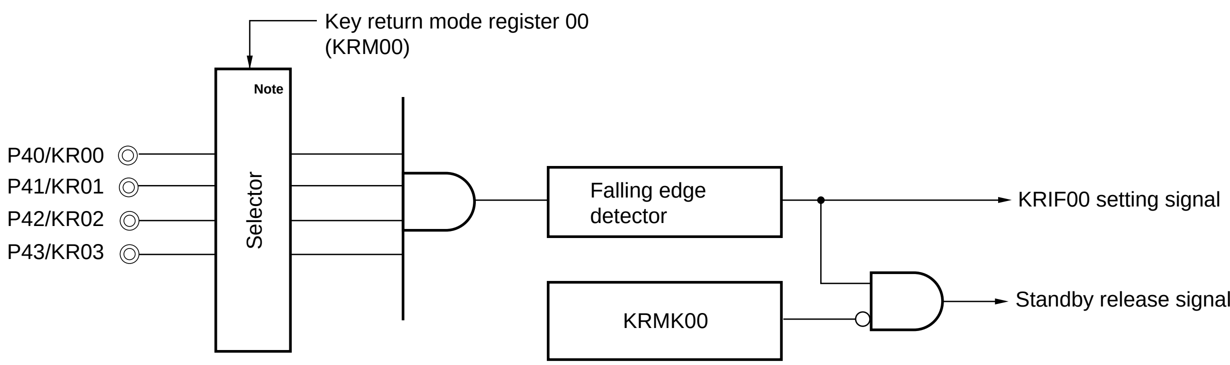
KRM000	Key return signal detection control
0	Key return signal not detected
1	Key return signal detected (port 4 falling edge detection)

Cautions 1. Always set bits 1 to 7 to 0.

2. Before setting KRM00, set (1) bit 6 of MK0 (KRMK00) to disable interrupts. To enable interrupts, clear (0) KRMK00 after clearing (0) bit 6 of IF0 (KRIF00).

3. On-chip pull-up resistors are automatically connected in input mode to the pins specified for key return signal detection (P40 to P43). Although these resistors are disconnected when the mode changes to output, key return signal detection continues unchanged.

Figure 6-7. Block Diagram of Falling Edge Detector



Note For selecting the pin to be used as falling edge input.

7. STANDBY FUNCTION

7.1 Standby Function

A standby function is incorporated to minimize the system's power consumption. There are two standby modes: HALT and STOP.

The HALT and STOP modes are selected using the HALT and STOP instructions.

(1) HALT mode

In this mode, the CPU operating clock is stopped. The average current consumption can be reduced by intermittent operation combining this mode with the normal operation mode.

(2) STOP mode

In this mode, main system clock oscillation is stopped. All operations performed with the main system clock are suspended, thus minimizing power consumption.

Caution When shifting to STOP mode, execute the STOP instruction after first stopping the operation of the hardware.

Table 7-1. Operation Statuses in HALT Mode

Item	HALT Mode Operation Status During Main System Clock Operation		HALT Mode Operation Status During Subsystem Clock Operation	
	Subsystem Clock Operating	Subsystem Clock Stopped	Main System Clock Operating	Main System Clock Stopped
Main system clock	Can be oscillated			Oscillation stopped
CPU	Operation stopped			
Ports (output latches)	Status before HALT mode setting retained			
8-bit timer 30, 40	Operable			Operation stopped
Watch timer	Operable	Operable[Note 1]	Operable	Operable[Note 2]
Watchdog timer	Operable		Operation stopped	
Power-on-clear circuit	Operable			
Key return circuit	Operable			
A/D converter	Operable			Operation stopped
LCD controller/driver	Operable[Note 3]	Operable[Notes 1, 3]	Operable[Note 3]	Operable[Notes 2, 3]
External interrupts	Operable[Note 4]			

Notes 1. Operation is enabled when the main system clock is selected
2. Operation is enabled when the subsystem clock is selected
3. The HALT instruction can be set after display instruction execution
4. Operation is enabled only for a maskable interrupt that is not masked

Table 7-2. Operation Statuses in STOP Mode

Item	STOP Mode Operation Status During Main System Clock Operation	
	Subsystem Clock Operating	Subsystem Clock Stopped
Main system clock	Oscillation stopped	
CPU	Operation stopped	
Ports (output latches)	Status before STOP mode setting retained	
8-bit timer 30, 40	Operation stopped	
Watch timer	Operable[Note 1]	Operation stopped
Watchdog timer	Operation stopped	
Power-on-clear circuit	Operable	
Key return circuit	Operable	
A/D converter	Operation stopped	
LCD controller/driver	Operable[Note 1]	Operation stopped
External interrupts	Operable[Note 2]	

Notes 1. Operation is enabled when the subsystem clock is selected.
2. Operation is enabled only for a maskable interrupt that is not masked

7.2 Standby Function Control Register

The oscillation stabilization time selection register (OSTS) is used to control the wait time from the time STOP mode is released by an interrupt request until oscillation stabilizes.

OSTS is set using an 8-bit memory manipulation instruction.

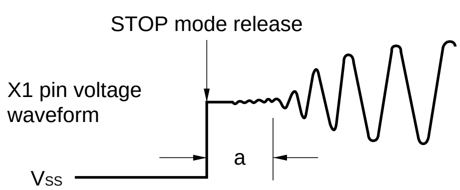
$\overline{\text{RESET}}$ input sets this register to 04H. Note that the time required for oscillation to stabilize after $\overline{\text{RESET}}$ input will be $2^{15}/f_X$, rather than $2^{17}/f_X$.

Figure 7-1. Format of Oscillation Stabilization Time Selection Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0	FFFAH	04H	R/W

OSTS2	OSTS1	OSTS0	Oscillation stabilization time selection
0	0	0	$2^{12}/f_X$ (819 μs)
0	1	0	$2^{15}/f_X$ (6.55 ms)
1	0	0	$2^{17}/f_X$ (26.2 ms)
Other than above			Setting prohibited

Caution The wait time required after releasing STOP mode does not include the time (“a” in the following figure) required for the clock oscillation to restart after STOP mode is released, regardless of whether STOP mode is released by $\overline{\text{RESET}}$ input or interrupt.



Remarks 1. f_X: Main system clock oscillation frequency

2. The parenthesized values apply to operation at f_X = 5.0 MHz.

8. RESET FUNCTION

8.1 Reset Function

The μPD789462, 789464, 789466, and 789467 can be reset using the following three signals.

(1) External reset signal input via $\overline{\text{RESET}}$ pin
(2) Internal reset by watchdog timer runaway time detection
(3) Internal reset using power-on-clear circuit (POC)Note

The external and internal reset signals are functionally equivalent. When $\overline{\text{RESET}}$ is input, program execution begins from the addresses written at addresses 0000H and 0001H.

If a low-level signal is applied to the $\overline{\text{RESET}}$ pin, or if the watchdog timer overflows, a reset occurs, causing each item of the hardware to enter the states listed in Table 8-1. While a reset is being applied, or while the oscillation frequency is stabilizing immediately after the end of a reset sequence, each pin remains in the high-impedance state.

If a high-level signal is applied to the $\overline{\text{RESET}}$ pin, the reset sequence is terminated, and program execution begins once the oscillation stabilization time ($2^{15}/f_X$) has elapsed. A reset sequence caused by a watchdog timer overflow is terminated automatically and again program execution begins upon the elapse of the oscillation stabilization time ($2^{15}/f_X$). A reset sequence caused by a power-on-clear (POC)Note is terminated after the power supply has reached a certain voltage level, and program execution begins upon the elapse of the oscillation stabilization time($2^{15}/f_X$).

Note Only when the POC circuit is selected by mask option (refer to **9. MASK OPTION**).

Cautions 1. To use an external reset sequence, input a low-level signal to the $\overline{\text{RESET}}$ pin for at least 10 μs.

2. When a reset is used to release STOP mode, the data of when STOP mode was entered is retained during the reset sequence, except for the port pins, which are in the high-impedance state.

Figure 8-1. Reset Function Block Diagram

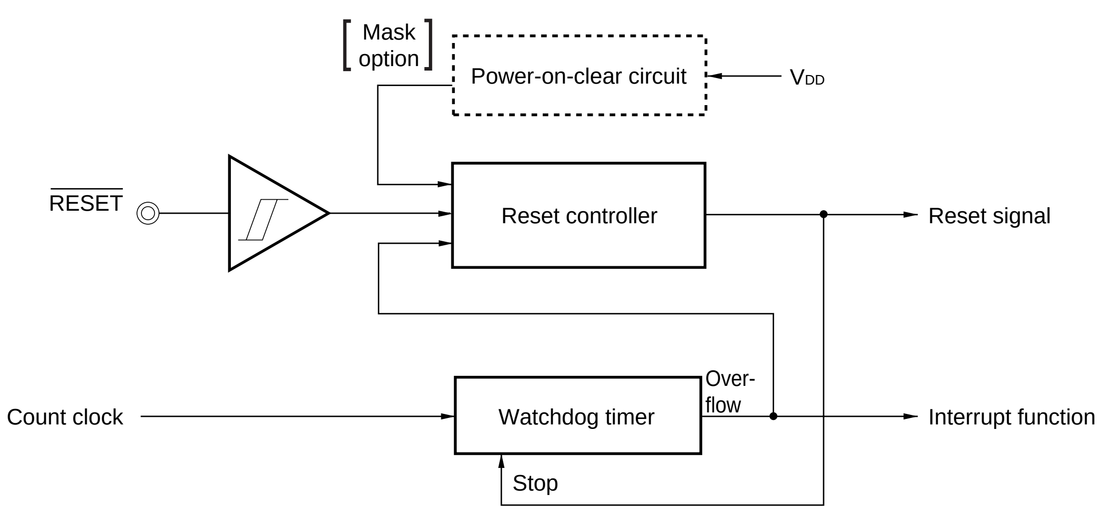


Table 8-1. Status of Hardware After Reset

Hardware		Status After Reset
Program counter (PC)[Note 1]		Contents of reset vector table (0000H, 0001H) set
Stack pointer (SP)		Undefined
Program status word (PSW)		02H
RAM	Data memory	Undefined[Note 2]
	General-purpose registers	Undefined[Note 2]
Ports (P0, P1, P4, P6) (output latches)		00H
Port mode registers (PM0, PM1, PM4, PM6)		FFH
Port function register (PF8)		00H
Pull-up resistor option registers (PU0)		00H
Processor clock control register (PCC)		02H
Subclock oscillation mode register (SCKM)		00H
Subclock control register (CSS)		00H
Oscillation stabilization time selection register (OSTS)		04H
8-bit timer 30, 40	Timer counters (TM30, TM40)	00H
	Compare registers (CR30, CR40, CRH40)	Undefined
	Mode control registers (TMC30, TMC40)	00H
	Carrier generator output control register (TCA 40)	00H
Watch timer	Mode control register (WTM)	00H
Watchdog timer	Clock selection resister (WDCS)	00H
	Mode register (WDTM)	00H
A/D converter	Mode register (ADM0)	00H
	Input channel specification register (ADS0)	00H
	A/D conversion result register (ADCR0)	Undefined
LCD controller/driver	Display mode register (LCDM0)	00H
	Clock control register (LCDC0)	00H
	LCD voltage amplification control register (LCDVA0)	00H
Interrupts	Request flag register (IF0)	00H
	Mask flag register (MK0)	FFH
	External interrupt mode register (INTM0)	00H
	Key return mode register (KRM00)	00H

Notes 1. While a reset signal is being input, and during the oscillation stabilization period, only the contents of the PC will be undefined; the remainder of the hardware will be in the same state as after reset.

2. In standby mode, RAM enters the hold state after reset.

9. MASK OPTION

The following mask option is available for the μPD789462, 789464, 789466, 789467.

- Power-on clear (POC) circuit

  Use/non use of the POC circuit can be selected.

  <1> POC circuit used

  <2> POC circuit not used

10. INSTRUCTION SET OVERVIEW

The instruction set for the μPD789462, 789464, 789466, and 789467 is listed in this section.

10.1 Conventions

10.1.1 Operand formats and descriptions

The description made in the operand field of each instruction conforms to the operand format for the instructions listed below (the details conform to the assembly specification). If more than one operand format is listed for an instruction, one is selected. Uppercase letters, #, !, $, and brackets [ ] are used to specify keywords, which must be written exactly as they appear. The meanings of these special characters are as follows:

- #: Immediate data specification
- $: Relative address specification
- !: Absolute address specification
- [ ]: Indirect address specification

Immediate data should be described using appropriate values or labels. The specification of values and labels must be accompanied by #, !, $, or [ ].

Operand registers, expressed as r or rp in the formats, can be described using both functional names (X, A, C, etc.) and absolute names (R0, R1, R2, and other names listed in Table 10-1 below).

Table 10-1. Operand Formats and Descriptions

Format	Description
r rp sfr	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7) AX (RP0), BC (RP1), DE (RP2), HL (RP3) Special function register symbol
saddr saddrp	FE20H to FF1FH Immediate data or label FE20H to FF1FH Immediate data or label (even addresses only)
addr16 addr5	0000H to FFFFH Immediate data or label (only even addresses for 16-bit data transfer instructions) 0040H to 007FH Immediate data or label (even addresses only)
word byte bit	16-bit immediate data or label 8-bit immediate data or label 3-bit immediate data or label

Remark For details concerning special function register symbols, refer to **Table 4-1 Special Function Registers**.

10.1.2 Operation field definitions

A: A register (8-bit accumulator)
X: X register
B: B register
C: C register
D: D register
E: E register
H: H register
L: L register
AX: AX register pair (16-bit accumulator)
BC: BC register pair
DE: DE register pair
HL: HL register pair
PC: Program counter
SP: Stack pointer
PSW: Program status word
CY: Carry flag
AC: Auxiliary carry flag
Z: Zero flag
IE: Interrupt request enable flag
NMIS: Flag to indicate that a non-maskable interrupt is being processed
(): Contents of a memory location indicated by a parenthesized address or register name
X_H, X_L: Higher and lower 8 bits of a 16-bit register
$\wedge$: Logical product (AND)
$\vee$: Logical sum (OR)
$\veebar$: Exclusive OR
$\overline{}$: Inverted data
addr16: 16-bit immediate data or label
jdisp8: Signed 8-bit data (displacement value)

10.1.3 Flag operation field definitions

(Blank): No change
0: Clear to 0
1: Set to 1
×: Set or clear according to the result
R: Restore to the previous value

10.2 Operations

Mnemonic	Operand	Byte	Clock	Operation	Flag Z	Flag AC	Flag CY
MOV	r, #byte	3	6	r ← byte			
	saddr , #byte	3	6	(saddr) ← byte			
	sfr, #byte	3	6	sfr ← byte			
	A, r Note 1	2	4	A ← r			
	r, A Note 1	2	4	r ← A			
	A, saddr	2	4	A ← (saddr)			
	saddr, A	2	4	(saddr) ← A			
	A, sfr	2	4	A ← sfr			
	sfr, A	2	4	sfr ← A			
	A, !addr16	3	8	A ← (addr16)			
	!addr16, A	3	8	(addr16) ← A			
	PSW, #byte	3	6	PSW ← byte	×	×	×
	A, PSW	2	4	A ← PSW			
	PSW, A	2	4	PSW ← A	×	×	×
	A, [DE]	1	6	A ← (DE)			
	[DE], A	1	6	(DE) ← A			
	A, [HL]	1	6	A ← (HL)			
	[HL], A	1	6	(HL) ← A			
	A, [HL + byte]	2	6	A ← (HL + byte)			
	[HL + byte], A	2	6	(HL + byte) ← A			
XCH	A, X	1	4	A ↔ X			
	A, r Note 2	2	6	A ↔ r			
	A, saddr	2	6	A ↔ (saddr)			
	A, sfr	2	6	A ↔ (sfr)			
	A, [DE]	1	8	A ↔ (DE)			
	A, [HL]	1	8	A ↔ (HL)			
	A, [HL + byte]	2	8	A ↔ (HL + byte)			
MOVW	rp, #word	3	6	rp ← word			
	AX, saddrp	2	6	AX ← (saddrp)			
	saddrp, AX	2	8	(saddrp) ← AX			
	AX, rp Note 3	1	4	AX ← rp			
	rp, AX Note 3	1	4	rp ← AX			
XCHW	AX, rp Note 3	1	8	AX ↔ rp			

Notes 1. Except when r = A.
2. Except when r = A or X.
3. Only when rp = BC, DE, or HL.

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}) specified by the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
ADD	A, #byte	2	4	A, CY ← A + byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte	×	×	×
	A, r	2	4	A, CY ← A + r	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte)	×	×	×
ADDC	A, #byte	2	4	A, CY ← A + byte + CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte + CY	×	×	×
	A, r	2	4	A, CY ← A + r + CY	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr) + CY	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16) + CY	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL) + CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte) + CY	×	×	×
SUB	A, #byte	2	4	A, CY ← A – byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte	×	×	×
	A, r	2	4	A, CY ← A – r	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte)	×	×	×
SUBC	A, #byte	2	4	A, CY ← A – byte – CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte – CY	×	×	×
	A, r	2	4	A, CY ← A – r – CY	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr) – CY	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16) – CY	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL) – CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte) – CY	×	×	×
AND	A, #byte	2	4	A ← A ∧ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∧ byte	×		
	A, r	2	4	A ← A ∧ r	×		
	A, saddr	2	4	A ← A ∧ (saddr)	×		
	A, !addr16	3	8	A ← A ∧ (addr16)	×		
	A, [HL]	1	6	A ← A ∧ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∧ (HL + byte)	×		

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}) specified by the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
OR	A, #byte	2	4	$A \leftarrow A \vee byte$	×		
	saddr, #byte	3	6	$(saddr) \leftarrow (saddr) \vee byte$	×		
	A, r	2	4	$A \leftarrow A \vee r$	×		
	A, saddr	2	4	$A \leftarrow A \vee (saddr)$	×		
	A, !addr16	3	8	$A \leftarrow A \vee (addr16)$	×		
	A, [HL]	1	6	$A \leftarrow A \vee (HL)$	×		
	A, [HL + byte]	2	6	$A \leftarrow A \vee (HL + byte)$	×		
XOR	A, #byte	2	4	$A \leftarrow A \veebar byte$	×		
	saddr, #byte	3	6	$(saddr) \leftarrow (saddr) \veebar byte$	×		
	A, r	2	4	$A \leftarrow A \veebar r$	×		
	A, saddr	2	4	$A \leftarrow A \veebar (saddr)$	×		
	A, !addr16	3	8	$A \leftarrow A \veebar (addr16)$	×		
	A, [HL]	1	6	$A \leftarrow A \veebar (HL)$	×		
	A, [HL + byte]	2	6	$A \leftarrow A \veebar (HL + byte)$	×		
CMP	A, #byte	2	4	A – byte	×	×	×
	saddr, #byte	3	6	(saddr) – byte	×	×	×
	A, r	2	4	A – r	×	×	×
	A, saddr	2	4	A – (saddr)	×	×	×
	A, !addr16	3	8	A – (addr16)	×	×	×
	A, [HL]	1	6	A – (HL)	×	×	×
	A, [HL + byte]	2	6	A – (HL + byte)	×	×	×
ADDW	AX, #word	3	6	$AX, CY \leftarrow AX + word$	×	×	×
SUBW	AX, #word	3	6	$AX, CY \leftarrow AX - word$	×	×	×
CMPW	AX, #word	3	6	AX – word	×	×	×
INC	r	2	4	$r \leftarrow r + 1$	×	×	
	saddr	2	4	$(saddr) \leftarrow (saddr) + 1$	×	×	
DEC	r	2	4	$r \leftarrow r - 1$	×	×	
	saddr	2	4	$(saddr) \leftarrow (saddr) - 1$	×	×	
INCW	rp	1	4	$rp \leftarrow rp + 1$			
DECW	rp	1	4	$rp \leftarrow rp - 1$			
ROR	A, 1	1	2	$(CY, A_7 \leftarrow A_0, A_{m-1} \leftarrow A_m) \times 1$			×
ROL	A, 1	1	2	$(CY, A_0 \leftarrow A_7, A_{m+1} \leftarrow A_m) \times 1$			×
RORC	A, 1	1	2	$(CY \leftarrow A_0, A_7 \leftarrow CY, A_{m-1} \leftarrow A_m) \times 1$			×
ROLC	A, 1	1	2	$(CY \leftarrow A_7, A_0 \leftarrow CY, A_{m+1} \leftarrow A_m) \times 1$			×

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}) specified by the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag Z	Flag AC	Flag CY
SET1	saddr.bit	3	6	(saddr.bit) ← 1			
	sfr.bit	3	6	sfr.bit ← 1			
	A.bit	2	4	A.bit ← 1			
	PSW.bit	3	6	PSW bit ← 1	×	×	×
	[HL].bit	2	10	(HL).bit ← 1			
CLR1	saddr.bit	3	6	(saddr.bit) ← 0			
	sfr.bit	3	6	sfr.bit ← 0			
	A.bit	2	4	A.bit ← 0			
	PSW.bit	3	6	PSW.bit ← 0	×	×	×
	[HL].bit	2	10	(HL).bit ← 0			
SET1	CY	1	2	CY ← 1			1
CLR1	CY	1	2	CY ← 0			0
NOT1	CY	1	2	CY ← $\overline{CY}$			×
CALL	!addr16	3	6	(SP – 1) ← $(PC + 3)_H$, (SP – 2) ← $(PC + 3)_L$, PC ← addr16, SP ← SP – 2			
CALLT	[addr5]	1	8	(SP – 1) ← $(PC + 1)_H$, (SP – 2) ← $(PC + 1)_L$, PC_H ← (00000000, addr5 + 1), PC_L ← (00000000, addr5), SP ← SP – 2			
RET		1	6	PC_H ← (SP + 1), PC_L ← (SP), SP ← SP + 2			
RETI		1	8	PC_H ← (SP + 1), PC_L ← (SP), PSW ← (SP + 2), SP ← SP + 3, NMIS ← 0	R	R	R
PUSH	PSW	1	2	(SP – 1) ← PSW, SP ← SP – 1			
	rp	1	4	(SP – 1) ← rp_H, (SP – 2) ← rp_L, SP ← SP – 2			
POP	PSW	1	4	PSW ← (SP), SP ← SP + 1	R	R	R
	rp	1	6	rp_H ← (SP + 1), rp_L ← (SP), SP ← SP + 2			
MOVW	SP, AX	2	8	SP ← AX			
	AX, SP	2	6	AX ← SP			
BR	!addr16	3	6	PC ← addr16			
	$addr16	2	6	PC ← PC + 2 + jdisp8			
	AX	1	6	PC_H ← A, PC_L ← X			

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}) specified by the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag Z AC CY
BC	\$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 1	
BNC	\$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 0	
BZ	\$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 1	
BNZ	\$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 0	
BT	saddr.bit, \$addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr.bit) = 1	
	sfr.bit, \$addr16	4	10	PC ← PC + 4 + jdisp8 if sfr.bit = 1	
	A.bit, \$addr16	3	8	PC ← PC + 3 + jdisp8 if A.bit = 1	
	PSW.bit, \$addr16	4	10	PC ← PC + 4 + jdisp8 if PSW.bit = 1	
BF	saddr.bit, \$addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr.bit) = 0	
	sfr.bit, \$addr16	4	10	PC ← PC + 4 + jdisp8 if sfr.bit = 0	
	A.bit, \$addr16	3	8	PC ← PC + 3 + jdisp8 if A.bit = 0	
	PSW.bit, \$addr16	4	10	PC ← PC + 4 + disp8 if PSW.bit = 0	
DBNZ	B, \$addr16	2	6	B ← B – 1, then PC ← PC + 2 + jdisp8 if B ≠ 0	
	C, \$addr16	2	6	C ← C – 1, then PC ← PC + 2 + jdisp8 if C ≠ 0	
	saddr, \$addr16	3	8	(saddr) ← (saddr) – 1, then PC ← PC + 3 + jdisp8 if (saddr) ≠ 0	
NOP		1	2	No Operation	
EI		3	6	IE ← 1 (Enable Interrupt)	
DI		3	6	IE ← 0 (Disable Interrupt)	
HALT		1	2	Set HALT Mode	
STOP		1	2	Set STOP Mode	

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}) specified by the processor clock control register (PCC).

11. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

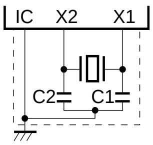
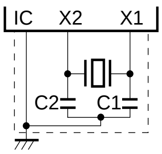
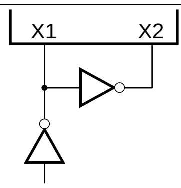
Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.3 to +6.5	V
Input voltage	V_I		–0.3 to V_{DD} + 0.3 Note	V
Output voltage	V_{O1}	P00 to P03, P10, P11, P40 to P43, P60, P61	–0.3 to V_{DD} + 0.3 Note	V
	V_{O2}	COM0 to COM3, S0 to S16, P80/S22 to P85/S17	–0.3 to V_{LC0} + 0.3 Note	V
Output current, high	I_{OH}	Pin P60/TO40	–30	mA
		Per pin (except P60/TO40)	–10	mA
		Total for all pins (except P60/TO40)	–30	mA
Output current, low	I_{OL}	Per pin	30	mA
		Total for all pins	80	mA
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

Note 6.5 V or lower

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Main System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)[Note 1]		1.0		5.0	MHz
		Oscillation stabilization time[Note 2]	After V_{DD} has reached the oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency [Note 1]		1.0		5.0	MHz
		Oscillation stabilization time[Note 2]	V_{DD} = 4.5 to 5.5 V			10	ms
						30	ms
External clock		X1 input frequency (f_X)[Note 1]		1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release. Use the resonator to stabilize oscillation within the oscillation wait time.

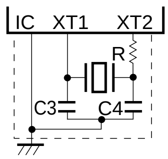
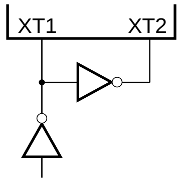
Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Remark For the resonator selection and oscillator constant, users are required to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Subsystem Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})Note 1		32	32.768	35	kHz
		Oscillation stabilization timeNote 2	V_{DD} = 4.5 to 5.5 V		1.2	2	s
						10	s
External clock		XT1 input frequency (f_{XT})Note 1		32		35	kHz
		XT1 input high-/low-level width (t_{XTH}, t_{XTL})		14.3		15.6	μs

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. The time required for oscillation to stabilize after V_{DD} reaches the MIN. oscillation voltage range. Use a resonator to stabilize oscillation during the oscillation wait time.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Remark For the resonator selection and oscillator constant, users are required to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low	I_{OL}	Per pin				10	mA
		Total for all pins				80	mA
Output current, high	I_{OH}	Per pin (except P60/TO40)				–1	mA
		P60/TO40	V_{DD} = 3.0 V, V_{OH} = 1.0 V	–7	–15	–24	mA
		Total for all pins (except P60/TO40)				–15	mA
Input voltage, high	V_{IH1}	P00 to P03, P10, P11, P60	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		V_{DD}	V
				0.9V_{DD}		V_{DD}	V
	V_{IH2}	$\overline{\text{RESET}}$, P40 to P43, P61	V_{DD} = 2.7 to 5.5 V	0.8V_{DD}		V_{DD}	V
				0.9V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2		V_{DD} – 0.1		V_{DD}	V
	V_{IH4}	XT1, XT2		V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P03, P10, P11, P60	V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
				0		0.1V_{DD}	V
	V_{IL2}	$\overline{\text{RESET}}$, P40 to P43, P61	V_{DD} = 2.7 to 5.5 V	0		0.2V_{DD}	V
				0		0.1V_{DD}	V
	V_{IL3}	X1, X2		0		0.1	V
	V_{IL4}	XT1, XT2		0		0.1	V
Output voltage, high	V_{OH11}	P00 to P03, P10, P11, P40 to P43, P61	1.8 ≤ V_{DD} ≤ 5.5 V, I_{OH} = –100 μA	V_{DD} – 0.5			V
	V_{OH12}		1.8 ≤ V_{DD} ≤ 5.5 V, I_{OH} = –500 μA	V_{DD} – 0.7			V
	V_{OH21}	P60/TO40	1.8 ≤ V_{DD} ≤ 5.5 V, I_{OH} = –400 μA	V_{DD} – 0.5			V
	V_{OH22}		1.8 ≤ V_{DD} ≤ 5.5 V, I_{OH} = –2 mA	V_{DD} – 0.7			V
Output voltage, low	V_{OL1}	P00 to P03, P10, P11, P40 to P43, P60, P61	1.8 ≤ V_{DD} ≤ 5.5 V, I_{OL} = 400 μA			0.5	V
	V_{OL2}		1.8 ≤ V_{DD} ≤ 5.5 V, I_{OL} = 2 mA			0.7	V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	$V_{IN} = V_{DD}$	P00 to P03, P10, P11, P40 to P43, P60, P61, $\overline{RESET}$			3	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	P00 to P03, P10, P11, P40 to P43, P60, P61, $\overline{RESET}$			–3	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
Output leakage current, high	I_{LOH}	$V_{OUT} = V_{DD}$				3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Software pull-up resistors	R_1	V_{IN} = 0 V	P00 to P03, P10, P11, P40 to P43	50	100	200	kΩ
Supply current[Note 1] Ceramic/crystal oscillation	I_{DD1}	5.0 MHz crystal oscillation operating mode	V_{DD} = 5.5 V[Note 2]		5.0	15.0	mA
			V_{DD} = 3.3 V[Note 3]		2.0	5.0	mA
	I_{DD2}	5.0 MHz crystal oscillation HALT mode	V_{DD} = 5.5 V		1.2	3.6	mA
			V_{DD} = 3.3 V		0.5	1.5	mA
	I_{DD4}	32.768 kHz crystal oscillation HALT mode[Note 4]	V_{DD} = 5.5 V		25	55	μA
			V_{DD} = 3.3 V		5	25	μA
	I_{DD5}	STOP mode	V_{DD} = 5.5 V		2	30	μA
			V_{DD} = 3.3 V		1	10	μA

Notes 1. Current flowing through ports (including current flowing through on-chip pull-up resistors) is not included.

2. High-speed mode operation (when the processor clock control register (PCC) is set to 00H).

3. Low-speed mode operation (when PCC is set to 02H)

4. When the main system clock operation is stopped.

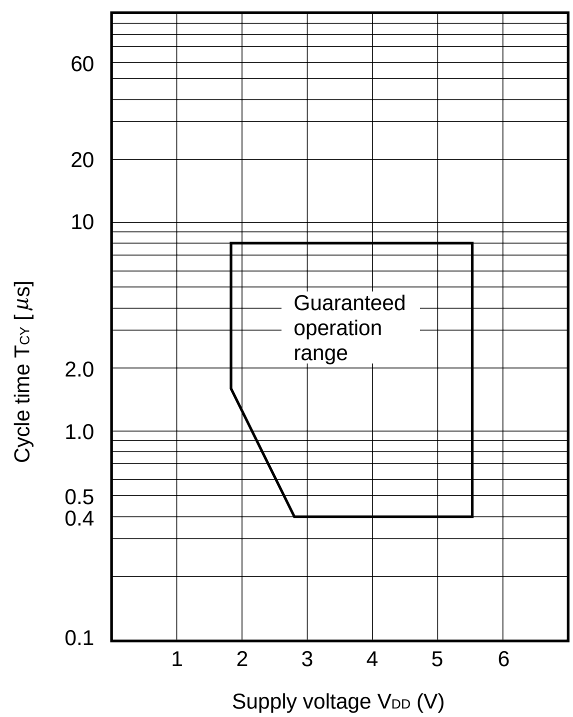
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

AC Characteristics

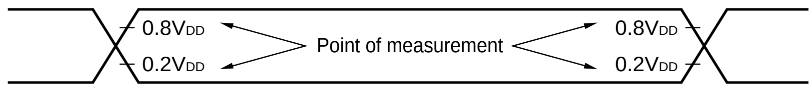
(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T_{CY}	V_{DD} = 2.7 to 5.5 V	0.4		8.0	μs
			1.6		8.0	μs
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INT	10			μs
Key return pin low-level width	t_{KRIL}	KR00 to KR03	10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}		10			μs

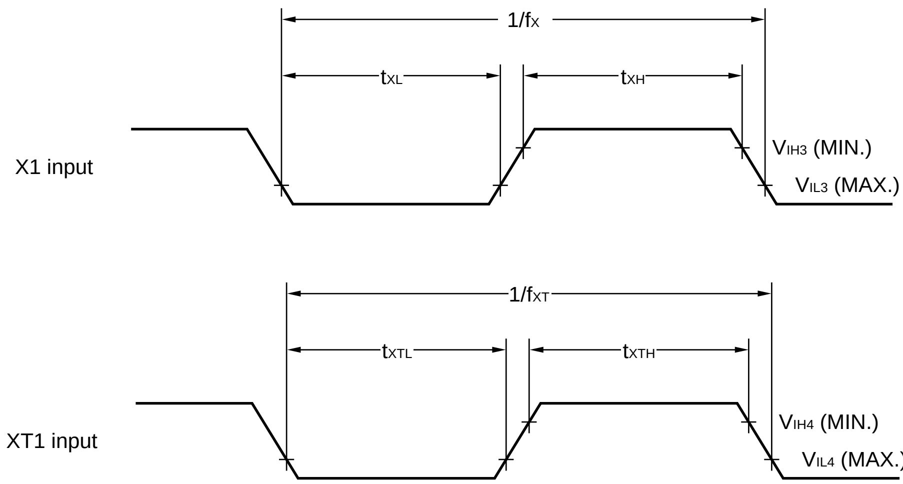
T_{CY} vs. V_{DD} (Main System Clock)



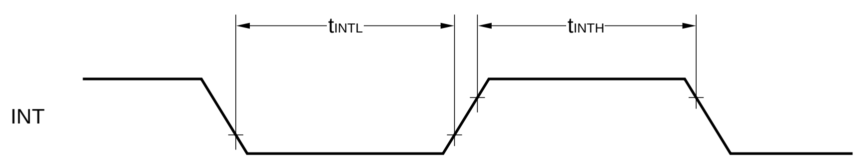
AC Timing Measurement Points (Excluding X1, XT1 Input)



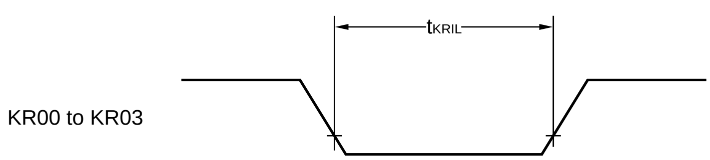
Clock Timing



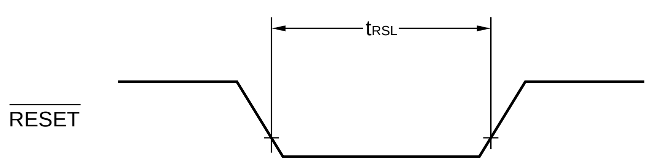
Interrupt Input Timing



Key Return Input Timing



$\overline{\text{RESET}}$ Input Timing



8-Bit A/D Converter Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error[Notes 1, 2]		V_{DD} = 2.7 to 5.5 V			±0.6	%FSR
					±1.2	%FSR
Conversion time	t_{CONV}	V_{DD} = 2.7 to 5.5 V	14		100	μs
			28		100	μs

Notes 1. Excludes quantization error (±0.2% FSR).
2. The overall error is indicated as a ratio to the full-scale value.

Remark FSR: Full scale range

LCD Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD amplification output voltage	V_{LC20}	GAIN = 0	V_{LC2} pin		1.5		V
	V_{LC10}		V_{LC1} pin		3.0		V
	V_{LC00}		V_{LC0} pin		4.5		V
	V_{LC21}	GAIN = 1	V_{LC2} pin		1.0		V
	V_{LC11}		V_{LC1} pin		2.0		V
	V_{LC01}		V_{LC0} pin		3.0		V
LCD output voltage differential[Note] (common)	V_{ODC}	I_O = ±5 μA		0		±0.2	V
LCD output voltage differential[Note] (segment)	V_{ODS}	I_O = ±1 μA		0		±0.2	V

Note The voltage differential is the difference between the output voltage and the ideal value of the segment and common signal outputs.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8		5.5	V
Low voltage detection (POC) voltage[Note1]	V_{POC}	Response time: 2 ms[Note 2]	1.8	1.9	2.0	V
Release signal set time	t_{SREL}	STOP released by $\overline{\text{RESET}}$	10			μs
Oscillation stabilization wait time[Note 3]	t_{WAIT}	Cancelled by $\overline{\text{RESET}}$		$2^{15}/f_X$		s
		Cancelled by interrupt request		**Note 4**		s

Notes 1. Only when the POC circuit is selected by mask option (refer to **9.MASK OPTION**).

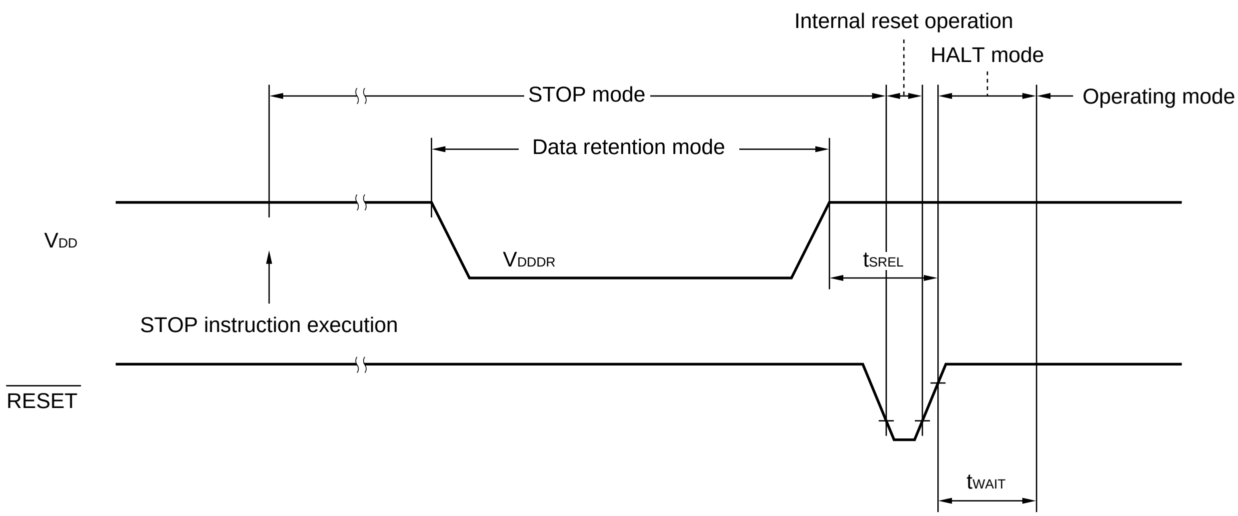
2. The response time is the time until the output is inverted following detection of voltage by POC, or the time until operation stabilizes after the shift from the operation stopped state to the operating state.

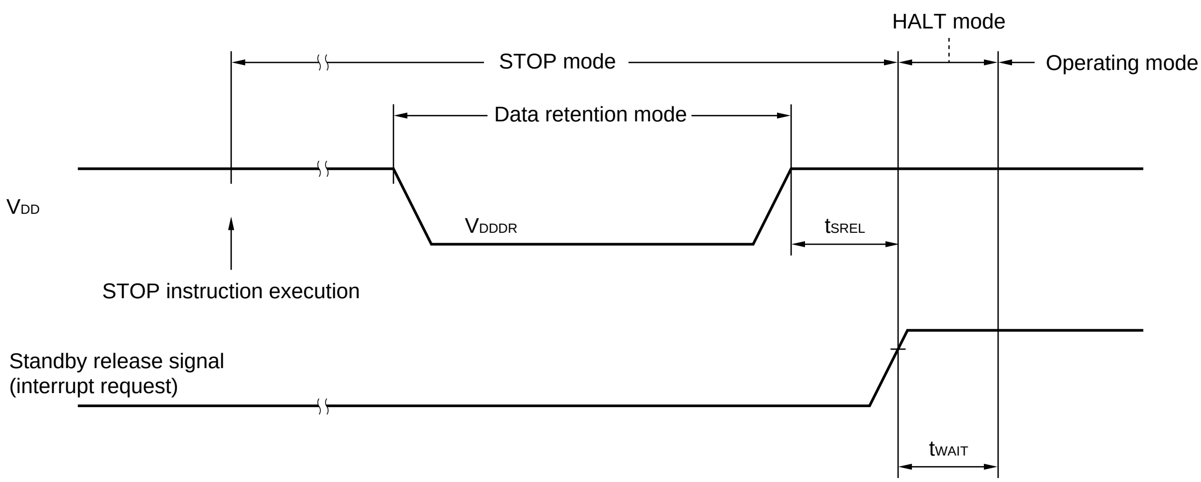
3. The oscillation stabilization time is the amount of time the CPU operation is stopped in order to avoid unstable operation at the start of oscillation. Program operation does not start until both the oscillation stabilization time and the time until oscillation starts have elapsed.

4. Selection of $2^{12}/f_X$, $2^{15}/f_X$, and $2^{17}/f_X$ is possible with bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time selection register (OSTS) (refer to **7.2 Standby Function Control Register**).

Remark f_X: Main system clock oscillation frequency

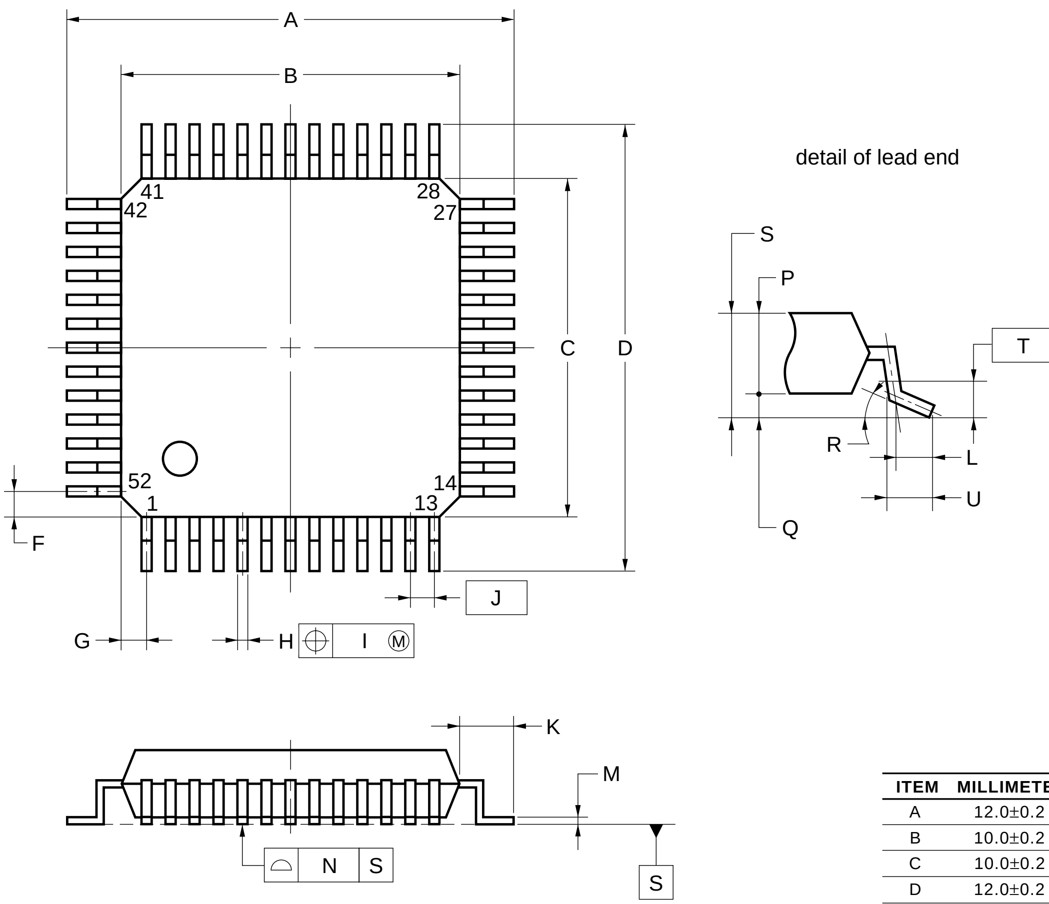
Data Retention Timing





12. PACKAGE DRAWING

52-PIN PLASTIC LQFP (10x10)



ITEM	MILLIMETERS
A	12.0±0.2
B	10.0±0.2
C	10.0±0.2
D	12.0±0.2
F	1.1
G	1.1
H	0.32±0.06
I	0.13
J	0.65 (T.P.)
K	1.0±0.2
L	0.5
M	$0.17^{+0.03}_{-0.05}$
N	0.10
P	1.4
Q	0.1±0.05
R	$3°^{+4°}_{-3°}$
S	1.5±0.1
T	0.25
U	0.6±0.15

S52GB-65-8ET-1

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD789462, 789464, 789466, and 789467.

Language Processing Software

RA78K0S[Notes 1, 2, 3]	Assembler package common to 78K/0S Series
CC78K0S[Notes 1, 2 ,3]	C compiler package common to 78K/0S Series
DF789468[Notes 1, 2, 3, 6]	Device file for μPD789467 Subseries
CC78K0S-L[Notes 1, 2, 3]	C compiler library source file common to 78K/0S Series

Flash Memory Writing Tools

Flashpro III (Part number: FL-PR3[Note 4], PG-FP3)	Dedicated flash memory programmer
FA-52GB-8ET[Notes 4, 6]	Adapter for writing to flash memory designed for 52-pin plastic LQFP (GB-8ET type)

Debugging Tools

IE-78K0S-NS In-circuit emulator	In-circuit emulator to debug hardware or software when application systems using the 78K/0S Series are developed. The IE-78K0S-NS supports an integrated debugger (ID78K0S-NS). The IE-78K0S-NS is used in combination with an interface adapter for connection to an AC adapter, emulation probe, or host machine.
IE-70000-MC-PS-B AC adapter	AC adapter to supply power from a 100- to 240-V AC outlet.
IE-70000-98-IF-C Interface adapter	Interface adapter required when using a PC-9800 series computer (except notebook type) as the host machine for the IE-78K0S-NS (C bus supported).
IE-70000-CD-IF-A PC card interface	PC card and interface cable required when a notebook PC is used as the host machine for the IE-78K0S-NS (PCMCIA socket supported).
IE-70000-PC-IF-C Interface adapter	Interface adapter required when using an IBM PC/AT™ or compatible as the host machine for the IE-78K0S-NS (ISA bus supported).
IE-70000-PCI-IF Interface adapter	Interface adapter required when using a PC incorporating a PCI bus as the host machine for the IE-78K0S-NS.
IE-789468-NS-EM1[Note 6] Emulation board	Emulation board to emulate the peripheral hardware specific to the device. The IE-789468-NS-EM1 is used in combination with the in-circuit emulator.
NP-H52GB-NQ[Notes 4, 6] Emulation probe	Board to connect an in-circuit emulator to the target system. This board is dedicated for a 52-pin plastic LQFP (GB-8ET type).
NQPACK052SB[Notes 5, 6] YQPACK052SB[Notes 5, 6] Conversion adapter	Conversion adapter to connect the NP-H52GB-NQ and a target system board on which a 52-pin plastic LQFP (GB-8ET Type) can be mounted.
SM78K0S[Notes 1, 2]	System simulator common to 78K/0S Series
ID78K0S-NS[Notes 1, 2]	Integrated debugger common to 78K/0S Series
DF789468[Notes 1, 2, 6]	Device file for μPD789467 Subseries

Real-Time OS

MX78K0S[Notes 1, 2]	OS for 78K/0S Series

Notes

1. Based on the PC-9800 series (Japanese Windows™)
2. Based on IBM PC/AT or compatibles (Japanese/English Windows)
3. Based on the HP9000 series 700™ (HP-UX™), SPARCstation™ (SunOS™, Solaris™), and NEWS™ (NEWS-OS™)
4. Manufactured by Naito Densei Machida Mfg. Co, Ltd. (+81-44-822-3813).
5. Manufactured by Tokyo Eletech Corp.
   For further information, contact Daimaru Kogyo, Ltd.
   Tokyo Electronics Department (TEL: +81-3-3820-7112)
   Osaka Electronics Department (TEL: +81-6-6244-6672)
6. Under development

Remark The RA78K0S, CC78K0S, and SM78K0S are used in combination with the DF789468 device file.

APPENDIX B. RELATED DOCUMENTS

Documents Related to Devices

Document Name	Document No.	
	Japanese	English
μPD789462, 789464, 789466, 789467 Preliminary Product Information	U14788J	This document
μPD78F9468 Preliminary Product Information	U14558J	U14558E
μPD789327, 789467 Subseries User's Manual	To be prepared	To be prepared
78K/0S Series User's Manual Instructions	U11047J	U11047E
78K/0, 78K/0S Series Application Note Flash Memory Write	U14458J	U14458E

Documents Related to Development Tools (User's Manuals)

Document Name		Document No.	
		Japanese	English
RA78K0S Assembler Package	Operation	U11622J	U11622E
	Assembly Language	U11599J	U11599E
	Structured Assembly Language	U11623J	U11623E
CC78K0S C Compiler	Operation	U11816J	U11816E
	Language	U11817J	U11817E
SM78K0S System Simulator Windows Based	Reference	U11489J	U11489E
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092J	U10092E
ID78K0S-NS Integrated Debugger Windows Based	Reference	U12901J	U12901E
IE-78K0S-NS In-circuit Emulator		U13549J	U13549E
IE-789468-NS-EM1 Emulation Board		To be prepared	To be prepared

Documents Related to Embedded Software (User's Manuals)

Document Name		Document No.	
		Japanese	English
78K/0S Series OS MX78K0S	Fundamental	U12938J	U12938E

Other Documents

Document Name	Document No.	
	English	Japanese
SEMICONDUCTORS SELECTION GUIDE Products & Packages (CD-ROM)	X13769X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Devices	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892J	C11892E
Guide to Microcomputer-Related Products by Third Party	U11416J	–

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics Inc. (U.S.)
Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

NEC Electronics (Germany) GmbH
Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

NEC Electronics Italiana s.r.l.
Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

NEC Electronics (Germany) GmbH
Benelux Office
Eindhoven, The Netherlands
Tel: 040-2445845
Fax: 040-2444580

NEC Electronics (France) S.A.
Velizy-Villacoublay, France
Tel: 01-30-67 58 00
Fax: 01-30-67 58 99

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Spain Office
Madrid, Spain
Tel: 91-504-2787
Fax: 91-504-2860

NEC Electronics (Germany) GmbH
Scandinavia Office
Taeby, Sweden
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Fax: 08-63 80 388

NEC Electronics Hong Kong Ltd.
Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.
Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.
United Square, Singapore 1130
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Fax: 65-250-3583

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
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Fax: 02-2719-5951

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Rodovia Presidente Dutra, Km 214
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Tel: 55-11-6465-6810
Fax: 55-11-6465-6829

J99.1

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