

## P-Channel 20-V (D-S) MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
- 20	0.015 at $V_{GS} = - 4.5$ V	- 13.2
	0.020 at $V_{GS} = - 2.5$ V	- 11.4
	0.029 at $V_{GS} = - 1.8$ V	- 9.5

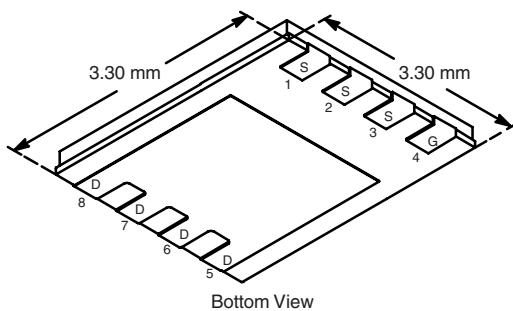
### FEATURES

- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET® Power MOSFET
- New PowerPAK® Package
- Low Thermal Resistance,  $R_{thJC}$
- Low 1.07 mm Profile



**RoHS**  
COMPLIANT  
**HALOGEN**  
**FREE**  
Available

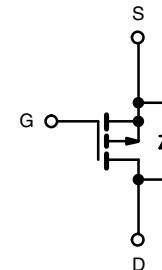
PowerPAK 1212-8



**Ordering Information:** Si7413DN-T1-E3 (Lead (Pb)-free)  
Si7413DN-T1-GE3 (Lead (Pb)-free and Halogen-free)

### APPLICATIONS

- Load Switch



P-Channel MOSFET

### ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	10 s	Steady State	Unit
Drain-Source Voltage	$V_{DS}$	- 20		V
Gate-Source Voltage	$V_{GS}$		± 8	
Continuous Drain Current ( $T_J = 150$ °C) <sup>a</sup>	$I_D$	- 13.2	- 8.4	A
		- 9.5	- 6.1	
Pulsed Drain Current	$I_{DM}$	- 30		A
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$		- 3.2	
Maximum Power Dissipation <sup>a</sup>	$P_D$	3.8	1.5	W
		2.0	0.8	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) <sup>b, c</sup>			260	

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$t \leq 10$ s	R <sub>thJA</sub>	26	33
	Steady State		65	81
Maximum Junction-to-Case	Steady State	R <sub>thJC</sub>	1.9	2.4

Notes:

- Surface Mounted on 1" x 1" FR4 board.
- See Solder Profile ([www.vishay.com/ppg?73257](http://www.vishay.com/ppg?73257)). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

**SPECIFICATIONS**  $T_J = 25^\circ\text{C}$ , unless otherwise noted

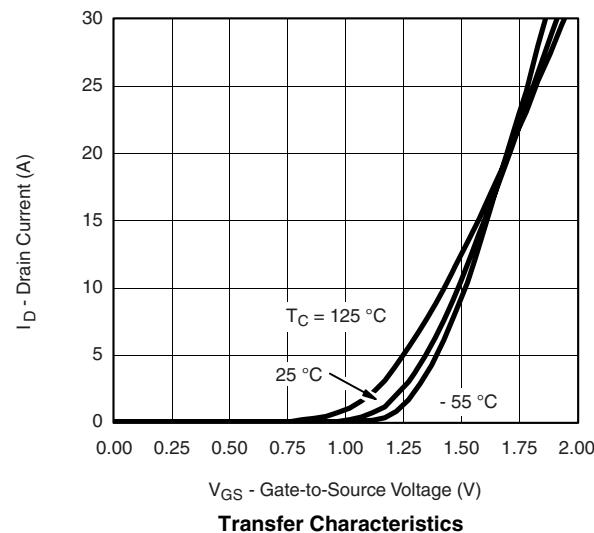
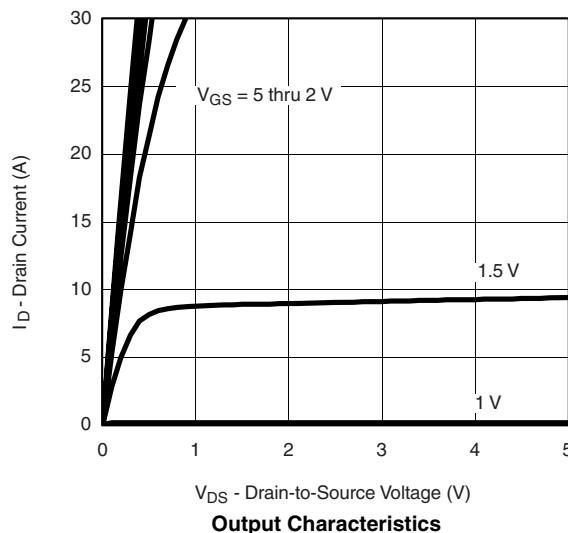
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$ , $I_D = -400 \mu\text{A}$	- 0.4		- 1.0	V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}$ , $V_{GS} = \pm 8 \text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -20 \text{ V}$ , $V_{GS} = 0 \text{ V}$			- 1	$\mu\text{A}$
		$V_{DS} = -20 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $T_J = 85^\circ\text{C}$			- 5	
On-State Drain Current <sup>a</sup>	$I_{D(\text{on})}$	$V_{DS} \leq -5 \text{ V}$ , $V_{GS} = -4.5 \text{ V}$	- 30			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(\text{on})}$	$V_{GS} = -4.5 \text{ V}$ , $I_D = -13.2 \text{ A}$		0.012	0.015	$\Omega$
		$V_{GS} = -2.5 \text{ V}$ , $I_D = -11.4 \text{ A}$		0.016	0.020	
		$V_{GS} = -1.8 \text{ V}$ , $I_D = -3.5 \text{ A}$		0.023	0.029	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = -15 \text{ V}$ , $I_D = -13.2 \text{ A}$		47		S
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = -3.2 \text{ A}$ , $V_{GS} = 0 \text{ V}$		- 0.8	- 1.2	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = -10 \text{ V}$ , $V_{GS} = -4.5 \text{ V}$ , $I_D = -13.2 \text{ A}$		34	51	nC
Gate-Source Charge	$Q_{gs}$			5.4		
Gate-Drain Charge	$Q_{gd}$			8.8		
Gate Resistance	$R_g$	$f = 1 \text{ MHz}$		5		$\Omega$
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = -10 \text{ V}$ , $R_L = 10 \Omega$ $I_D \geq -1 \text{ A}$ , $V_{GEN} = -4.5 \text{ V}$ , $R_g = 6 \Omega$		30	45	ns
Rise Time	$t_r$			50	75	
Turn-Off Delay Time	$t_{d(\text{off})}$			200	300	
Fall Time	$t_f$			95	140	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = -3.2 \text{ A}$ , $dl/dt = 100 \text{ A}/\mu\text{s}$		35	55	

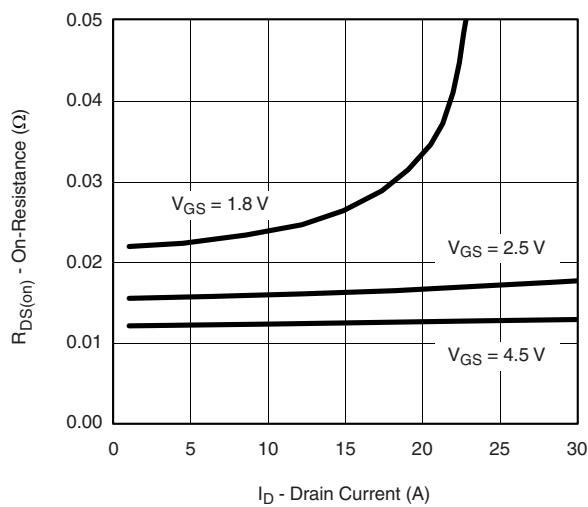
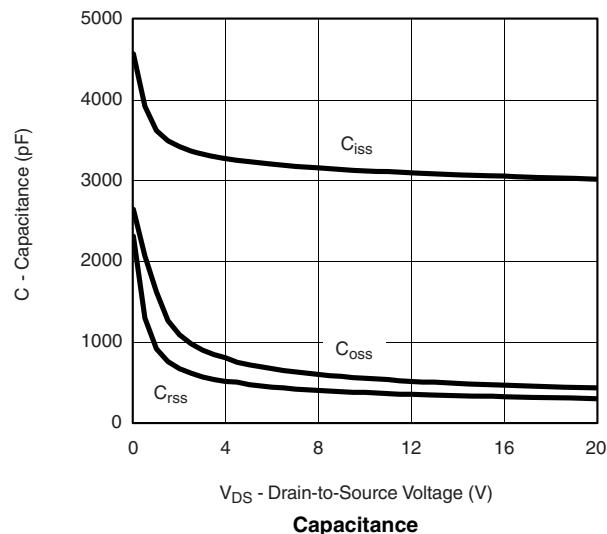
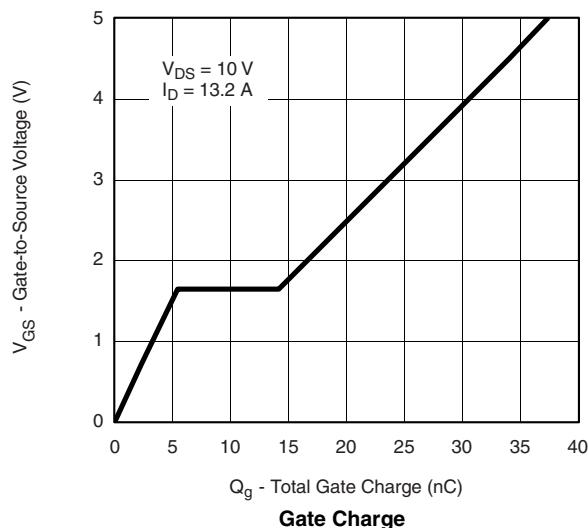
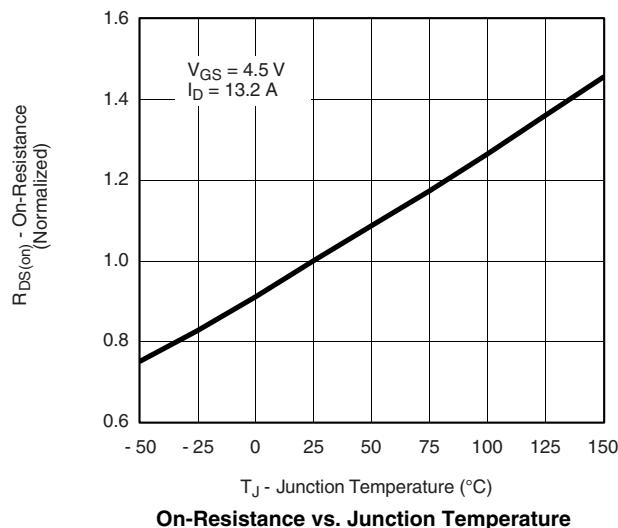
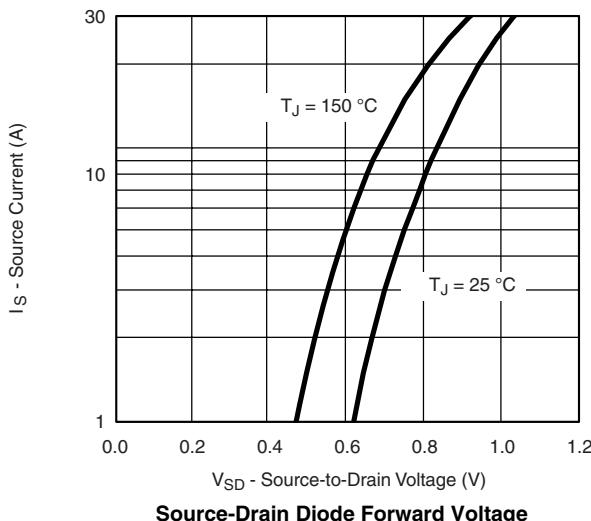
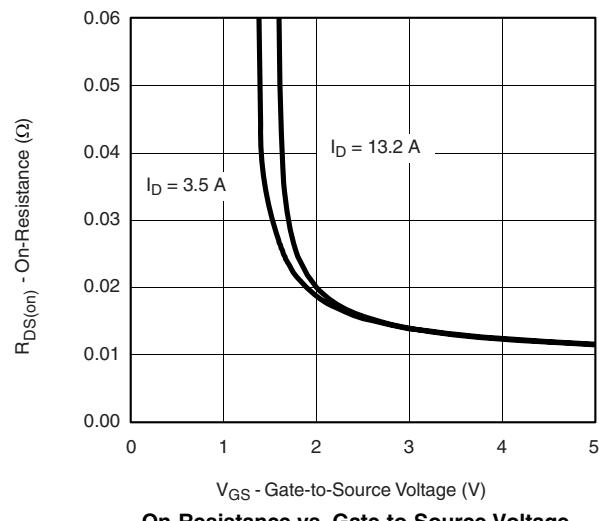
Notes:

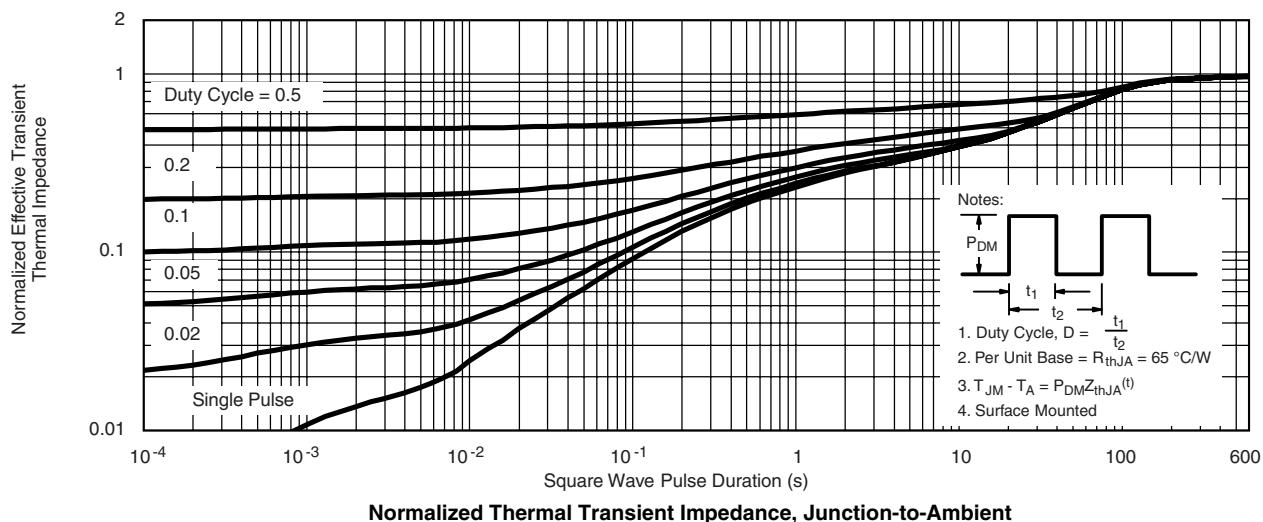
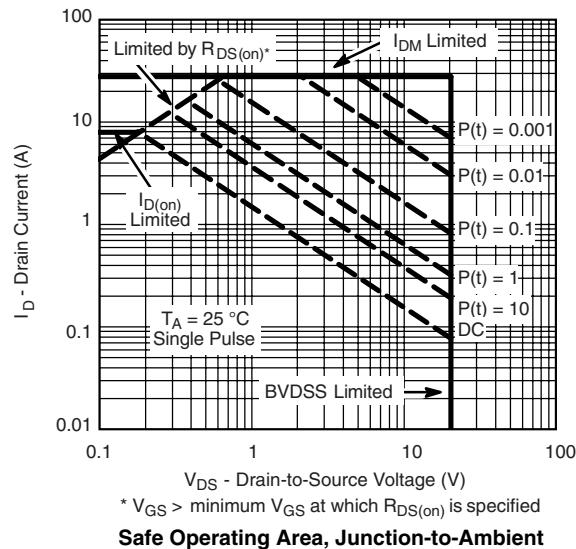
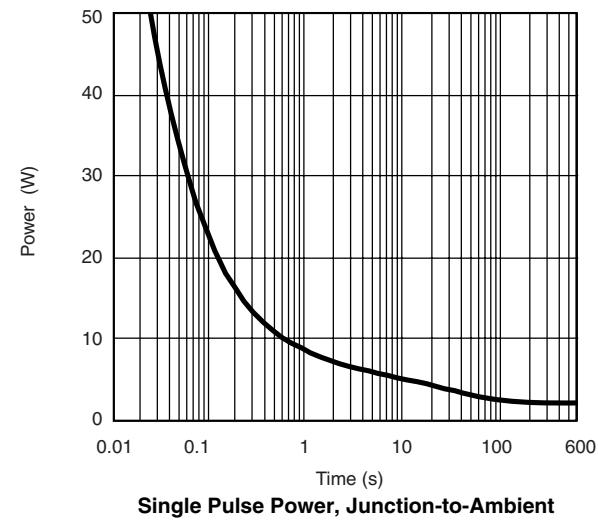
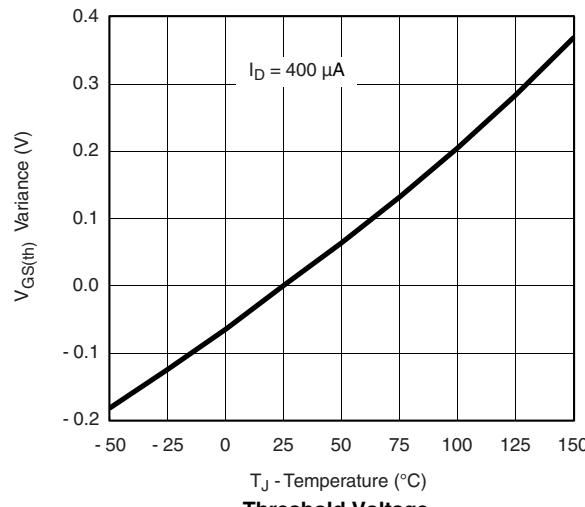
a. Pulse test; pulse width  $\leq 300 \mu\text{s}$ , duty cycle  $\leq 2\%$ .

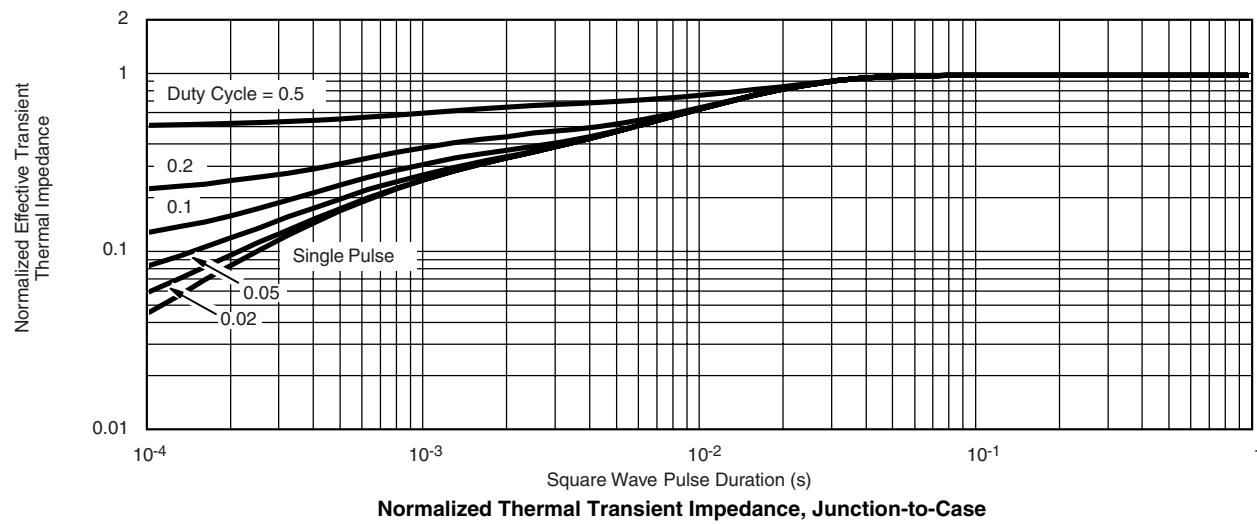
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS**  $25^\circ\text{C}$ , unless otherwise noted

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**On-Resistance vs. Drain Current**

**Capacitance**

**Gate Charge**

**On-Resistance vs. Junction Temperature**

**Source-Drain Diode Forward Voltage**

**On-Resistance vs. Gate-to-Source Voltage**

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted


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