19-3885; Rev 0; 12/05

EVALUATION KIT AVAILABLE

Low-Cost Battery Charger

MAX8730

General Description

The MAX8730 highly integrated, multichemistry, battery-charger control IC simplifies construction of accurate and efficient chargers. The MAX8730 operates at high switching frequency to minimize external component size and cost. The MAX8730 uses analog inputs to control charge current and voltage, and can be programmed by a microcontroller or hardwired.

The MAX8730 reduces charge current to give priority to the system load, effectively limiting the adapter current and reducing the adapter current requirements.

The MAX8730 provides a digital output that indicates the presence of an AC adapter, and an analog output that monitors the current drawn from the AC adapter. Based on the presence and absence of the AC adapter, the MAX8730 automatically selects the appropriate source for supplying power to the system by controlling two external switches. Under system control, the MAX8730 allows the battery to undergo a relearning cycle in which the battery is completely discharged through the system load and then recharged.

An analog output indicates adapter current or battery-discharge current. The MAX8730 provides a low-quiescent-current linear regulator, which may be used when the adapter is absent, or disabled for reduced current consumption

The MAX8730 is available in a small, 5mm x 5mm, 28-pin, thin (0.8mm) QFN package. An evaluation kit is available to reduce design time. The MAX8730 is available in a lead-free package.

Applications

Notebook Computers

Tablet PCs

Portable Equipment with Rechargeable Batteries

Pin Configuration appears at end of data sheet.

Features

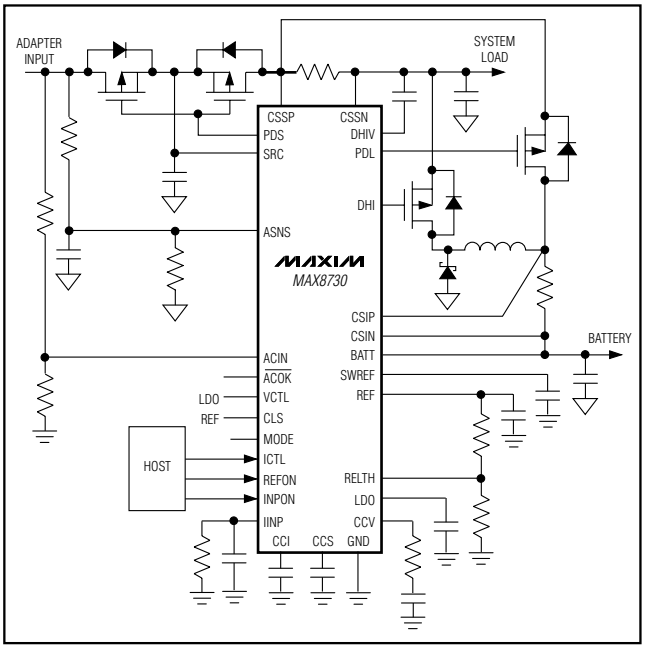
- ♦ **Small Inductor (3.5µH)**
- ♦ **Programmable Charge Current > 4.5A**
- ♦ **Automatic Power-Source Selection**
- ♦ **Analog Inputs Control Charge Current and Charge Voltage**
- ♦ **Monitor Outputs for**
  AC Adapter Current
  Battery-Discharge Current
  AC Adapter Presence
- ♦ **Independent 3.3V 20mA Linear Regulator**
- ♦ **Up to 17.6V (max) Battery Voltage**
- ♦ **+8V to +28V Input Voltage Range**
- ♦ **Reverse Adapter Protection**
- ♦ **System Short-Circuit Protection**
- ♦ **Cycle-by-Cycle Current Limit**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX8730ETI+	-40°C to +85°C	28 Thin QFN (5mm x 5mm)	T2855-5

+Denotes lead-free package.

Typical Operating Circuit



ABSOLUTE MAXIMUM RATINGS

CSSP, SRC, ACOK, ASNS, DHIV, BATT, CSIP to GND .....-0.3V to +30V
CSIP to CSIN or CSSP to CSSN .....-0.3V to +0.3V
DHIV to SRC .....-6V to (SRC + 0.3V)
DHI to DHIV .....-0.3V to (SRC + 0.3V)
PDL, PDS to GND .....-0.3V to (SRC + 0.3)
CCI, CCS, CCV, IINP, SWREF, REF, MODE, ACIN to GND.....-0.3V to (LDO + 0.3V)
RELTH, VCTL, ICTL, REFON, CLS, LDO, INPON to GND .....-0.3V to +6V
LDO Short-Circuit Current.....50mA
Continuous Power Dissipation (T_A = +70°C)
28-Pin TQFN (derate 20.8mW/°C above +70°C) 1667mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1. V_{SRC} = V_{ASNS} = V_{CSSP} = V_{CSSN} = 18V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12V, V_{VCTL} = V_{ICTL} = 1.8V, MODE = float, ACIN = 0, CLS = REF, REFON = LDO, INPON = LDO, RELTH = 2V. **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CHARGE-VOLTAGE REGULATION							
VCTL Range				0		3.6	V
Battery-Regulation Voltage Accuracy		V_{VCTL} = 3.6V or 0V	Not including resistor tolerances	-1.0		+1.0	%
			Including 1% resistor tolerances	-1.05		+1.05	
		V_{VCTL} = V_{LDO} (3 or 4 cells)		-0.5		+0.5	
V_{VCTL} Default Threshold		V_{VCTL} rising		4.4			V
VCTL Input Bias Current		V_{VCTL} = 3V		0		4	µA
		SRC = BATT, ASNS = GND INPON = REFON = 0, V_{VCTL} = 5V		0		16	
CHARGE-CURRENT REGULATION							
ICTL Range				0		3.6	V
Full-Charge-Current Accuracy (CSIP to CSIN)		V_{ICTL} = 3.6V		128.25	135	141.75	mV
				-5		+5	%
		V_{ICTL} = 2.0V		71.25	75	78.75	mV
				-5		+5	%
Trickle-Charge-Current Accuracy		V_{ICTL} = 120mV		2.5	4.5	7.5	mV
Charge-Current Gain Error		Based on V_{ICTL} = 3.6V and V_{ICTL} = 0.12V		-1.9		+1.9	%
Charge-Current Offset Error		Based on V_{ICTL} = 3.6V and V_{ICTL} = 0.12V		-2		+2	mV
BATT/CSIP/CSIN Input Voltage Range				0		19	V
CSIP/CSIN Input Current		Charging enabled			300	600	µA
		Charging disabled, SRC = BATT, ASNS = GND or V_{ICTL} = 0V			8	16	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{SRC} = V_{ASNS} = V_{CSSP} = V_{CSSN} = 18V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12V, V_{VCTL} = V_{ICTL} = 1.8V, MODE = float, ACIN = 0, CLS = REF, REFON = LDO, INPON = LDO, RELTH = 2V. **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ICTL Power-Down Mode Threshold		ICTL falling	50	65	80	mV
		ICTL rising	70	90	110	
ICTL Input Bias Current		V_{ICTL} = 3V	-1		+1	µA
		SRC = BATT, ASNS = GND, V_{ICTL} = 5V	-1		+1	
CSSP-to-CSSN Full-Scale Current-Sense Voltage			72.75	75.75	78.75	mV
Input Current-Limit Accuracy		V_{CLS} = REF (trim point)	72.75	75.75	78.75	mV
			-4		+4	%
		V_{CLS} = REF x 0.7	50	53	56	mV
			-5.6		+5.6	%
		V_{CLS} = REF x 0.5	36	38	40.5	mV
			-6.6		+6.6	%
CSSP/CSSN Input Voltage Range			8.0		28	V
CSSP/CSSN Input Current		V_{CSSP} = V_{CSSN} = V_{SRC} > 8.0V		400	800	µA
		V_{SRC} = 0V		0.1	1	
CLS Input Range			1.1		REF	V
CLS Input Bias Current		V_{CLS} = 2.0V	-1		+1	µA
IINP Transconductance		V_{CSSP} - V_{CSSN} = 56mV	2.66	2.8	2.94	µA/mV
IINP Accuracy		V_{CSSP} - V_{CSSN} = 100mV, V_{IINP} = 0 to 4.5V	-5		+5	%
		V_{CSSP} - V_{CSSN} = 75mV	-8		+8	
		V_{CSSP} - V_{CSSN} = 56mV	-5		+5	
		V_{CSSP} - V_{CSSN} = 20mV	-12.5		+12.5	
IINP Gain Error		Based on V_{ICTL} = REF x 0.5 and V_{ICTL} = REF	-7		+7	%
IINP Offset Error		Based on V_{ICTL} = REF x 0.5 and V_{ICTL} = REF	-2		+2	mV
IINP Fault threshold		IINP rising	4.1	4.2	4.3	V
SUPPLY AND LINEAR REGULATOR						
SRC Input Voltage Range			8.0		28	V
SRC Undervoltage Lockout Threshold		SRC falling	7	7.4		V
		SRC rising		7.5	8	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{SRC} = V_{ASNS} = V_{CSSP} = V_{CSSN} = 18V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12V, V_{VCTL} = V_{ICTL} = 1.8V, MODE = float, ACIN = 0, CLS = REF, REFON = LDO, INPON = LDO, RELTH = 2V. **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SRC Quiescent Current (INPON/REFON = Don't Care)		Normal mode			4	6	mA
		V_{SRC} = V_{BATT} = 12V, ASNS = GND (Note 2)	V_{INPON} = V_{REFON} = low		10	20	µA
			V_{INPON} = low, V_{REFON} = high		300	600	
			V_{INPON} = high, V_{REFON} = low		300	600	
			V_{INPON} = V_{REFON} = high		350	600	
BATT Input Current		V_{BATT} = 16.8V, V_{SRC} = 19V, ICTL = 0			8	16	µA
		V_{BATT} = 2V to 19V, V_{SRC} > V_{BATT} + 0.3V			300	600	
Battery-Leakage Current		I_{CSIP} + I_{CSIN} + I_{BATT}, ASNS = GND			2	5	µA
		I_{CSIP} + I_{CSIN} + I_{BATT} + I_{CSSP} + I_{CSSN} + I_{SRC}, ASNS = REFON = GND	V_{REFON} = 5.4V		300	600	
			INPON = GND		2	5	
LDO Output Voltage		8.0V < V_{SRC} < 28V, no load		5.2	5.35	5.5	V
LDO Load Regulation		0 < I_{LDO} < 10mA			20	50	mV
LDO Undervoltage Lockout Threshold		V_{SRC} = 8.0V			4		V
REFERENCES							
REF Output Voltage	Ref			4.18	4.20	4.22	V
REF Undervoltage Lockout Threshold		REF falling			3.1	3.9	V
SWREF Output Voltage		8.0V < V_{SRC} < 28V, no load		3.234	3.3	3.366	V
SWREF Load Regulation		0.1mA < I_{SWREF} < 20mA			20	50	mV
TRIP POINTS							
ACIN Threshold		ACIN rising		2.037	2.1	2.163	V
ACIN Threshold Hysteresis					60		mV
ACIN Input Bias Current		V_{ACIN} = 2.048V		-1		+1	µA
SWITCHING REGULATOR							
DHI Off-Time		V_{BATT} = 16.0V		300	350	400	ns
DHI Off-Time K Factor		V_{BATT} = 16.0V		4.8	5.6	6.4	V x µs
Sense Voltage for Minimum Discontinuous Mode Ripple Current		V_{CSIP} - V_{CSIN}			7		mV
Cycle-by-Cycle Current-Limit Sense Voltage				160	200	240	mV
Charge Disable Threshold		V_{SRC} - V_{BATT}, SRC falling		40	60	80	mV
DHIV Output Voltage		With respect to SRC		-4.3	-4.8	-5.5	V
DHIV Sink Current				10			mA

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{SRC} = V_{ASNS} = V_{CSSP} = V_{CSSN} = 18V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12V, V_{VCTL} = V_{ICTL} = 1.8V, MODE = float, ACIN = 0, CLS = REF, REFON = LDO, INPON = LDO, RELTH = 2V. **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DHI Resistance Low		I_{DHI} = -10mA			2	4	Ω
DHI Resistance High		I_{DHI} = 10mA			1	2	Ω
ERROR AMPLIFIERS							
GMV Loop Transconductance		VCTL = 3.6V, V_{BATT} = 16.8V, MODE = LDO		0.0625	0.125	0.250	mA/V
		VCTL = 3.6V, V_{BATT} = 12.6V, MODE = FLOAT		0.0833	0.167	0.333	
GMI Loop Transconductance		ICTL = 3.6V, V_{CSSP} - V_{CSIN} = 75mV		0.5	1	2	mA/V
GMS Loop Transconductance		V_{CLS} = 2.048V, V_{CSSP} - V_{CSSN} = 75mV		0.5	1	2	mA/V
CCI/CCS/CCV Clamp Voltage		1.1V < V_{CCV} < 3.0V, 1.1V < V_{CCI} < 3.0V, 1.1V < V_{CCS} < 3.0V		150	300	600	mV
LOGIC LEVELS							
MODE, REFON Input Low Voltage						0.5	V
MODE Input Middle Voltage				1.9	2.65	3.3	V
MODE, REFON Input High Voltage				3.4			V
MODE, REFON, INPON Input Bias Current		MODE = 0 or 3.6V		-2		+2	µA
INPON Threshold		V_{INPON} rising		2.2			V
		V_{INPON} falling				0.8	V
ADAPTER DETECTION							
ACOK Voltage Range				0		28	V
ACOK Sink Current		V_{ACOK} = 0.4V, ACIN = 1.5V		1			mA
ACOK Leakage Current		V_{ACOK} = 28V, ACIN = 2.5V				1	µA
BATTERY DETECTION							
BATT Overvoltage Threshold		V_{VCTL} = V_{LDO} , BATT rising; result with respect to battery-set voltage	V_{MODE} = V_{LDO}		+140		mV
			V_{MODE} = FLOAT		+100		
BATT Overvoltage Hysteresis					100		mV
RELTH Operating Voltage Range				0.9		2.6	V
RELTH Input Bias Current		V_{RELTH} = 0.9V to 2.6V		-50		+50	nA
BATT Minimum Voltage Trip Threshold		V_{BATT} falling	V_{RELTH} = 0.9V	4.42	4.5	4.58	V
			V_{RELTH} = 2.6V	12.77	13.0	13.23	
PDS, PDL SWITCH CONTROL							
Adapter-Absence Detect Threshold		V_{ASNS} - V_{BATT}, V_{ASNS} falling		-300	-280	-240	mV
Adapter-Detect Threshold		V_{ASNS} - V_{BATT}		-140	-100	-60	mV
PDS Output Low Voltage		Result with respect to SRC, I_{PDS} = 0		-8	-10	-12	V
PDS/PDL Output High Voltage		Result with respect to SRC, $I_{PD\_}$ = 0			-0.2	-0.5	V
PDS/PDL Turn-Off Current		V_{PDS} = V_{SRC} - 2V, V_{SRC} = 16V		6	12		mA

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{SRC} = V_{ASNS} = V_{CSSP} = V_{CSSN} = 18V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12V, V_{VCTL} = V_{ICTL} = 1.8V, MODE = float, ACIN = 0, CLS = REF, REFON = LDO, INPON = LDO, RELTH = 2V. **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PDS Turn-On Current		PDS = SRC	6	12		mA
PDL Turn-On Resistance		PDL = GND	50	100	200	kΩ
PDS/PDL Delay Time				5.0		µs

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1. V_{SRC} = V_{ASNS} = V_{CSSP} = V_{CSSN} = 18V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12V, V_{VCTL} = V_{ICTL} = 1.8V, MODE = float, ACIN = 0, CLS = REF, REFON = LDO, INPON = LDO, RELTH = 2V. **T_A = -40°C to +85°C**, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CHARGE-VOLTAGE REGULATION							
VCTL Range				0		3.6	V
Battery-Regulation-Voltage Accuracy		V_{VCTL} = 3.6V or 0V	Not including resistor tolerances	-1.2		+1.2	%
			Including 1% resistor tolerances	-1.25		+1.25	
		V_{VCTL} = V_{LDO} (3 or 4 cells)		-0.8		+0.8	
V_{VCTL} Default Threshold		V_{VCTL} rising		4.4			V
VCTL Input Bias Current		SRC = BATT, ASNS = GND INPON = REFON = 0, V_{VCTL} = 5V		0		16	µA
CHARGE-CURRENT REGULATION							
ICTL Range				0		3.6	V
Full-Charge-Current Accuracy (CSIP to CSIN)		V_{ICTL} = 3.6V		128.25		141.75	mV
				-5		+5	%
		V_{ICTL} = 2.0V		70		80	mV
				-6.7		+6.7	%
Trickle-Charge-Current Accuracy		V_{ICTL} = 120mV		2		10	mV
Charge-Current Gain Error		Based on V_{ICTL} = 3.6V and V_{ICTL} = 0.12V		-1.9		+1.9	%
Charge-Current Offset Error		Based on V_{ICTL} = 3.6V and V_{ICTL} = 0.12V		-2		+2	mV
BATT/CSIP/CSIN Input Voltage Range				0		19	V
CSIP/CSIN Input Current		Charging enabled				1000	µA
		Charging disabled, SRC = BATT, ASNS = GND, or V_{ICTL} = 0V				16	
ICTL Power-Down Mode Threshold		ICTL falling		50		80	mV
		ICTL rising		70		110	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{SRC} = V_{ASNS} = V_{CSSP} = V_{CSSN} = 18V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12V, V_{VCTL} = V_{ICTL} = 1.8V, MODE = float, ACIN = 0, CLS = REF, REFON = LDO, INPON = LDO, RELTH = 2V. **T_A = -40°C to +85°C**, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT-CURRENT REGULATION							
CSSP-to-CSSN Full-Scale Current-Sense Voltage				72.75		78.25	mV
Input Current-Limit Accuracy		V_{CLS} = REF (trim point)		72.75		78.25	mV
		V_{CLS} = REF x 0.7		50.0		56.0	mV
		V_{CLS} = REF x 0.5		36.00		40.50	mV
CSSP/CSSN Input Voltage Range				8.0		28	V
CSSP/CSSN Input Current		V_{CSSP} = V_{CSSN} = V_{SRC} > 8.0V				1000	µA
CLS Input Range				1.1		REF	V
IINP Transconductance		V_{CSSP} - V_{CSSN} = 56mV		2.66		2.94	µA/mV
IINP Accuracy		V_{CSSP} - V_{CSSN} = 100mV, V_{IINP} = 0 to 4.5V		-5		+5	%
		V_{CSSP} - V_{CSSN} = 75mV		-8		+8	
		V_{CSSP} - V_{CSSN} = 56mV		-5		+5	
		V_{CSSP} - V_{CSSN} = 20mV		-12.5		+12.5	
IINP Gain Error		Based on V_{ICTL} = REF x 0.5 and V_{ICTL} = REF		-7		+7	%
IINP Offset Error		Based on V_{ICTL} = REF x 0.5 and V_{ICTL} = REF		-2		+2	mV
IINP Fault Threshold		IINP rising		4.1		4.3	V
SUPPLY AND LINEAR REGULATOR							
SRC Input Voltage Range				8.0		28	V
SRC Undervoltage Lockout Threshold		SRC falling		7			V
		SRC rising				8	
SRC Quiescent Current (INPON/REFON = Don't Care)		Normal mode				6	mA
		SRC = V_{BATT} = 12V, ASNS = GND (Note 2)	V_{INPON} = V_{REFON} = low			20	µA
			V_{INPON} = low, V_{REFON} = high			600	
			V_{INPON} = high, V_{REFON} = low			600	
			V_{INPON} = V_{REFON} = high			600	
BATT Input Current		V_{BATT} = 2V to 19V, V_{SRC} > V_{BATT} + 0.3V				600	µA
Battery Leakage Current		I_{CSIP} + I_{CSIN} + I_{BATT} + I_{CSSP} + I_{CSSN} + I_{SRC}, ASNS = REFON = GND	V_{REFON} = 5.4V			600	µA
			INPON = GND			16	
LDO Output Voltage		8.0V < VSRC < 28V, no load		5.2		5.5	V
LDO Load Regulation		0 < I_{LDO} < 10mA				50	mV

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{SRC} = V_{ASNS} = V_{CSSP} = V_{CSSN} = 18V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12V, V_{VCTL} = V_{ICTL} = 1.8V, MODE = float, ACIN = 0, CLS = REF, REFON = LDO, INPON = LDO, RELTH = 2V. **T_A = -40°C to +85°C**, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCES						
REF Output Voltage	Ref	0 < I_{REF} < 500µA	4.16		4.24	V
REF Undervoltage Lockout Threshold		REF falling			3.9	V
SWREF Output Voltage		8.0V < V_{SRC} < 28V, no load	3.224		3.376	V
SWREF Load Regulation		0.1mA < I_{SWREF} < 20mA			50	mV
TRIP POINTS						
ACIN Threshold		ACIN rising	2.037		2.163	V
SWITCHING REGULATOR						
DHI Off-Time		V_{BATT} = 16.0V	300		400	ns
DHI Off-Time K Factor		V_{BATT} = 16.0V	4.8		6.4	V x µs
Cycle-by-Cycle Current-Limit Sense Voltage			160		240	mV
DHIV Output Volatge		With respect to SRC	-4.3		-5.5	V
DHIV Sink Current			10			mA
DHI Resistance Low		I_{DHI} = -10mA			4	Ω
DHI Resistance High		I_{DHI} = 10mA			2	Ω
ERROR AMPLIFIERS						
GMV Loop Transconductance		VCTL = 3.6V, V_{BATT} = 16.8V, MODE = LDO	0.0625		0.250	mA/V
		VCTL = 3.6V, V_{BATT} = 12.6V, MODE = FLOAT	0.0833		0.333	
GMI Loop Transconductance		ICTL = 3.6V, V_{CSSP} - V_{CSIN} = 75mV	0.5		2	mA/V
GMS Loop Transconductance		V_{CLS} = 2.048V, V_{CSSP} - V_{CSSN} = 75mV	0.5		2	mA/V
CCI/CCS/CCV Clamp Voltage		1.1V < V_{CCV} < 3.0V, 1.1V < V_{CCI} < 3.0V, 1.1V < V_{CCS} < 3.0V	150		600	mV
LOGIC LEVELS						
MODE, REFON Input Low Voltage					0.5	V
MODE Input Middle Voltage			1.9		3.3	V
MODE, REFON Input High Voltage			3.4			V
INPON Threshold		V_{INPON} rising	2.2			V
		V_{INPON} falling			0.8	
ADAPTER DETECTION						
ACOK Voltage Range			0		28	V
ACOK Sink Current		V_{ACOK} = 0.4V, ACIN = 1.5V	1			mA

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{SRC} = V_{ASNS} = V_{CSSP} = V_{CSSN} = 18V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12V, V_{VCTL} = V_{ICTL} = 1.8V, MODE = float, ACIN = 0, CLS = REF, REFON = LDO, INPON = LDO, RELTH = 2V. **T_A = -40°C to +85°C**, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BATTERY DETECTION							
RELTH Operating Voltage Range				0.9		2.6	V
BATT Minimum Voltage Trip Threshold		V_{BATT} falling	V_{RELTH} = 0.9V	4.42		4.58	V
			V_{RELTH} = 2.6V	12.77		13.23	
PDS, PDL SWITCH CONTROL							
Adapter-Absence-Detect Threshold		V_{ASNS} - V_{BATT}, V_{ASNS} falling		-310		-240	mV
Adapter-Detect Threshold		V_{ASNS} - V_{BATT}		-140		-60	mV
PDS Output Low Voltage		Result with respect to SRC, I_{PDS} = 0		-7		-12	V
PDS/PDL Output High Voltage		Result with respect to SRC, $I_{PD\_}$ = 0				-0.5	V
PDS/ PDL Turn-Off Current		V_{PDS} = V_{SRC} - 2V, V_{SRC} = 16V		6			mA
PDS Turn-On Current		PDS = SRC		6			mA
PDL Turn-On Resistance		PDL = GND		50	100	200	kΩ

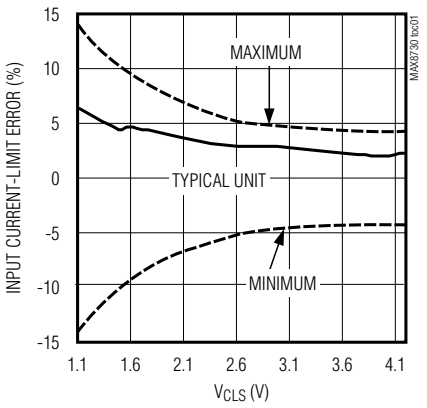
Note 1: Accuracy does not include errors due to external-resistance tolerances.
Note 2: In this mode, SRC current is drawn from the battery.

Low-Cost Battery Charger

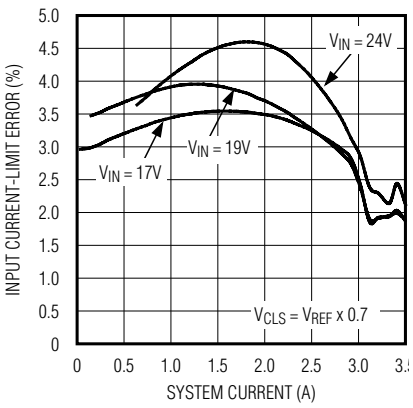
Typical Operating Characteristics

(Circuit of Figure 1, adapter = 19.5V, V_{BATT} = 12V, V_{ICTL} = 2.4V, MODE > 1.8V, REFON = INPON = LDO, V_{RELTH} = V_{REF}/2, T_A = +25°C, unless otherwise noted.)

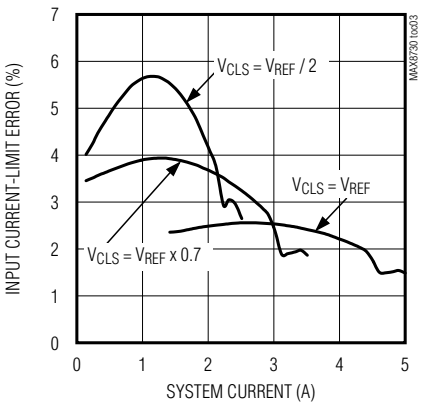
INPUT CURRENT-LIMIT ERROR vs. CLS



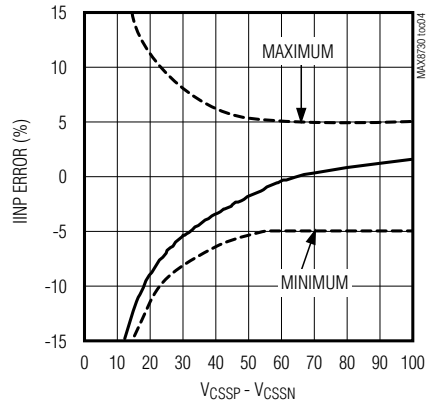
INPUT CURRENT-LIMIT ERROR vs. SYSTEM CURRENT



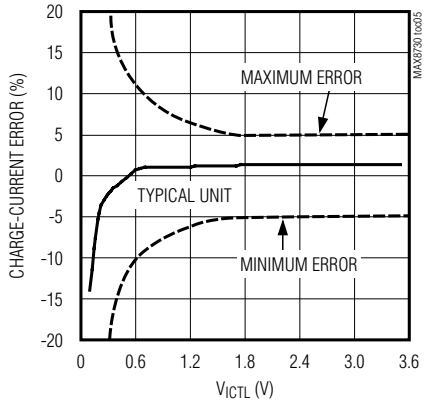
INPUT CURRENT-LIMIT ERROR vs. SYSTEM CURRENT



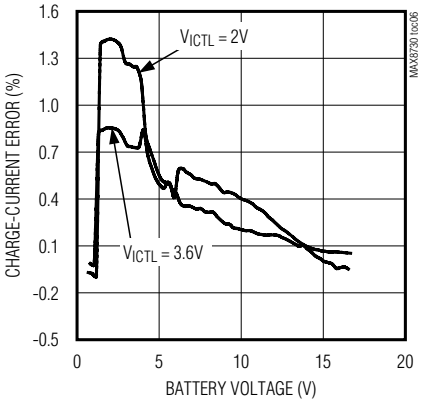
IINP ERROR vs. V_{CSSP} - V_{CSSN}



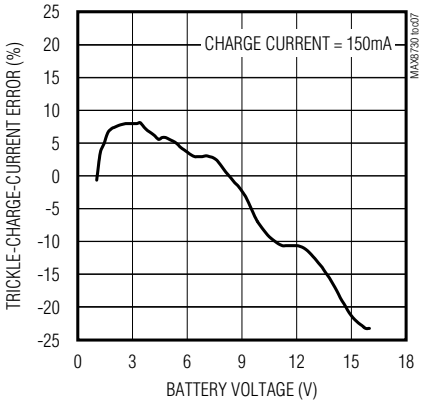
CHARGE-CURRENT ERROR vs. CHARGE-CURRENT SETTING



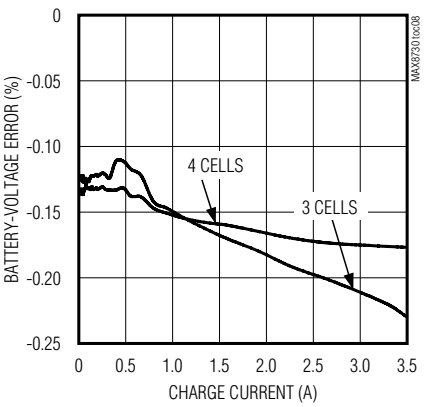
CHARGE-CURRENT ERROR vs. BATTERY VOLTAGE



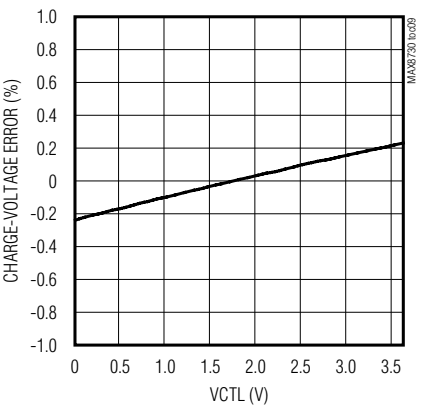
TRICKLE-CHARGE CURRENT vs. BATTERY VOLTAGE



BATTERY-VOLTAGE ERROR vs. CHARGE CURRENT



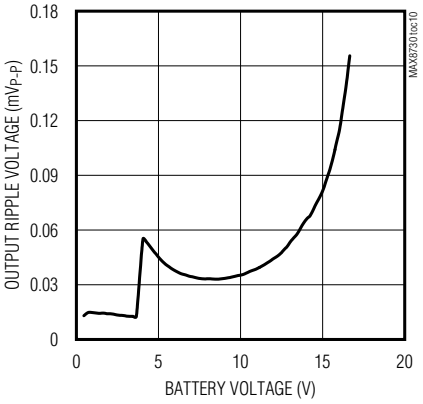
BATTERY-VOLTAGE ERROR vs. VCTL



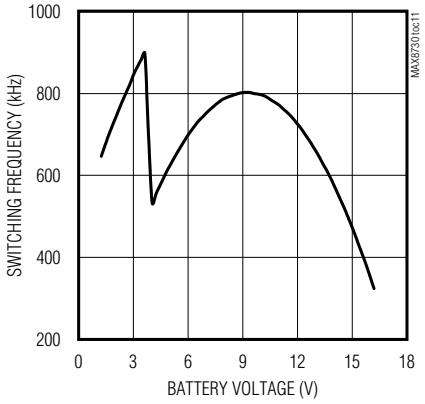
Typical Operating Characteristics (continued)

(Circuit of Figure 1, adapter = 19.5V, V_{BATT} = 12V, V_{ICTL} = 2.4V, MODE > 1.8V, REFON = INPON = LDO, V_{RELTH} = V_{REF}/2, T_A = +25°C, unless otherwise noted.)

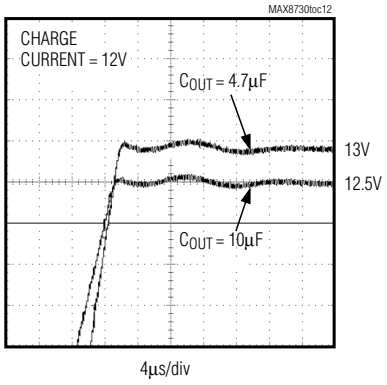
OUTPUT RIPPLE VOLTAGE vs. BATTERY VOLTAGE



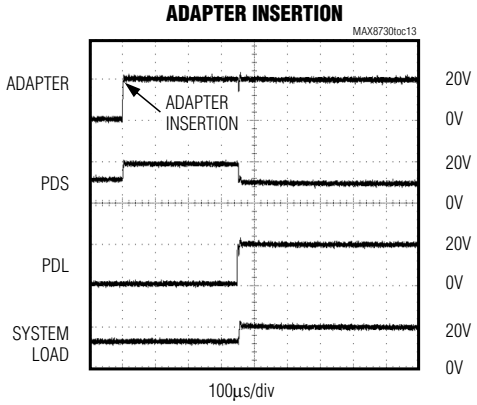
SWITCHING FREQUENCY vs. BATTERY VOLTAGE



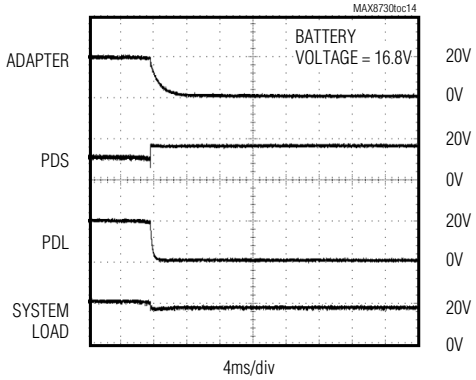
BATTERY REMOVAL



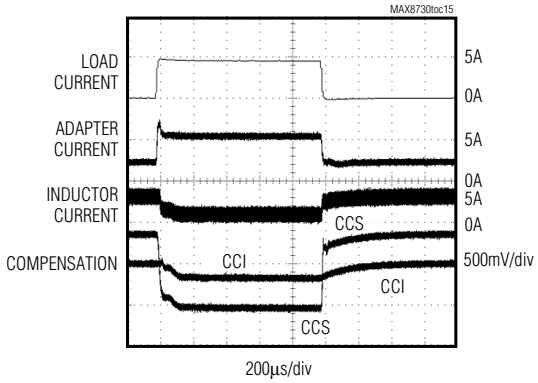
ADAPTER INSERTION



ADAPTER REMOVAL



SYSTEM LOAD TRANSIENT

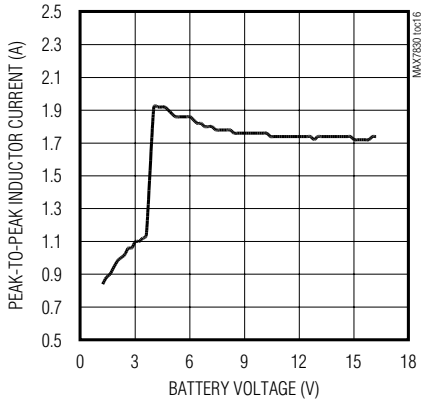


Low-Cost Battery Charger

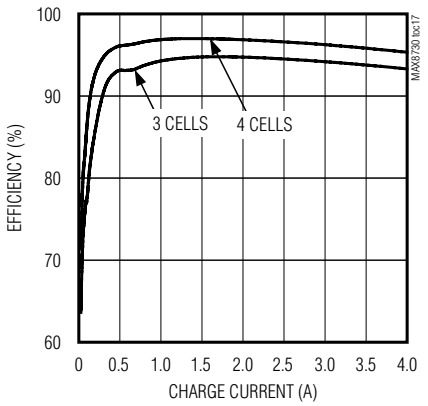
Typical Operating Characteristics (continued)

(Circuit of Figure 1, adapter = 19.5V, V_{BATT} = 12V, V_{ICTL} = 2.4V, MODE > 1.8V, REFON = INPON = LDO, V_{RELTH} = V_{REF}/2, T_A = +25°C, unless otherwise noted.)

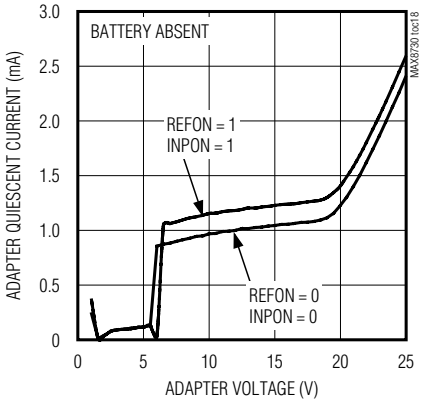
PEAK-TO-PEAK INDUCTOR CURRENT vs. BATTERY VOLTAGE



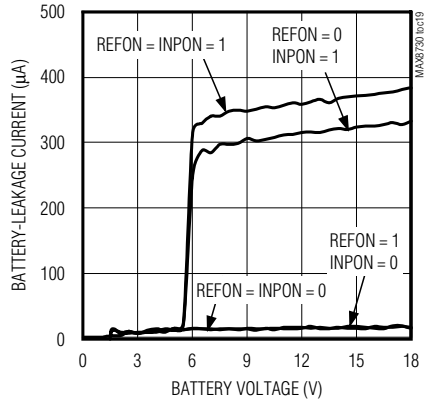
EFFICIENCY vs. CHARGE CURRENT



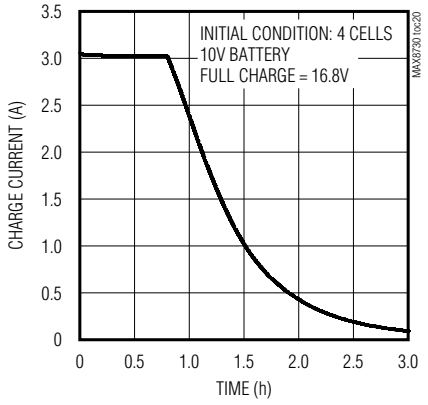
ADAPTER QUIESCENT CURRENT vs. ADAPTER VOLTAGE



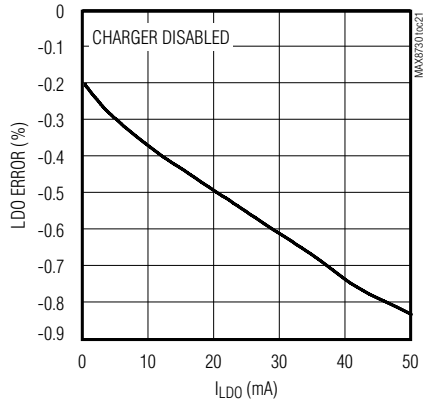
BATTERY LEAKAGE CURRENT vs. BATTERY VOLTAGE



CHARGE CURRENT vs. TIME



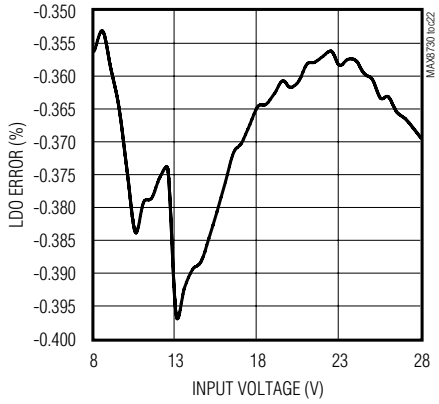
LDO LOAD REGULATION



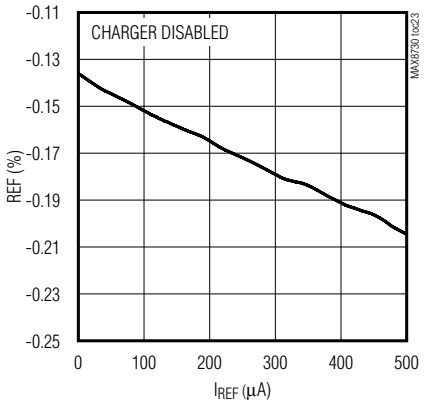
Typical Operating Characteristics (continued)

(Circuit of Figure 1, adapter = 19.5V, V_{BATT} = 12V, V_{ICTL} = 2.4V, MODE > 1.8V, REFON = INPON = LDO, V_{RELTH} = V_{REF}/2, T_A = +25°C, unless otherwise noted.)

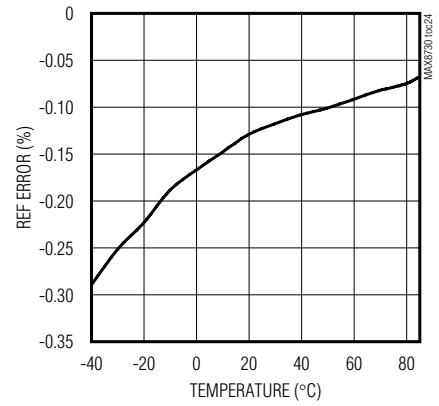
LDO LINE REGULATION



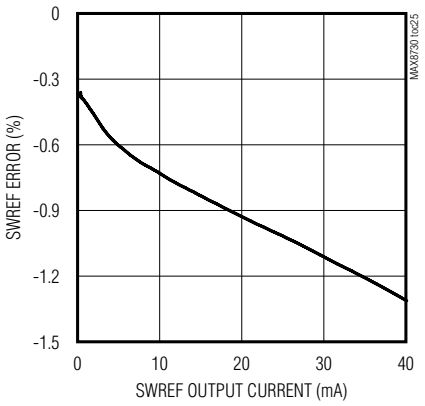
REFERENCE LOAD REGULATION



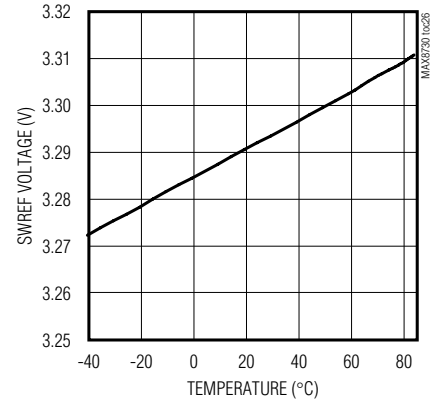
REF ERROR vs. TEMPERATURE



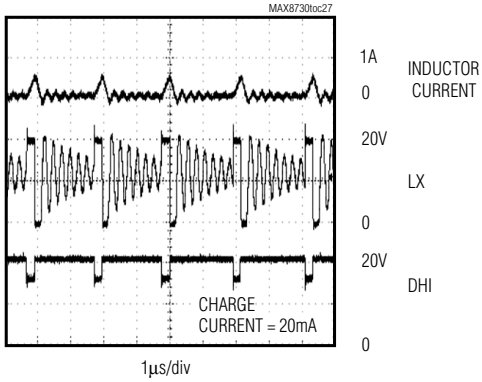
SWREF LOAD REGULATION



SWREF VOLTAGE vs. TEMPERATURE



DISCONTINUOUS MODE SWITCHING WAVEFORM



Low-Cost Battery Charger

Pin Description

PIN	NAME	FUNCTION
1	ASNS	Adapter Voltage Sense. When $V_{ASNS} > V_{BATT}$ - 280mV, the battery switch is turned off and the adapter switch is turned on. Connect to the adapter input using an RC filter as shown in Figure 1.
2	LDO	Linear-Regulator Output. LDO is the output of the 5.35V linear regulator supplied from SRC. Bypass LDO with a 1µF ceramic capacitor from LDO to GND.
3	SWREF	3.3V Switched Reference. SWREF is a 1% accurate linear regulator that can deliver 20mA. SWREF remains active when the adapter is absent and may be disabled by setting REFON to zero. Bypass SWREF with a 1µF capacitor to GND.
4	REF	4.2V Voltage Reference. Bypass REF with a 1µF capacitor to GND.
5	CLS	Source Current-Limit Input. Voltage input for setting the current limit of the input source.
6	ACIN	AC-Adapter-Detect Input. ACIN is the input to an uncommitted comparator. ACIN does not influence adapter and battery selection.
7	VCTL	Charge-Voltage-Control Input. Connect VCTL to LDO for default 4.2V/cell.
8	RELTH	Relearn Threshold for Relearn Mode. In relearn mode, when $V_{BATT} < 5 \times V_{RELTH}$, the MAX8730 drives PDS low and drives PDL high to terminate relearning of a discharged battery. See the *Relearn Mode* section for more details.
9	$\overline{ACOK}$	AC Detect Output. This open-drain output pulls low when ACIN is greater than REF/2 and ASNS is greater than BATT - 100mV. The $\overline{ACOK}$ output is high impedance when the MAX8730 is powered down. Connect a 10kΩ pullup resistor from LDO to $\overline{ACOK}$.
10	MODE	Tri-Level Input for Setting Number of Cells or Asserting the Conditioning Mode: MODE = GND; asserts relearn mode. MODE = Float; charge with 3 times the cell voltage programmed at VCTL. MODE = LDO; charge with 4 times the cell voltage programmed at VCTL.
11	IINP	Input-Current-Monitor Output. IINP sources the current proportional to the current sensed across CSSP and CSSN. The transconductance from (CSSP – CSSN) to IINP is 2.8µA/mV (typ).
12	ICTL	Charge-Current-Control Input. Pull ICTL to GND to shut down the charger.
13	REFON	SWREF Enable. Drive REFON high to enable SWREF.
14	INPON	Input Current-Monitor Enable. Drive INPON high to enable IINP.
15	CCI	Output Current-Regulation Loop Compensation Point. Connect a 0.01µF capacitor from CCS to GND.
16	CCV	Voltage-Regulation Loop Compensation Point. Connect a 10kΩ resistor in series with a 0.01µF capacitor to GND.
17	CCS	Input Current-Regulation Loop Compensation Point. Connect a 0.01µF capacitor from CCS to GND.
18	GND	Analog Ground
19	BATT	Battery-Voltage Feedback Input
20	CSIN	Charge-Current-Sense Negative Input
21	CSIP	Charge-Current-Sense Positive Input. Connect a current-sense resistor from CSIP to CSIN.
22	DHIV	High-Side Driver Supply. Connect a 0.1µF capacitor from DHIV to CSSN.
23	DHI	High-Side Power MOSFET Driver Output. Connect to high-side, p-channel MOSFET gate.
24	SRC	DC Supply Input Voltage and Connection for Driver for PDS/PDL Switches. Bypass SRC to power ground with a 1µF capacitor.
25	CSSN	Input Current Sense for Negative Input
26	CSSP	Input Current Sense for Positive Input. Connect a 15mΩ current-sense resistor from CSSP to CSSN.
27	PDS	Power-Source PMOS Switch Driver Output. When the adapter is absent, the PDS output is pulled to SRC through an internal 1MΩ resistor.
28	PDL	System-Load PMOS Switch Driver Output. When the adapter is absent, the PDL output is pulled to ground through an internal 100kΩ resistor.
29	Backside Paddle	Backside Paddle. Connect the backside paddle to analog ground.

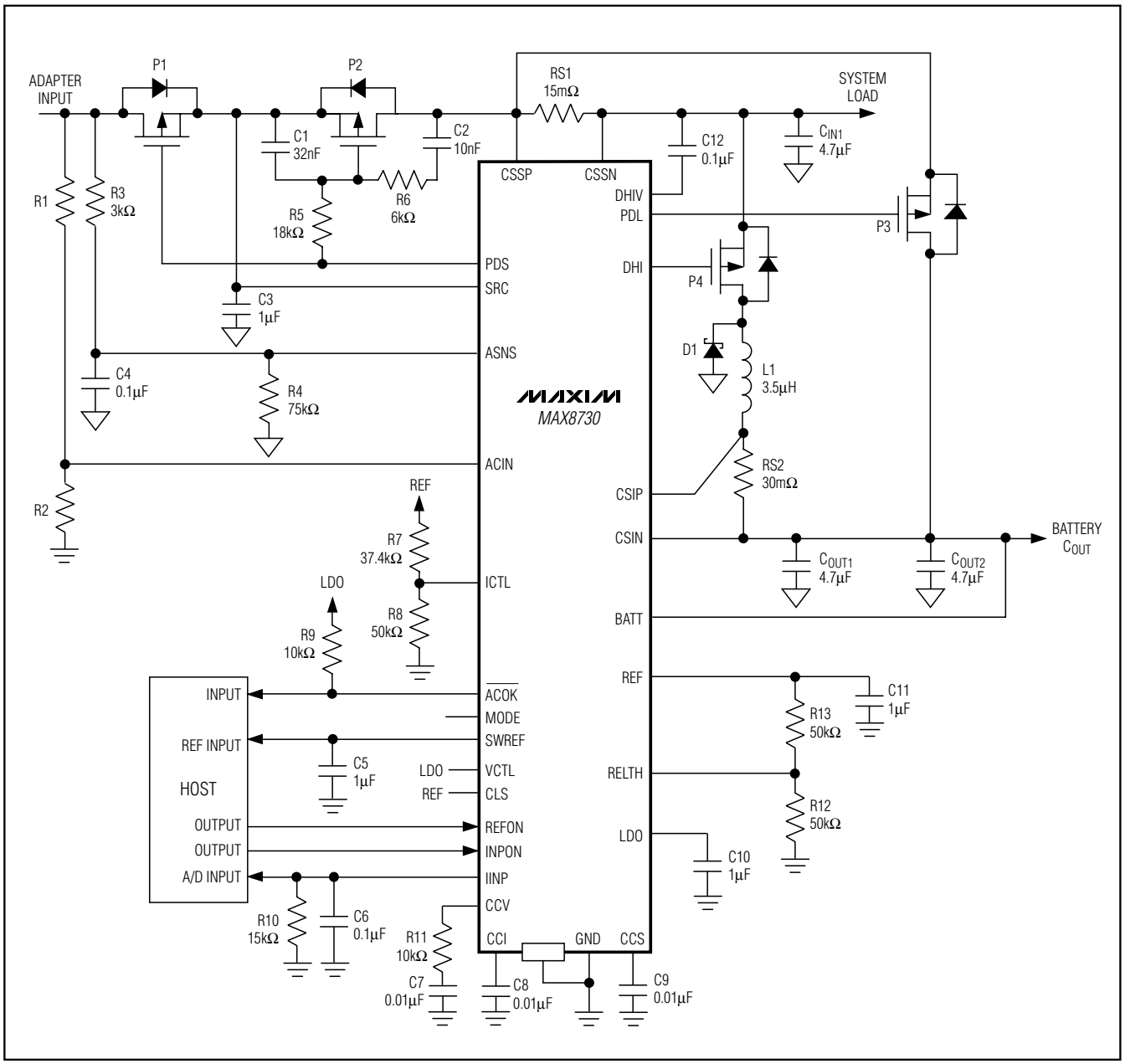


Figure 1. Typical Application Circuit

Low-Cost Battery Charger

Detailed Description

The MAX8730 includes all the functions necessary to charge Li+, NiMH, and NiCd batteries. A high-efficiency, step-down, DC-DC converter is used to implement a precision constant-current, constant-voltage charger. The DC-DC converter drives a p-channel MOSFET and uses an external free-wheeling Schottky diode. The charge current and input current-sense amplifiers have low-input offset errors, allowing the use of small-value sense resistors for reduced power dissipation. Figure 2 is the functional diagram.

The MAX8730 features a voltage-regulation loop (CCV) and two current-regulation loops (CCI and CCS). The loops operate independently of each other. The CCV voltage-regulation loop monitors BATT to ensure that its voltage never exceeds the voltage set by VCTL. The CCI battery current-regulation loop monitors current delivered to BATT to ensure that it never exceeds the current limit set by ICTL. The charge-current-regulation loop is in control as long as the battery voltage is below the set point. When the battery voltage reaches its set point, the voltage-regulation loop takes control and maintains the battery voltage at the set point. A third loop (CCS) takes control and reduces the charge current when the adapter current exceeds the input current limit set by CLS.

The ICTL, VCTL, and CLS analog inputs set the charge current, charge voltage, and input-current limit, respectively. For standard applications, default set points for VCTL provide 4.2V per-cell charge voltage. The MODE input selects a 3- or 4-cell mode.

Based on the presence or absence of the AC adapter, the MAX8730 provides an open-drain logic output signal (ACOK) and connects the appropriate source to the system. P-channel MOSFETs controlled from the PDL and PDS select the appropriate power source. The MODE input allows the system to perform a battery relearning cycle. During a relearning cycle, the battery is isolated from the charger and completely discharged through the system load. When the battery reaches 100% depth of discharge, PDL turns off and PDS turns on to connect the adapter to the system and to allow the battery to be recharged to full capacity.

Setting Charge Voltage

The VCTL input adjusts the battery output voltage, V_{BATT}. This voltage is calculated by the following equation:

$$V_{BATT} = CELLS \times (4V + \frac{V_{VCTL}}{9})$$

where CELLS is the number of cells selected with the MODE input (see Table 1). Connect MODE to LDO for 4-cell operation. Float the MODE input for 3-cell operation.

The battery-voltage accuracy depends on the absolute value of VCTL, and the accuracy of the resistive voltage-divider that sets VCTL. Calculate the battery voltage accuracy according to the following equation:

$$V_{BATT\_ERROR} = E_0 + 100\% \times \left(\frac{I_{VCTL} \times R_{VCTL}}{36} - 1\right)$$

where E_0 is the worst-case MAX8730 battery voltage error when using 1% resistors (0.83%), I_{VCTL} is the VCTL input bias current (4µA), and R_{VCTL} is the impedance at VCTL. Connect VCTL to LDO for the default setting of 4.20V/cell with 0.7% accuracy.

Connect MODE to GND to enter relearn mode, which allows the battery to discharge into the system while the adapter is present; see the *Relearn Mode Section*.

Table 1. Cell-Count Programming

CELLS	CELL COUNT
GND	Relearn mode
Float	3
LDO	4

Setting Charge Current

ICTL sets the maximum voltage across current-sense resistor RS2, which determines the charge current. The full-scale differential voltage between CSIP and CSIN is 135mV (4.5A for RS2 = 30mΩ). Set ICTL according to the following equation:

$$V_{ICTL} = I_{CHG} \times RS2 \times \frac{3.6V}{135mV}$$

The input range for ICTL is 0 to 3.6V. To shut down the charger, pull ICTL below 65mV. Choose a current-sense resistor (RS2) to have a sufficient power rating to handle the full-charge current. The current-sense voltage may be reduced to minimize the power dissipation. However, this can degrade accuracy due to the current-sense amplifier's input offset (±2mV). See the *Typical Operating Characteristics* to estimate the charge-current accuracy at various set points. The charge-current error amplifier (GMI) is compensated at the CCI pin. See the *Compensation* section.

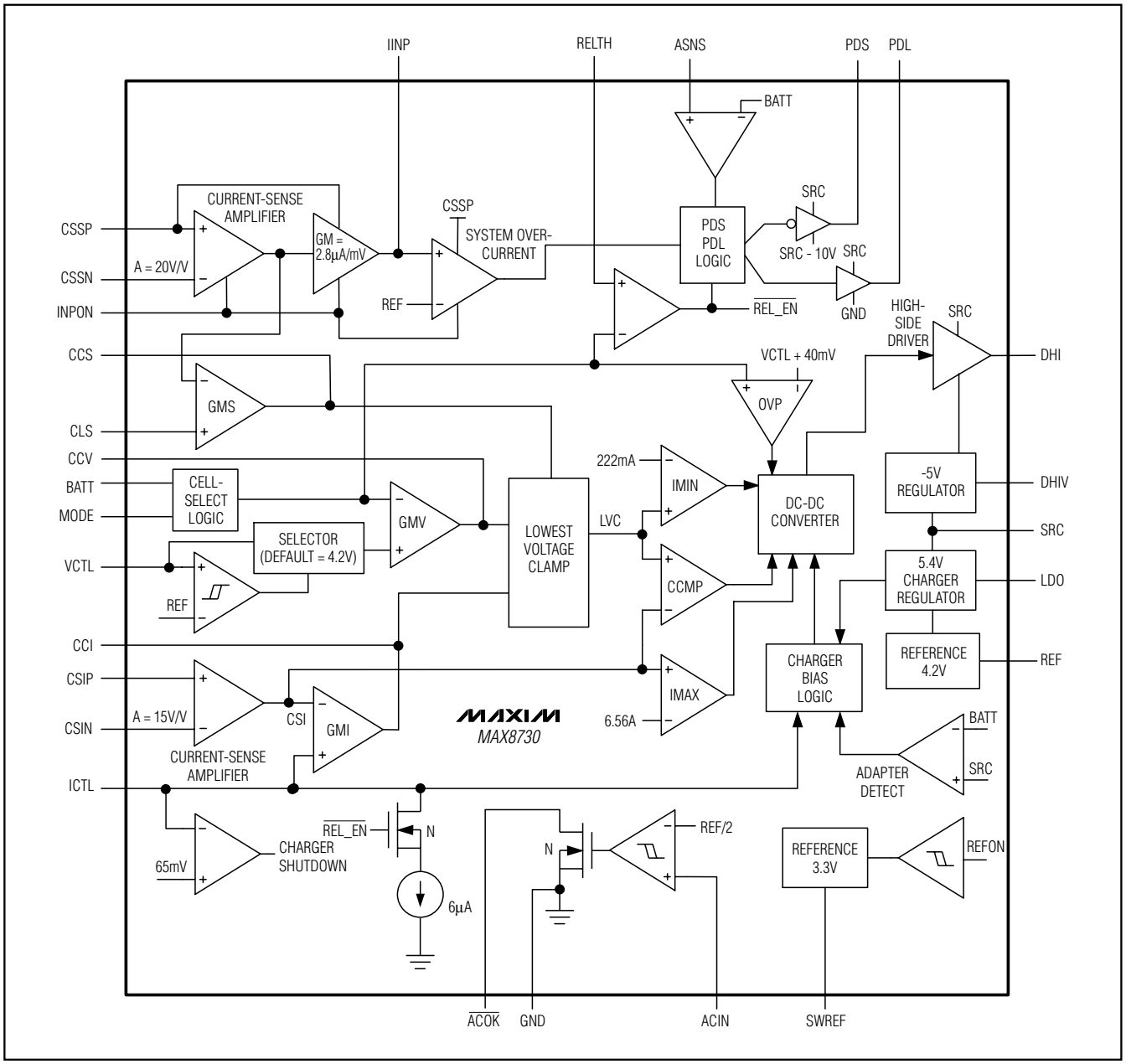


Figure 2. Functional Diagram

Low-Cost Battery Charger

The MAX8730 includes a foldback feature, which reduces the Schottky requirement at low battery voltages. See the *Foldback Current Section*.

Setting Input-Current Limit

The total input current, from a wall adapter or other DC source, is the sum of the system supply current and the current required by the charger. When the input current exceeds the set input current limit, the MAX8730 decreases the charge current to provide priority to system load current. System current normally fluctuates as portions of the system are powered up or put to sleep. The input-current-limit circuit reduces the power requirement of the AC wall adapter, which reduces adapter cost. As the system supply rises, the available charge current drops linearly to zero. Thereafter, the total input current can increase without limit.

The total input current is the sum of the device supply current, the charger input current, and the system load current. The total input current can be estimated as follows:

$$I_{INPUT} = I_{LOAD} + \frac{I_{CHARGE} \times V_{BATTERY}}{V_{IN} \times \eta}$$

where η is the efficiency of the DC-DC converter (typically 85% to 95%).

CLS sets the maximum voltage across the current-sense resistor RS1, which determines the input current limit. The full-scale differential voltage between CSSP and CSSN is 75mV (5A for RS1 = 15mΩ). Set CLS according to the following equation:

$$V_{CLS} = I_{LIMIT} \times RS1 \times \frac{V_{REF}}{75mV}$$

The input range for CLS is 1.1V to V_{REF}. Choose a current-sense resistor (RS1) to have a sufficient power rating to handle the full system current. The current-sense resistor may be reduced to improve efficiency, but this degrades accuracy due to the current-sense amplifier's input offset (±3mV). See the *Typical Operating Characteristics* to estimate the input current-limit accuracy at various set points. The input current-limit error amplifier (GMS) is compensated at the CCS pin; see the *Compensation* section.

Input-Current Measurement

IINP monitors the system-input current sensed across CSSP and CSSN. The voltage of IINP is proportional to the input current according to the following equation:

$$V_{IINP} = I_{INPUT} \times RS1 \times G_{IINP} \times R_{10}$$

where I_{INPUT} is the DC current supplied by the AC adapter, G_{IINP} is the transconductance of IINP (2.8µA/mV typ), and R_{10} is the resistor connected between IINP and ground. Connect a 0.1µF filter capacitor from IINP to GND to reduce ripple. IINP has a 0 to 4.5V output-voltage range. Connect IINP to GND if it is not used.

The MAX8730 provides a short-circuit latch to protect against system overload or short. The latch is set when V_{IINP} rises above 4.2V, and disconnects the adapter from the system by turning PDS off (PDL does not change). The latch is reset by bringing SRC below UVLO (remove and reinsert the adapter). Choose a filter capacitor that is large enough to provide appropriate debouncing and prevent accidental faults, yet results in a response time that is fast enough to thermally protect the MOSFETs. See the *System Short Circuit* section.

IINP can be used to measure battery-discharge current (see Figure 1) when the adapter is absent. To disable IINP and reduce battery consumption to 10µA, drive INPON to low. Charging is disabled when INPON is low, even if the adapter is present.

AC-Adapter Detection and Power-Source Selection

The MAX8730 includes a hysteretic comparator that detects the presence of an AC power adapter and automatically selects the appropriate power source. When the adapter is present ($V_{ASNS} > V_{BATT}$ - -100mV) the battery is disconnected from the system load with the p-channel (P3) MOSFET. When the adapter is removed ($V_{ASNS} < V_{BATT}$ - -270mV), PDS turns off and PDL turns on with a 5µs break-before-make sequence.

The ACOK output can be used to indicate the presence of the adapter. When $V_{ACIN} > 2.1V$ and $V_{ASNS} > V_{BATT}$ - 100mV, ACOK becomes low. Connect a 10kΩ pullup resistor between LDO and ACOK. Use a resistive voltage-divider from the adapter's output to the ACIN pin to set the appropriate detection threshold. Since ACIN has a 6V absolute maximum rating, set the adapter threshold according to the following equation:

$$V_{ADAPTER\_THRESHOLD} > \frac{V_{ADAPTER\_MAX}}{3}$$

Relearn Mode

The MAX8730 can be programmed to perform a relearn cycle to calibrate the battery's fuel gauge. This cycle consists of isolating the battery from the charger and discharging it through the system load. When the battery

reaches 100% depth of discharge, it is then recharged. Connect MODE to GND to place the MAX8730 in relearn mode. In relearn mode, charging stops, PDS turns off, and PDL turns on.

To utilize relearn mode, there must be two source-connected MOSFETs to prevent the AC adapter from supplying current to the system through the P1's body diode. Connect SRC to the common source node of two MOSFETs.

The system must alert the user before performing a relearn cycle. If the user removes the battery during relearn mode, the MAX8730 detects battery removal and reconnects the AC adapter (PDS turns on and PDL turns off). Battery removal is detected when the battery falls below 5xRELTH.

LDO Regulator, REF, and SWREF

An integrated linear regulator (LDO) provides a 5.35V supply derived from SRC, and delivers over 10mA of load current. LDO biases the 4.2V reference (REF) and most of the control circuitry. Bypass LDO to GND with a 1µF ceramic capacitor. An additional standalone 1%, 3.3V linear regulator (SWREF) provides 20mA and can remain on when the adapter is absent. Set REFON low to disable SWREF. Set REFON high for normal operation. SWREF must be enabled to allow charging.

Operating Conditions

- **Adapter present:** The adapter is considered to be present when:
  V_{SRC} > 8V (max)
  V_{ASNS} > V_{BATT} - 300mV (max)
- **Charging:** The MAX8730 allows charging when:
  V_{SRC} - V_{CSIN} > 100mV (typ)
  3 or 4 cells selected (MODE float or high condition)
  ICTL > 110mV (max)
  INPON is high
- **Relearn mode:** The MAX8730 enables relearn mode when:
  V_{BATT} / 5 > V_{RELTH}
  MODE is grounded

DC-DC Converter

The MAX8730 employs a step-down DC-DC converter with a p-channel MOSFET switch and an external Schottky diode. The MAX8730 features a constant-current-ripple, current-mode control scheme with cycle-by-cycle current limit. For light loads, the MAX8730 operates in discontinuous conduction mode for improved efficiency. The operation of the DC-DC controller is determined by the following four comparators as shown in the functional block diagram in Figure 3:

- The **IMIN** comparator sets the peak inductor current in discontinuous mode. IMIN compares the control signal (LVC) against 100mV (corresponding to 222mA when RS2 = 30mΩ). The comparator terminates the switch on-time when IMIN exceeds the threshold.
- The **CCMP** comparator is used for current-mode regulation in continuous conduction mode. CCMP compares LVC against the charging-current feedback signal (CSI). The comparator output is high and the MOSFET on-time is terminated when the CSI voltage is higher than LVC.
- The **IMAX** comparator provides a cycle-by-cycle current limit. IMAX compares CSI to 2.95V (corresponding to 6.56A when RS2 = 30mΩ). The comparator output is high and the MOSFET on-time is terminated when the current-sense signal exceeds 6.56A. A new cycle cannot start until the IMAX comparator output goes low.
- The **OVP** comparator is used to prevent overvoltage at the output due to battery removal. OVP compares BATT against the set voltage; see the *Setting Charge Voltage* section. When BATT is 20mV x CELLS above the set value, OVP goes high and the MOSFET on-time is terminated.

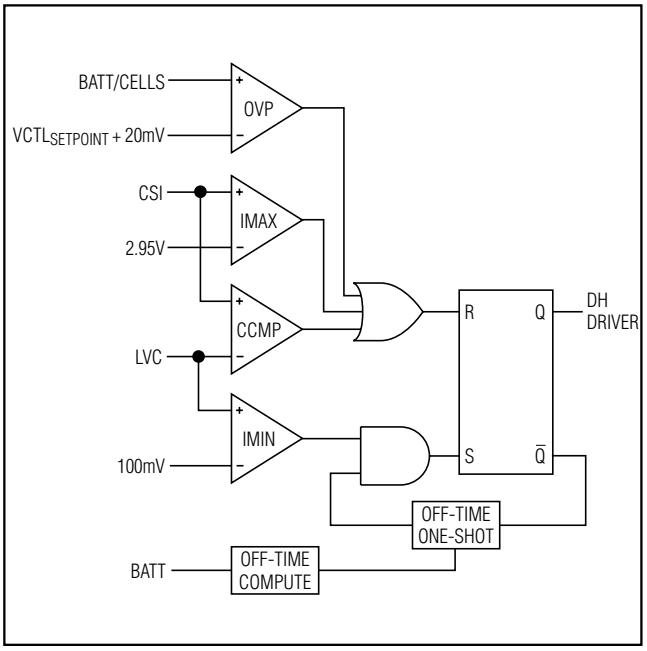


Figure 3. DC-DC Converter Block Diagram

Low-Cost Battery Charger

CCV, CCI, CCS, and LVC Control Blocks

The MAX8730 controls input current (CCS control loop), charge current (CCI control loop), or charge voltage (CCV control loop), depending on the operating condition. The three control loops—CCV, CCI, and CCS—are brought together internally at the lowest voltage clamp (LVC) amplifier. The output of the LVC amplifier is the feedback control signal for the DC-DC controller. The minimum voltage at the CCV, CCI, or CCS appears at the output of the LVC amplifier and clamps the other control loops to within 0.3V above the control point. Clamping the other two control loops close to the lowest control loop ensures fast transition with minimal overshoot when switching between different control loops (see the *Compensation* section).

Continuous-Conduction Mode

With sufficient charge current, the MAX8730's inductor current never crosses zero, which is defined as continuous-conduction mode. The controller starts a new cycle by turning on the high-side MOSFET. When the charge-current feedback signal (CSI) is greater than the control point (LVC), the CCMP comparator output goes high and the controller initiates the off-time by turning off the MOSFET. The operating frequency is governed by the off-time, which depends upon V_{BATT}.

At the end of the fixed off-time, the controller initiates a new cycle only if the control point (LVC) is greater than 100mV, and the peak charge current is less than the cycle-by-cycle current limit. Restated another way, IMIN must be high, IMAX must be low, and OVP must be low for the controller to initiate a new cycle. If the peak inductor current exceeds the IMAX comparator threshold or the output voltage exceeds the OVP threshold, then the on-time is terminated. The cycle-by-cycle current limit protects against overcurrent and short-circuit faults.

The MAX8730 computes the off-time by measuring V_{BATT}:

$$t_{OFF} = 5.6\mu s / V_{BATT}$$

for $V_{BATT} > 4V$.

The switching frequency in continuous mode varies according to the equation:

$$f = \frac{1}{5.6V \times \mu s \times \left(\frac{1}{V_{SRC} - V_{BATT}} + \frac{1}{V_{BATT}} \right)}$$

Discontinuous Conduction

The MAX8730 operates in discontinuous conduction mode at light loads to make sure that the inductor current is always positive. The MAX8730 enters discontinuous conduction mode when the output of the LVC control point falls below 100mV. For RS2 = 30mΩ, this corresponds to a peak inductor current of 222mA:

$$I_{DIS} = \frac{1}{2} \times \frac{100mV}{15 \times RS2} = 111mA$$

The MAX8730 implements slope compensation in discontinuous mode to eliminate multipulsing. This prevents audible noise and minimizes the output ripple.

Compensation

The charge-voltage and charge current-regulation loops are compensated separately and independently at the CCV, CCI, and CCS pins.

CCV Loop Compensation

The simplified schematic in Figure 4 is sufficient to describe the operation of the MAX8730 when the voltage loop (CCV) is in control. The required compensation network is a pole-zero pair formed with C_{CV} and R_{CV}. The pole is necessary to roll off the voltage loop's response at low frequency. The zero is necessary to compensate the pole formed by the output capacitor and the load. R_{ESR} is the equivalent series resistance (ESR) of the charger output capacitor (C_{OUT}). R_L is the equivalent charger output load, where $R_L = \Delta V_{BATT} / \Delta I_{CHG}$. The equivalent output impedance of the GMV

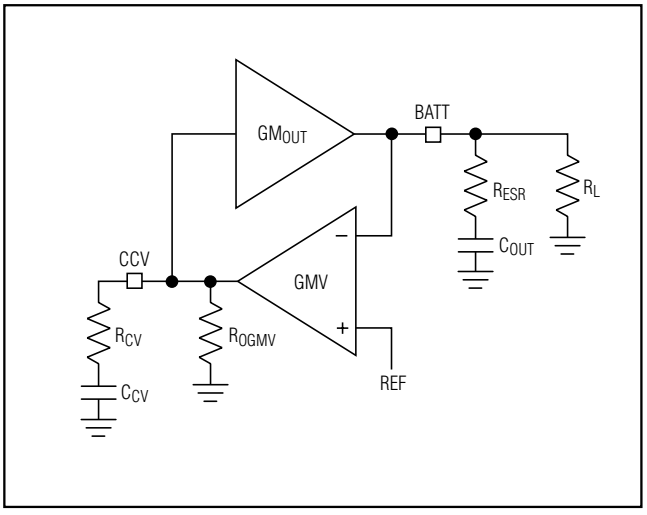


Figure 4. CCV Loop Diagram

amplifier, R_{OGMV}, is greater than 10MΩ. The voltage amplifier transconductance, GMV = 0.125µA/mV for 4 cells and 0.167µA/mV for 3 cells. The DC-DC converter transconductance is dependent upon the charge current-sense resistor RS2:

$$GM_{OUT} = \frac{1}{A_{CSI} \times RS2}$$

where A_{CSI} = 15V/V and RS2 = 30mΩ in the typical application circuits, so GM_{OUT} = 2.22A/V.

The loop transfer function is given by:

$$LTF = GM_{OUT} \times R_L \times GMV \times R_{OGMV} \times \frac{(1 + sC_{OUT} \times R_{ESR})(1 + sC_{CV} \times R_{CV})}{(1 + sC_{CV} \times R_{OGMV})(1 + sC_{OUT} \times R_L)}$$

The poles and zeros of the voltage-loop transfer function are listed from lowest frequency to highest frequency in Table 2.

Near crossover, C_{CV} is much lower impedance than R_{OGMV}. Since C_{CV} is in parallel with R_{OGMV}, C_{CV} dominates the parallel impedance near crossover. Additionally R_{CV} is much higher impedance than C_{CV} and dominates the series combination of R_{CV} and C_{CV}, so:

$$\frac{R_{OGMV} \times (1 + sC_{CV} \times R_{CV})}{(1 + sC_{CV} \times R_{OGMV})} \cong R_{CV}$$

C_{OUT} is typically much lower impedance than R_L near crossover so the parallel impedance is mostly capacitive and:

$$\frac{R_L}{(1 + sC_{OUT} \times R_L)} \cong \frac{1}{sC_{OUT}}$$

If R_{ESR} is small enough, its associated output zero has a negligible effect near crossover and the loop-transfer function can be simplified as follows:

$$LTF = GM_{OUT} \times \frac{R_{CV}}{sC_{OUT}} G_{MV}$$

Setting the LTF = 1 to solve for the unity-gain frequency yields:

$$f_{CO\_CV} = GM_{OUT} \times G_{MV} \times \frac{R_{CV}}{2\pi \times C_{OUT}}$$

For stability, choose a crossover frequency lower than 1/5 the switching frequency. For example, choosing a crossover frequency of 45kHz and solving for R_{CV} using the component values listed in Figure 1 yields R_{CV} = 10kΩ:

$$R_{CV} = \frac{2\pi \times C_{OUT} \times f_{CO\_CV}}{GMV \times GM_{OUT}} \cong 10k\Omega$$

Table 2. CCV Loop Poles and Zeros

NAME	EQUATION	DESCRIPTION
CCV pole	$f_{P\_CV} = \frac{1}{2\pi R_{OGMV} \times C_{CV}}$	Lowest frequency pole created by C_{CV} and GMV's finite output resistance. Since R_{OGMV} is very large and not well controlled, the exact value for the pole frequency is also not well controlled (R_{OGMV} > 10MΩ).
CCV zero	$f_{Z\_CV} = \frac{1}{2\pi R_{CV} \times C_{CV}}$	Voltage-loop compensation zero. If this zero is at the same frequency or lower than the output pole f_{P_OUT}, then the loop-transfer function approximates a single-pole response near the crossover frequency. Choose C_{CV} to place this zero at least 1 decade below crossover to ensure adequate phase margin.
Output pole	$f_{P\_OUT} = \frac{1}{2\pi R_L \times C_{OUT}}$	Output pole formed with the effective load resistance R_L and output capacitance C_{OUT}. R_L influences the DC gain but does not affect the stability of the system or the crossover frequency.
Output zero	$f_{Z\_OUT} = \frac{1}{2\pi R_{ESR} \times C_{OUT}}$	Output ESR Zero. This zero can keep the loop from crossing unity gain if f_{Z_OUT} is less than the desired crossover frequency; therefore, choose a capacitor with an ESR zero greater than the crossover frequency.

Low-Cost Battery Charger

where:

V_{BATT} = 16.8V

GMV = 0.125µA/mV

GM_{OUT} = 2.22A/V

C_{OUT} = 10µF

f_{OSC} = 350kHz (minimum occurs at V_{IN} = 19V and V_{BATT} = 16.8V)

R_L = 0.2Ω

f_{CO-CV} = 45kHz

To ensure that the compensation zero adequately cancels the output pole, select $f_{Z\_CV} \le f_{P\_OUT}$:

$$C_{CV} \ge (R_L / R_{CV})\, C_{OUT}$$

$$C_{CV} \ge 200pF$$

Figure 5 shows the Bode plot of the voltage-loop frequency response using the values calculated above.

CCI Loop Compensation

The simplified schematic in Figure 6 is sufficient to describe the operation of the MAX8730 when the battery current loop (CCI) is in control. Since the output capacitor's impedance has little effect on the response of the current loop, only a simple single pole is required to compensate this loop. A_{CSI} is the internal gain of the current-sense amplifier. RS2 is the charge-current-sense resistor (30mΩ). R_{OGMI} is the equivalent output impedance of the GMI amplifier, which is greater than 10MΩ. GMI is the charge-current amplifier transconductance = 1µA/mV. GM_{OUT} is the DC-DC converter transconductance = 2.22A/V.

The loop transfer function is given by:

$$LTF = GM_{OUT} \times A_{CSI} \times RS \times GMI \frac{R_{OGMI}}{1 + sR_{OGMI} \times C_{CI}}$$

that describes a single-pole system. Since:

$$GM_{OUT} = \frac{1}{A_{CSI} \times RS}$$

the loop-transfer function simplifies to:

$$LTF = GMI \frac{R_{OGMI}}{1 + sR_{OGMI} \times C_{CI}}$$

The crossover frequency is given by:

$$f_{CO\_CI} = \frac{GMI}{2\pi C_{CI}}$$

For stability, choose a crossover frequency lower than 1/10 of the switching frequency:

$$C_{CI} > \frac{10 \times GMI}{2\pi \times C_{CI}} = 4nF$$

Values for C_{CI} greater than 10 times the minimum value may slow down the current-loop response. Choosing C_{CI} = 10nF yields a crossover frequency of 15.9kHz. Figure 7 shows the Bode plot of the current-loop frequency response using the values calculated above.

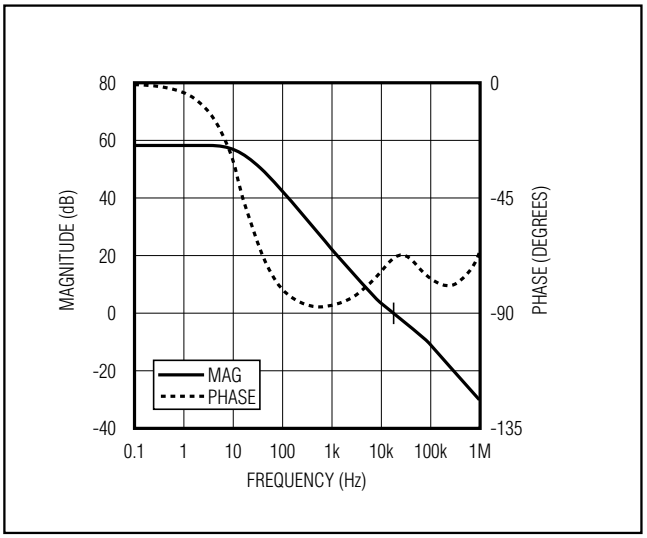


Figure 5. CCV Loop Response

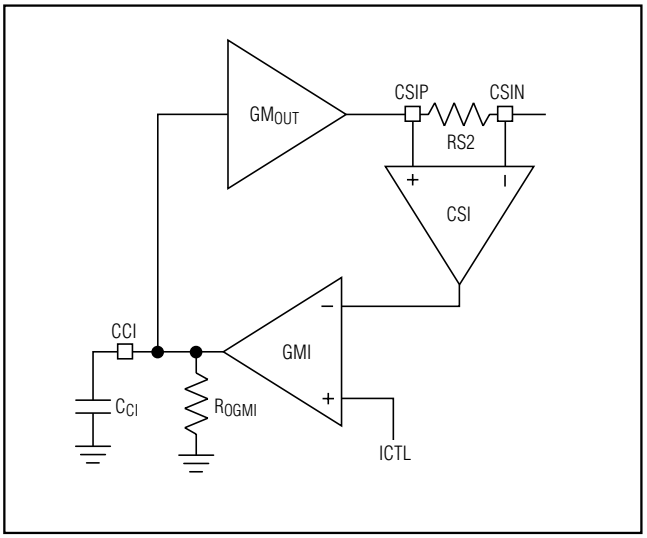


Figure 6. CCI Loop Diagram

CCS Loop Compensation

The simplified schematic in Figure 8 is sufficient to describe the operation of the MAX8730 when the input current-limit loop (CCS) is in control. Since the output capacitor's impedance has little effect on the response of the input current-limit loop, only a single pole is required to compensate this loop. A_{CSS} is the internal gain of the current-sense amplifier, RS1 = 10mΩ in the typical application circuits. R_{OGMS} is the equivalent output impedance of the GMS amplifier, which is greater than 10MΩ. GMS is the charge-current amplifier transconductance = 1µA/mV. GM_{IN} is the DC-DC converter's input-referred transconductance = GM_{OUT}/D = 2.22A/V/D.

The loop-transfer function is given by:

$$LTF = GM_{IN} \times A_{CSS} \times RSI \times GMS \frac{R_{OGMS}}{1 + SR_{OGMS} \times C_{CS}}$$

$$\text{Since } GM_{IN} = \frac{1}{A_{CSS} \times RS2}$$

the loop-transfer function simplifies to:

$$LTF = GMS \frac{R_{OGMS}}{1 + SR_{OGMS} \times C_{CS}} \times RS1/RS2$$

The crossover frequency is given by:

$$f_{CO\_CS} = \frac{GMS}{2\pi C_{CS}} \times \frac{V_{IN\_MAX}}{V_{BATT\_MIN}}$$

For stability, choose a crossover frequency lower than 1/10 of the switching frequency:

$$C_{CS} = 5 \times \frac{GMS}{2\pi f_{OSC}} \times \frac{V_{IN\_MAX}}{V_{BATT\_MIN}}$$

Values for CCS greater than 10 times the minimum value may slow down the current-loop response excessively. Figure 9 shows the Bode plot of the input current-limit-loop frequency response using the values calculated above.

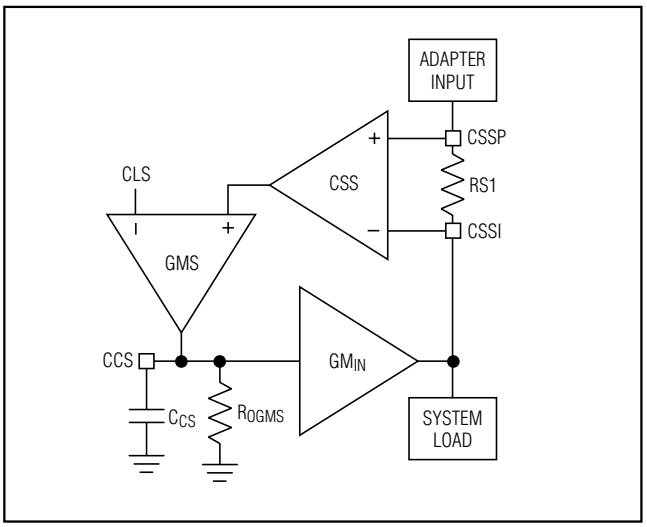


Figure 8. CCI Loop Diagram

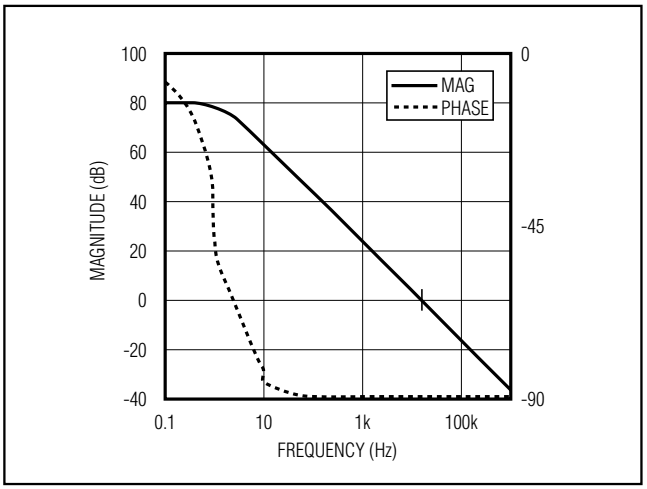


Figure 7. CCI Loop Response

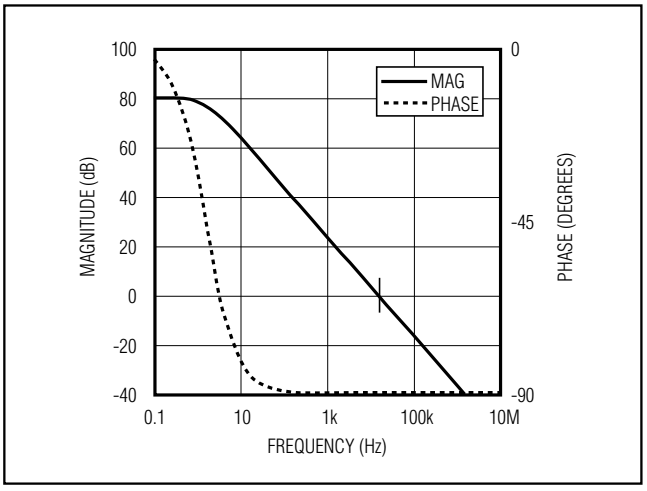


Figure 9. CCS Loop Response

Low-Cost Battery Charger

MOSFET Drivers

The DHI output is optimized for driving moderate-sized power MOSFETs. This is consistent with the variable duty factor that occurs in the notebook computer environment where the battery voltage changes over a wide range. DHI swings from SRC to DHIV and has a typical impedance of 1Ω sourcing and 4Ω sinking.

Design Procedure

MOSFET Selection

Choose the p-channel MOSFETs according to the maximum required charge current. The MOSFET (P4) must be able to dissipate the resistive losses plus the switching losses at both $V_{SRC(MIN)}$ and $V_{SRC(MAX)}$.

The worst-case resistive power losses occur at the maximum battery voltage. Calculate the resistive losses according to the following equation:

$$PD_{Resistance} = \frac{V_{BATT}}{V_{SRC}} \times I_{CHG}^2 \times R_{DS(ON)}$$

Calculate the switching losses according to the following equation:

$$PD_{SWITCHING} = \frac{1}{2} \times \frac{\left(\frac{2 \times Q_G}{I_{GATE}} \times V_{SRC(MAX)} \times I_{CHG}\right) + \left(V_{SRC(MAX)}^2 \times C_{RSS}\right)}{f}$$

where C_{RSS} is the reverse transfer capacitance of the MOSFET, and I_{GATE} is the peak gate-drive source/sink current.

These calculations provide an estimate and are not a substitute for breadboard evaluation, preferably including a verification using a thermocoupler mounted on the MOSFET.

Generally, a small MOSFET is desired to reduce switching losses at $V_{BATT} = V_{SRC} / 2$. This requires a tradeoff between gate charge and resistance. Switching losses in the MOSFET can become significant when the maximum AC adapter voltage is applied. If the MOSFET that was chosen for adequate $R_{DS(ON)}$ at low supply voltages becomes hot when subjected to $V_{SRC(MAX)}$, then choose a MOSFET with lower gate charge. The actual switching losses that can vary due to factors include the internal gate resistance, threshold voltage, source inductance, and PC board layout characteristics.

See Table 3 for suggestions about MOSFET selection.

Schottky Selection

The Schottky diode conducts the inductor current during the off-time. Choose a Schottky diode with the appropriate thermal resistance to guarantee that it does not overheat:

$$\theta_{JA} < \frac{T_{J\_MAX} - T_{A\_MAX}}{V_F \times I_{CHG} \times \left(1 - \frac{V_{BATT\_MIN}}{V_{SRC\_MAX}}\right)}$$

Table 3. Recommended MOSFETs

CHARGE CURRENT (A)	MOSFET	PIN-PACKAGE	MAX		$R\theta_{JA}$ (°/W)	T_{MAX} (°C)
			Q_G (nC)	R_{DSON} (mΩ)		
3	Si3457DV	6-SOT23	8	75	78	+150
2.5	FDC658P	6-SOT23	12	75	78	+150
3.5	FDS9435A	8-SO	14	80	50	+175
3.5	NDS9435A	8-SO	14	80	50	+175
4	FDS4435	8-SO	24	35	50	+175
4	FDS6685	8-SO	24	35	50	+175
4.5	FDS6675A	8-SO	34	19	50	+175

where θ_{JA} is the thermal resistance of the package (in °C/W), T_{J_MAX} is the maximum junction temperature of the diode, T_{A_MAX} is the maximum ambient temperature of the system, and V_F is the forward voltage of the Schottky diode.

The Schottky size and cost can be reduced by utilizing the MAX8730 foldback function. See the *Foldback Current* section for more information.

Select the Schottky diode to minimize the battery leakage current when the charger is shut down.

Inductor Selection

The MAX8730 uses a fixed inductor current ripple architecture to minimize the inductance. The charge current, ripple, and operating frequency (off-time) affects inductor selection. For a good trade-off of inductor size and efficiency, choose the inductance according to the following equation:

$$L = \frac{k_{OFF}}{0.4 \times I_{CHG}}$$

where k_{OFF} is the off-time constant (5.6V x µs typically).

Higher inductance values decrease the RMS current at the cost of inductor size.

Inductor L1 must have a saturation current rating of at least the maximum charge current plus 1/2 of the ripple current (ΔI_L):

$$I_{SAT} = I_{CHG} + (1/2)\,\Delta I_L$$

The ripple current is determined by:

$$\Delta I_L = \frac{k_{OFF}}{L}$$

The ripple current is only dependent on inductance value and is independent of input and output voltage. See the Ripple Current vs. V_{BATT} graph in the *Typical Operating Characteristics*.

See Table 4 for suggestions about inductor selection.

Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. Ceramic capacitors are preferred due to their resilience to power-up surge currents:

$$I_{RMS} = I_{CHG}\left(\frac{\sqrt{V_{BATT}(V_{SRC} - V_{BATT})}}{V_{SRC}}\right) = \frac{I_{CHG}}{2}$$

at 50% duty cycle.

The input capacitors should be sized so that the temperature rise due to ripple current in continuous conduction does not exceed about 10°C. The maximum ripple current occurs at 50% duty factor or $V_{SRC} = 2 \times V_{BATT}$, which equates to $0.5 \times I_{CHG}$. If the application of interest does not achieve the maximum value, size the input capacitors according to the worst-case conditions. See Table 5 for suggestions about input capacitor selection.

Table 4. Recommended Inductors

APPLICATION (A)	INDUCTOR	SIZE (mm)	L (µH)	I_{SAT} (A)	R_L (mΩ)
2.5	CDRH6D38	8.3 x 8.3 x 3	3.3	3.5	20
2.5	CDRH8D28	7 x 7 x 4	4.7	3.4	24.7
3.5	CDRH8D38	8.3 x 8.3 x 4	3.5	4.4	24

Table 5. Recommended Input Capacitors

APPLICATION (A)	INPUT CAPACITOR	CAPACITANCE(µF)	VOLTS (V)	RMS AT 10°C (A)
< 3	GMK316F47S2G	4.7	35	1.8
< 4	GMK325F106ZH	4.7	35	2.4
< 4	TMK325BJ475MN	10	25	2.5

Low-Cost Battery Charger

Output Capacitor Selection

The output capacitor absorbs the inductor ripple current and must tolerate the surge current delivered from the battery when it is initially plugged into the charger. As such, both capacitance and ESR are important parameters in specifying the output capacitor as a filter and to ensure stability of the DC-DC converter (see the *Compensation* section). Beyond the stability requirements, it is often sufficient to make sure that the output capacitor's ESR is much lower than the battery's ESR. Either tantalum or ceramic capacitors can be used on the output. Ceramic devices are preferable because of their good voltage ratings and resilience to surge currents. For a ceramic output capacitor, select the capacitance according to the following equation:

$$C_{OUT} > \frac{k_{OFF}^2}{8 \times L \times V_{RIPPLE}} \times \left(\frac{1}{V_{SRC} - V_{BATT}} + \frac{1}{V_{BATT}} \right)$$

The output ripple requirement of a charger is typically only constrained by the overvoltage protection circuitry of the battery protector and the overvoltage protection of the charger. For proper operation, ensure that the ripple is smaller than the overvoltage protection threshold of both the charger and the battery protector. If the protector's overvoltage protection is filtered, the battery protector may not be a constraint.

Applications Information

Adapter Soft-Start

The adapter selection MOSFETs may be soft-started to reduce adapter surge current upon adapter selection. Figure 10 shows the adapter soft-start application using Miller capacitance for optimum soft-start timing and power dissipation.

System Short-Circuit IINP Configuration

The MAX8730 has a system short-circuit protection feature. When V_{IINP} is greater than 4.2V, the MAX8730 latches off PDS. PDS remains off until the adapter is removed and reinserted. For fast response to system overcurrent, add an RC (C13 and R15), as shown in Figure 11.

Select R15 according to the following equation:

$$R15 = \frac{V_{SST}}{G_{IINP} \times RS1 \times I_{SST} \times 0.7} - R10$$

where:

V_{SST} = 4.2V.

I_{SST} = Short-circuit system current threshold. Since system short-circuit triggers a latch, it is important to choose I_{SST} high enough to prevent unintentional triggers.

Select C13 according to the following equation:

$$C13 = \frac{t_{Delay}}{R15}$$

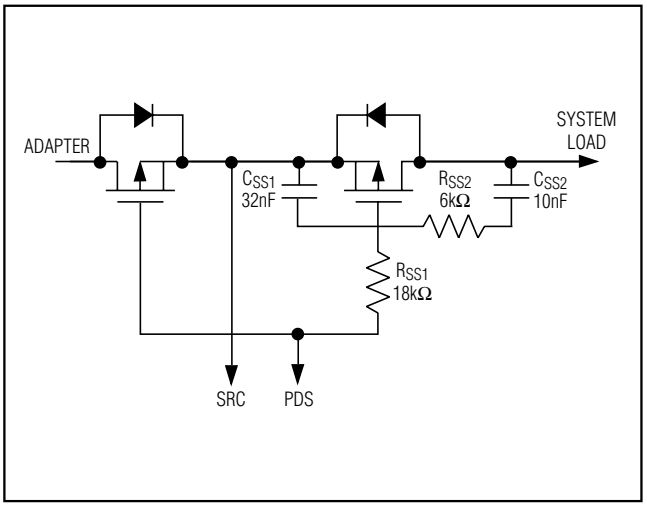


Figure 10. Adapter Soft-Start Modification

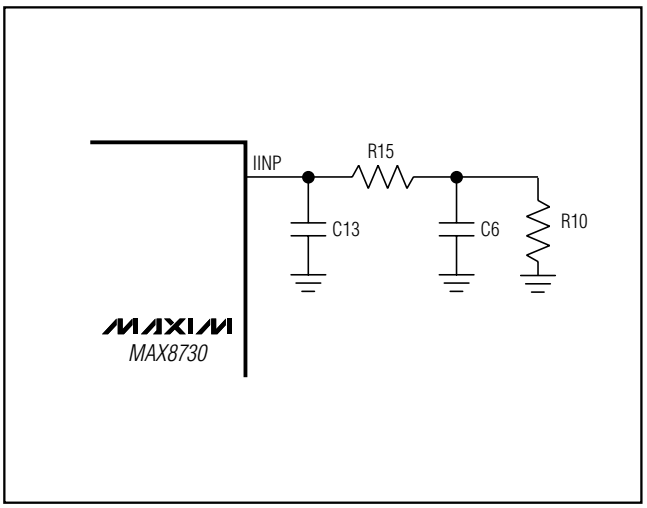


Figure 11. System Short-Circuit IINP Configuration

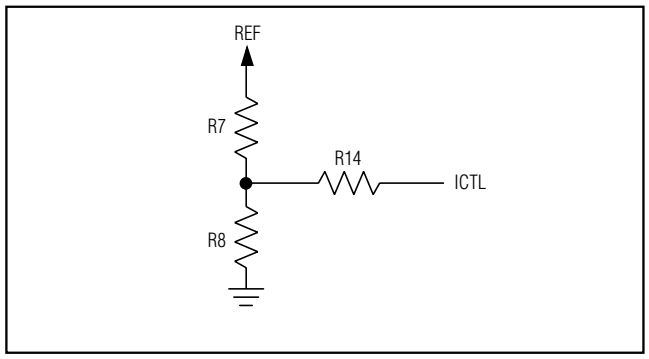


Figure 12. ICTL Foldback Current Adjustment

For typical applications, choose t_{Delay} = 20µs (depends on the p-MOSFET selected for the PDS switch).

The following components can be used for a 10A system short-current design:

R10 = 8.66kΩ

C6 = 0.1µF

R15 = 7.15kΩ

C13 = 2.7nF

Foldback Current

At low duty cycles, most of the charge current is conducted through the Schottky diode (D1). To reduce the requirements of the Schottky diode, the MAX8730 has a foldback charge current feature. When the battery voltage falls below 5 x V_{RELTH}, ICTL sinks 6µA. Add a series resistor to ICTL to adjust the charge current foldback, as shown in Figure 12:

$$R14 = \frac{1}{6\mu A}\left(\frac{R8}{R7+R8} \times V_{REF} - \frac{I_{FOLDBACK} \times RS2 \times 3.6V}{135mV}\right) - \frac{R8 \times R7}{R7+R8}$$

Layout and Bypassing

Bypass SRC, ASNS, LDO, DHIV, and REF as shown in Figure 1.

Good PC board layout is required to achieve specified noise immunity, efficiency, and stable performance. The PC board layout artist must be given explicit instructions—preferably, a sketch showing the placement of the power-switching components and high-current routing. Refer to the PC board layout in the MAX8730 evaluation kit for examples.

Use the following step-by-step guide:

1) Place the high-power connections first, with their grounds adjacent:
   - Minimize the current-sense resistor trace lengths, and ensure accurate current sensing with Kelvin connections.
   - Minimize ground trace lengths in the high-current paths.
   - Minimize other trace lengths in the high-current paths.
   - Use > 5mm wide traces in the high-current paths.
   - Connect to the input capacitors directly to the source of the high-side MOSFET (10mm max length). Place the input capacitor between the input current-sense resistor and the source of the high-side MOSFET.
2) Place the IC and signal components. Quiet connections to REF, CCV, CCI, CCS, ACIN, SWREF, and LDO SRC should be returned to a separate ground (GND) island. There is very little current flowing in these traces, so the ground island need not be very large. When placed on an inner layer, a sizable ground island can help simplify the layout because the low current connections can be made through vias. The ground pad on the backside of the package should be the star connection to this quiet ground island.
3) Keep the gate drive trace (DHI) and SRC path as short as possible (L < 20mm), and route them away from the current-sense lines and REF. Bypass DHIV directly to the source of the high-side MOSFET. These traces should also be relatively wide (W > 1.25mm).
4) Place ceramic bypass capacitors close to the IC. The bulk capacitors can be placed further away.

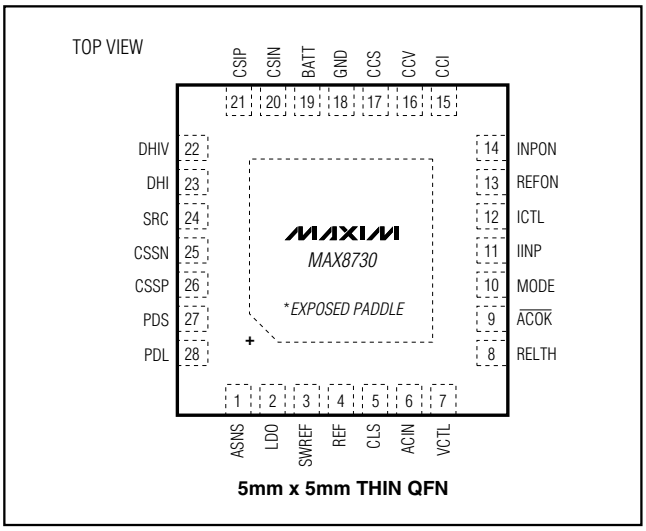
Low-Cost Battery Charger

Chip Information

TRANSISTOR COUNT: 3307

PROCESS: BiCMOS

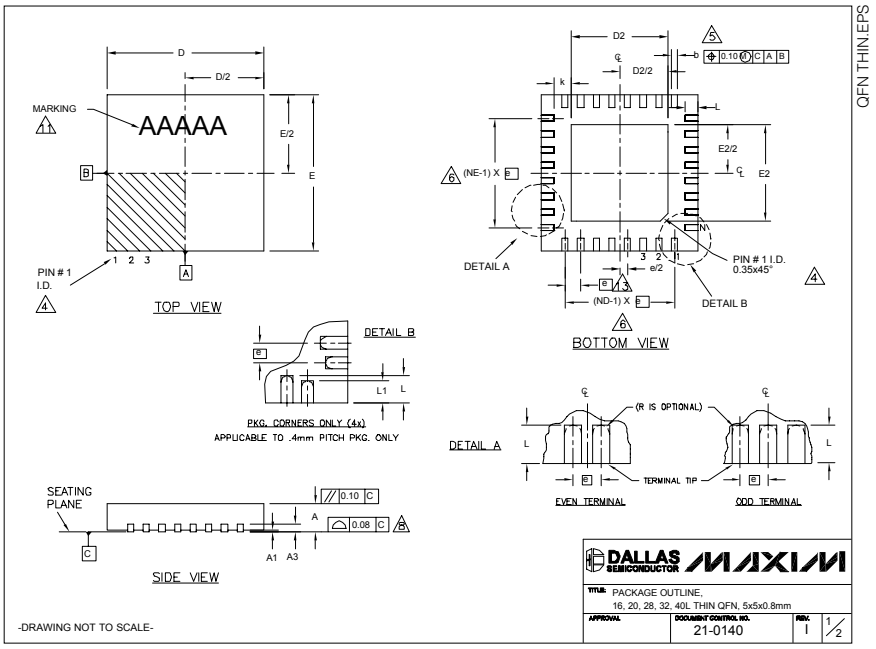
Pin Configuration



5mm x 5mm THIN QFN

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS

PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3		0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.	
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e		0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.	
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	0.35	0.45
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.40	0.50	0.60
L1	-	-	-	-	-	-	-	-	-	-	-	-	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			L	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	±0.15	
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35	0.40	YES
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35	**	YES
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80	**	NO
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35	0.40	YES
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T4055-1	3.20	3.30	3.40	3.20	3.30	3.40	**	YES

** SEE COMMON DIMENSIONS TABLE

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3 AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM
TITLE: PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm
APPROVAL
DOCUMENT CONTROL NO. 21-0140
REV. I
2/2