EXEL MICROELECTRONICS Excellence in E²

XL24C04

Preliminary

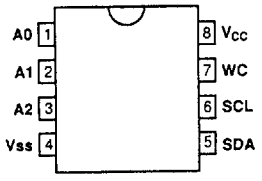
4,096-Bit Serial Electrically Erasable PROM
5 Volt Only Operation

FEATURES

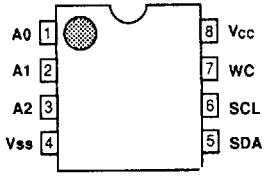
- **Low Power CMOS**
  - **— Active current less than 1mA**
  - **— Standby current less than 2μA**
- **Hardware Write Protection**
  - **— Write Control pin**
  - **— Low V_{CC} lockout write protection**
- **Internally Organized as Two Banks**
  - **— Each 256 x 8**
- **Two Wire Serial Interface (I^2C™)**
  - **—Bidirectional data transfer protocol**
- **Sixteen-Byte Page-Write Mode**
  - **— Minimizes total write time per byte**
- **Automatic Word Address Incrementing**
  - **— Sequential register read**
- **Self-Timed Write Cycle**
  - **— Maximum write cycle time of 10ms**
- **High Reliability**
  - **— Endurance: 100,000 write cycles per byte**
  - **— Data retention: 10 years**
- **8-Pin PDIP or SOIC Packages**

PIN CONFIGURATIONS

Plastic Dual-In-line
"P" Package



EIAJ Small Outline
"JR" Package



PIN NAMES

A0-A2	Address Inputs
SDA	Serial Data I/O
SCL	Serial Clock Input
WC	Write Control Input
V_{SS}	Ground
V_{CC}	Supply Voltage

OVERVIEW

The XL24C04 is a low-cost, 4,096-bit serial E²PROM. It is fabricated using EXEL's advanced CMOS E²PROM technology. The part operates from a single 5 volt supply.

The XL24C04 is internally organized as two 256 x 8 memory banks. The XL24C04 features the I^2C™serial interface and software protocol allowing operation on a simple two-wire bus. Up to four XL24C04s may be individually addressed on the two-wire bus by establishing their device address using the address input pins (A1 and A2).

PIN DESCRIPTIONS

Serial Clock (SCL) - The SCL input is used to clock all data into and out of the device. In the WRITE mode, data must remain stable when SCL is HIGH. In the READ mode, data is clocked out on the falling edge of SCL.

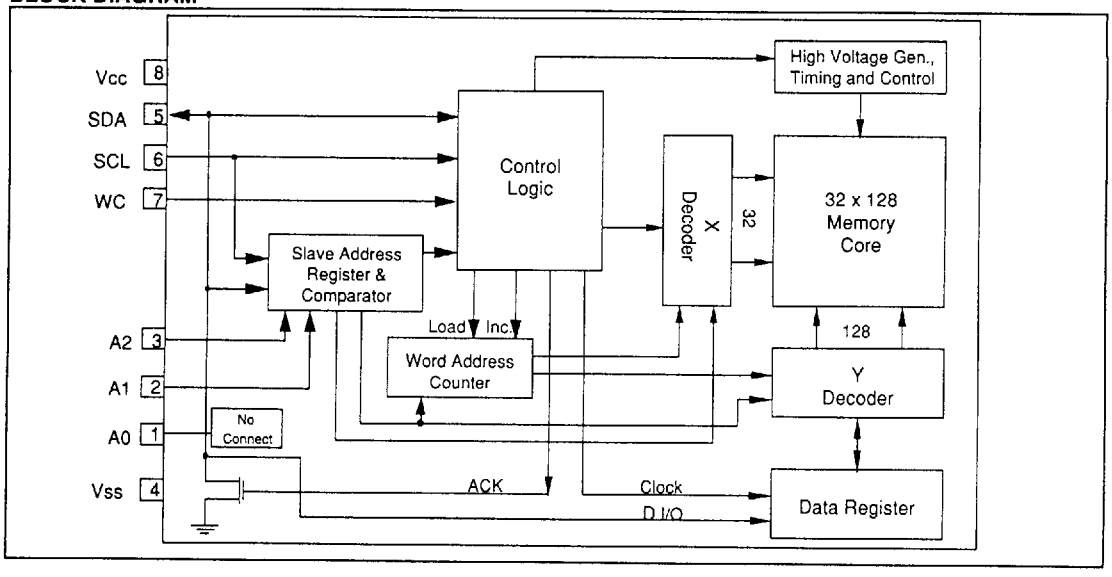
Serial Data (SDA) - The SDA pin is a bidirectional pin used to transfer data into and out of the device. Data may change only when SCL is LOW. It is an open-drain output and may be wire-ORed with any number of open-drain or open-collector outputs.

Address (A0) - The A0 pin is not electrically connected to the XL24C04 device.

Address (A1, A2) - The address input pins are used to set the two-bit device address of the XL24C04 which will identify it on the two-wire bus. These inputs may be tied HIGH, LOW, or they may be actively driven. These inputs allow up to four XL24C04 devices to be distinguished on the bus.

Write Control (WC) - The Write Control input pin is used to disable the write circuitry to the memory. When HIGH, the write function is disabled, protecting data; when LOW, the write function is enabled.

BLOCK DIAGRAM



ENDURANCE AND DATA RETENTION

The XL24C04 is designed for applications requiring up to 100,000 write cycles per bit and unlimited read cycles. It provides 10 years of secure data retention, with or without power applied, after the execution of 100,000 write cycles.

APPLICATIONS

The XL24C04 is ideal for high volume applications requiring low power and low density storage. This device uses a low-cost, space-saving, 8-pin plastic package. Candidate applications include robotics, alarm devices, electronic locks, meters and instrumentation.

CHARACTERISTICS OF THE I²C™ BUS

General Description

The I²C™ bus was designed for two-way, two-line serial communication between different integrated circuits. The two lines are: a serial data line (SDA), and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus. (See Figure 1.) Data transfer between devices may be initiated only when SCL and SDA are HIGH.

Input Data Protocol

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, because changes on the data line when SCL is HIGH will be interpreted as control signals. (See Figure 2.)

START and STOP Conditions

When both the data and clock lines are HIGH, the bus is said to be not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the "START" condition. A LOW-to-HIGH transition of the data line, while the clock is HIGH, is defined as the "STOP" condition. (See Figure 3.)

DEVICE OPERATION

The XL24C04 is a 4,096-bit serial E²PROM. The device supports the I²C™ bidirectional data transmission protocol. The protocol defines any device sending data onto the bus as a "transmitter," and any device which is receiving data as a "receiver." The device controlling the data transmission is defined as the "master," and the controlled device is called the "slave." In all cases, the XL24C04 will be a "slave" device, since it never initiates any data transfers.

Up to four XL24C04s can be connected to the bus, selected by the A1 and A2 device addresses. A0 is not electrically connected. A1 and A2 must be connected to either V_{CC} or V_{SS}. A1 and A2 define the device address. Other devices may be connected to the bus, but need a different device identification code.

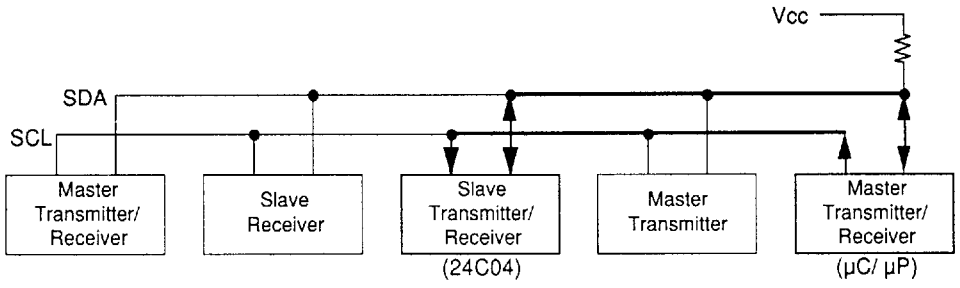


FIGURE 1. TYPICAL SYSTEM CONFIGURATION

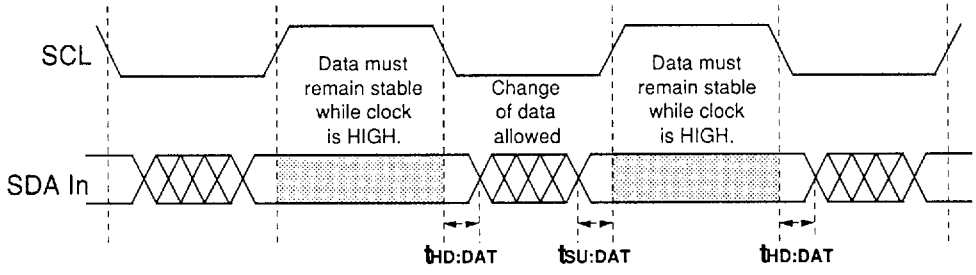


FIGURE 2. INPUT DATA PROTOCOL

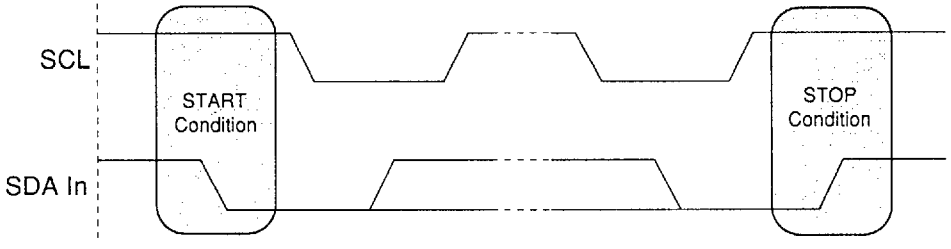


FIGURE 3. START AND STOP CONDITIONS

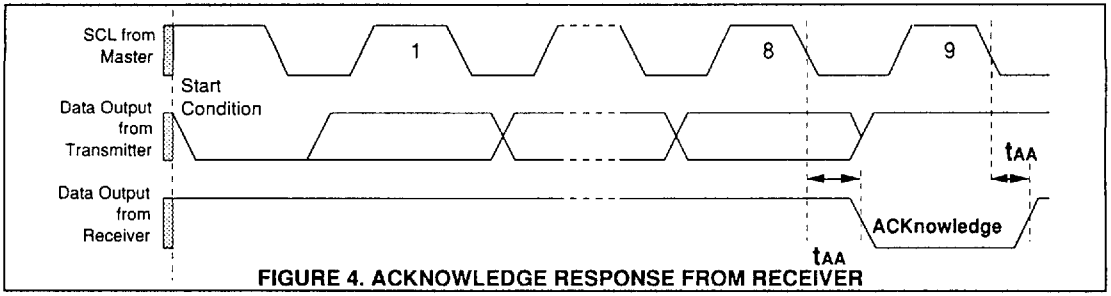


FIGURE 4. ACKNOWLEDGE RESPONSE FROM RECEIVER

Acknowledge (ACK)
Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to ACKnowledge that it received the eight bits of data. (See Figure 4.)

The XL24C04 will respond with an ACKnowledge after recognition of a START condition and its slave address byte. If both the device and a write operation have been selected, the XL24C04 will respond with an ACKnowledge, after the receipt of each subsequent 8-bit word.

In the READ mode, the XL24C04 will transmit eight bits of data, release the SDA line, and monitor the line for an ACKnowledge. If an ACKnowledge is detected, and no STOP condition is generated by the master, the XL24C04 will continue to transmit data. If an ACKnowledge is not detected, the XL24C04 will terminate further data transmissions and await a STOP condition before returning to the standby power mode.

Slave Address Byte
Following a START condition, the master must output the device address of the slave to be accessed. The most significant four bits of the slave address are the "device type identifier." For the XL24C04 this is fixed as 1010. (See Figure 5.)

The next two bits (device address), address a particular device. Using this addressing scheme, a system may have up to four XL24C04 devices on the bus. The device address is defined by the state of the A1 and A2 input pins.

Bank Select Bit
The next bit of the serial stream is the bank select bit. It is used by the host to toggle between the two 2K banks of memory. It is, in effect, the most significant bit of the word address, or A8.

Op Code
The last bit of the stream defines the operation to be performed. When set to "1," a read operation is selected; when set to "0," a write operation is selected.

WRITE OPERATIONS

The XL24C04 allows two types of write operations: byte write and page write. The first writes a single byte during the nonvolatile write period (t_{WR}). The page write operation allows for a full 16-byte page to be stored during t_{WR}.

Byte Write
After the slave address is sent (to identify the slave device, select the bank and specify a read or write instruction), a second field is sent from the master to the slave. This field contains the word address and is comprised of eight bits providing access to any one of the 256 words in the bank.

Upon receipt of the word address, the XL24C04 responds with an ACKnowledge, and waits for the eight bits of data, again responding with an ACKnowledge. The master then terminates the transfer by generating a STOP condition, at which time the XL24C04 begins the internal write cycle to the nonvolatile array.

While the internal write cycle is in progress, the XL24C04 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 6 for the address, ACKnowledge and data transfer sequence.

Device Type Identifier				Device Address		Bank Select	Read/ Write
Slave Address							
1	0	1	0	A2	A1	BS (A8)	Read = 1 Write = 0

FIGURE 5. SLAVE ADDRESS BYTE

Page Write

The XL24C04 is capable of a 16-byte page write operation. It is initiated in the same manner as the byte-write operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to 15 more words of data. After the receipt of each word, the XL24C04 will respond with an ACKnowledge.

The XL24C04 automatically increments the address for subsequent data words. After the receipt of each word, the four low order address bits are internally incremented by one. The high order five bits of the address remain constant. If the master should transmit more than sixteen words, prior to generating the STOP condition, the address counter will "roll over," and the previously written data will be overwritten. As with the byte-write operation, all inputs are disabled during the internal write cycle. Refer to Figure 6 for the address, ACKnowledge and data transfer sequence.

V_{CC} Lockout – Inadvertent Write Protection

To ensure against inadvertent write operations, the XL24C04 has been equipped with an internal V_{CC} sensor circuit which inhibits data alteration when the supply voltage (V_{CC}) falls below V_{WI}. If the applied V_{CC} is below V_{WI}, the XL24C04 is inhibited from executing write operations, thereby protecting the nonvolatile data from inadvertent write operations.

READ OPERATIONS

Read operations are initiated in the same manner as write operations except that the R/W bit of the identification field is set to "1." There are four different read operation options:

1. Current Address Byte Read
2. Random Address Byte Read
3. Current Address Sequential Read
4. Random Address Sequential Read

Current Address Byte Read

The XL24C04 contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a read or write) was to address n, the next read operation would access data from address n+1 and update the current address pointer. When the XL24C04 receives the slave address field with the R/W bit set to "1," it issues an acknowledge and transmits the 8-bit word stored at address n+1.

If the current address read operation only accesses a single byte of data, the master does not acknowledge the transfer but does generate a stop condition. At this point, the XL24C04 discontinues transmission. See Figure 7 for the address acknowledge and data transfer sequence.

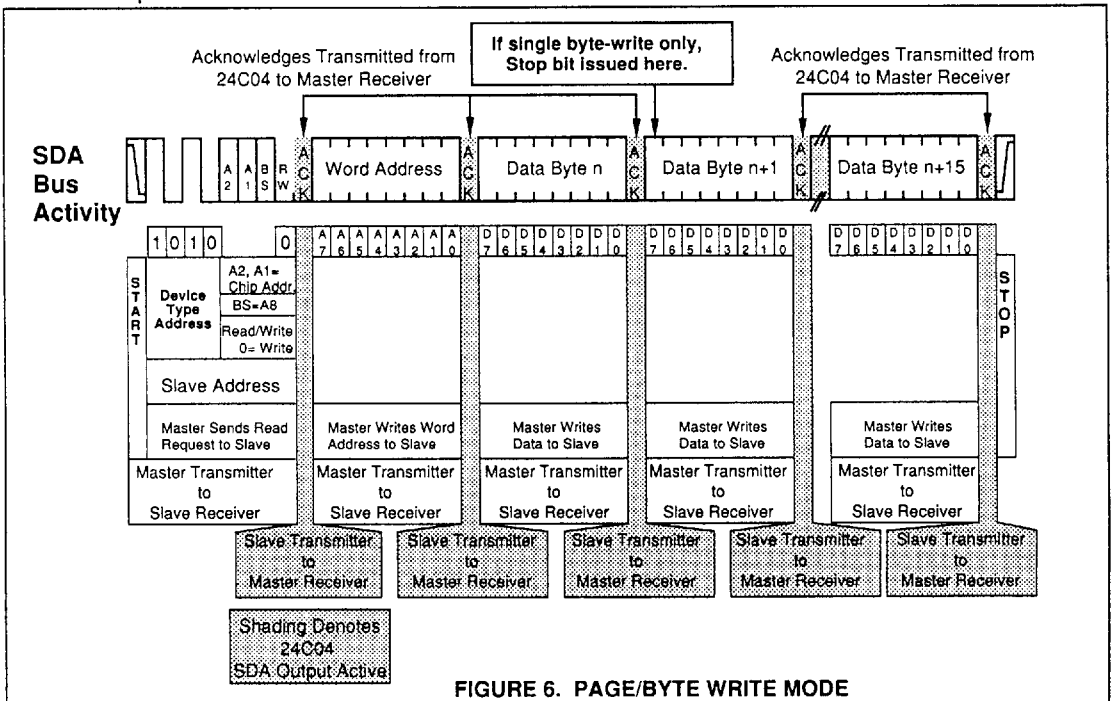


FIGURE 6. PAGE/BYTE WRITE MODE

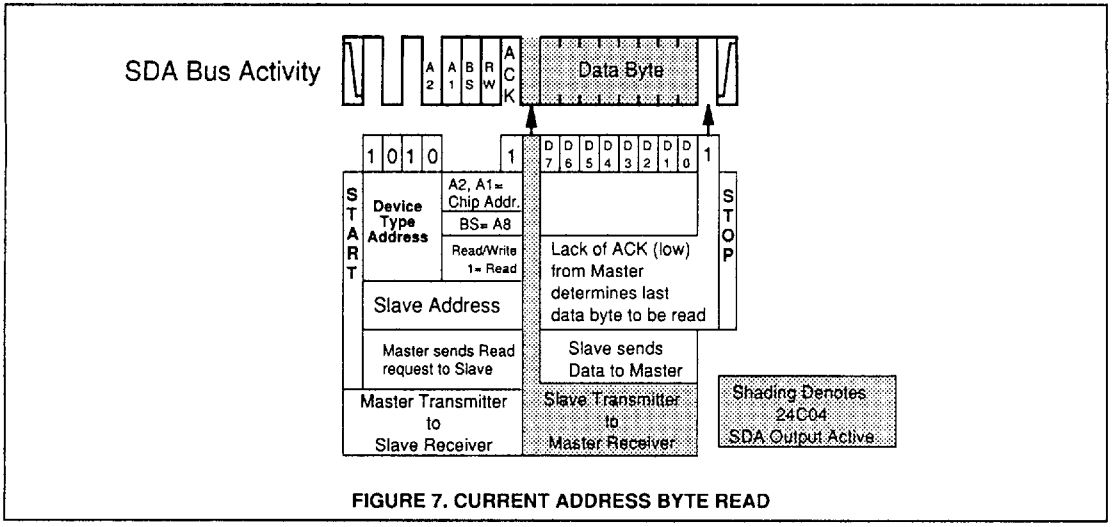


FIGURE 7. CURRENT ADDRESS BYTE READ

Random Address Byte Read

Random address read operations allow the master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a write command which includes the start condition and the slave address field (with the R/W bit set to "0") followed by the address of the word it is to read. This procedure sets the internal address counter of the XL24C04 to the desired address.

After the word address acknowledge is received by the master, the master immediately reissues a start condition followed by another slave address field with the R/W bit set to "1." The XL24C04 will respond with an acknowledge and then transmit the 8-data bits stored at the addressed location. At this point, the master does not acknowledge the transmission but does generate the stop condition. The XL24C04 discontinues transmission and reverts to its standby power mode. See Figure 8 for the address, acknowledge and data transfer sequence.

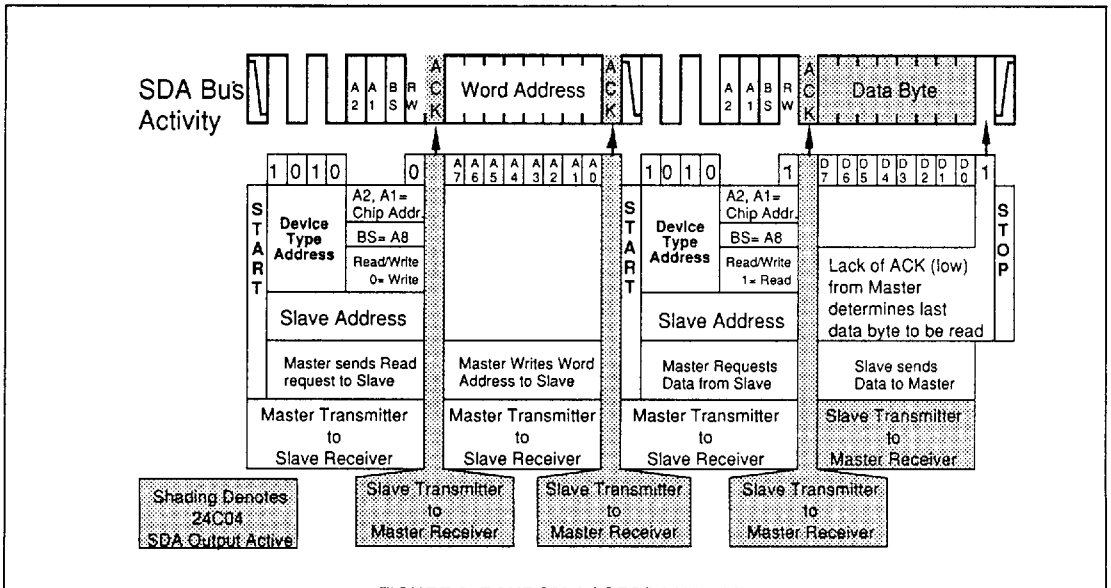


FIGURE 8. RANDOM ACCESS BYTE READ

Sequential Read

The sequential address read operation can be initiated as either a current address read or a random address read. The first data accessed is transmitted by the XL24C04 just as with other byte read modes; however, instead of responding with a stop condition, the master now responds with an acknowledge indicating it requires additional data from the XL24C04. The XL24C04 transmits a new byte of data for each acknowledge received. The sequential address read operation is terminated by the master withholding the acknowledge and generating a stop condition.

During the sequential address read operation, the internal address counter of the XL24C04 automatically increments with each acknowledge received, ensuring that the data from address n will be followed by the data from address n+1. For read operations, all bits of the address counter are incremented, allowing the entire array to be read using a single read command. When the counter reaches the top of the array, it will "roll over" to the bottom of the array and continue to transmit data for each acknowledge it receives. See Figure 9 for the address, acknowledge and data transfer sequence.

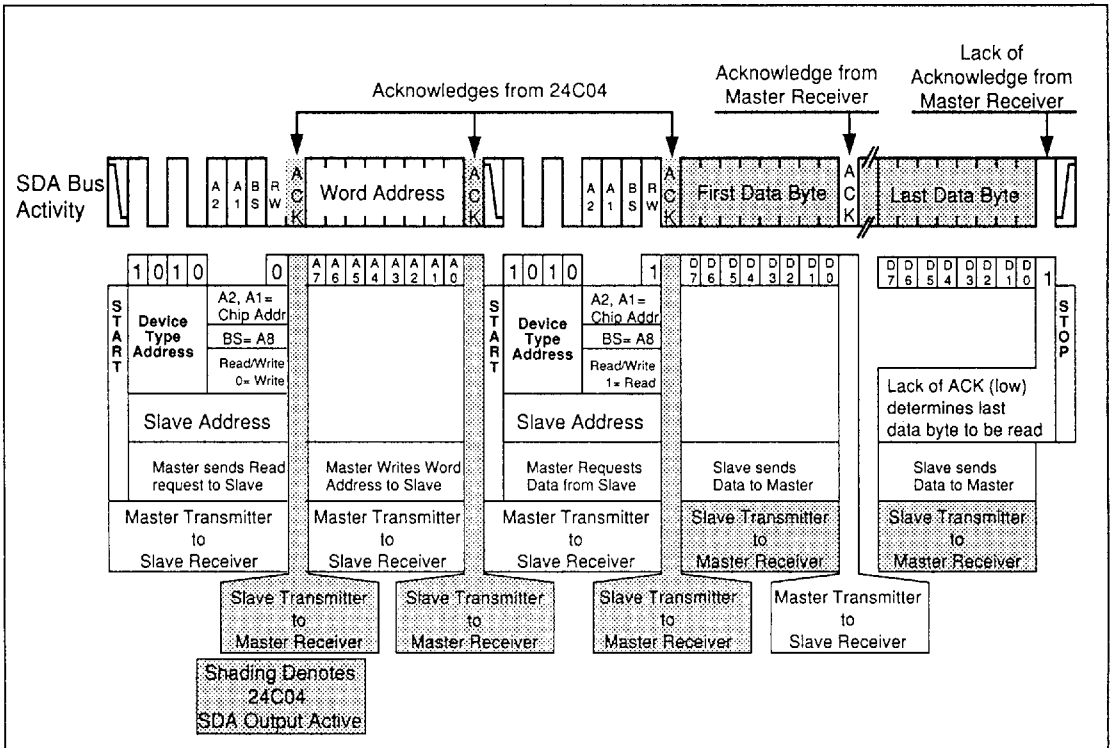


FIGURE 9. SEQUENTIAL READ (starting with a Random Address)

ABSOLUTE MAXIMUM RATINGS

Temperature under bias: .....-40°C to +85°C
Storage Temperature .....-65°C to +125°C
Soldering Temperature (less than 10 seconds) .....300°C
Supply Voltage .....0 to 6.5V
Voltage on Any Pin .....-0.5V to V_{CC}+0.5V
Output Current .....+5mA
Electrostatic Discharge Voltage (JEDEC method) 2,000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS24C04 or -40°C to +85°C for the XLE24C04, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC1}	Supply Current (CMOS)	SCL=CMOS Levels @ 100KHz SDA=Open, all other inputs=GND or Vcc			1	mA
I_{SB}	Standby Current (CMOS)	SCL=SDA=Vcc All other inputs=GND or Vcc			2	µA
I_{LI}	Input Leakage	V_{IN} = 0V to 5V			10	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to 5V			10	µA
V_{IL}	Input Low Voltage	A1-A2, SCL, SDA			0.3 x V_{CC}	V
V_{IH}	Input High Voltage	A1-A2, SCL, SDA	0.7 x V_{CC}			V
V_{OL}	Output Low Voltage	I_{OL} = 3mA (SDA only)			0.4	V
V_{WI}	Write Inhibit Voltage		2.5	3.4	4.5	V

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS24C04 or -40°C to +85°C for the XLE24C04, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	Min	Max	Units
f_{SCL}	SCL Clock Frequency		0	100	KHz
t_{LOW}	Clock Low Period		4.7		µs
t_{HIGH}	Clock High Period		4.0		µs
t_{BUF}	Bus Free Time	Before New Transmission	4.7		µs
$t_{SU:STA}$	Start Condition Setup Time		4.7		µs
$t_{HD:STA}$	Start Condition Hold Time		4.0		µs
$t_{SU:STO}$	Stop Condition Setup Time		4.7		µs
t_{AA}	Clock to Output	SCL Low to SDA Data Out Valid	0.3	3.5	µs
t_{DH}	Data Out Hold Time	SCL Low to SDA Data Out Change	0.3		µs
t_R	SCL and SDA Rise Time			1.0	µs
t_F	SCL and SDA Fall Time			300	ns
$t_{SU:DAT}$	Data In Setup Time		250		ns
$t_{HD:DAT}$	Data In Hold Time		0		ns
T_I	Noise Spike Width	Time constant @ SCL, SDA inputs		100	ns
t_{WR}	Write Cycle Time			10	ms

CAPACITANCE

T_A = 25°C, f = 100KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	8	pF

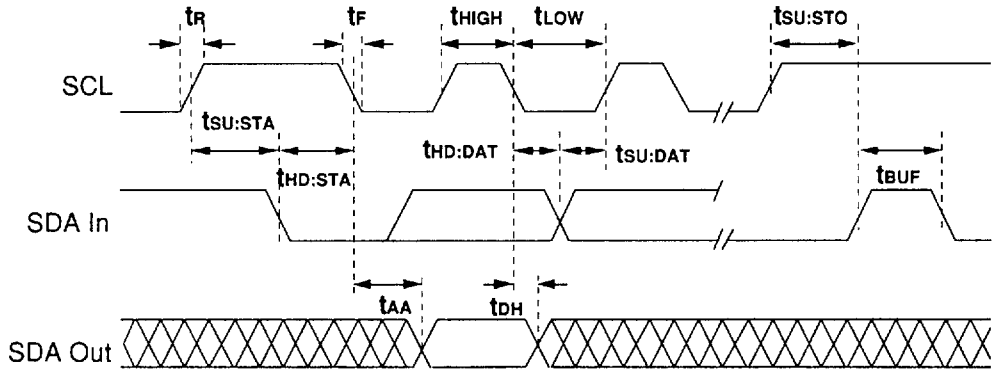


FIGURE 10. BUS TIMING