

# DATA SHEET

## **74ALVCH162245**

16-bit bus transceiver with direction pin  
and 30Ω termination resistor (3-State)

Product specification

1998 Jun 29

IC24 Data Handbook

# 16-bit bus transceiver with direction pin and 30Ω termination resistor (3-State)

## 74ALVCH162245

### FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple  $V_{CC}$  and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Bus hold on all data inputs
- Integrated 30Ω termination resistor

### DESCRIPTION

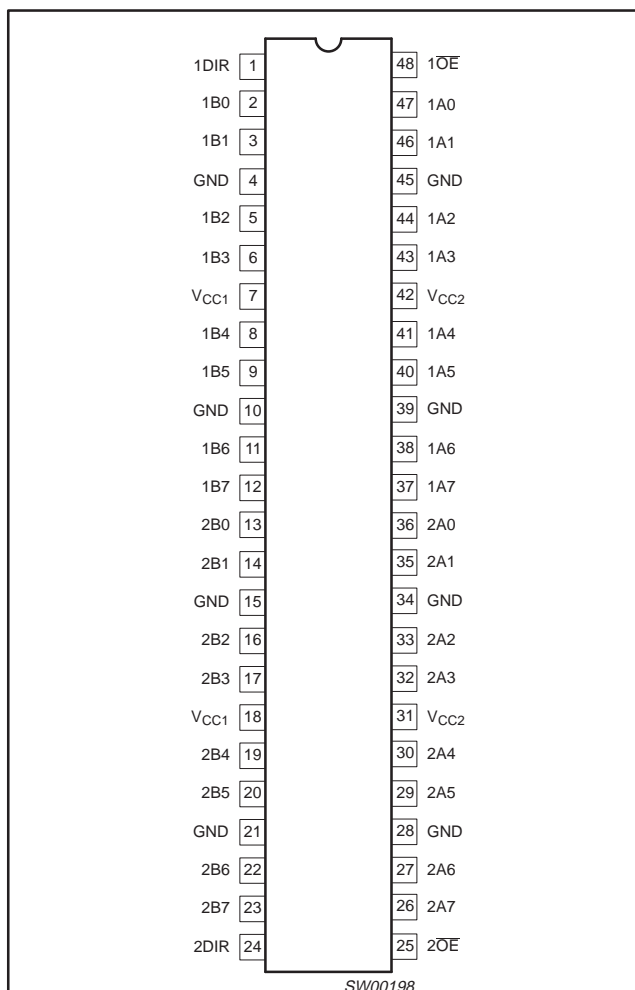
The 74ALVCH162245 is a 16-bit transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions.

The 74ALVCH162245 features two output enable ( $\overline{nOE}$ ) inputs for easy cascading and two send/receive ( $\overline{nDIR}$ ) inputs for direction control.  $\overline{nOE}$  controls the outputs so that the buses are effectively isolated. This device can be used as two 8-bit transceivers or one 16-bit transceiver.

The 74ALVCH162245 is designed with 30Ω series resistors in both HIGH and LOW output states.

The 74ALVCH162245 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

### PIN CONFIGURATION



SW00198

### QUICK REFERENCE DATA

GND = 0V;  $T_{amb} = 25^{\circ}\text{C}$ ;  $t_r = t_f \leq 2.5\text{ns}$

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	Propagation delay An to Bn; Bn to An	$V_{CC} = 2.5\text{V}$ , $C_L = 30\text{pF}$ $V_{CC} = 3.3\text{V}$ , $C_L = 50\text{pF}$		2.4	ns
$C_I$	Input capacitance			4.0	pF
$C_{I/O}$	Input/output capacitance			8.0	pF
$C_{PD}$	Power dissipation capacitance per buffer	$V_I = \text{GND to } V_{CC}^1$	Outputs enabled	27	pF
			Outputs disabled	4	pF

#### NOTES:

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  $f_i$  = input frequency in MHz;  $C_L$  = output load capacitance in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	74ALVCH162245 DL	ACH162245 DL	SOT370-1
48-Pin Plastic TSSOP Type II	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	74ALVCH162245 DGG	ACH162245 DGG	SOT362-1

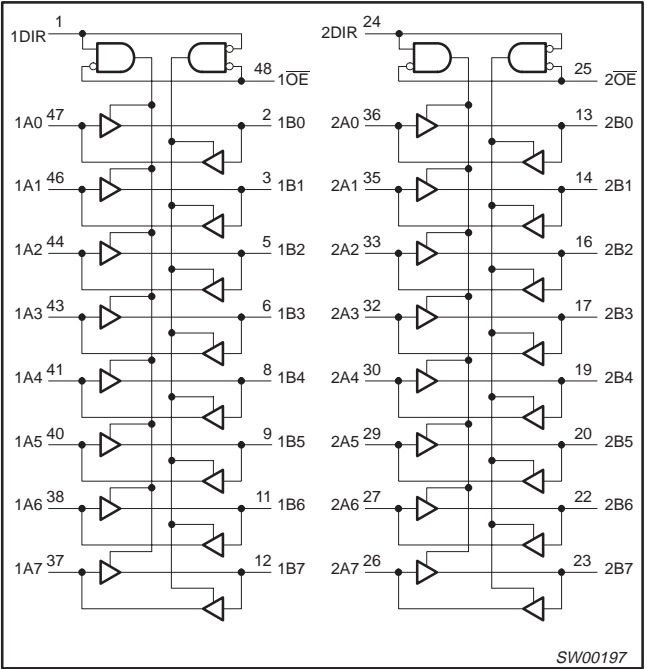
16-bit bus transceiver with direction pin and 30Ω termination resistor (3-State)

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PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	1DIR	Direction control
2, 3, 5, 6, 8, 9, 11, 12	1B0 to 1B7	Data inputs/outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V <sub>CC</sub>	Positive supply voltage
13, 14, 16, 17, 19, 20, 22, 23	2B0 to 2B7	Data inputs/outputs
24	2DIR	Direction control
25	2OE	Output enable input (active LOW)
36, 35, 33, 32, 30, 29, 27, 26	2A0 to 2A7	Data inputs/outputs
47, 46, 44, 43, 41, 40, 38, 37	1A0 to 1A7	Data inputs/outputs
48	1OE	Output enable input (active LOW)

LOGIC SYMBOL

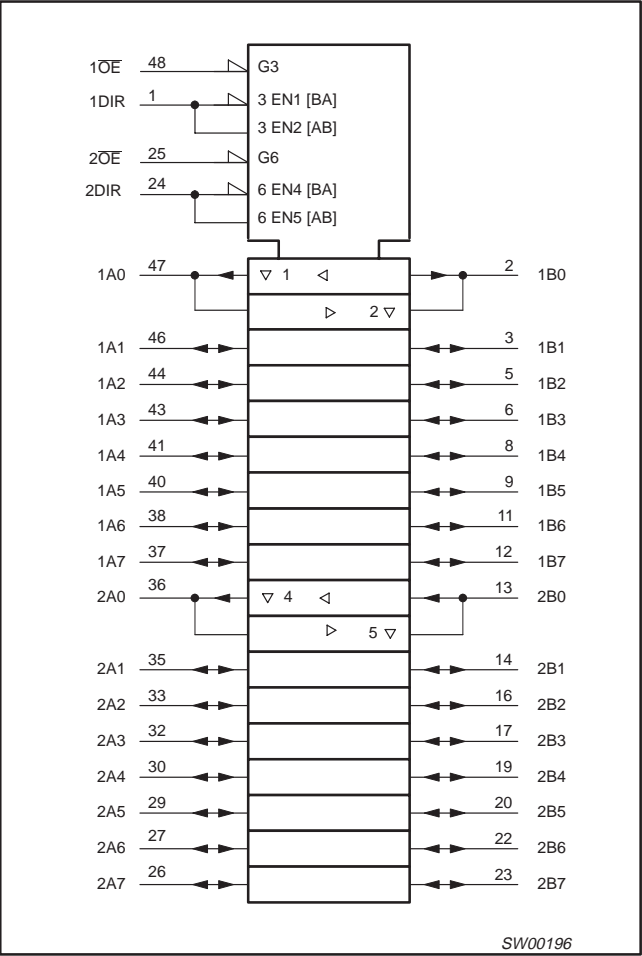


FUNCTION TABLE

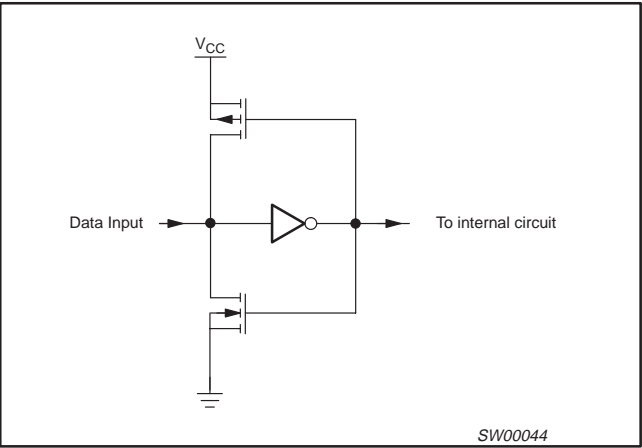
INPUTS		INPUTS/OUTPUT	
nOE	nDIR	nAn	nBn
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
Z = high impedance OFF-state

LOGIC SYMBOL (IEEE/IEC)



BUS HOLD CIRCUIT



# 16-bit bus transceiver with direction pin and 30Ω termination resistor (3-State)

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
$V_{CC}$	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
$V_I$	DC Input voltage range		0	$V_{CC}$	V
$V_O$	DC output voltage range		0	$V_{CC}$	V
$T_{amb}$	Operating free-air temperature range		-40	+85	°C
$t_r, t_f$	Input rise and fall times	$V_{CC} = 2.3$ to $3.0V$ $V_{CC} = 3.0$ to $3.6V$	0 0	20 10	ns/V

## ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +4.6	V
$I_{IK}$	DC input diode current	$V_I < 0$	-50	mA
$V_I$	DC input voltage	For data inputs with bus hold <sup>1</sup>	-0.5 to $V_{CC} + 0.5$	V
		For control pins <sup>1</sup>	-0.5 to +4.6	
$I_{OK}$	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
$V_O$	DC output voltage	Note 1	-0.5 to $V_{CC} + 0.5$	V
$I_O$	DC output source or sink current	$V_O = 0$ to $V_{CC}$	±50	mA
$I_{GND}, I_{CC}$	DC $V_{CC}$ or GND current		±100	mA
$T_{stg}$	Storage temperature range		-65 to +150	°C
$P_{TOT}$	Power dissipation per package -plastic medium-shrink (SSOP) -plastic thin-medium-shrink (TSSOP)	For temperature range: -40 to +125 °C above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	850 600	mW

### NOTE:

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

# 16-bit bus transceiver with direction pin and 30Ω termination resistor (3-State)

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## DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP <sup>1</sup>	MAX	
V <sub>IH</sub>	HIGH level Input voltage	V <sub>CC</sub> = 2.3 to 2.7V	1.7	1.2		V
		V <sub>CC</sub> = 2.7 to 3.6V	2.0	1.5		
V <sub>IL</sub>	LOW level Input voltage	V <sub>CC</sub> = 2.3 to 2.7V		1.2	0.7	V
		V <sub>CC</sub> = 2.7 to 3.6V		1.5	0.8	
V <sub>OH</sub>	HIGH level output voltage	V <sub>CC</sub> = 2.3 to 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -100μA	V <sub>CC</sub> -0.2	V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -4mA	V <sub>CC</sub> -0.4	V <sub>CC</sub> -0.11		
		V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -6mA	V <sub>CC</sub> -0.6	V <sub>CC</sub> -0.17		
		V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -4mA	V <sub>CC</sub> -0.5	V <sub>CC</sub> -0.09		
		V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -8mA	V <sub>CC</sub> -0.7	V <sub>CC</sub> -0.19		
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -6mA	V <sub>CC</sub> -0.6	V <sub>CC</sub> -0.13		
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12mA	V <sub>CC</sub> -1.0	V <sub>CC</sub> -0.27		
V <sub>OL</sub>	LOW level output voltage	V <sub>CC</sub> = 2.3 to 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100μA		GND	0.20	V
		V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 4mA		0.07	0.40	
		V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 6mA		0.11	0.55	
		V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 4mA		0.06	0.40	
		V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 8mA		0.13	0.60	
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 6mA		0.09	0.55	
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA		0.19	0.80	
I <sub>I</sub>	Input leakage current per data pin with bus hold	V <sub>CC</sub> = 2.3 to 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND		0.1	5	μA
I <sub>OZ</sub>	3-State output OFF-state current	V <sub>CC</sub> = 2.3 to 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND		0.1	10	μA
I <sub>CC</sub>	Quiescent supply current	V <sub>CC</sub> = 2.3 to 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0		0.2	40	μA
ΔI <sub>CC</sub>	Additional quiescent supply current given per data I/O pin with bus hold	V <sub>CC</sub> = 2.3V to 3.6V; V <sub>I</sub> = V <sub>CC</sub> - 0.6V; I <sub>O</sub> = 0		150	750	μA
I <sub>BHL</sub> <sup>2</sup>	Bus hold LOW sustaining current	V <sub>CC</sub> = 2.3V; V <sub>I</sub> = 0.7V	45	—		μA
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = 0.8V	75	150		
I <sub>BHH</sub> <sup>2</sup>	Bus hold HIGH sustaining current	V <sub>CC</sub> = 2.3V; V <sub>I</sub> = 1.7V	-45			μA
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = 2.0V	-75	-175		
I <sub>BHLO</sub> <sup>2</sup>	Bus hold LOW overdrive current	V <sub>CC</sub> = 3.6V	500			μA
I <sub>BHHO</sub> <sup>2</sup>	Bus hold HIGH overdrive current	V <sub>CC</sub> = 3.6V	-500			μA

### NOTES:

1. All typical values are at  $T_{amb} = 25^{\circ}C$ .
2. Valid for data inputs of bus hold parts.

# 16-bit bus transceiver with direction pin and 30Ω termination resistor (3-State)

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## AC CHARACTERISTICS FOR $V_{CC} = 2.3V$ TO $2.7V$ RANGE

GND = 0V;  $t_r = t_f \leq 2.0ns$ ;  $C_L = 30pF$ 

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V <sub>CC</sub> = 2.3 to 2.7V			
			MIN	TYP <sup>1, 2</sup>	MAX	
t <sub>PHL</sub> /t <sub>PLH</sub>	Propagation delay nAn to nBn; nBn to nAn	1, 3	1.0	2.5	4.9	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-State output enable time nOE to nAn; nOE to nBn	2, 3	1.0	2.9	6.8	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-State output disable time nOE to nAn; nOE to nBn	2, 3	1.0	3.0	6.3	ns

### NOTES:

1. All typical values are measured  $T_{amb} = 25^\circ C$ .
2. Typical value is measured at  $V_{CC} = 2.5V$

## AC CHARACTERISTICS FOR $V_{CC} = 3.0V$ TO $3.6V$ RANGE AND $V_{CC} = 2.7V$

GND = 0V;  $t_r = t_f \leq 2.5ns$ ;  $C_L = 50pF$ 

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V <sub>CC</sub> = 3.3 ± 0.3V			V <sub>CC</sub> = 2.7V			
			MIN	TYP <sup>1, 2</sup>	MAX	MIN	TYP <sup>1</sup>	MAX	
t <sub>PHL</sub> /t <sub>PLH</sub>	Propagation delay nAn to nBn; nBn to nAn	1, 3	1.0	2.4	4.2	1.0	2.7	4.7	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-State output enable time nOE to nAn; nOE to nBn	2, 3	1.0	3.0	5.6	1.0	3.9	6.7	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-State output disable time nOE to nAn; nOE to nBn	2, 3	1.0	2.6	5.5	1.0	2.9	5.7	ns

### NOTES:

1. All typical values are measured  $T_{amb} = 25^\circ C$ .
2. Typical value is measured at  $V_{CC} = 3.3V$

16-bit bus transceiver with direction pin and  
30Ω termination resistor (3-State)

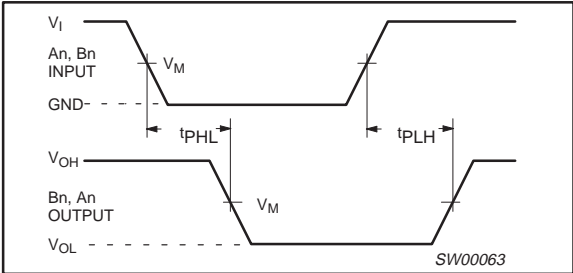
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**AC WAVEFORMS FOR  $V_{CC} = 2.3V$  TO  $2.7V$  AND  $V_{CC} < 2.3V$  RANGE**

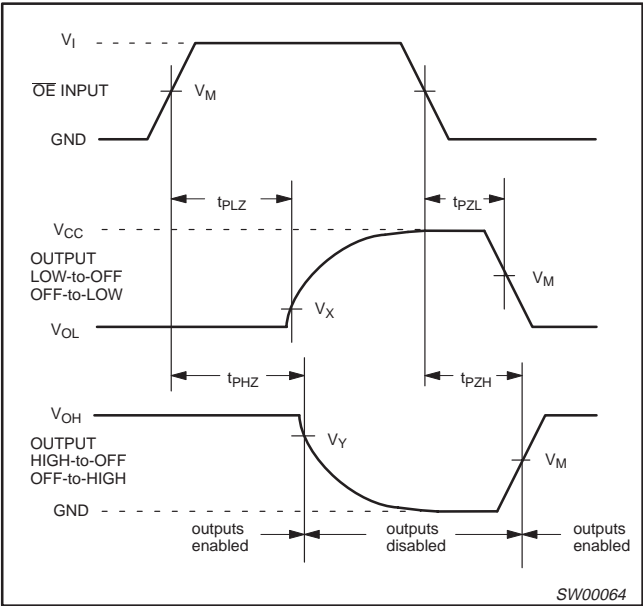
$V_M = 0.5 V_{CC}$   
 $V_X = V_{OL} + 0.15V$   
 $V_Y = V_{OH} - 0.15V$   
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.  
 $V_I = V_{CC}$

**AC WAVEFORMS FOR  $V_{CC} = 3.0V$  TO  $3.6V$  AND  $V_{CC} = 2.7V$  RANGE**

$V_M = 1.5 V$   
 $V_X = V_{OL} + 0.3V$   
 $V_Y = V_{OH} - 0.3V$   
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.  
 $V_I = 2.7V$



Waveform 1. Input (nAn, nBn) to output (nBn, nAn) propagation delay times



Waveform 2. 3-State enable and disable times

**TEST CIRCUIT**

**Test Circuit for switching times**

**DEFINITIONS**

$R_L$  = Load resistor  
 $C_L$  = Load capacitance includes jig and probe capacitance  
 $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

**SWITCH POSITION**

TEST	$S_1$	$V_{CC}$	$V_I$
$t_{PLH}/t_{PHL}$	Open	$< 2.7V$	$V_{CC}$
$t_{PLZ}/t_{PZL}$	$2 * V_{CC}$	$2.7-3.6V$	$2.7V$
$t_{PHZ}/t_{PZH}$	GND		

SV00906

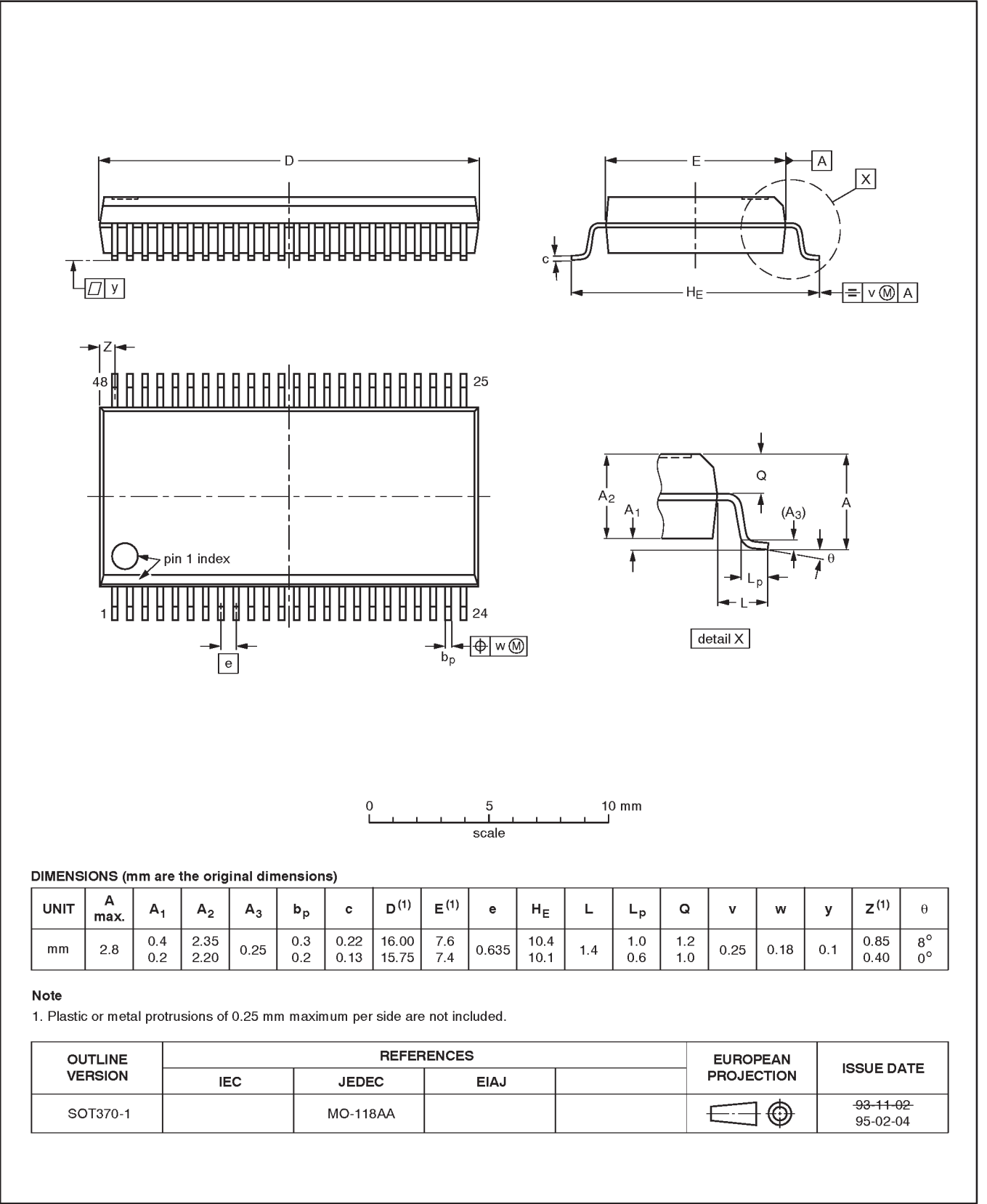
Waveform 3. Load circuitry for switching times

16-bit bus transceiver with direction pin and  
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SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1



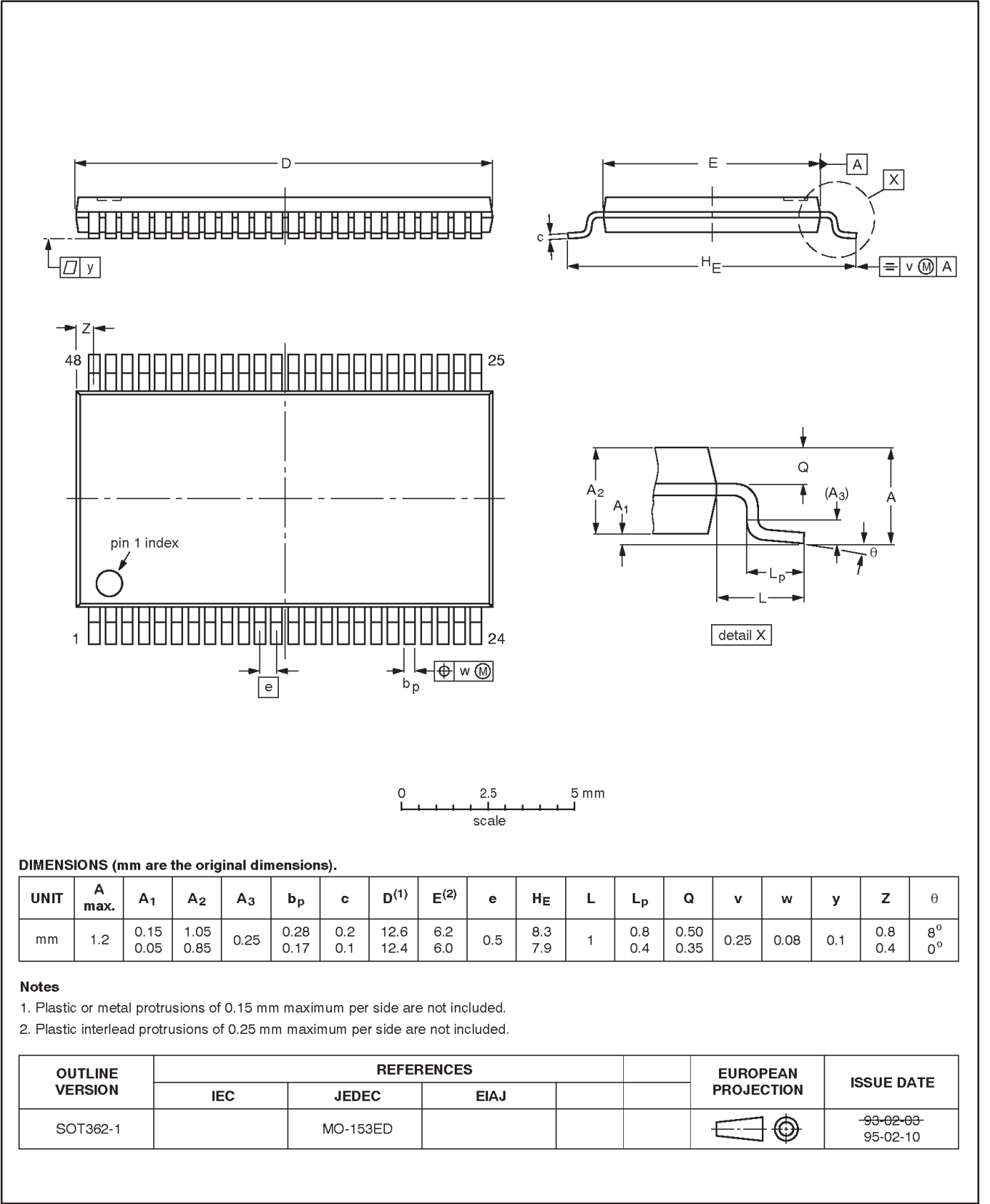


16-bit bus transceiver with direction pin and  
30Ω termination resistor (3-State)

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TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm

SOT362-1



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16-bit bus transceiver with direction pin and  
30 $\Omega$  termination resistor (3-State)

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#### NOTES

# 16-bit bus transceiver with direction pin and 30Ω termination resistor (3-State)

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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