FAIRCHILD SEMICONDUCTOR™

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CD4541BC
Programmable Timer

General Description

The CD4541BC Programmable Timer is designed with a 16-stage binary counter, an integrated oscillator for use with an external capacitor and two resistors, output control logic, and a special power-on reset circuit. The special features of the power-on reset circuit are first, no additional static power consumption and second, the part functions across the full voltage range (3V–15V) whether power-on reset is enabled or disabled.

Timing and the counter are initialized by turning on power, if the power-on reset is enabled. When the power is already on, an external reset pulse will also initialize the timing and counter. After either reset is accomplished, the oscillator frequency is determined by the external RC network. The 16-stage counter divides the oscillator frequency by any of 4 digitally controlled division ratios.

Features

- Available division ratios 2^8, 2^{10}, 2^{13}, or 2^{16}
- Increments on positive edge clock transitions
- Built-in low power RC oscillator (±2% accuracy over temperature range and ±10% supply and ±3% over processing @ < 10 kHz)
- Oscillator frequency range ≈ DC to 100 kHz
- Oscillator may be bypassed if external clock is available (apply external clock to pin 3)
- Automatic reset initializes all counters when power turns on
- External master reset totally independent of automatic reset operation
- Operates at 2^n frequency divider or single transition timer
- Q/$\overline{Q}$ select provides output logic level flexibility
- Reset (auto or master) disables oscillator during resetting to provide no active power dissipation
- Clock conditioning circuit permits operation with very slow clock rise and fall times
- Wide supply voltage range—3.0V to 15V
- High noise immunity—0.45 V_{DD} (typ.)
- 5V–10V–15V parameter ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range
- High output drive (pin 8) min. one TTL load

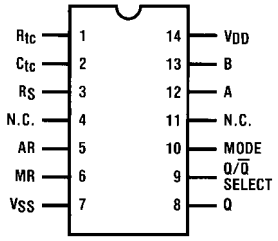
Ordering Code:

Order Number	Package Number	Package Description
CD4541BCN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide
CD4541BCM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150” Narrow

Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering code.

Connection Diagram

Pin Assignments for DIP and SOIC



N.C.—Not connected

Top View

Truth Table

Pin	State	
	0	1
5	Auto Reset Operating	Auto Reset Disabled
6	Timer Operational	Master Reset On
9	Output Initially Low after Reset	Output Initially High after Reset
10	Single Cycle Mode	Recycle Mode

Division Ratio Table

A	B	Number of Counter Stages n	Count 2^n
0	0	13	8192
0	1	10	1024
1	0	8	256
1	1	16	65536

Operating Characteristics

With Auto Reset pin set to a “0” the counter circuit is initialized by turning on power. Or with power already on, the counter circuit is reset when the Master Reset pin is set to a “1”. Both types of reset will result in synchronously resetting all counter stages independent of counter state.

The RC oscillator frequency is determined by the external RC network, i.e.:

$$f = \frac{1}{2.3\ R_{tc}C_{tc}} \text{ if } (1\ kHz \leq f \leq 100\ kHz)$$

and $R_S \approx 2\ R_{tc}$ where $R_S \geq 10\ k\Omega$

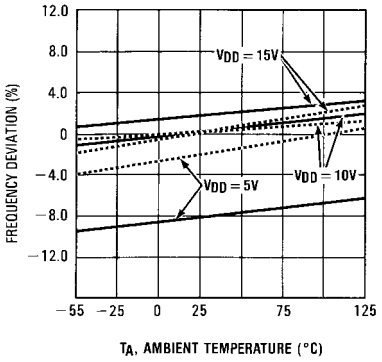
The time select inputs (A and B) provide a two-bit address to output any one of four counter stages (2^8, 2^{10}, 2^{13}, and 2^{16}). The 2^n counts as shown in the Division Ratio Table represent the Q output of the Nth stage of the counter. When A is “1”, 2^{16} is selected for both states of B.

However, when B is “0”, normal counting is interrupted and the 9th counter stage receives its clock directly from the oscillator (i.e., effectively outputting 2^8).

The Q/$\overline{Q}$ select output control pin provides for a choice of output level. When the counter is in a reset condition and Q/$\overline{Q}$ select pin is set to a “0” the Q output is a “0”. Correspondingly, when Q/$\overline{Q}$ select pin is set to a “1” the Q output is a “1”.

When the mode control pin is set to a “1”, the selected count is continually transmitted to the output. But, with mode pin “0” and after a reset condition the RS flip-flop resets (see Logic Diagram), counting commences and after 2^{n-1} counts the RS flip-flop sets which causes the output to change state. Hence, after another 2^{n-1} counts the output will not change. Thus, a Master Reset pulse must be applied or a change in the mode pin level is required to reset the single cycle operation.

Typical RC Oscillator Characteristics



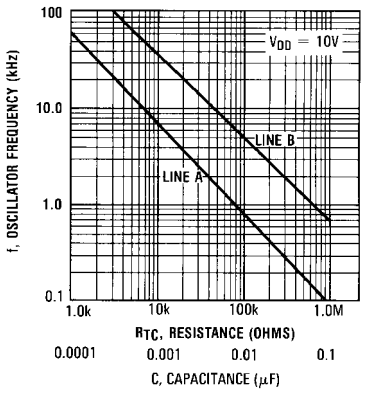
Solid Line = R_{TC} = 56 kΩ, R_S = 1 kΩ and C = 1000 pF

f = 10.2 kHz @ V_{DD} = 10V and T_A = 25°

Dashed Line = R_{TC} = 56 kΩ, R_S = 120 kΩ and C = 1000 pF

f = 7.75 kHz @ V_{DD} = 10V and T_A = 25°

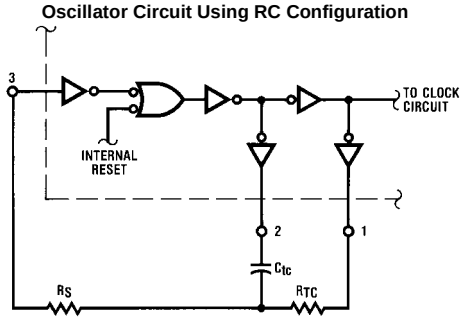
RC Oscillator Frequency as a Function of R_{TC} and C



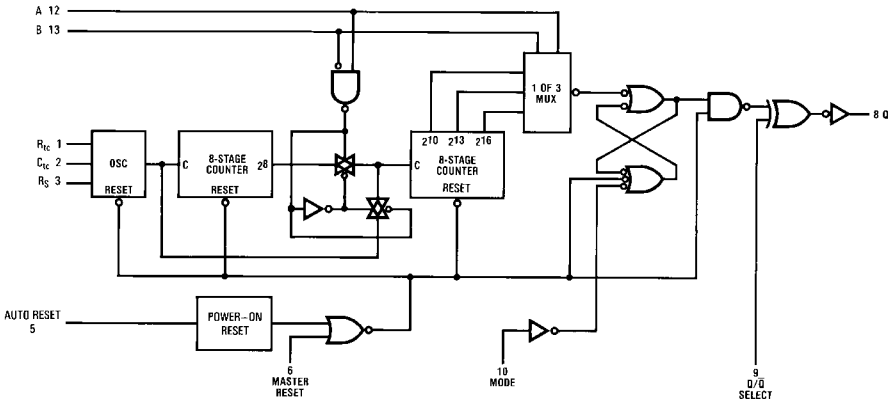
Line A: f as a function of C and (R_{TC} = 56 kΩ; R_S = 120k

Line B: f as a function of R_{TC} and (C = 100 pF; $R_S = 2\ R_{TC}$

Oscillator Circuit Using RC Configuration



Logic Diagram



V_{DD} = Pin 14

V_{SS} = Pin 7

Absolute Maximum Ratings (Note 1)

(Note 2)

Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5V to V_{DD} +0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{DD})	3V to 15V
Input Voltage (V_{IN})	0 to V_{DD}
Operating Temperature Range	−40°C to +85°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20		0.005	20		150	µA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40		0.010	40		300	µA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80		0.015	80		600	µA
V_{OL}	LOW Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V $\|I_O\| < 1\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	HIGH Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V $\|I_O\| < 1$ µA	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	LOW Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	HIGH Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	LOW Level Output Current	V_{DD} = 5V, V_O = 0.4V	2.32		1.96	3.6		1.6		mA
	(Note 3)	V_{DD} = 10V, V_O = 0.5V	3.18		2.66	9.0		2.18		mA
		V_{DD} = 15V, V_O = 1.5V	12.4		10.4	34.0		8.50		mA
I_{OH}	HIGH Level Output Current	V_{DD} = 5V, V_O = 2.5V	5.1		4.27	130		3.5		mA
	(Note 3)	V_{DD} = 10V, V_O = 9.5V	2.69		2.25	8.0		1.85		mA
		V_{DD} = 15V, V_O = 13.5V	10.5		8.8	30.0		7.22		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	µA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	µA

Note 3: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics (Note 4)

$T_A = 25°C$, $C_L = 50$ pF (refer to test circuits)

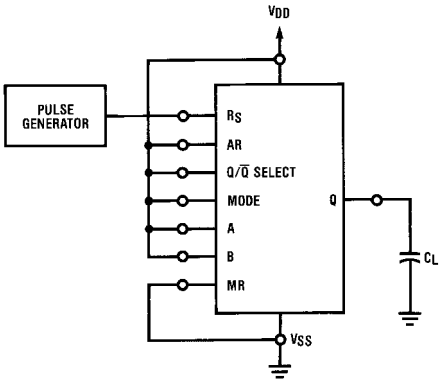
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{TLH}	Output Rise Time	$V_{DD} = 5V$		50	200	ns
		$V_{DD} = 10V$		30	100	ns
		$V_{DD} = 15V$		25	80	ns
t_{THL}	Output Fall Time	$V_{DD} = 5V$		50	200	ns
		$V_{DD} = 10V$		30	100	ns
		$V_{DD} = 15V$		25	80	ns
t_{PLH}, t_{PHL}	Turn-Off, Turn-On Propagation Delay, Clock to Q (2^8 Output)	$V_{DD} = 5V$		1.8	4.0	μs
		$V_{DD} = 10V$		0.6	1.5	μs
		$V_{DD} = 15V$		0.4	1.0	μs
t_{PHL}, t_{PLH}	Turn-On, Turn-Off Propagation Delay, Clock to Q (2^{16} Output)	$V_{DD} = 5V$		3.2	8.0	μs
		$V_{DD} = 10V$		1.5	3.0	μs
		$V_{DD} = 15V$		1.0	2.0	μs
$t_{WH(CL)}$	Clock Pulse Width	$V_{DD} = 5V$	400	200		ns
		$V_{DD} = 10V$	200	100		ns
		$V_{DD} = 15V$	150	70		ns
f_{CL}	Clock Pulse Frequency	$V_{DD} = 5V$		2.5	1.0	MHz
		$V_{DD} = 10V$		6.0	3.0	MHz
		$V_{DD} = 15V$		8.5	4.0	MHz
$t_{WH(R)}$	MR Pulse Width	$V_{DD} = 5V$	400	170		ns
		$V_{DD} = 10V$	200	75		ns
		$V_{DD} = 15V$	150	50		ns
C_I	Average Input Capacitance	Any Input		5.0	7.5	pF
C_{PD}	Power Dissipation Capacitance (Note 5)			100		pF

Note 4: AC Parameters are guaranteed by DC correlated testing.

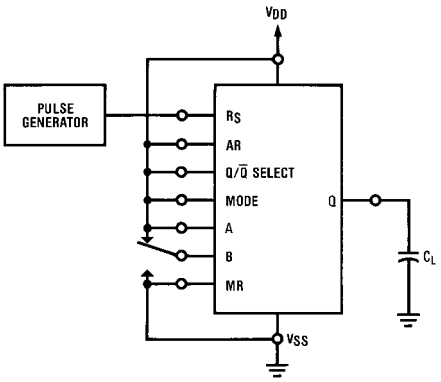
Note 5: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see Family Characteristics application note: AN-90.

Test Circuits and Waveforms

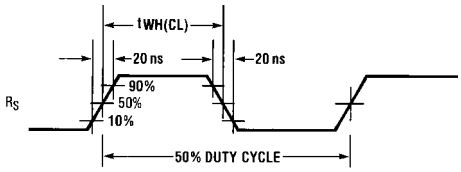
Power Dissipation Test Circuit and Waveforms

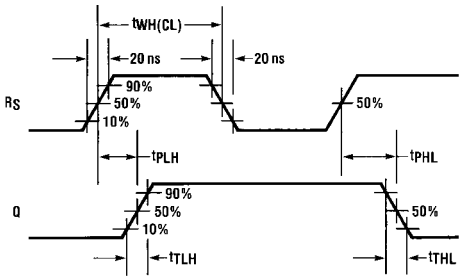


Switching Time Test Circuit and Waveforms



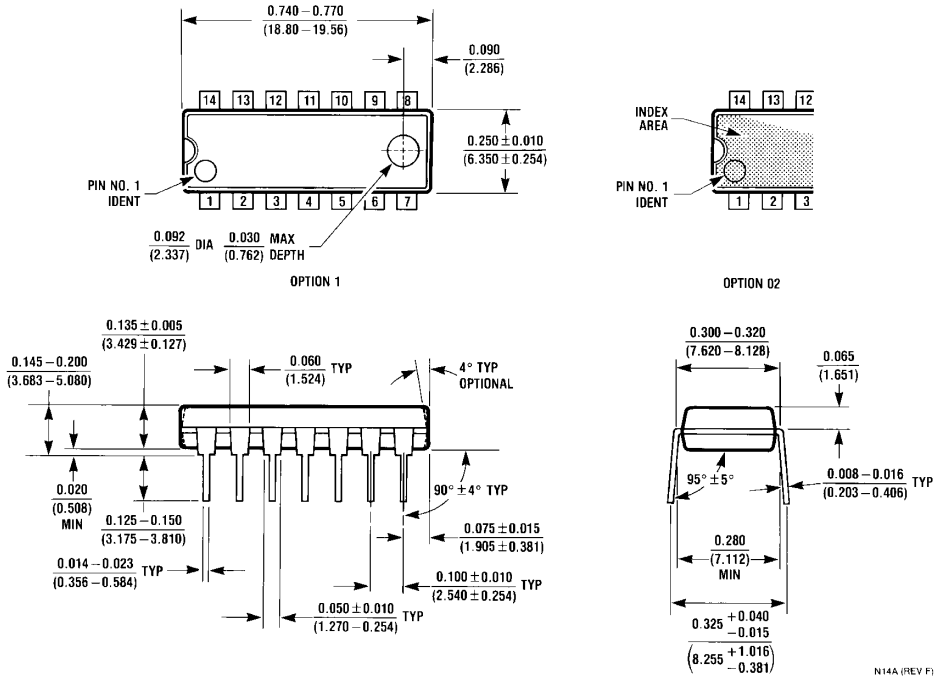
(R_{tc} and C_{tc} outputs are left open)





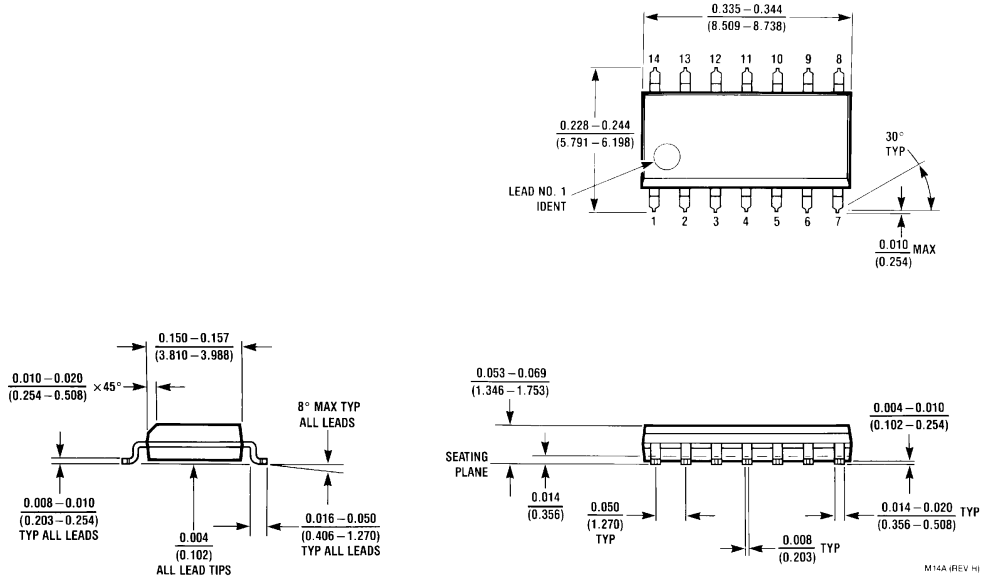
C

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150” Narrow
Package Number M16A

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