

FEATURES

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- DOC™ (Dynamic Output Control) Circuit Dynamically Changes Output Impedance, Resulting in Noise Reduction Without Speed Degradation
- Less Than 2-ns Maximum Propagation Delay at 2.5-V and 3.3-V V_{CC}

- Dynamic Drive Capability Is Equivalent to Standard Outputs With I_{OH} and I_{OL} of ± 24 mA at 2.5-V V_{CC}
- Overvoltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- Package Options Include Plastic Thin Shrink Small-Outline (DGG) and Thin Very Small-Outline (DGV) Packages

DESCRIPTION

A Dynamic Output Control (DOC™) circuit is implemented, which, during the transition, initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. [Figure 1](#) shows typical V_{OL} vs I_{OL} and V_{OH} vs I_{OH} curves to illustrate the output impedance and drive capability of the circuit. At the beginning of the signal transition, the DOC circuit provides a maximum dynamic drive that is equivalent to a high-drive standard-output device. For more information, refer to the TI application reports, *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

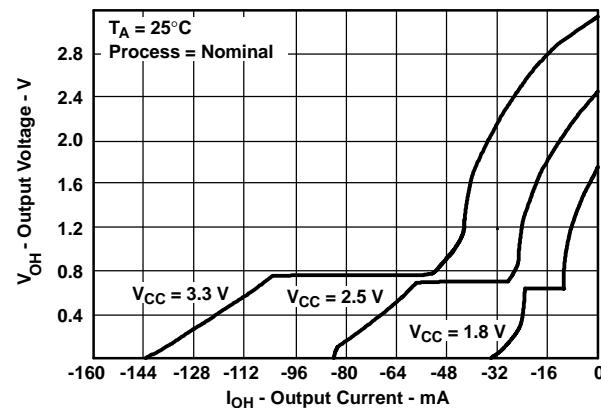
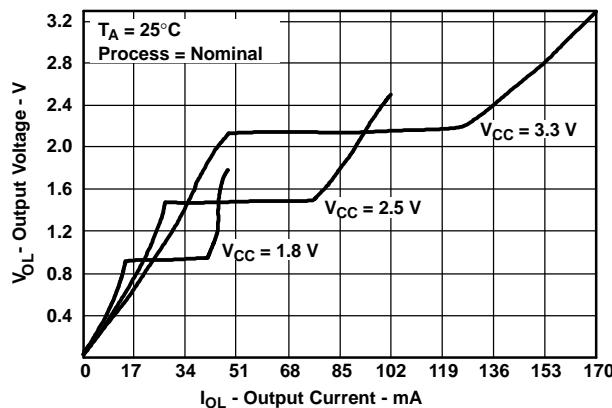


Figure 1. Output Voltage vs Output Current

This 20-bit noninverting buffer/driver is operational at 1.2-V to 3.6-V V_{CC} , but is designed specifically for 1.65-V to 3.6-V V_{CC} operation.

The SN74AVC16827 is composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable ($1\overline{OE}1$ and $1\overline{OE}2$ or $2\overline{OE}1$ and $2\overline{OE}2$) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The SN74AVC16827 is characterized for operation from -40°C to 85°C .



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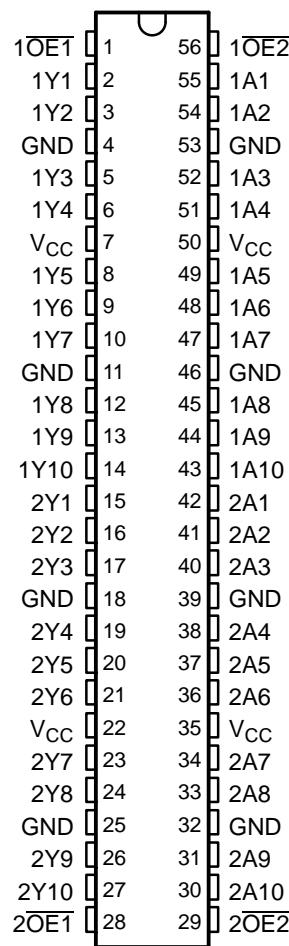
SN74AVC16827
20-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

SCES176I—DECEMBER 1998—REVISED JUNE 2005

 **TEXAS**
INSTRUMENTS
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TERMINAL ASSIGNMENTS

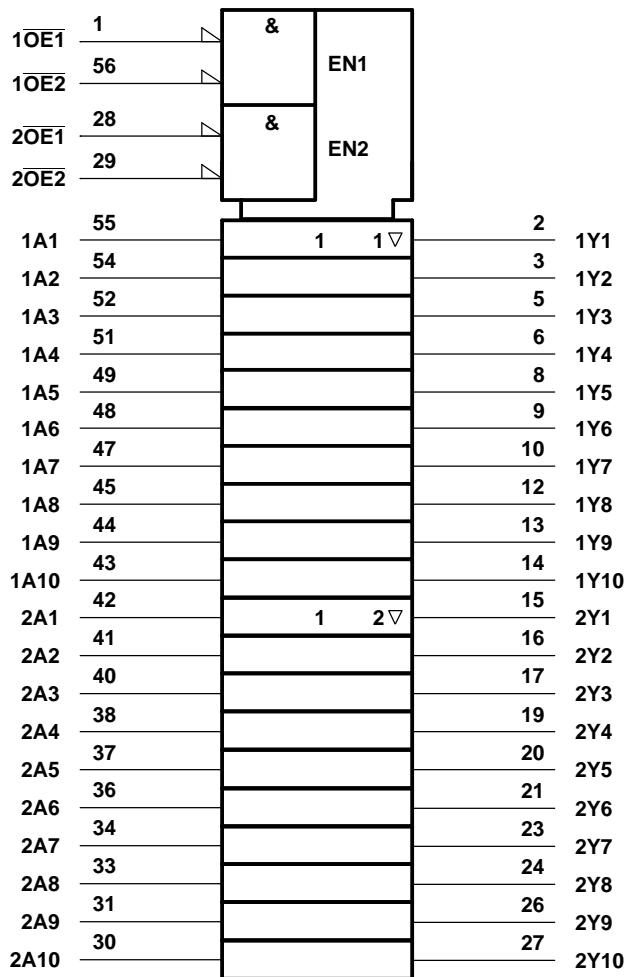
**DGG OR DGV PACKAGE
(TOP VIEW)**



**FUNCTION TABLE
(EACH 10-BIT BUFFER/DRIVER)**

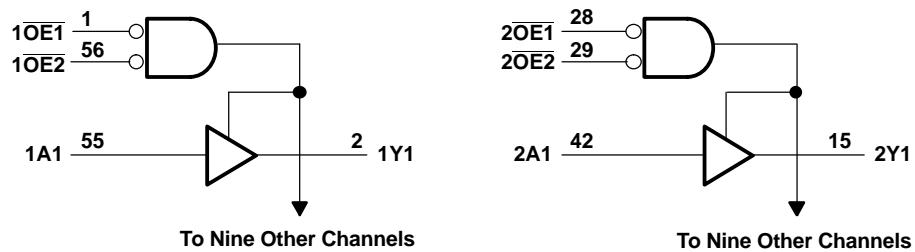
INPUTS			OUTPUT Y
OE1	OE2	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

LOGIC SYMBOL⁽¹⁾



(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM (POSITIVE LOGIC)



SN74AVC1682T

20-BIT BUFFER/DRIVER

WITH 3-STATE OUTPUTS

SCES176I—DECEMBER 1998—REVISED JUNE 2005



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	4.6	V
V_I	Input voltage range ⁽²⁾	-0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	4.6	V
V_O	Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$	-50	mA
I_{OK}	Output clamp current	$V_O < 0$	-50	mA
I_O	Continuous output current		± 50	mA
	Continuous current through each V_{CC} or GND		± 100	mA
θ_{JA}	Package thermal impedance ⁽⁴⁾	DGG package	64	°C/W
		DGV package	48	
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output ratings may be exceeded if the input and output current ratings are observed.

(3) This value is limited to 4.6 V maximum.

(4) The package thermal impedance is calculated in accordance with JESD 51.

Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	1.2	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 1.2$ V	V_{CC}	V
		$V_{CC} = 1.4$ V to 1.6 V	$0.65 \times V_{CC}$	
		$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$	
		$V_{CC} = 2.3$ V to 2.7 V	1.7	
		$V_{CC} = 3$ V to 3.6 V	2	
V_{IL}	Low-level input voltage	$V_{CC} = 1.2$ V	GND	V
		$V_{CC} = 1.4$ V to 1.6 V	$0.35 \times V_{CC}$	
		$V_{CC} = 1.65$ V to 1.95 V	$0.35 \times V_{CC}$	
		$V_{CC} = 2.3$ V to 2.7 V	0.7	
		$V_{CC} = 3$ V to 3.6 V	0.8	
V_I	Input voltage	0	3.6	V
V_O	Output voltage	Active state	0	V_{CC}
		3-state	0	
I_{OHS}	Static high-level output current ⁽¹⁾	$V_{CC} = 1.4$ V to 1.6 V	-2	mA
		$V_{CC} = 1.65$ V to 1.95 V	-4	
		$V_{CC} = 2.3$ V to 2.7 V	-8	
		$V_{CC} = 3$ V to 3.6 V	-12	
I_{OLS}	Static low-level output current ⁽¹⁾	$V_{CC} = 1.4$ V to 1.6 V	2	mA
		$V_{CC} = 1.65$ V to 1.95 V	4	
		$V_{CC} = 2.3$ V to 2.7 V	8	
		$V_{CC} = 3$ V to 3.6 V	12	
$\Delta t/\Delta V$	Input transition rise or fall rate	$V_{CC} = 1.4$ V to 3.6 V	5	ns/V
T_A	Operating free-air temperature	-40	85	°C

(1) Dynamic drive capability is equivalent to standard outputs with I_{OH} and I_{OL} of ± 24 mA at 3.3-V V_{CC} . See Figure 1 for V_{OL} vs I_{OL} and V_{OH} vs I_{OH} characteristics. Refer to the TI application reports, *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	I _{OHS} = -100 μ A, V _{IH} = V _{CC}	1.4 V to 3.6 V	V _{CC} - 0.2			V
	I _{OHS} = -2 mA, V _{IH} = 0.91 V	1.4 V		1.05		
	I _{OHS} = -4 mA, V _{IH} = 1.07 V	1.65 V		1.2		
	I _{OHS} = -8 mA, V _{IH} = 1.7 V	2.3 V		1.75		
	I _{OHS} = -12 mA, V _{IH} = 2 V	3 V		2.3		
V _{OL}	I _{OLS} = 100 μ A	1.4 V to 3.6 V		0.2		V
	I _{OLS} = 2 mA, V _{IL} = 0.49 V	1.4 V		0.4		
	I _{OLS} = 4 mA, V _{IL} = 0.57 V	1.65 V		0.45		
	I _{OLS} = 8 mA, V _{IL} = 0.7 V	2.3 V		0.55		
	I _{OLS} = 12 mA, V _{IL} = 0.8 V	3 V		0.7		
I _I	V _I = V _{CC} or GND	3.6 V		\pm 2.5	μ A	
I _{off}	V _I or V _O = 3.6 V	0		\pm 10	μ A	
I _{OZ}	V _O = V _{CC} or GND, V _{IH} = V _{CC}	3.6 V		\pm 12.5	μ A	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V		40	μ A	
C _i	Control inputs	V _I = V _{CC} or GND	2.5 V		4	pF
			3.3 V		4	
	Data inputs	V _I = V _{CC} or GND	2.5 V		2.5	
			3.3 V		2.5	
C _o	Outputs	V _O = V _{CC} or GND	2.5 V		6.5	pF
			3.3 V		6.5	

(1) Typical values are measured at T_A = 25°C.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2 through Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.2 V	V _{CC} = 1.5 V \pm 0.1 V	V _{CC} = 1.8 V \pm 0.15 V	V _{CC} = 2.5 V \pm 0.2 V	V _{CC} = 3.3 V \pm 0.3 V	UNIT
			TYP	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	3	0.4	3.2	0.9	2.9	0.8 1.9 0.5 1.7 ns
t _{en}	\overline{OE}	Y	8.7	2.3	9.1	2.1	8	1.4 5.6 1.2 5.1 ns
t _{dis}	\overline{OE}	Y	7.5	2.7	8.3	2.5	7.3	0.9 4.9 1 4.7 ns

Switching Characteristics⁽¹⁾

T_A = 0°C to 85°C, C_L = 0 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V \pm 0.15 V	UNIT
			MIN	
t _{pd}	A	Y	0.09 0.67 ns	

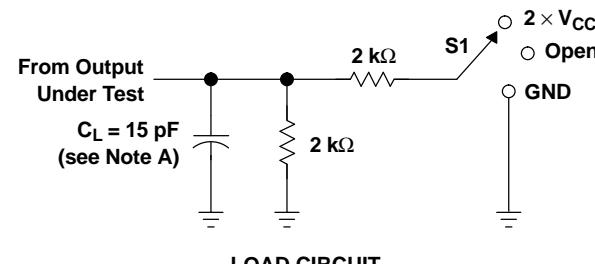
(1) Texas Instruments SPICE simulation data

Operating Characteristics

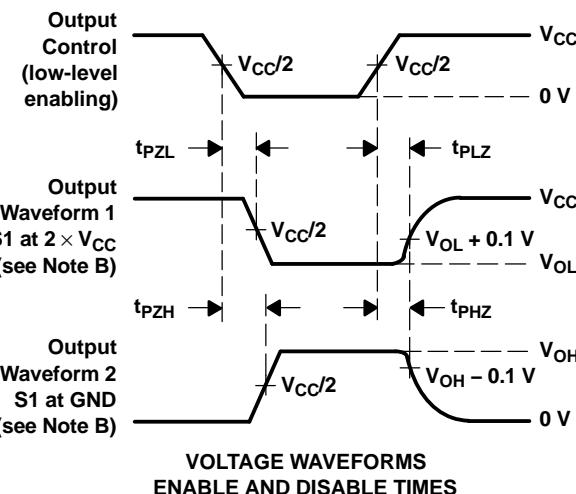
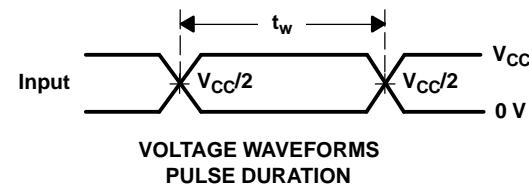
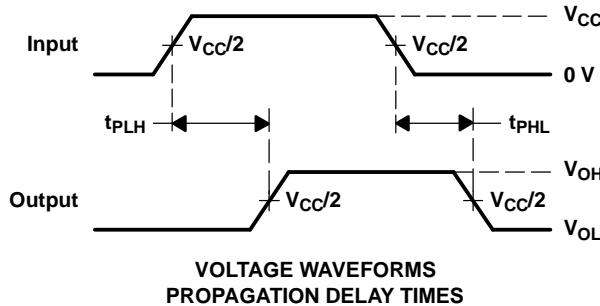
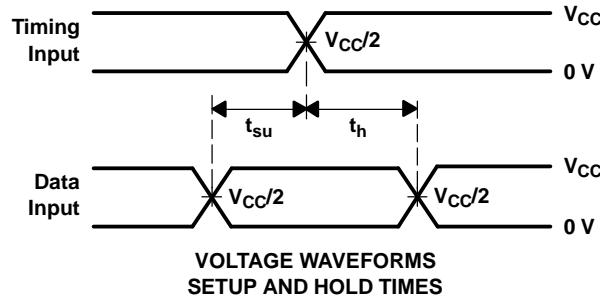
T_A = 25°C

PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT	
		TYP	TYP	TYP		
C _{pd}	Power dissipation capacitance	C _L = 0, f = 10 MHz	31	35	40	pF
			6	6	6	

PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 1.2 \text{ V AND } 1.5 \text{ V} \pm 0.1 \text{ V}$



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

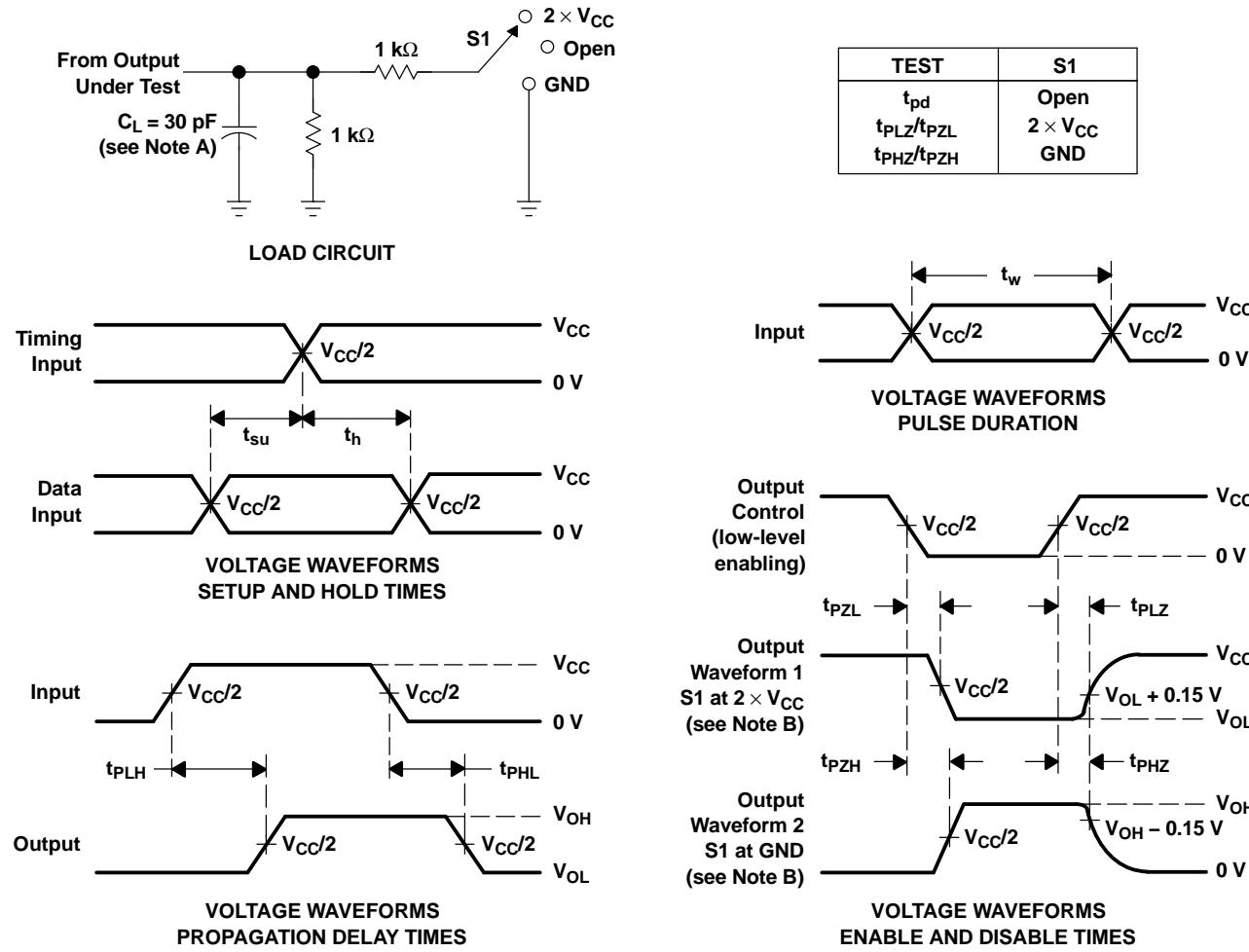


NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- The outputs are measured one at a time, with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$



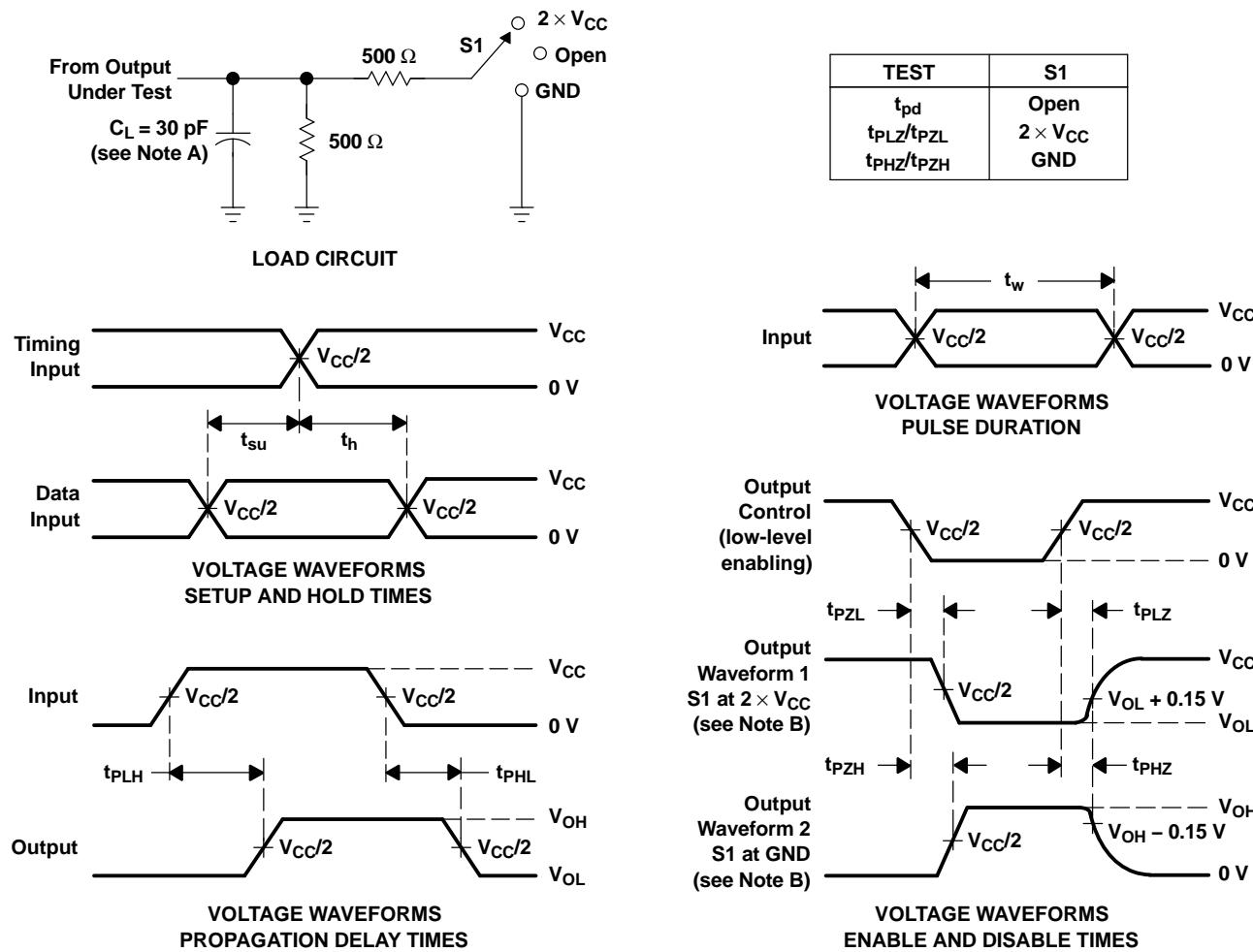
NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- The outputs are measured one at a time, with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

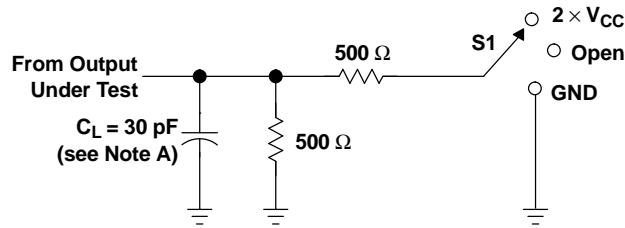


NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- The outputs are measured one at a time, with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLH} and t_{PHL} are the same as t_{pd} .

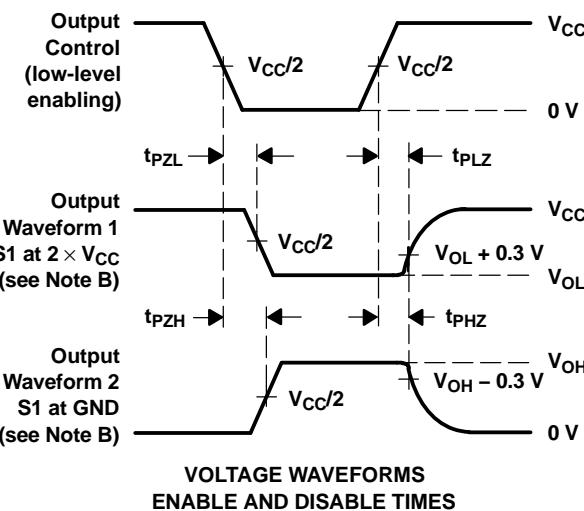
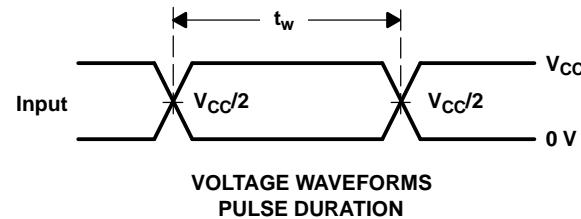
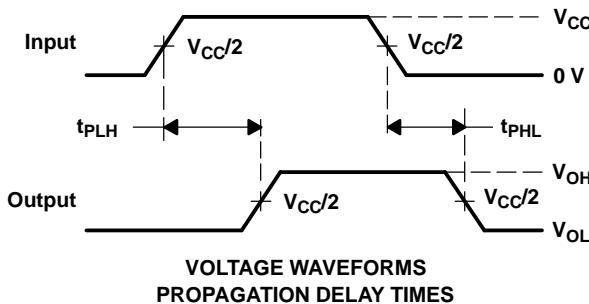
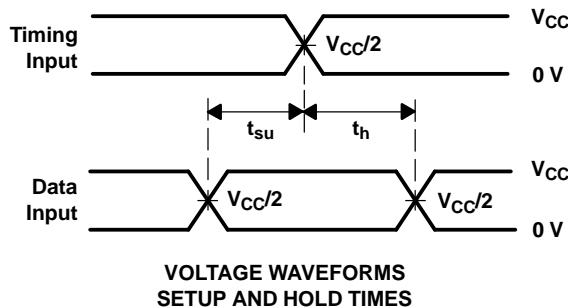
Figure 4. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- The outputs are measured one at a time, with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 5. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74AVC16827DGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AVC16827DGVR4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AVC16827DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AVC16827DGVR	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

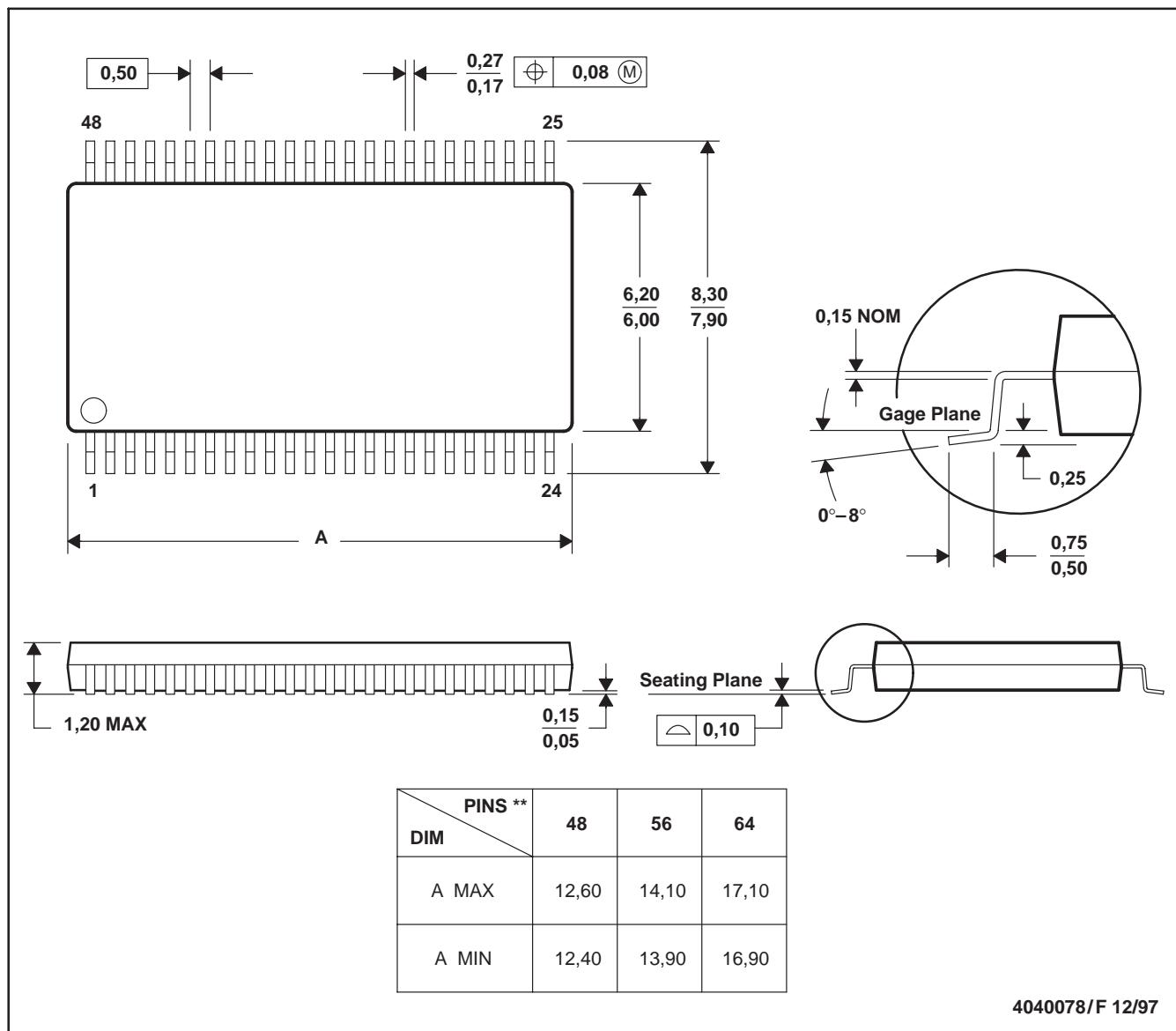


NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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