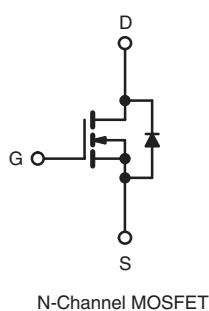
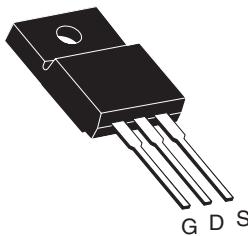


Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	60	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10$ V	0.028
Q_g (Max.) (nC)	95	
Q_{gs} (nC)	27	
Q_{gd} (nC)	46	
Configuration	Single	

TO-220 FULLPAK


FEATURES

- Isolated Package
- High Voltage Isolation = 2.5 kV_{RMS} ($t = 60$ s; $f = 60$ Hz)
- Sink to Lead Creepage Distance = 4.8 mm
- 175 °C Operating Temperature
- Dynamic dV/dt Rating
- Low Thermal Resistance
- Lead (Pb)-free Available


RoHS*
COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 FULLPAK eliminates the need for additional insulating hardware in commercial-industrial applications. The molding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. The isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The FULLPAK is mounted to a heatsink using a single clip or by a single screw fixing.

ORDERING INFORMATION

Package	TO-220 FULLPAK
Lead (Pb)-free	IRFIZ44GPbF SiHFIZ44G-E3
SnPb	IRFIZ44G SiHFIZ44G

ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	60	
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	30	A
		21	
Pulsed Drain Current ^a	I_{DM}	120	
Linear Derating Factor		0.32	W/°C
Single Pulse Avalanche Energy ^b	E_{AS}	100	mJ
Maximum Power Dissipation	P_D	48	W
Peak Diode Recovery dV/dt ^c	dV/dt	4.5	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	
Mounting Torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. $V_{DD} = 25$ V, starting $T_J = 25$ °C, $L = 129$ μ H, $R_G = 25$ Ω , $I_{AS} = 30$ A (see fig. 12).

c. $I_{SD} \leq 52$ A, $dI/dt \leq 250$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 175$ °C.

d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	65	$^{\circ}\text{C}/\text{W}$
Maximum Junction-to-Case (Drain)	R_{thJC}	-	3.1	

SPECIFICATIONS $T_J = 25^{\circ}\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}$	$I_D = 250 \mu\text{A}$	60	-	-	V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25°C , $I_D = 1 \text{ mA}$		-	0.060	-	$^{\circ}\text{C}/\text{V}$	
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$		2.0	-	4.0	V	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60 \text{ V}$, $V_{GS} = 0 \text{ V}$		-	-	25	μA	
		$V_{DS} = 48 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 150^{\circ}\text{C}$		-	-	250		
Drain-Source On-State Resistance	$R_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}$	$I_D = 18 \text{ A}^b$	-	-	0.028	Ω	
Forward Transconductance	g_{fs}	$V_{DS} = 25 \text{ V}$, $I_D = 18 \text{ A}^b$		15	-	-	S	
Dynamic								
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}$, $V_{DS} = 25 \text{ V}$, $f = 1.0 \text{ MHz}$, see fig. 5		-	2500	-	pF	
Output Capacitance	C_{oss}			-	1200	-		
Reverse Transfer Capacitance	C_{rss}			-	200	-		
Drain to Sink Capacitance	C	$f = 1.0 \text{ MHz}$		-	12	-	nC	
Total Gate Charge	Q_g	$V_{GS} = 10 \text{ V}$	$I_D = 52 \text{ A}$, $V_{DS} = 48 \text{ V}$, see fig. 6 and 13 ^b	-	-	95		
Gate-Source Charge	Q_{gs}			-	-	27		
Gate-Drain Charge	Q_{gd}			-	-	46		
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = 30 \text{ V}$, $I_D = 52 \text{ A}$, $R_G = 9.1 \Omega$, $R_D = 0.54 \Omega$, see fig. 10 ^b		-	19	-	ns	
Rise Time	t_r			-	120	-		
Turn-Off Delay Time	$t_{d(\text{off})}$			-	55	-		
Fall Time	t_f			-	86	-		
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH	
Internal Source Inductance	L_S			-	7.5	-		
Drain-Source Body Diode Characteristics								
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	30	A	
Pulsed Diode Forward Current ^a	I_{SM}			-	-	120		
Body Diode Voltage	V_{SD}	$T_J = 25^{\circ}\text{C}$, $I_S = 30 \text{ A}$, $V_{GS} = 0 \text{ V}^b$		-	-	2.5	V	
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}\text{C}$, $I_F = 52 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}^b$		-	140	300	ns	
Body Diode Reverse Recovery Charge	Q_{rr}			-	1.2	2.8	μC	
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)						

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width $\leq 300 \mu\text{s}$; duty cycle $\leq 2\%$.

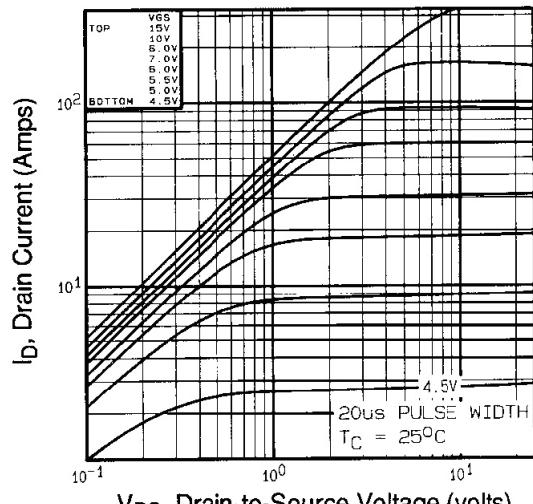
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ\text{C}$

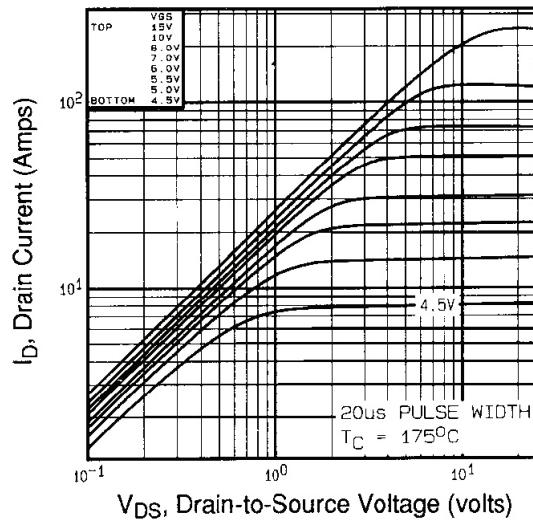
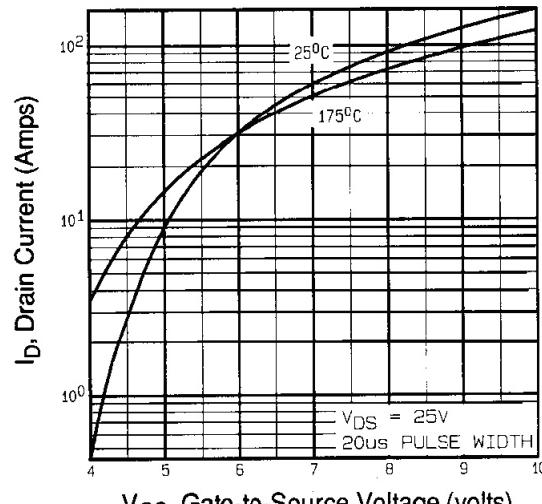
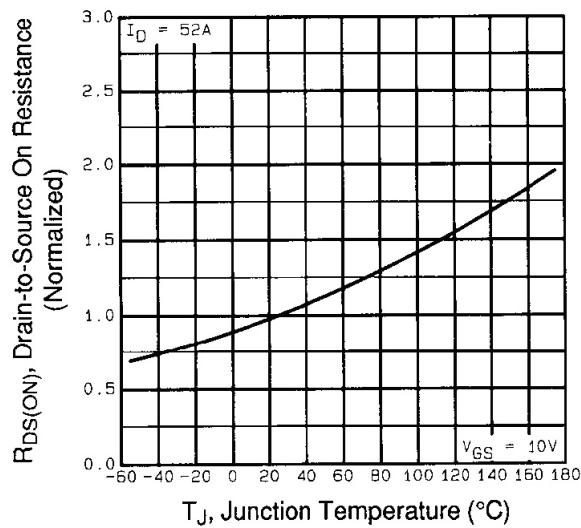


Fig. 2 - Typical Output Characteristics, $T_C = 175^\circ\text{C}$



IRFIZ44G, SiHFIZ44G

Vishay Siliconix

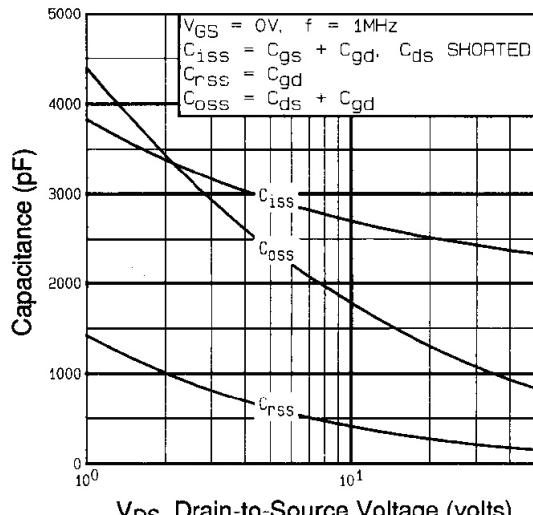


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

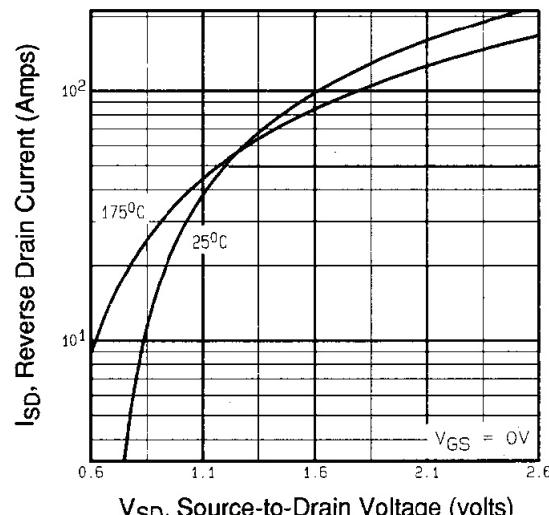


Fig. 7 - Typical Source-Drain Diode Forward Voltage

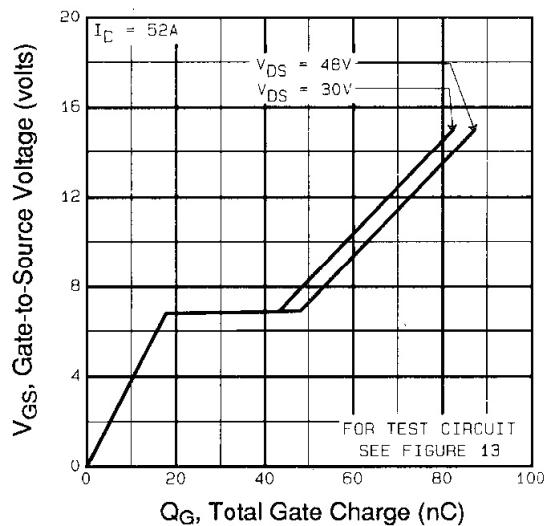


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

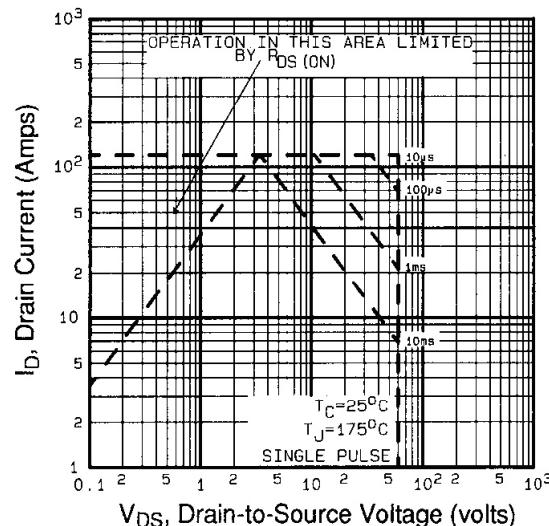


Fig. 8 - Maximum Safe Operating Area

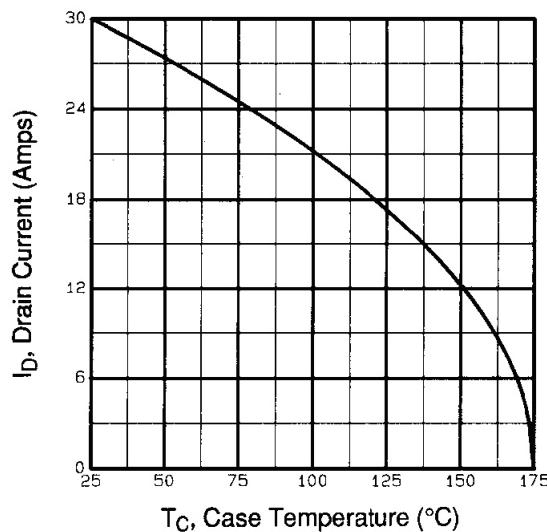


Fig. 9 - Maximum Drain Current vs. Case Temperature

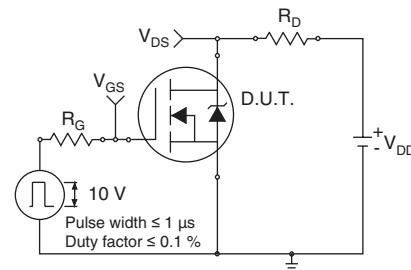


Fig. 10a - Switching Time Test Circuit

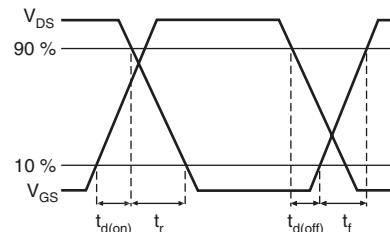


Fig. 10b - Switching Time Waveforms

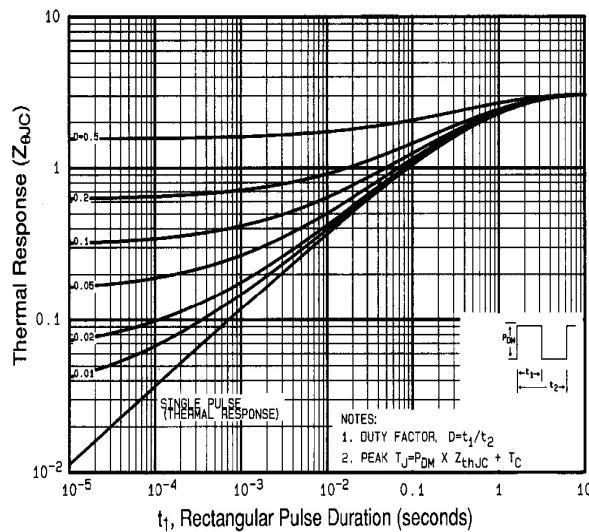


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

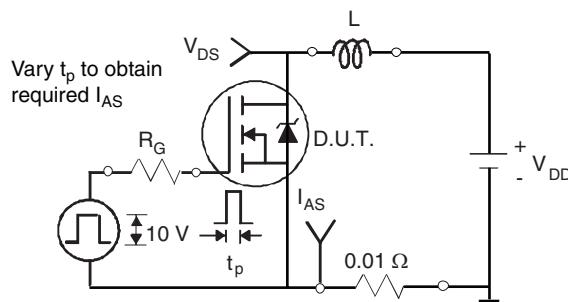


Fig. 12a - Unclamped Inductive Test Circuit

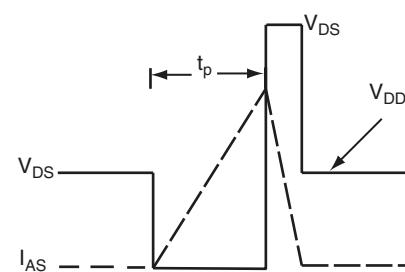


Fig. 12b - Unclamped Inductive Waveforms

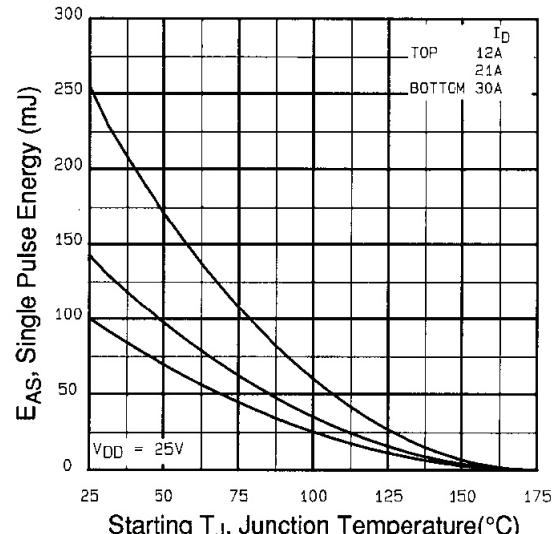


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

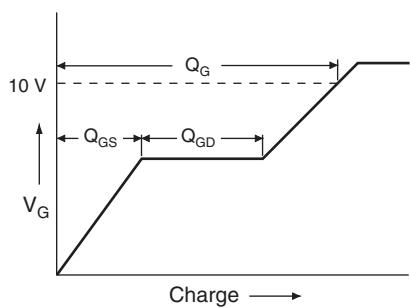


Fig. 13a - Basic Gate Charge Waveform

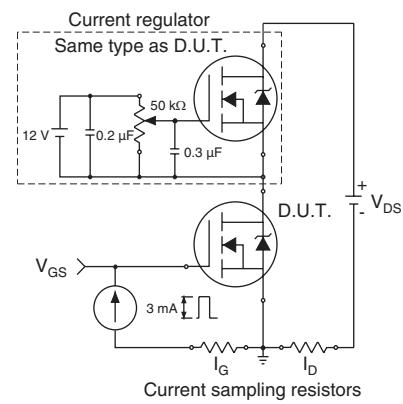
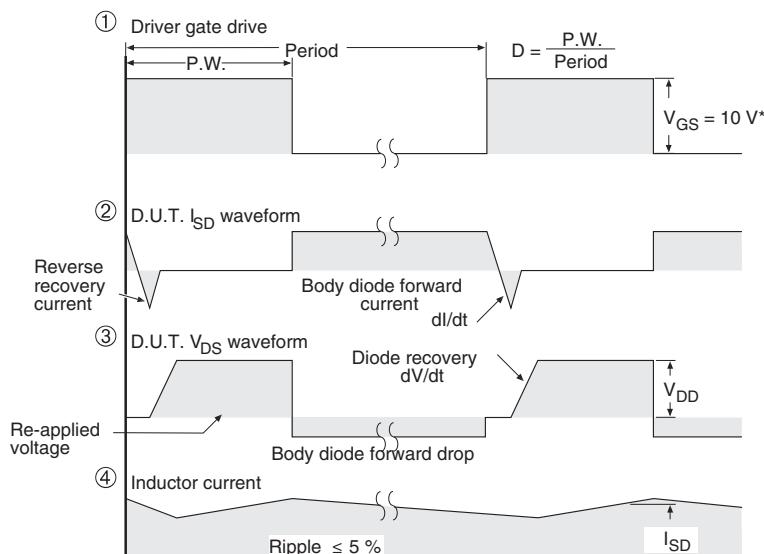
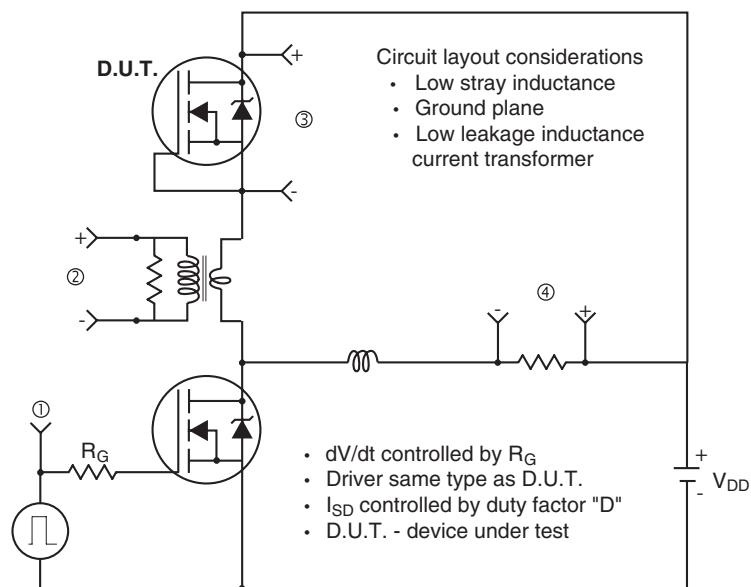


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5 \text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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