



CYPRESS

**ADVANCE  
INFORMATION**

**CY2410**

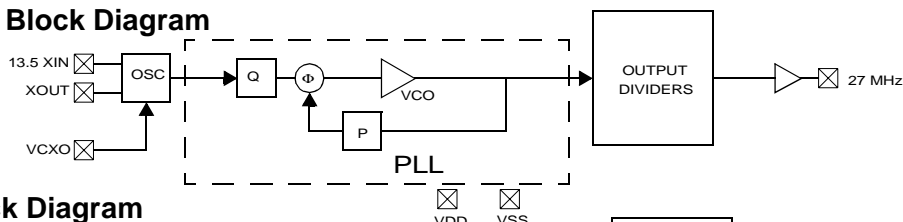
## MPEG Clock Generator with VCXO

| Features   | Benefits   |
|--|--|
| • Integrated phase-locked loop (PLL)             | Highest performance PLL tailored for multimedia applications |
| • Low-jitter, high-accuracy outputs              | Meets critical timing requirements in complex system designs |
| • VCXO with analog adjust                        | Large +/-150 ppm range, better linearity                     |
| • 3.3V operation                                 | Application compatibility for a wide variety of designs      |
| • Pin-for-pin compatible with MK3727 (-1,-4, -5) | Enables design compatibility                                 |

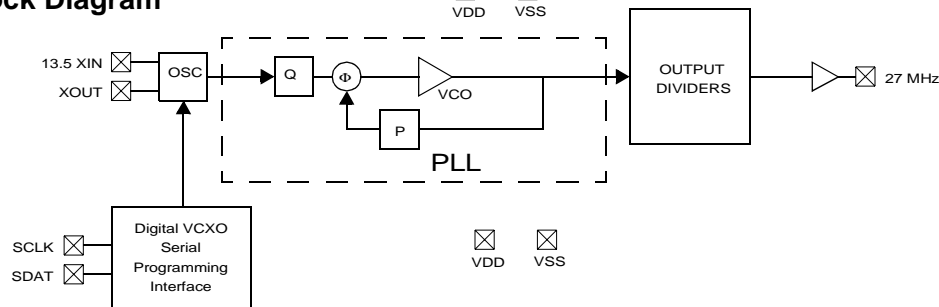
| Advanced Features   | Benefits  |
|---|---|
| • Serial programming interface (CY2410-3 only)                | Digital VCXO control  |
| • Lower drive strength settings (CY2410-4 only)               | Electromagnetic interference (EMI) reduction for standards compliance |
| • Matches nonlinear MK3727 VCXO control curve (CY2410-5 only) | Drop in replacement for existing designs                              |

| Part Number | Outputs | Input Frequency Range                                     | Output Frequencies | VCXO Control Curve | Other Features  |
|-------------|---------|---|--------------------|--------------------|---|
| CY2410-1    | 1       | 13.5-MHz pullable crystal input per Cypress specification | 1 copy of 27 MHz   | linear             | Pin-for-pin compatible with MK3727                    |
| CY2410-3    | 1       | 13.5-MHz pullable crystal input per Cypress specification | 1 copy of 27 MHz   | linear             | Serial programming interface                          |
| CY2410-4    | 1       | 13.5-MHz pullable crystal input per Cypress specification | 1 copy of 27 MHz   | linear             | Same as CY2410-1 except lower drive strength settings |
| CY2410-5    | 1       | 13.5-MHz pullable crystal input per Cypress specification | 1 copy of 27 MHz   | nonlinear          | Matches MK3727 nonlinear VCXO Control Curve           |

### CY2410-1,-4,-5 Logic Block Diagram

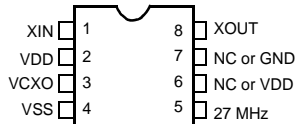


### CY2410-3 Logic Block Diagram

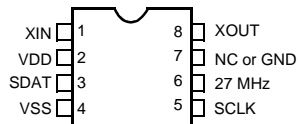


### Pin Configuration

#### CY2410-1,4,5 8-pin SOIC



#### CY2410-3 8-pin SOIC



**CY2410-1, -4, -5 Pin Descriptions**

| Name                            | Pin Number | Description                               |
|---------------------------------|------------|---|
| X <sub>IN</sub>                 | 1          | Reference crystal input                   |
| V <sub>DD</sub>                 | 2          | Voltage supply                            |
| V <sub>CXO</sub>                | 3          | Input analog control for V <sub>CXO</sub> |
| V <sub>SS</sub>                 | 4          | Ground                                    |
| 27 MHz                          | 5          | 27-MHz clock output                       |
| No Connect (NC)/V <sub>DD</sub> | 6          | NC or voltage supply                      |
| NC/V <sub>SS</sub>              | 7          | NC or ground                              |
| X <sub>OUT</sub> <sup>[1]</sup> | 8          | Reference crystal output                  |

**CY2410-3 Pin Description**

| Name                            | Pin Number | Description                         |
|---------------------------------|------------|-------------------------------------|
| X <sub>IN</sub>                 | 1          | Reference crystal input             |
| V <sub>DD</sub>                 | 2          | Voltage supply                      |
| SDAT                            | 3          | Serial data input for DCXO control  |
| V <sub>SS</sub>                 | 4          | Ground                              |
| SCLK                            | 5          | Serial clock input for DCXO control |
| 27 MHz                          | 6          | 27-MHz clock output                 |
| NC/V <sub>SS</sub>              | 7          | NC or ground                        |
| X <sub>OUT</sub> <sup>[1]</sup> | 8          | Reference crystal output            |

**Pullable Crystal Specifications**

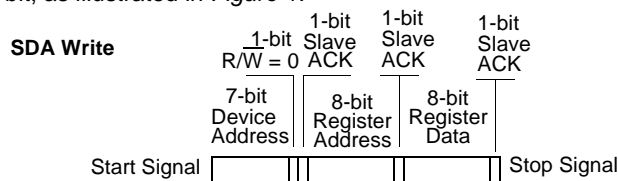
| Parameter          | Name                                 | Min. | Typ. | Max. | Unit |
|--------------------|--------------------------------------|------|------|------|------|
| CR <sub>load</sub> | Crystal load capacitance             |      | 14   |      | pF   |
| C0/C1              |                                      |      | 240  |      |      |
| ESR                | Equivalent series resistance         |      | 35   |      | W    |
| T <sub>o</sub>     | Operating temperature                | 0    |      | 70   | °C   |
| Crystal Accuracy   | Crystal accuracy                     |      |      | ±20  | ppm  |
| TT <sub>s</sub>    | Stability over temperature and aging |      |      | ±50  | ppm  |

**Note:**

1. Float X<sub>OUT</sub> if X<sub>IN</sub> is externally driven.

## Serial Programmable Interface Protocol

The CY2410-3 utilizes a two-wire-interface SDAT and SCLK that operates up to 400 kbits/sec in Read or Write mode. The basic Write serial format is as follows: start bit; 7-bit device address (DA); R/W bit; slave clock acknowledge (ACK); 8-bit memory address (MA); ACK; 8-bit data; ACK; 8-bit data in MA+1 if desired; ACK; 8-bit data in MA+2; ACK; etc. until stop bit, as illustrated in *Figure 1*.



**Figure 1. Data Frame Architecture**

## Data Valid

Data is valid when the clock is HIGH, and may only be transitioned when the clock is low as illustrated in *Figure 2*.

## Data Frame

Every new data frame is indicated by a start and stop sequence, as illustrated in *Figure 3*.

## Start Sequence

A start frame is indicated by SDAT going LOW when SCLK is HIGH. Every time a start signal is given, the next 8-bit data must be the device address (7 bits) and a R/W bit (0 for Write), followed by register address (8 bits) and register data (8 bits). See *Figure 3*.

## Stop Sequence

A stop frame is indicated by SDAT going HIGH when SCLK is HIGH. A stop frame frees the bus for writing to another part on the same bus or writing to another random register address. See *Figure 3*.

## Acknowledge Pulse

During Write mode, the CY2410-3 will respond with an ACK pulse after every 8 bits. This is accomplished by pulling the

SDAT line LOW during the next clock cycle after the eighth bit is shifted in.

## Device Address

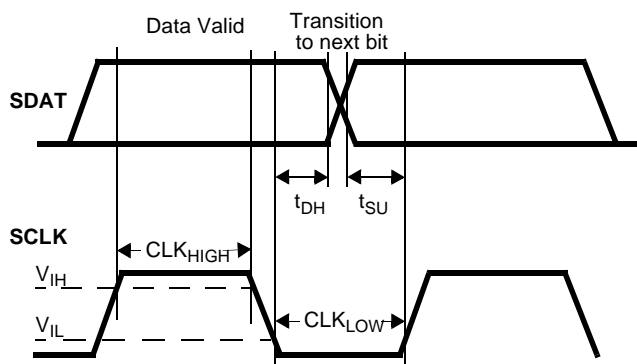
The 7-bit device address is 1101001.

## Register Address

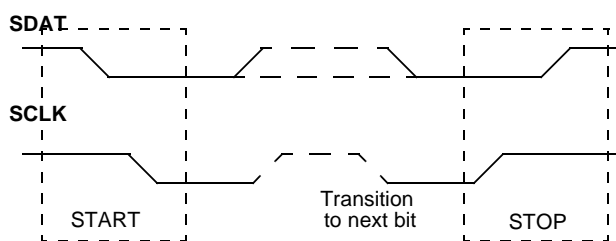
The 8-bit address for the VCXO register is 00010011.

## Register Data

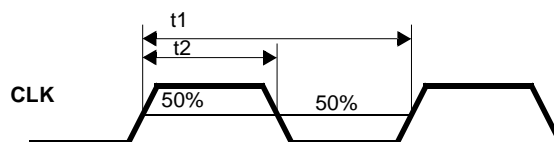
The register data can be any value between 00H–FFH. As you increase the value, the capacitance on the  $X_{IN}$  and  $X_{OUT}$  pins will increase, thereby decreasing the xtal frequency.



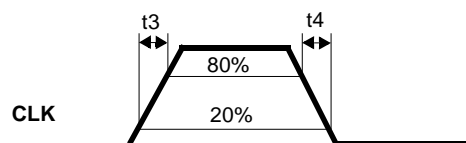
**Figure 2. Data Valid and Data Transition Periods**



**Figure 3. Start and Stop Frame**



**Figure 4. Duty Cycle Definition;  $DC = t_2/t_1$**



**Figure 5. Rise and Fall Time Definitions**

**Absolute Maximum Conditions**

| Parameter | Description                          | Min.           | Max.           | Unit |
|-----------|--------------------------------------|----------------|----------------|------|
| $V_{DD}$  | Supply Voltage                       | -0.5           | 7.0            | V    |
| $T_S$     | Storage Temperature <sup>[2]</sup>   | -65            | 125            | °C   |
| $T_J$     | Junction Temperature                 |                | 125            | °C   |
|           | Digital Inputs                       | $V_{SS} - 0.3$ | $V_{DD} + 0.3$ | V    |
|           | Digital Outputs referred to $V_{DD}$ | $V_{SS} - 0.3$ | $V_{DD} + 0.3$ | V    |
|           | Electrostatic Discharge              |                | 2000           | V    |
|           | Analog Input                         |                | 10 sec         |      |

**Recommended Operating Conditions**

| Parameter  | Description           | Min.  | Typ. | Max.  | Unit |
|------------|-----------------------|-------|------|-------|------|
| $V_{DD}$   | Operating Voltage     | 3.135 | 3.3  | 3.465 | V    |
| $T_A$      | Ambient Temperature   | 0     |      | 70    | °C   |
| $C_{LOAD}$ | Max. Load Capacitance |       |      | 15    | pF   |
| $f_{REF}$  | Reference Frequency   |       | 13.5 |       | MHz  |

**DC Electrical Characteristics**

| Parameter       | Name                        | Description                               | Min. | Typ.      | Max.     | Unit |
|-----------------|-----------------------------|---|------|-----------|----------|------|
| $I_{OH}$        | Output HIGH Current -1,3,5  | $V_{OH} = V_{DD} - 0.5$ , $V_{DD} = 3.3V$ | 12   | 24        |          | mA   |
| $I_{OL}$        | Output LOW Current -1,3,5   | $V_{OL} = 0.5$ , $V_{DD} = 3.3V$          | 12   | 24        |          | mA   |
| $I_{OH}$        | Output HIGH Current -4      | $V_{OH} = V_{DD} - 0.5$ , $V_{DD} = 3.3V$ | 6    | 18        |          | mA   |
| $I_{OL}$        | Output LOW Current -4       | $V_{OL} = 0.5$ , $V_{DD} = 3.3V$          | 6    | 18        |          | mA   |
| $C_{IN}$        | Input Capacitance           |   |      |           | 7        | pF   |
| $I_{IZ}$        | Input Leakage Current       |   |      | 5         |          | μA   |
| $f_{\Delta XO}$ | $V_{CXO}$ pullability range |   | -150 |           | +150     | ppm  |
| $V_{VCXO}$      | $V_{CXO}$ input range       |   | 0    |           | $V_{DD}$ | V    |
| $f_{VBW}$       | $V_{CXO}$ input bandwidth   |   |      | DC to 200 |          | kHz  |
| $I_{VDD}$       | Supply Current              |   |      | 30        | 35       | mA   |

**AC Electrical Characteristics ( $V_{DD} = 3.3V$ )<sup>[3]</sup>**

| Parameter <sup>[3]</sup> | Name                          | Description  | Min. | Typ. | Max. | Unit |
|--------------------------|-------------------------------|--|------|------|------|------|
| DC                       | Output Duty Cycle             | Duty Cycle is defined in <i>Figure 4</i> , 50% of $V_{DD}$ | 45   | 50   | 55   | %    |
| $t_3$                    | Rising Edge Slew Rate -1,3,5  | Output Clock Rise Time, 20%–80% of $V_{DD}$                | 0.8  | 1.4  |      | V/ns |
| $t_4$                    | Falling Edge Slew Rate -1,3,5 | Output Clock Fall Time, 80%–20% of $V_{DD}$                | 0.7  | 1.4  |      | V/ns |
| $t_3$                    | Rising Edge Slew Rate -4      | Output Clock Rise Time, 20%–80% of $V_{DD}$                | 0.7  | 1.1  |      | V/ns |
| $t_4$                    | Falling Edge Slew Rate -4     | Output Clock Fall Time, 80%–20% of $V_{DD}$                | 0.7  | 1.1  |      | V/ns |
| $t_9$                    | Clock Jitter -1,3,5           | Peak-to-peak period jitter                                 |      | 140  |      | ps   |
| $t_9$                    | Clock Jitter -4               | Peak-to-peak period jitter                                 |      | 150  |      | ps   |
| $t_{10}$                 | PLL Lock Time                 |  |      |      | 3    | ms   |

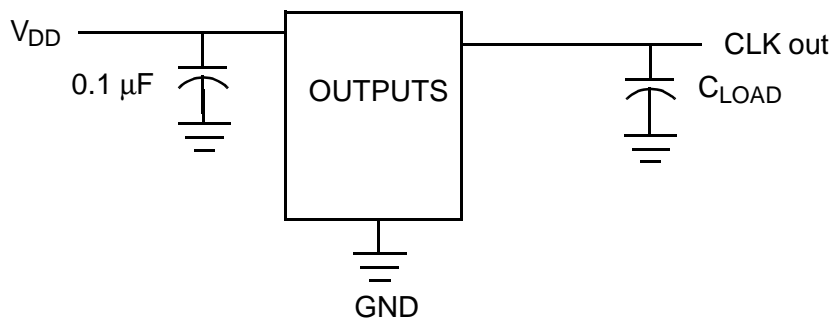
**Notes:**

2. Rated for ten years.
3. Not 100% tested.

## Serial Programming Interface Timing Specifications

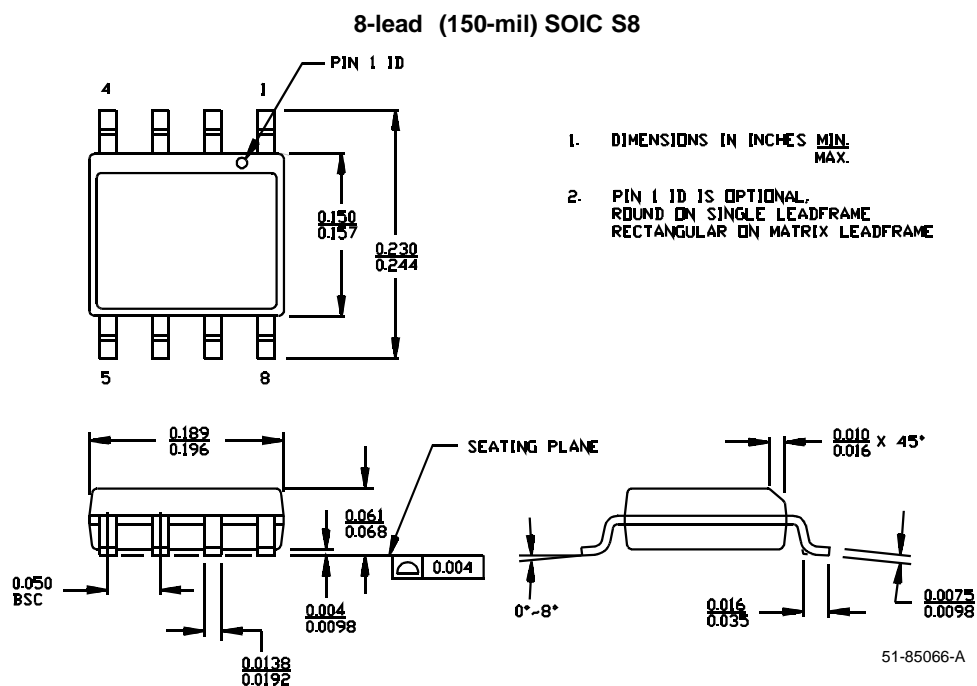
| Parameter    | Description                               | Min. | Max. | Unit    |
|--------------|---|------|------|---------|
| $f_{SCL}$    | Frequency of SCLK                         |      | 400  | kHz     |
|              | Start mode time from SDAT LOW to SCLK LOW | 0.6  |      | $\mu$ S |
| $CLK_{LOW}$  | SCLK LOW period                           | 1.3  |      | $\mu$ S |
| $CLK_{HIGH}$ | SCLK HIGH period                          | 0.6  |      | $\mu$ S |
| $t_{SU}$     | Data transition to SCLK HIGH              | 100  |      | ns      |
| $t_{DH}$     | Data hold (SCLK LOW to data transition)   | 0    |      | ns      |
|              | Rise time of SCLK and SDAT                |      | 300  | ns      |
|              | Fall time of SCLK and SDAT                |      | 300  | ns      |
|              | Stop mode time from SCLK HIGH to SDA HIGH | 0.6  |      | $\mu$ s |
|              | Stop mode to start mode                   | 1.3  |      | $\mu$ s |

## Test Circuit



## Ordering Information

| Ordering Code | Package Name | Package Type | Operating Range | Operating Voltage | Features                                    |
|---------------|--------------|--------------|-----------------|-------------------|---|
| CY2410SC-1    | S8           | 8-pin SOIC   | Commercial      | 3.3V              |   |
| CY2410SC-3    | S8           | 8-pin SOIC   | Commercial      | 3.3V              | Digital VCXO control                        |
| CY2410SC-4    | S8           | 8-pin SOIC   | Commercial      | 3.3V              | Lower drive strength (reduced EMI)          |
| CY2410SC-5    | S8           | 8-pin SOIC   | Commercial      | 3.3V              | Matches nonlinear MK3727 VCXO control curve |

**Package Diagram**


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| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
|------|---------|------------|-----------------|-----------------------|
| **   | 111553  | 02/12/02   | CKN             | New Data Sheet        |