

The ISL97642 integrates a high performance boost regulator with 2 LDO controllers for  $V_{ON}$  and  $V_{OFF}$ , a  $V_{ON}$ -slice circuit with adjustable delay and three amplifiers for  $V_{COM}$  and  $V_{GAMMA}$  applications.

The boost converter in the ISL97642 is a current mode PWM type integrating an 18V N-Channel MOSFET.

Using external low-cost transistors, the LDO controllers provide tight regulation for  $V_{ON}$ ,  $V_{OFF}$ , as well as providing start-up sequence control and fault protection.

The amplifiers are ideal for  $V_{COM}$  and  $V_{GAMMA}$  applications, with 150mA peak output current drive, 12MHz bandwidth, and 12V/ $\mu$ s slew rate. All inputs and outputs are rail-to-rail.

Available in the 32 Ld thin QFN (5mmx5mm) Pb-free package, the ISL97642 is specified for operation over the -40°C to +85°C temperature range.

## Features

- Current mode boost regulator
  - Fast transient response
  - 1% accurate output voltage
  - 18V/2.4A integrated FET
  - >90% efficiency
- 2.6V to 5.5V  $V_{IN}$  supply
- 2 LDO controllers for  $V_{ON}$  and  $V_{OFF}$ 
  - 2% output regulation
  - $V_{ON}$ -slice circuit
- High speed amplifiers
  - 150mA short-circuit output current
  - 12V/ $\mu$ s slew rate
  - 12MHz -3dB bandwidth
  - Rail-to-rail inputs and outputs
- Built-in power sequencing
- Internal soft-start
- Multiple overload protection
- Thermal shutdown
- 32 Ld 5x5 thin QFN package
- Pb-free plus anneal available (RoHS compliant)

## Applications

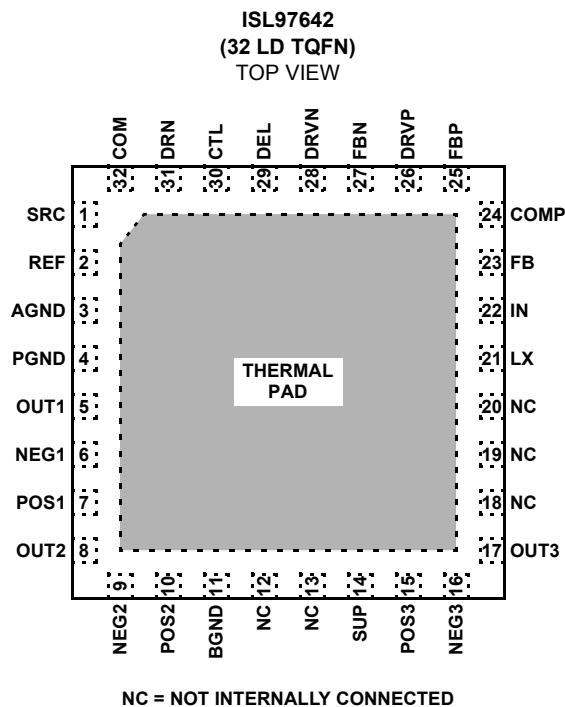
- TFT-LCD panels
- LCD monitors
- Notebooks
- LCD-TVs

## Ordering Information

PART NUMBER (Note)	PART MARKING	PACKAGE (Pb-free)	PKG. DWG. #
ISL97642IRTZ*	97642 IRTZ	32 Ld 5x5x0.75 TQFN	L32.5x5A

\*Add “-T” or “-TK” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

**Pinouts**

**Absolute Maximum Ratings** ( $T_A = +25^\circ\text{C}$ )

IN, CTL to AGND	-0.3V to +6.5V
COMP, FB, FBP, FBN, DEL, REF to AGND	-0.3V to $V_{IN} + 0.3V$
PGND, BGND to AGND	$\pm 0.3V$
LX to PGND	-0.3V to +24V
SUP to AGND	-0.3V to +18V
DRV <sub>P</sub> , SRC to AGND	-0.3V to +36V
POS1, NEG1, OUT1, POS2, NEG2, OUT2, POS3, OUT3	
DRV <sub>N</sub> to AGND	$V_{IN} - 20V$ to $V_{IN} + 0.3V$
COM, DRN to AGND	-0.3V to $V_{SRC} + 0.3V$
LX Maximum Continuous RMS Output Current	1.6A
OUT1, OUT2, OUT3, OUT4, OUT5	
Maximum Continuous Output Current	$\pm 75\text{mA}$

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

**IMPORTANT NOTE:** All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore:  $T_J = T_C = T_A$

**Electrical Specifications**  $V_{IN} = 3V$ ,  $V_{BOOST} = V_{SUP} = 12V$ ,  $V_{SRC} = 20V$ , Over-temperature from  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ . Unless Otherwise Specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY</b>						
$V_{IN}$	Input Supply Range		2.6		5.5	V
$V_{LOR}$	Undervoltage Lockout Threshold	$V_{IN}$ rising	2.4	2.5	2.6	V
$V_{LOF}$	Undervoltage Lockout Threshold	$V_{IN}$ falling	2.2	2.3	2.4	V
$I_S$	Quiescent Current	LX not switching			2.5	mA
$I_{SS}$	Quiescent Current - Switching	LX switching		5	10	mA
$T_{FD}$	Fault Delay Time	$C_{DEL} = 100\text{nF}$		23		ms
$V_{REF}$	Reference Voltage	$T_A = +25^\circ\text{C}$	1.19	1.215	1.235	V
			1.187	1.215	1.238	V
SHUTDN	Thermal Shutdown Temperature			140		$^\circ\text{C}$
<b>MAIN BOOST REGULATOR</b>						
$V_{BOOST}$	Output Voltage Range	(Note 1)	$V_{IN} + 15\%$		18	V
$f_{OSC}$	Oscillator Frequency		1050	1200	1350	kHz
$D_{CM}$	Maximum Duty Cycle		82	85		%
$V_{FB}$	Boost Feedback Voltage	$T_A = +25^\circ\text{C}$	1.192	1.205	1.218	V
			1.188	1.205	1.222	V
$V_{FTB}$	FB Fault Trip Level	Falling edge	0.85	0.925	1.020	V
$\Delta V_{BOOST}/\Delta I_{BOOST}$	Load Regulation	$50\text{mA} < I_{LOAD} < 250\text{mA}$		0.1		%
$\Delta V_{BOOST}/\Delta V_{IN}$	Line Regulation	$V_{IN} = 2.6V$ to $5.5V$		0.08		%/V
$I_{FB}$	Input Bias Current	$V_{FB} = 1.35V$			500	nA
$gmV$	FB Transconductance	$dl = \pm 2.5\mu\text{A}$ at COMP, FB = COMP		160		$\mu\text{A}/\text{V}$
$r_{ONLX}$	LX ON-resistance		150	200	250	$\text{m}\Omega$
$I_{LEAKLX}$	LX Leakage Current	$V_{FB} = 1.35V$ , $V_{LX} = 13V$		0.02	40	$\mu\text{A}$
$I_{LIMLX}$	LX Current Limit	Duty cycle = 65% (Note 1)	2.4	2.8	3.3	A
$t_{ssB}$	Soft-Start Period	$C_{DEL} = 100\text{nF}$		7		ms

**Thermal Information**

Storage Temperature	-65°C to +150°C
Maximum Continuous Junction Temperature	+125°C
Power Dissipation	See Curves
Operating Ambient Temperature	-40°C to +85°C
Pb-free reflow profile	see link below <a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a>

**Electrical Specifications**  $V_{IN} = 3V$ ,  $V_{BOOST} = V_{SUP} = 12V$ ,  $V_{SRC} = 20V$ , Over-temperature from  $-40^{\circ}C$  to  $+85^{\circ}C$ .  
Unless Otherwise Specified. (Continued)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
<b>OPERATIONAL AMPLIFIERS</b>						
$V_{SUP}$	Supply Operating Range		4.5		18	V
$I_{SUP}$	Supply Current per Amplifier			600	800	$\mu A$
$V_{OS}$	Offset Voltage			3	12	mV
$I_B$	Input Bias Current		-50		+50	nA
CMIR	Common Mode Input Range		0		$V_{SUP}$	V
CMRR	Common Mode Rejection Ratio		60	90		dB
$A_{OL}$	Open Loop Gain			110		dB
$V_{OH}$	Output Voltage High	$I_{OUT} = 100\mu A$	$V_{SUP}-15$	$V_{SUP}-2$		mV
		$I_{OUT} = 5mA$	$V_{SUP}-250$	$V_{SUP}-150$		mV
$V_{OL}$	Output Voltage Low	$I_{OUT} = -100\mu A$		2	30	mV
		$I_{OUT} = -5mA$		100	150	mV
$I_{SC}$	Short-Circuit Current		100	150		mA
$I_{CONT}$	Continuous Output Current		$\pm 50$			mA
PSRR	Power Supply Rejection Ratio		60	100		dB
$BW_{-3dB}$	-3dB Bandwidth			12		MHz
GBWP	Gain Bandwidth Product			8		MHz
SR	Slew Rate			12		V/ $\mu s$
<b>POSITIVE LDO</b>						
$V_{FBP}$	Positive Feedback Voltage	$I_{DRV_P} = 100\mu A$ , $T_A = +25^{\circ}C$	1.176	1.2	1.224	V
		$I_{DRV_P} = 100\mu A$	1.176	1.2	1.229	V
$V_{FTP}$	$V_{FBP}$ Fault Trip Level	$V_{FBP}$ falling	0.82	0.9	0.98	V
$I_{BP}$	Positive LDO Input Bias Current	$V_{FBP} = 1.4V$	-50		50	nA
$\Delta V_{POS}/\Delta I_{POS}$	FBP Load Regulation	$V_{DRV_P} = 25V$ , $I_{DRV_P} = 0\mu A$ to $20\mu A$		0.5		%
$I_{DRV_P}$	Sink Current	$V_{FBP} = 1.1V$ , $V_{DRV_P} = 10V$	2	4		mA
$I_{LEAKP}$	DRV_P Off Leakage Current	$V_{FBP} = 1.4V$ , $V_{DRV_P} = 30V$		0.1	10	$\mu A$
$t_{SSP}$	Soft-Start Period	$C_{DEL} = 100nF$		7		ms
<b>NEGATIVE LDO</b>						
$V_{FBN}$	FBN Regulation Voltage	$I_{DRV_N} = 0.2mA$ , $T_A = +25^{\circ}C$	0.173	0.203	0.233	V
		$I_{DRV_N} = 0.2mA$	0.171	0.203	0.235	V
$V_{FTN}$	$V_{FBN}$ Fault Trip Level	$V_{FBN}$ rising	380	430	480	mV
$I_{BN}$	Negative LDO Input Bias Current	$V_{FBN} = 250mV$	-50		50	nA
	FBN Load Regulation	$V_{DRV_N} = -6V$ , $I_{DRV_N} = 2\mu A$ to $20\mu A$		0.5		%
$I_{DRV_N}$	Source Current	$V_{FBN} = 500mV$ , $V_{DRV_N} = -6V$	2	4		mA
$I_{LEAKN}$	DRV_N Off Leakage Current	$V_{FBP} = 1.35V$ , $V_{DRV_P} = 30V$		0.1	10	$\mu A$
$t_{SSN}$	Soft-start Period	$C_{DEL} = 100nF$		7		ms
<b><math>V_{ON}</math>-SLICE CIRCUIT</b>						
$V_{LO}$	CTL Input Low Voltage	$V_{IN} = 2.6V$ to $5.5V$			$0.4V_{IN}$	V
$V_{HI}$	CTL Input High Voltage	$V_{IN} = 2.6V$ to $5.5V$	$0.6V_{IN}$			V

**Electrical Specifications**  $V_{IN} = 3V$ ,  $V_{BOOST} = V_{SUP} = 12V$ ,  $V_{SRC} = 20V$ , Over-temperature from  $-40^{\circ}C$  to  $+85^{\circ}C$ .  
Unless Otherwise Specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
$I_{LEAKCTL}$	CTL Input Leakage Current	CTL = AGND or IN	-1		1	$\mu A$
$t_{Drise}$	CTL to OUT Rising Prop Delay	$1k\Omega$ from DRN to 8V, $V_{CTL} = 0V$ to 3V step, no load on OUT, measured from $V_{CTL} = 1.5V$ to OUT = 20%		100		ns
$t_{Dfall}$	CTL to OUT Falling Prop Delay	$1k\Omega$ from DRN to 8V, $V_{CTL} = 3V$ to 0V step, no load on OUT, measured from $V_{CTL} = 1.5V$ to OUT = 80%		100		ns
$V_{SRC}$	SRC Input Voltage Range				30	V
ISRC	SRC Input Current	Start-up sequence not completed		150	250	$\mu A$
		Start-up sequence completed		150	250	$\mu A$
$r_{ONSRC}$	SRC ON-resistance	Start-up sequence completed		5	10	$\Omega$
$r_{ONDNR}$	DRN ON-resistance	Start-up sequence completed		30	60	$\Omega$
<b>SEQUENCING</b>						
$t_{ON}$	Turn On Delay	$C_{DEL} = 100nF$ (See Figure 22)		10		ms
$t_{DEL1}$	Delay Between $V_{BOOST}$ and $V_{OFF}$	$C_{DEL} = 100nF$ (See Figure 22)		10		ms
$t_{DEL2}$	Delay Between $V_{ON}$ and $V_{OFF}$	$C_{DEL} = 100nF$ (See Figure 22)		10		ms
$t_{DEL3}$	Delay From $V_{ON}$ to $V_{ON}$ -slice Enabled	$C_{DEL} = 100nF$ (See Figure 22)		10		ms
$C_{DEL}$	Delay Capacitor		22	100		nF

NOTE:

1. Limits should be considered typical and are not production tested.

**Pin Descriptions**

PIN NAME	ISL97642	PIN FUNCTION
SRC	1	Upper reference voltage for switch output
REF	2	Internal reference bypass terminal
AGND	3	Analog ground for boost converter and control circuitry
PGND	4	Power ground for boost switch
OUT1	5	Operational amplifier 1 output
NEG1	6	Operational amplifier 1 inverting input
POS1	7	Operational amplifier 1 non-inverting input
OUT2	8	Operational amplifier 2 output
NEG2	9	Operational amplifier 2 inverting input
POS2	10	Operational amplifier 2 non-inverting input
BGND	11	Operational amplifier ground
POS3	15	Operational amplifier 3 non-inverting input
NEG3	16	Operational amplifier 3 inverting input
OUT3	17	Operational amplifier 3 output
SUP	14	Amplifier positive supply rail. Bypass to BGND with 0.1 $\mu$ F capacitor
POS3	15	Operational amplifier 3 non-inverting input
NEG3	16	Operational amplifier 3 inverting input
OUT3	17	Operational amplifier 3 output
NC	18	
NC	19	
NC	20	
LX	21	Main boost regulator switch connection
IN	22	Main supply input; bypass to AGND with 1 $\mu$ F capacitor
FB	23	Main boost feedback voltage connection
COMP	24	Error amplifier compensation pin
FBP	25	Positive LDO feedback connection
DRV	26	Positive LDO transistor drive
FBN	27	Negative LDO feedback connection
DRV	28	Negative LDO transistor driver
DEL	29	Connection for switch delay timing capacitor
CTL	30	Input control for switch output
DRN	31	Lower reference voltage for switch output
COM	32	Switch output; when CTL = 1, COM is connected to SRC through a 15 $\Omega$ resistor; when CTL = 0, COM is connected to DRN through a 30 $\Omega$ resistor

## Typical Performance Curves

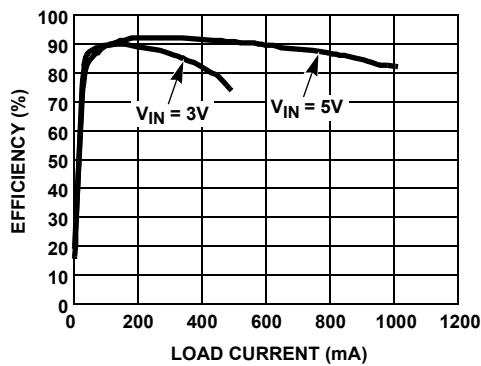
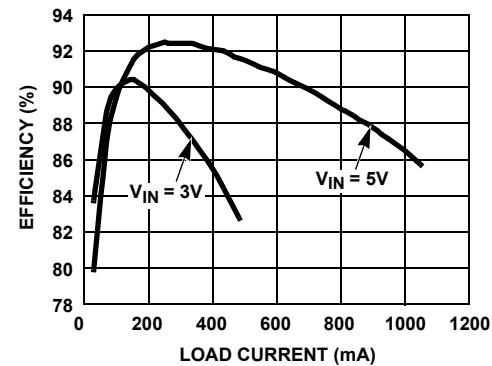
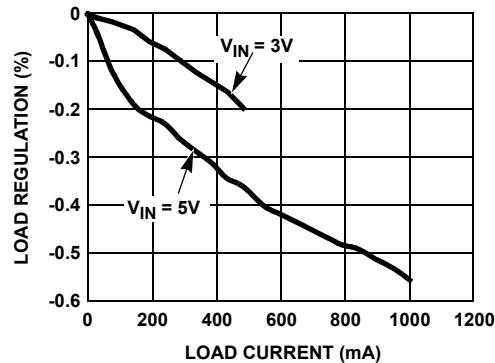
FIGURE 1. BOOST EFFICIENCY AT  $V_{OUT} = 12V$  (PI MODE)FIGURE 2. BOOST EFFICIENCY AT  $V_{OUT} = 12V$  (P MODE)

FIGURE 3. BOOST LOAD REGULATION vs LOAD CURRENT (PI MODE)

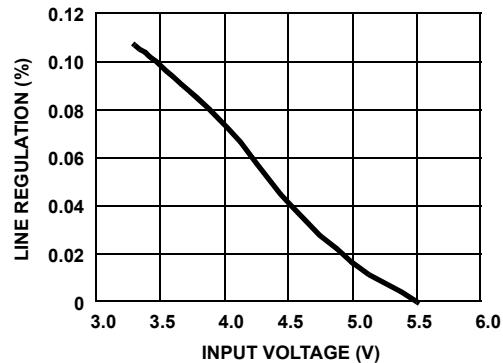


FIGURE 4. BOOST LINE REGULATION vs INPUT VOLTAGE (PI MODE)

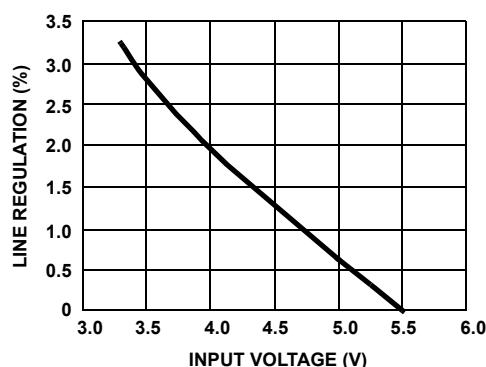


FIGURE 5. BOOST LINE REGULATION vs INPUT VOLTAGE (P MODE)

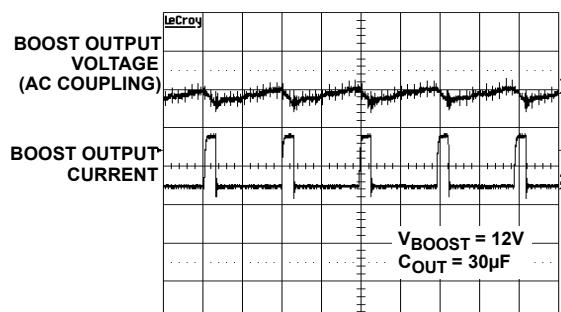


FIGURE 6. BOOST PULSE LOAD TRANSIENT RESPONSE

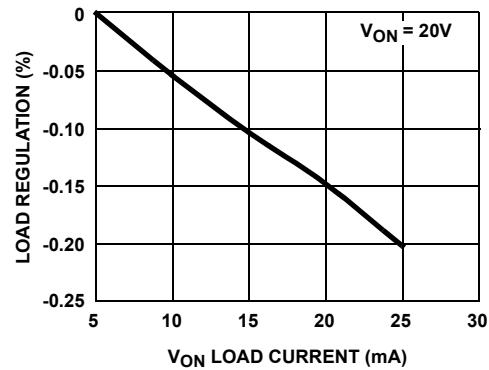
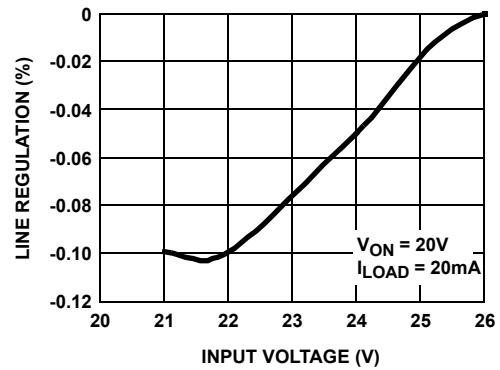
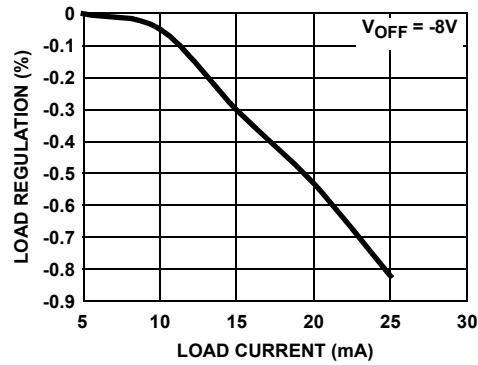
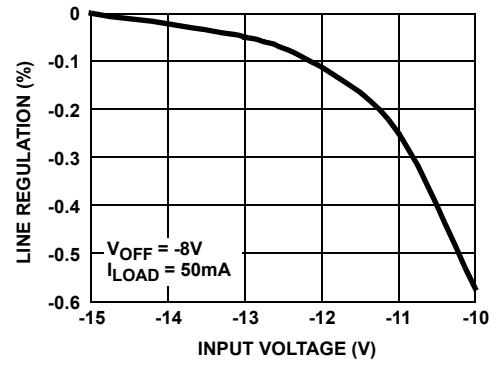
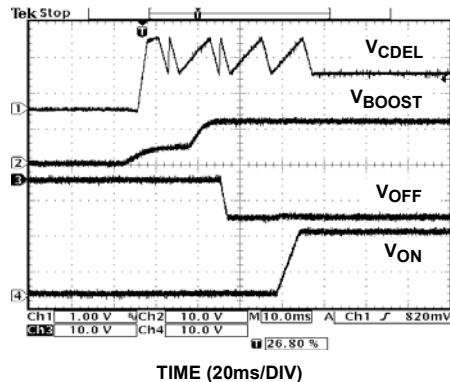
**Typical Performance Curves (Continued)**FIGURE 7.  $V_{ON}$  LOAD REGULATIONFIGURE 8.  $V_{ON}$  LINE REGULATIONFIGURE 9.  $V_{OFF}$  LOAD REGULATIONFIGURE 10.  $V_{OFF}$  LINE REGULATION

FIGURE 11. START-UP SEQUENCE

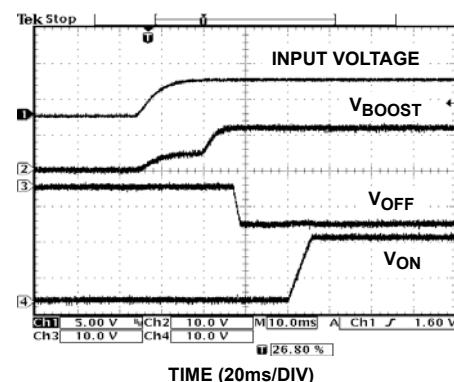


FIGURE 12. START-UP SEQUENCE

## Typical Performance Curves (Continued)

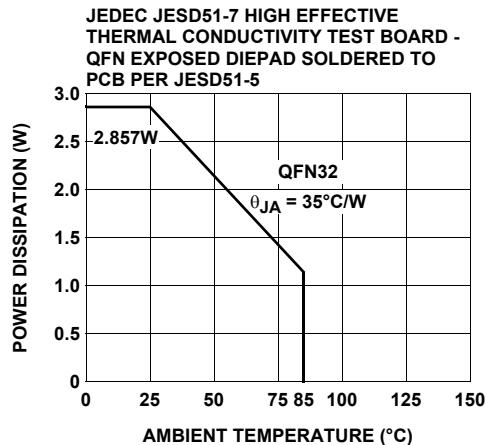


FIGURE 13. OP AMP RAIL-TO-RAIL INPUT/OUTPUT

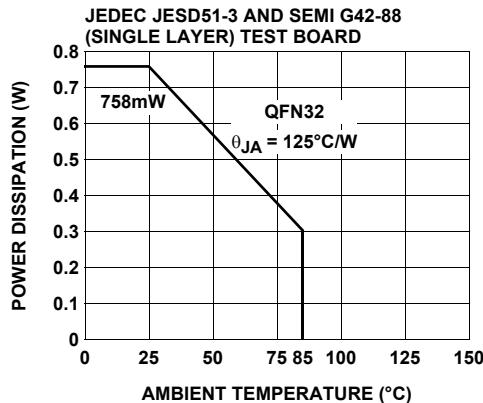


FIGURE 14. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

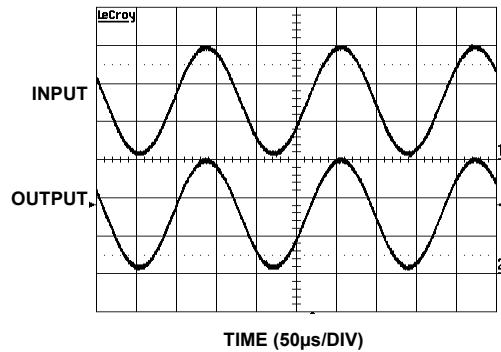


FIGURE 15. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

## Applications Information

The ISL97642 provides a highly integrated multiple output power solution for TFT-LCD applications. The system consists of one high efficiency boost converter and two low cost linear-regulator controllers ( $V_{ON}$  and  $V_{OFF}$ ) with multiple protection functions. The block diagram of the whole part is shown in Figure 16. Table 1 lists the recommended components.

The ISL97642 integrates an N-Channel MOSFET in boost converter to minimize the external component counts and cost. The  $V_{ON}$ ,  $V_{OFF}$  linear-regulators are independently regulated by using external resistors. To achieve higher voltage than  $V_{BOOST}$ , one or multiple stage charge pumps may be used.

TABLE 1. RECOMMENDED COMPONENTS

DESIGNATION	DESCRIPTION
$C_1$ , $C_2$ , $C_3$	10μF, 16V X5R ceramic capacitor (1210) TDK C3216X5R0J106K
$D_1$	1A 20V low leakage Schottky rectifier (CASE 457-04) ON SEMI MBRM120ET3
$D_{11}$ , $D_{12}$ , $D_{21}$	200mA, 30V Schottky barrier diode (SOT-23) Fairchild BAT54S
$L_1$	6.8μH, 1.3A Inductor TDK SLF6025T-6R8M1R3-PF
$Q_{11}$	200mA, 40V PNP amplifier (SOT-23) Fairchild MMBT3906
$Q_{21}$	200mA, 40V NPN amplifier (SOT-23) Fairchild MMBT3904

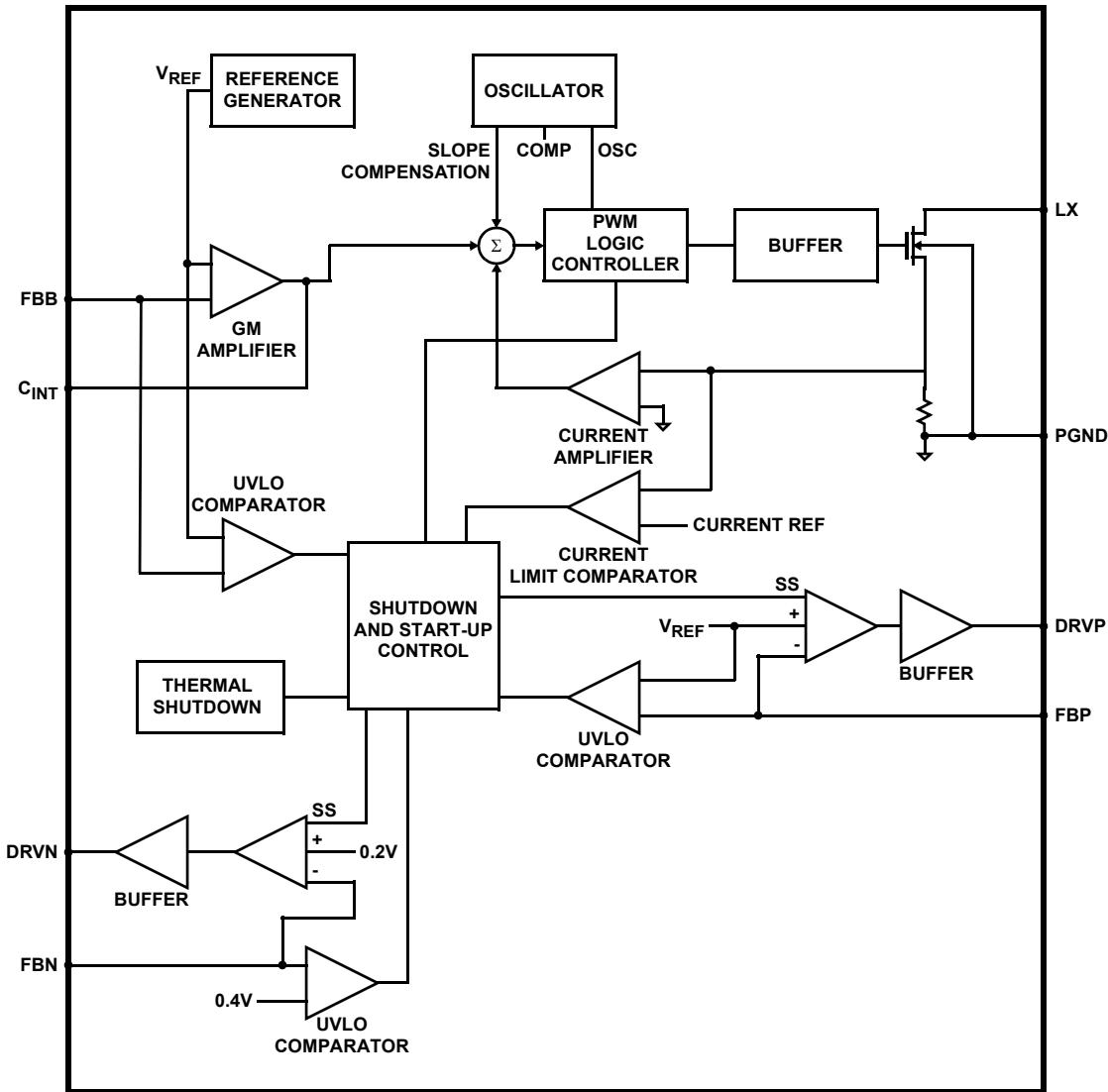


FIGURE 16. BLOCK DIAGRAM

### Boost Converter

The main boost converter is a current mode PWM converter operating at a fixed frequency. The 1.2MHz switching frequency enables the use of low profile inductor and multilayer ceramic capacitors, which results in a compact, low cost power system for LCD panel design.

The boost converter can operate in continuous or discontinuous inductor current mode. The ISL97642 is designed for continuous current mode, but it can also operate in discontinuous current mode at light load. In continuous current mode, current flows continuously in the inductor during the entire switching cycle in steady state operation. The voltage conversion ratio in continuous current mode is given by Equation 1:

$$\frac{V_{\text{BOOST}}}{V_{\text{IN}}} = \frac{1}{1-D} \quad (\text{EQ. 1})$$

Where D is the duty cycle of switching MOSFET.

Figure 17 shows the block diagram of the boost controller. It uses a summing amplifier architecture consisting of GM stages for voltage feedback, current feedback and slope compensation. A comparator looks at the peak inductor current cycle by cycle and terminates the PWM cycle if the current limit is reached.

An external resistor divider is required to divide the output voltage down to the nominal reference voltage. Current drawn by the resistor network should be limited to maintain the overall converter efficiency. The maximum value of the resistor network is limited by the feedback input bias current and the potential for noise being coupled into the feedback pin. A resistor network in the order of 60kΩ is recommended. The boost converter output voltage is determined using Equation 2:

$$V_{\text{BOOST}} = \frac{R_1 + R_2}{R_1} \times V_{\text{REF}} \quad (\text{EQ. 2})$$

The current through MOSFET is limited to 2.8A (typ) peak. This restricts the maximum output current based on Equation 3:

$$I_{OMAX} = \left( I_{LMT} - \frac{\Delta I_L}{2} \right) \times \frac{V_{IN}}{V_O} \quad (EQ. 3)$$

Where  $\Delta I_L$  is peak to peak inductor ripple current, and is set by Equation 4:

$$\Delta I_L = \frac{V_{IN}}{L} \times \frac{D}{f_S} \quad (EQ. 4)$$

where  $f_S$  is the switching frequency.

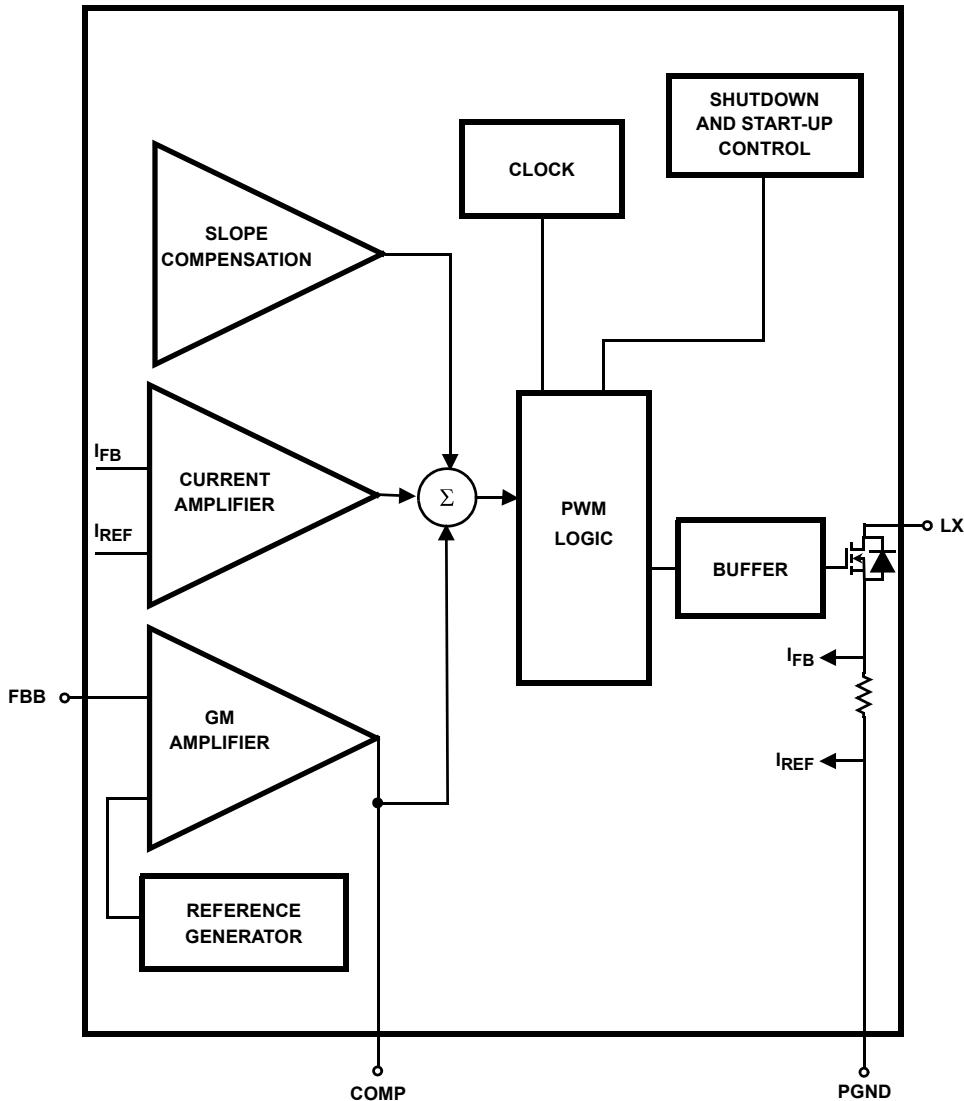


FIGURE 17. THE BLOCK DIAGRAM OF THE BOOST CONTROLLER

Table 2 gives typical values (margins are considered 10%, 3%, 20%, 10% and 15% on  $V_{IN}$ ,  $V_O$ ,  $L$ ,  $f_S$  and  $I_{LMT}$ ):

TABLE 2.

$V_{IN}$ (V)	$V_O$ (V)	$L$ ( $\mu$ H)	$f_S$ (MHz)	$I_{OMAX}$ (mA)
3.3	9	6.8	1.2	890
3.3	12	6.8	1.2	666
3.3	15	6.8	1.2	530
5	9	6.8	1.2	1350
5	12	6.8	1.2	1000
5	15	6.8	1.2	795

### **Input Capacitor**

The input capacitor is used to supply the current to the converter. It is recommended that  $C_{IN}$  be larger than  $10\mu$ F. The reflected ripple voltage will be smaller with larger  $C_{IN}$ . The voltage rating of input capacitor should be larger than the maximum input voltage.

### **Boost Inductor**

The boost inductor is a critical part which influences the output voltage ripple, transient response, and efficiency. Value of  $3.3\mu$ H to  $10\mu$ H inductor is recommended in applications to fit the internal slope compensation. The inductor must be able to handle the following average and peak current:

$$I_{LPK} = I_{LAVG} + \frac{\Delta I_L}{2}$$

$$I_{LAVG} = \frac{I_O}{1-D} \quad (\text{EQ. 5})$$

### **Rectifier Diode**

A high-speed diode is desired due to the high switching frequency. Schottky diodes are recommended because of their fast recovery time and low forward voltage. The rectifier diode must meet the output current and peak inductor current requirements.

### **Output Capacitor**

The output capacitor supplies the load directly and reduces the ripple voltage at the output. Output ripple voltage consists of two components: the voltage drop due to the inductor ripple current flowing through the ESR of output capacitor, and the charging and discharging of the output capacitor.

$$V_{RIPPLE} = I_{LPK} \times ESR + \frac{V_O - V_{IN}}{V_O} \times \frac{I_O}{C_{OUT}} \times \frac{1}{f_S} \quad (\text{EQ. 6})$$

For low ESR ceramic capacitors, the output ripple is dominated by the charging and discharging of the output capacitor. The voltage rating of the output capacitor should be greater than the maximum output voltage.

NOTE: Capacitors have a voltage coefficient that makes their effective capacitance drop as the voltage across them increases.  $C_{OUT}$  in the

Equation 6 assumes the effective value of the capacitor at a particular voltage and not the manufacturer's stated value, measured at zero volts.

### **Compensation**

The ISL97642 incorporates a transconductance amplifier in its feedback path to allow the user some adjustment on the transient response and better regulation. The ISL97642 uses current mode control architecture, which has a fast current sense loop and a slow voltage feedback loop. The fast current feedback loop does not require any compensation. The slow voltage loop must be compensated for stable operation. The compensation network is a series RC network from COMP pin to ground. The resistor sets the high frequency integrator gain for fast transient response and the capacitor sets the integrator zero to ensure loop stability. For most applications, a  $2.2n$ F capacitor and a  $180\Omega$  resistor are inserted in series between COMP pin and ground. To improve the transient response, either the resistor value can be increased or the capacitor value can be reduced, but too high resistor value or too low capacitor value will reduce loop stability.

### **Boost Feedback Resistors**

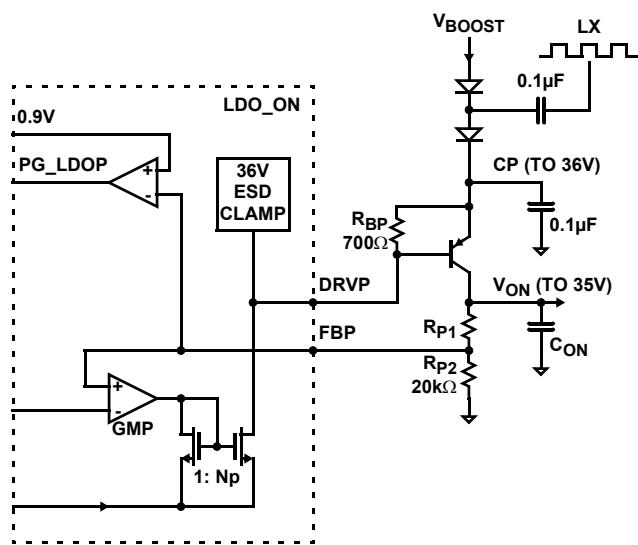
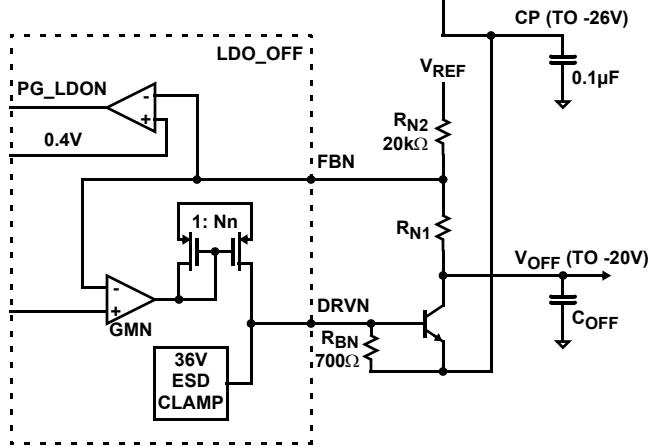
As the boost output voltage,  $V_{BOOST}$ , is reduced below 12V, the effective voltage feedback in the IC increases the ratio of voltage to current feedback at the summing comparator because  $R_2$  decreases relative to  $R_1$ . To maintain stable operation over the complete current range of the IC, the voltage feedback to the FBB pin should be reduced proportionally (as  $V_{BOOST}$  is reduced) by means of a series resistor-capacitor network ( $R_7$  and  $C_7$ ) in parallel with  $R_1$ , with a pole frequency ( $f_p$ ) set to approximately 10kHz for  $C_2$  (effective) =  $10\mu$ F and 4kHz for  $C_2$  (effective) =  $30\mu$ F.

$$R_7 = 1/0.1 \times R_2 - (1/R_1)^{-1} \quad (\text{EQ. 7})$$

$$C_7 = 1/2 \times 3.142 \times f_p \times R_7 \quad (\text{EQ. 8})$$

### **Linear-Regulator Controllers ( $V_{ON}$ and $V_{OFF}$ )**

The ISL97642 includes 2 independent linear-regulator controllers, in which there is one positive output voltage ( $V_{ON}$ ) and one negative voltage ( $V_{OFF}$ ). The  $V_{ON}$  and  $V_{OFF}$  linear-regulator controller function diagram, application circuit and waveforms are shown in Figures 18 and 19 respectively.

FIGURE 18. V<sub>ON</sub> FUNCTIONAL BLOCK DIAGRAMFIGURE 19. V<sub>OFF</sub> FUNCTIONAL BLOCK DIAGRAM

The V<sub>ON</sub> power supply is used to power the positive supply of the row driver in the LCD panel. The DC/DC consists of an external diode-capacitor charge pump powered from the inductor (LX) of the boost converter, followed by a low dropout linear regulator (LDO\_ON). The LDO\_ON regulator uses an external PNP transistor as the pass element. The onboard LDO controller is a wide band (>10MHz) transconductance amplifier capable of 5mA output current, which is sufficient for up to 50mA or more output current under the low dropout condition (forced beta of 10). Typical V<sub>ON</sub> voltage supported by ISL97642 ranges from +15V to +36V. A fault comparator is also included for monitoring the output voltage. The undervoltage threshold is set at 25% below the 1.2V reference.

The V<sub>OFF</sub> power supply is used to power the negative supply of the row driver in the LCD panel. The DC/DC consists of an external diode-capacitor charge pump powered from the inductor (LX) of the boost converter, followed by a low dropout linear regulator (LDO\_OFF). The LDO\_OFF regulator uses an external NPN transistor as the pass element. The onboard LDO controller is a wide band (>10MHz) transconductance amplifier capable of 5mA output current, which is sufficient for up to 50mA or more output current under the low dropout condition (forced beta of 10). Typical V<sub>OFF</sub> voltage supported by ISL97642 ranges from -5V to -25V. A fault comparator is also included for monitoring the output voltage. The undervoltage threshold is set at 200mV above the 0.2V reference level.

### Set-up Output Voltage

Refer to the “Typical Application Circuit” on page 18. The output voltages of V<sub>ON</sub>, V<sub>OFF</sub> and V<sub>LOGIC</sub> are determined by Equations 9 and 10:

$$V_{ON} = V_{REF} \times \left( 1 + \frac{R_{12}}{R_{11}} \right) \quad (\text{EQ. 9})$$

$$V_{OFF} = V_{REFN} + \frac{R_{22}}{R_{21}} \times (V_{REFN} - V_{REF}) \quad (\text{EQ. 10})$$

Where V<sub>REF</sub> = 1.2V, V<sub>REFN</sub> = 0.2V.

### High Charge Pump Output Voltage (>36V) Applications

In the applications where the charge pump output voltage is over 36V, an external NPN transistor needs to be inserted in between the DRVP pin and the base of pass transistor Q3, as shown in Figure 20, or the linear regulator can control only one stage charge pump and regulate the final charge pump output, as shown in Figure 21.

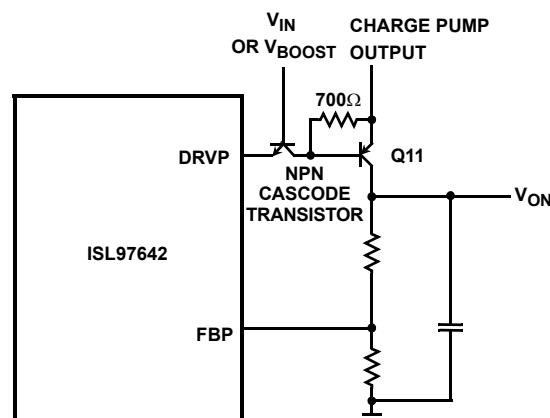


FIGURE 20. CASCODE NPN TRANSISTOR CONFIGURATION FOR HIGH CHARGE PUMP OUTPUT VOLTAGE (>36V)

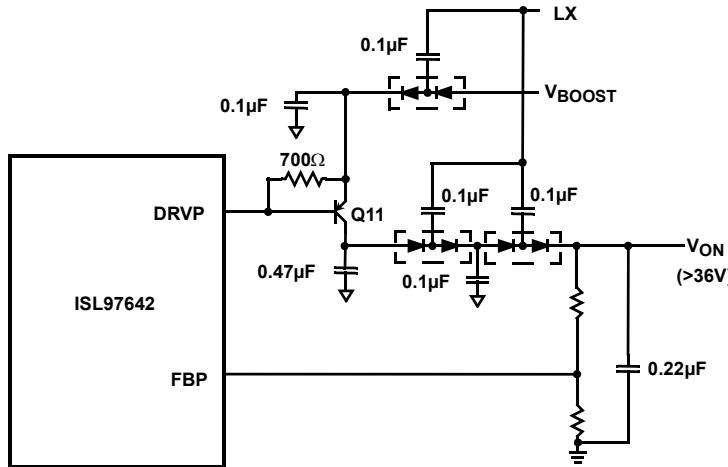


FIGURE 21. THE LINEAR REGULATOR CONTROLS ONE STAGE OF CHARGE PUMP

### Calculation of the Linear Regulator Base-emitter Resistors (RBP and RBN)

For the pass transistor of the linear regulator, low frequency gain ( $H_{fe}$ ) and unity gain frequency ( $f_T$ ) are usually specified in the datasheet. The pass transistor adds a pole to the loop transfer function at  $f_p = f_T/H_{fe}$ . Therefore, in order to maintain phase margin at low frequency, the best choice for a pass device is often a high frequency, low gain switching transistor. Further improvement can be obtained by adding a base-emitter resistor  $R_{BE}$  ( $R_{BP}$ ,  $R_{BL}$ ,  $R_{BN}$  in the Functional Block Diagram), which increases the pole frequency to:  $f_p = f_T * (1 + H_{fe} * r_e/R_{BE})/H_{fe}$ , where  $r_e = K_T/qI_c$ . So choose the lowest value  $R_{BE}$  in the design as long as there is still enough base current ( $I_B$ ) to support the maximum output current ( $I_c$ ).

We will take as an example the  $V_{ON}$  linear regulator. If a Fairchild MMBT3906 PNP transistor is used as the external pass transistor (Q11 in the application diagram), then for a maximum  $V_{ON}$  operating requirement of 50mA, the data sheet indicates  $H_{fe\_min} = 60$ . The base-emitter saturation voltage is:  $V_{be\_max} = 0.7V$ .

For the ISL97642, the minimum drive current is:

$$I_{DRVP\_min} = 2mA$$

The minimum base-emitter resistor,  $R_{BP}$ , can now be calculated as:

$$R_{BP\_min} = V_{BE\_max} / (I_{DRVP\_min} - I_c/H_{fe\_min}) = ((0.7V) / (2mA - (50mA) / 60)) = 600\Omega$$

(EQ. 11)

This is the minimum value that can be used – so, we now choose a convenient value greater than this minimum value; for example, 700Ω. Larger values may be used to reduce quiescent current, however, regulation may be adversely affected by supply noise if  $R_{BP}$  is made too high in value.

### Charge Pump

To generate an output voltage higher than  $V_{BOOST}$ , single or multiple stages of charge pumps are needed. The number of stage is determined by the input and output voltage. For positive charge pump stages:

$$N_{POSITIVE} \geq \frac{V_{OUT} + V_{CE} - V_{INPUT}}{V_{INPUT} - 2 \times V_F}$$

(EQ. 12)

where  $V_{CE}$  is the dropout voltage of the pass component of the linear regulator. It ranges from 0.3V to 1V depending on the transistor selected.  $V_F$  is the forward-voltage of the charge-pump rectifier diode.

The number of negative charge-pump stages is given by:

$$N_{NEGATIVE} \geq \frac{|V_{OUTPUT}| + V_{CE}}{V_{INPUT} - 2 \times V_F}$$

(EQ. 13)

To achieve high efficiency and low material cost, the lowest number of charge-pump stages, which can meet the above requirements, is always preferred.

### Charge Pump Output Capacitors

Ceramic capacitor with low ESR is recommended. With ceramic capacitors, the output ripple voltage is dominated by the capacitance value. The capacitance value can be chosen by Equation 14:

$$C_{OUT} \geq \frac{I_{OUT}}{2 \times V_{RIPPLE} \times f_{OSC}}$$

(EQ. 14)

where  $f_{OSC}$  is the switching frequency.

### Discontinuous/Continuous Boost Operation and its Effect on the Charge Pumps

The ISL97642  $V_{ON}$  and  $V_{OFF}$  architecture uses LX switching edges to drive diode charge pumps from which LDO regulators generate the  $V_{ON}$  and  $V_{OFF}$  supplies. It can be appreciated that should a regular supply of LX switching edges be

interrupted (for example during discontinuous operation at light boost load currents), then this may affect the performance of  $V_{ON}$  and  $V_{OFF}$  regulation – depending on their exact loading conditions at the time.

To optimize  $V_{ON}/V_{OFF}$  regulation, the boundary of discontinuous/continuous operation of the boost converter can be adjusted by suitable choice of inductor given  $V_{IN}$ ,  $V_{OUT}$ , switching frequency and the  $V_{BOOST}$  current loading, to be in continuous operation.

Equation 15 gives the boundary between discontinuous and continuous boost operation. For continuous operation ( $L$  switching every clock cycle) we require that:

$$I(V_{BOOST\_load}) > D \cdot 1 - D \cdot V_{IN}/2 \cdot L \cdot f_{OSC} \quad (\text{EQ. 15})$$

where the duty cycle,  $D = (V_{BOOST} - V_{IN})/V_{BOOST}$

For example, with  $V_{IN} = 5V$ ,  $f_{OSC} = 1.2\text{MHz}$  and  $V_{BOOST} = 12V$ , we find continuous operation of the boost converter can be guaranteed for:

$L = 10\mu\text{H}$  and  $I(V_{BOOST}) > 51\text{mA}$

$L = 6.8\mu\text{H}$  and  $I(V_{BOOST}) > 74\text{mA}$

$L = 3.3\mu\text{H}$  and  $I(V_{BOOST}) > 153\text{mA}$

## Start-up Sequence

Figure 22 shows a detailed start-up sequence waveform. For a successful power-up, there should be 6 peaks at  $V_{CDEL}$ . When a fault is detected, the device will latch off until either EN is toggled or the input supply is recycled.

When the input voltage is higher than 2.4V, an internal current source starts to charge  $C_{CDEL}$ . During the initial slow ramp, the device checks whether there is a fault condition. If no fault is found during the initial ramp,  $C_{CDEL}$  is discharged after the first peak.  $V_{REF}$  turns on at the peak of the first ramp.

Initially, the boost is not enabled so  $V_{BOOST}$  rises to  $V_{IN} - V_{DIODE}$  through the output diode. Hence, there is a step at  $V_{BOOST}$  during this part of the start-up sequence.

$V_{BOOST}$  soft-starts at the beginning of the third ramp, and is checked at the end of this ramp. The soft-start ramp depends on the value of the  $C_{DEL}$  capacitor. For  $C_{DEL}$  of 100nF, the soft-start time is ~7ms.

$V_{OFF}$  turns on at the start of the fourth peak.

$V_{ON}$  is enabled at the beginning of the sixth ramp.  $V_{OFF}$  and  $V_{ON}$  are checked at end of this ramp.

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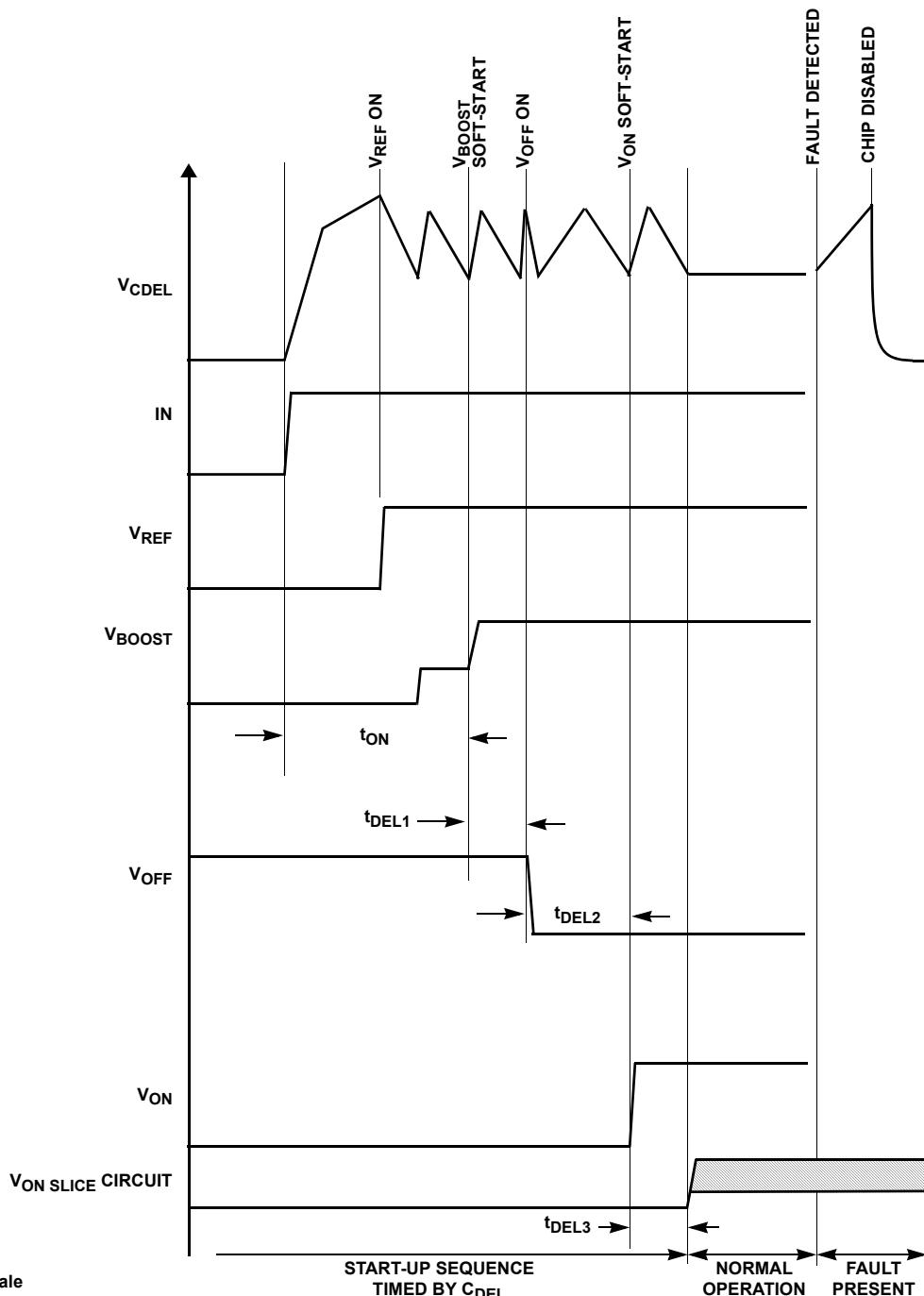


FIGURE 22. START-UP SEQUENCE

### Component Selection for Start-up Sequencing and Fault Protection

The  $C_{REF}$  capacitor is typically set at 220nF and is required to stabilize the  $V_{REF}$  output. The range of  $C_{REF}$  is from 22nF to 1 $\mu$ F and should not be more than five times the capacitor on  $C_{DEL}$  to ensure correct start-up operation.

The  $C_{DEL}$  capacitor is typically 100nF and has a usable range from 22nF minimum to several microfarads – only limited by the leakage in the capacitor reaching  $\mu$ A levels.  $C_{DEL}$  should be at least 1/5 of the value of  $C_{REF}$  (see Figure 22). Note that with

100nF on  $C_{DEL}$ , the fault time-out will be typically 23ms and the use of a larger/smaller value will vary this time proportionally (e.g. 1 $\mu$ F will give a fault time-out period of typically 230ms).

### Fault Sequencing

The ISL97642 has an advanced fault detection system, which protects the IC from both adjacent pin shorts during operation and shorts on the output supplies. A high quality layout/design of the PCB (in respect of grounding quality and decoupling) is necessary to avoid falsely triggering the fault detection scheme – especially during start-up. The user is directed to the layout

guidelines and component selection sections to avoid problems during initial evaluation and prototype PCB generation.

### ***V<sub>ON</sub>-Slice Circuit***

The V<sub>ON</sub>-slice Circuit functions as a three way multiplexer, switching the voltage on COM between ground, DRN and SRC, under control of the start-up sequence and the CTL pin.

Once the start-up sequence has completed, CTL is enabled and acts as a multiplexer control such that if CTL is low, COM connects to DRN through a 5Ω internal MOSFET, and if CTL is high, COM connects to SRC via a 30Ω MOSFET.

The slew rate of start-up of the switch control circuit is mainly restricted by the load capacitance at COM pin, as in Equation 16:

$$\frac{\Delta V}{\Delta t} = \frac{V_g}{(R_i \parallel R_L) \cdot C_L} \quad (\text{EQ. 16})$$

Where V<sub>g</sub> is the supply voltage applied to the switch control circuit, R<sub>i</sub> is the resistance between COM and DRN or SRC including the internal MOSFET r<sub>DS(ON)</sub>, the trace resistance and the resistor inserted; R<sub>L</sub> is the load resistance of the switch control circuit, and C<sub>L</sub> is the load capacitance of the switch control circuit.

In the "Typical Application Circuit" on page 18, R<sub>8</sub>, R<sub>9</sub> and C<sub>8</sub> give the bias to DRN based on Equation 17:

$$V_{DRN} = \frac{V_{ON} \cdot R_9 + A_{VDD} \cdot R_8}{R_8 + R_9} \quad (\text{EQ. 17})$$

and R<sub>10</sub> can be adjusted to adjust the slew rate.

### ***Op Amps***

The ISL97642 has 3 amplifiers respectively. The op amps are typically used to drive the TFT-LCD backplane (V<sub>COM</sub>) or the gamma-correction divider string. They feature rail-to-rail input and output capability. They are unity gain stable, and have low power consumption (typical 600μA per amplifier). The ISL97642 has a -3dB bandwidth of 12MHz while maintaining a 10V/μs slew rate.

### ***Short Circuit Current Limit***

The ISL97642 will limit the short circuit current to ±180mA if the output is directly shorted to the positive or the negative supply. If an output is shorted for a long time, the junction temperature will trigger the Over-Temperature Protection limit and, hence, the part will shut down.

### ***Driving Capacitive Loads***

ISL97642 can drive a wide range of capacitive loads. As load capacitance increases, however, the -3dB bandwidth of the device will decrease and the peaking will increase. The amplifiers drive 10pF loads in parallel with 10kΩ with just 1.5dB of peaking, and 100pF with 6.4dB of peaking. If less peaking is desired in these applications, a small series resistor (usually between 5Ω and 50Ω) can be placed in series with the output. However, this will obviously reduce the gain. Another

method of reducing peaking is to add a "snubber" circuit at the output. A snubber is a shunt load consisting of a resistor in series with a capacitor. Values of 150Ω and 10nF are typical. The advantage of a snubber is that it does not draw any DC load current and reduce the gain.

### ***Over-Temperature Protection***

An internal temperature sensor continuously monitors the die temperature. In the event that the die temperature exceeds the thermal trip point, the device will be latched off until either the input supply voltage or enable is cycled.

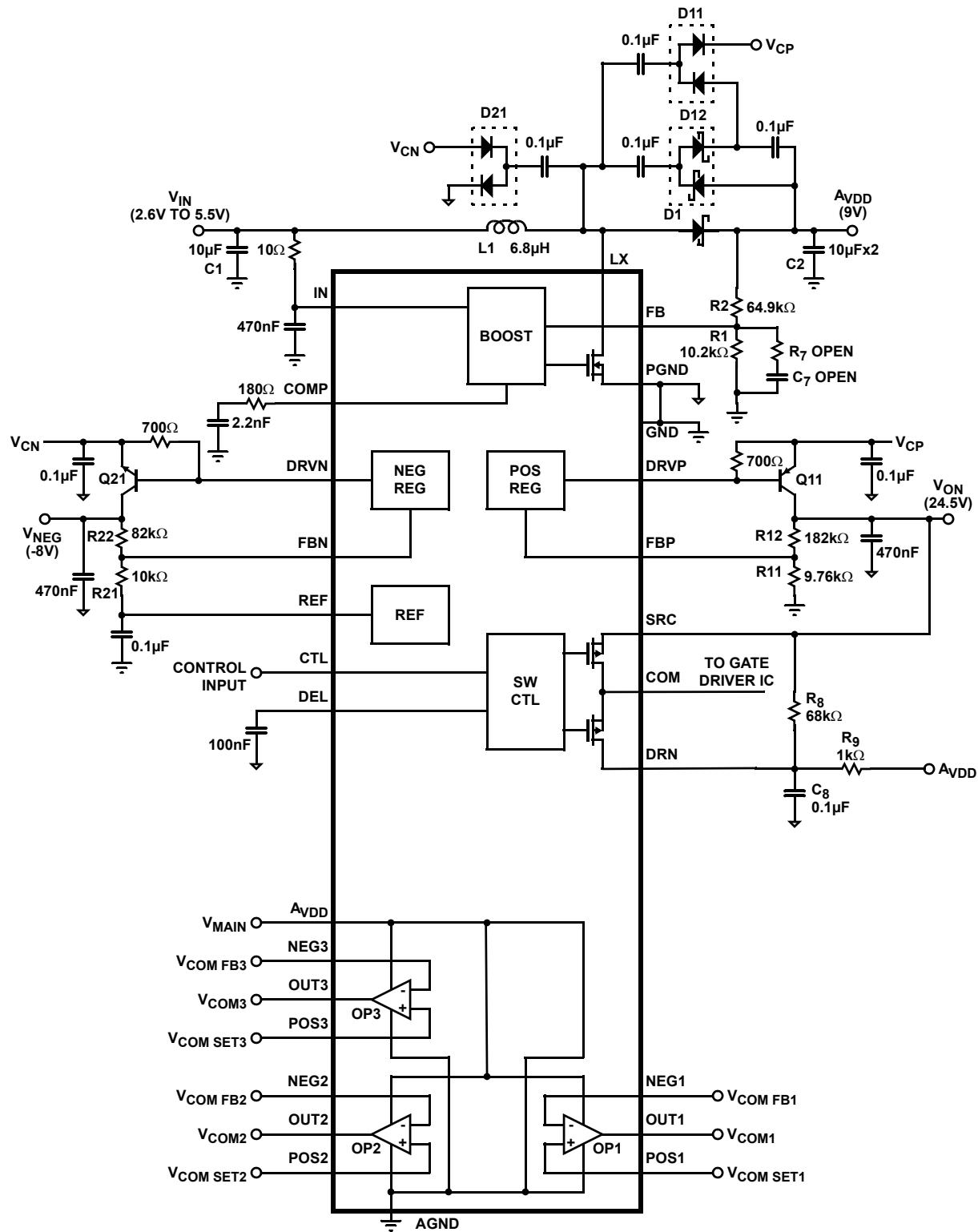
### ***Layout Recommendation***

The devices performance (including efficiency, output noise, transient response and control loop stability) is dramatically affected by the PCB layout. PCB layout is critical, especially at high switching frequency.

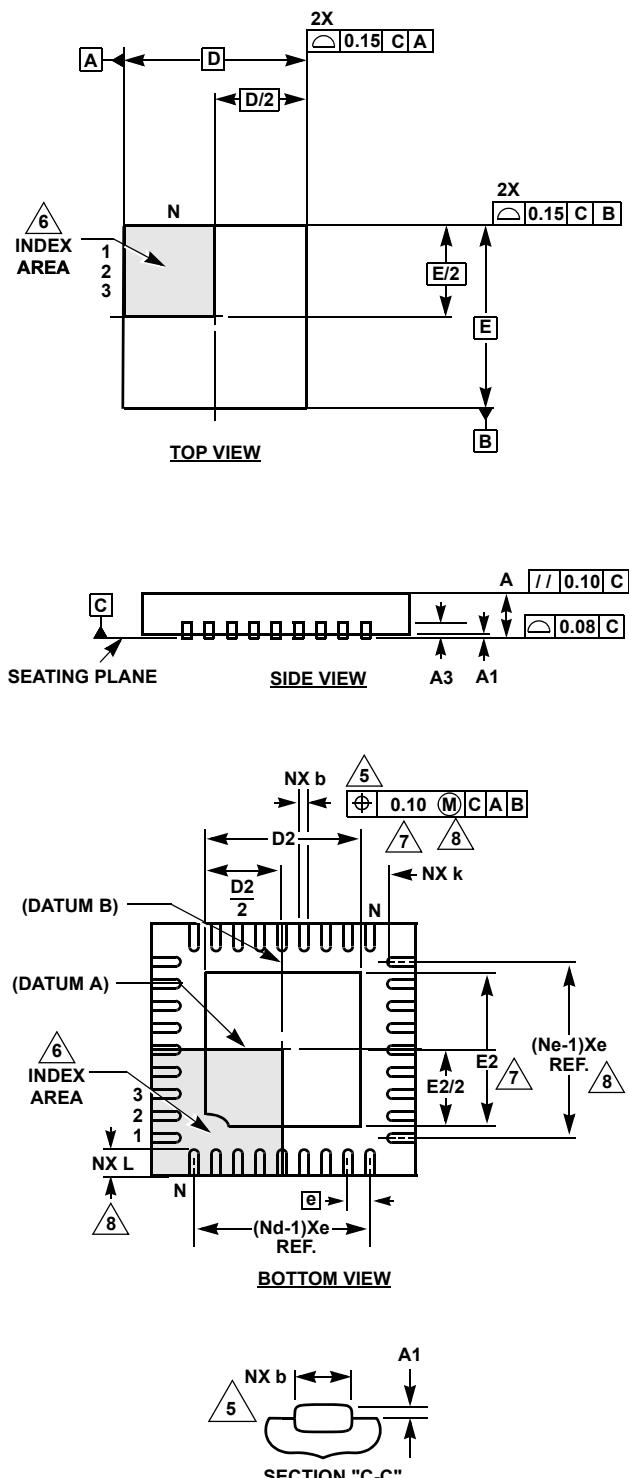
There are some general guidelines for layout:

1. Place the external power components (the input capacitors, output capacitors, boost inductor and output diodes, etc.) in close proximity to the device. Traces to these components should be kept as short and wide as possible to minimize parasitic inductance and resistance.
2. Place VREF and VDD bypass capacitors close to the pins.
3. Reduce the loop with large AC amplitudes and fast slew rate.
4. The feedback network should sense the output voltage directly from the point of load, and be as far away from LX node as possible.
5. The power ground (PGND) and signal ground (SGND) pins should be connected at only one point.
6. The exposed die plate, on the underneath of the package, should be soldered to an equivalent area of metal on the PCB. This contact area should have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers (if available) to maximize thermal dissipation away from the IC.
7. To minimize the thermal resistance of the package when soldered to a multi-layer PCB, the amount of copper track and ground plane area connected to the exposed die plate should be maximized and spread out as far as possible from the IC. The bottom and top PCB areas especially should be maximized to allow thermal dissipation to the surrounding air.
8. A signal ground plane, separate from the power ground plane and connected to the power ground pins only at the exposed die plate, should be used for ground return connections for feedback resistor networks (R<sub>1</sub>, R<sub>11</sub>, R<sub>41</sub>) and the V<sub>REF</sub> capacitor, C<sub>22</sub>, the C<sub>DELAY</sub> capacitor C<sub>7</sub> and the integrator capacitor C<sub>23</sub>.
9. Minimize feedback input track lengths to avoid switching noise pick-up.

A demo board is available to illustrate the proper layout implementation.

**Typical Application Circuit**

**Thin Quad Flat No-Lead Plastic Package (TQFN)**  
**Thin Micro Lead Frame Plastic Package (TMLFP)**

**L32.5x5A**

32 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE  
 (COMPLIANT TO JEDEC MO-220WJJ-1 ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.70	0.75	0.80	-
A1	-	-	0.05	-
A3	0.20 REF			-
b	0.18	0.25	0.30	5, 8
D	5.00 BSC			-
D2	3.30	3.45	3.55	7, 8
E	5.00 BSC			-
E1	5.75 BSC			9
E2	3.30	3.45	3.55	7, 8
e	0.50 BSC			-
k	0.20	-	-	-
L	0.30	0.40	0.50	8
N	32			2
Nd	8			3
Ne	8			3

Rev. 2 05/06

## NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.