

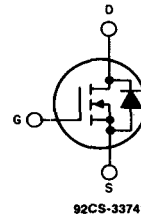
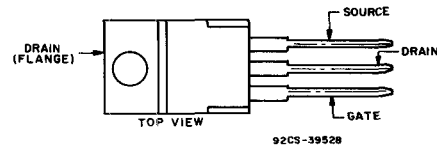
Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

4.0A and 5.0A, 150V-200V

 $r_{DS(on)} = 0.8\ \Omega$ and $1.2\ \Omega$ **Features:**

- SOA is power-dissipation limited
- Nanosecond switching speeds
- Linear transfer characteristics
- High input impedance
- Majority carrier device

N-CHANNEL ENHANCEMENT MODE**TERMINAL DIAGRAM****TERMINAL DESIGNATION****JEDEC TO-220AB**

The IRF620, IRF621, IRF622 and IRF623 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

Absolute Maximum Ratings

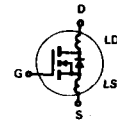
Parameter	IRF620	IRF621	IRF622	IRF623	Units
V_{DS} Drain - Source Voltage ①	200	150	200	150	V
V_{DGR} Drain - Gate Voltage ($R_{GS} = 20\text{ K}\Omega$) ①	200	150	200	150	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	5.0	5.0	4.0	4.0	A
$I_D @ T_C = 100^\circ\text{C}$ Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_{DM} Pulsed Drain Current ③	20	20	16	16	A
V_{GS} Gate - Source Voltage	± 20				V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	40 (See Fig. 14)				W
Linear Derating Factor	0.32 (See Fig. 14)				W/ $^\circ\text{C}$
I_{LM} Inductive Current, Clamped	20	20	16	16	A
T_J Operating Junction and Storage Temperature Range	-55 to 150				$^\circ\text{C}$
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				$^\circ\text{C}$

IRF620, IRF621, IRF622, IRF623

Electrical Characteristics @ $T_C = 25^\circ\text{C}$ (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DS} Drain-Source Breakdown Voltage	IRF620 IRF622	200	—	—	V	$V_{GS} = 0\text{V}$ $I_D = 250\mu\text{A}$
	IRF621 IRF623	150	—	—	V	
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$
I_{GSS} Gate-Source Leakage Forward	ALL	—	—	500	nA	$V_{GS} = 20\text{V}$
I_{GSS} Gate-Source Leakage Reverse	ALL	—	—	-500	nA	$V_{GS} = -20\text{V}$
I_{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0\text{V}$
		—	—	1000	μA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0\text{V}$, $T_C = 125^\circ\text{C}$
$I_{D(on)}$ On-State Drain Current ②	IRF620 IRF621	5.0	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., $V_{GS} = 10\text{V}$
	IRF622 IRF623	4.0	—	—	A	
$R_{DS(on)}$ Static Drain-Source On-State Resistance ②	IRF620 IRF621	—	0.5	0.8	Ω	$V_{GS} = 10\text{V}$, $I_D = 2.5\text{A}$
	IRF622 IRF623	—	0.8	1.2	Ω	
g_{fs} Forward Transconductance ②	ALL	1.3	2.5	—	S (S)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., $I_D = 2.5\text{A}$
C_{iss} Input Capacitance	ALL	—	450	—	pF	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1.0\text{MHz}$
C_{oss} Output Capacitance	ALL	—	150	—	pF	See Fig. 10
C_{rss} Reverse Transfer Capacitance	ALL	—	40	—	pF	
$t_{d(on)}$ Turn-On Delay Time	ALL	—	20	40	ns	$V_{DD} = 2.5 BV_{DSS}$, $I_D = 2.5\text{A}$, $Z_\theta = 50^\circ\text{C/W}$
t_r Rise Time	ALL	—	30	60	ns	See Fig. 17
$t_{d(off)}$ Turn-Off Delay Time	ALL	—	50	100	ns	IMOSFET switching times are essentially independent of operating temperature.)
t_f Fall Time	ALL	—	30	60	ns	
Q_g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	11	15	nC	$V_{GS} = 50\text{V}$, $I_D = 6.0\text{A}$, $V_{DS} = 0.8 \text{ Max. Rating}$. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs} Gate-Source Charge	ALL	—	5.0	7.5	nC	
Q_{gd} Gate-Drain ("Miller") Charge	ALL	—	6.0	9.0	nC	
L_D Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.
		—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC} Junction-to-Case	ALL	—	—	3.12	$^\circ\text{C/W}$	
R_{thCS} Case-to-Sink	ALL	—	1.0	—	$^\circ\text{C/W}$	Mounting surface flat, smooth, and greased.
R_{thJA} Junction-to-Ambient	ALL	—	—	80	$^\circ\text{C/W}$	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S Continuous Source Current (Body Diode)	IRF620 IRF621	—	—	5.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
	IRF622 IRF623	—	—	4.0	A	
I_{SM} Pulse Source Current (Body Diode) ③	IRF620 IRF621	—	—	20	A	
	IRF622 IRF623	—	—	16	A	
V_{SD} Diode Forward Voltage ②	IRF620 IRF621	—	—	1.8	V	$T_C = 25^\circ\text{C}$, $I_S = 5.0\text{A}$, $V_{GS} = 0\text{V}$
	IRF622 IRF623	—	—	1.4	V	$T_C = 25^\circ\text{C}$, $I_S = 4.0\text{A}$, $V_{GS} = 0\text{V}$
t_{rr} Reverse Recovery Time	ALL	—	350	—	ns	$T_J = 150^\circ\text{C}$, $I_F = 5.0\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR} Reverse Recovered Charge	ALL	—	2.3	—	μC	$T_J = 150^\circ\text{C}$, $I_F = 5.0\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on} Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

③ Repetitive Rating: Pulse width limited by max. junction temperature.

See Transient Thermal Impedance Curve (Fig. 5).

IRF620, IRF621, IRF622, IRF623

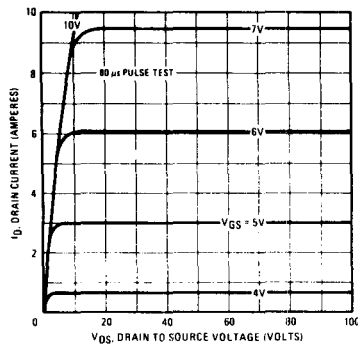


Fig. 1 - Typical Output Characteristics

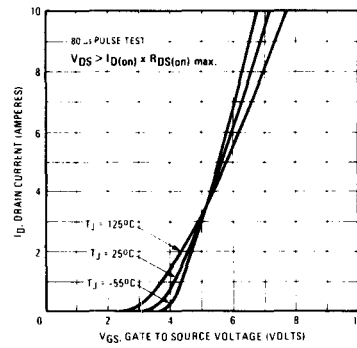


Fig. 2 - Typical Transfer Characteristics

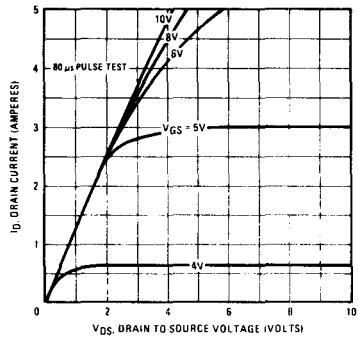


Fig. 3 - Typical Saturation Characteristics

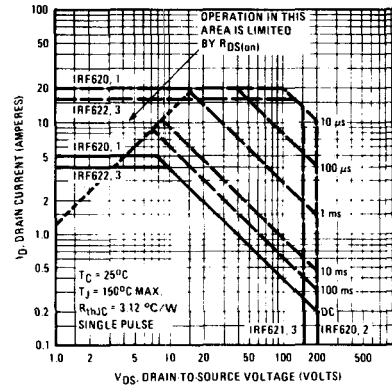


Fig. 4 - Maximum Safe Operating Area

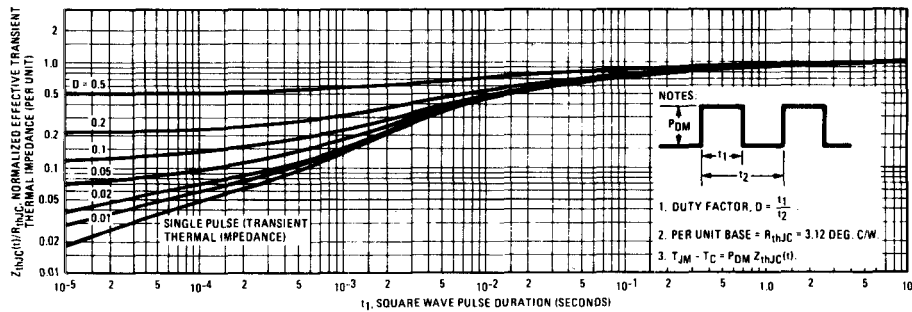


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRF620, IRF621, IRF622, IRF623

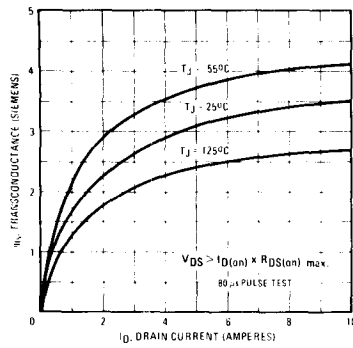


Fig. 6 - Typical Transconductance Vs. Drain Current

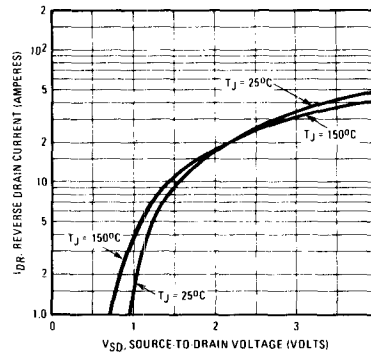


Fig. 7 - Typical Source-Drain Diode Forward Voltage

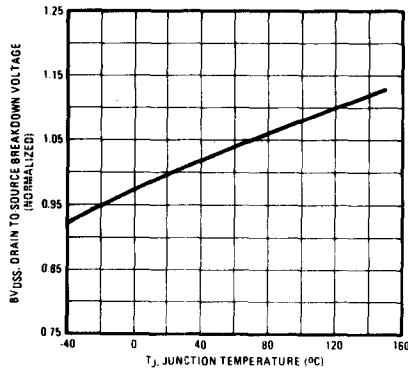


Fig. 8 - Breakdown Voltage Vs. Temperature

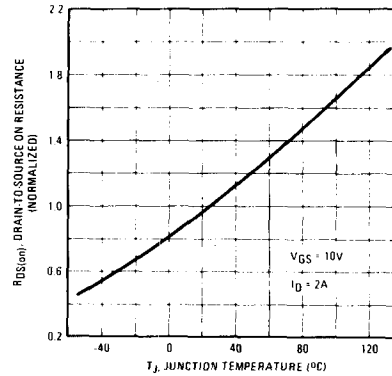


Fig. 9 - Normalized On-Resistance Vs. Temperature

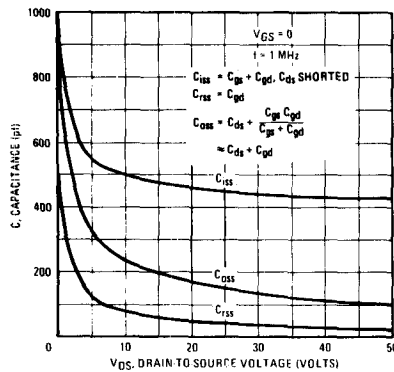


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

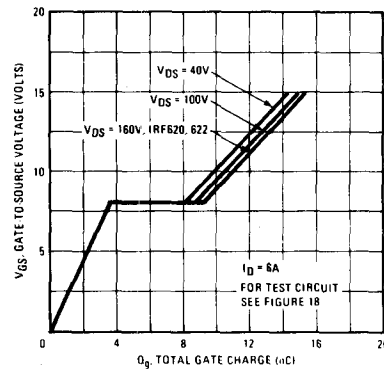


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

IRF620, IRF621, IRF622, IRF623

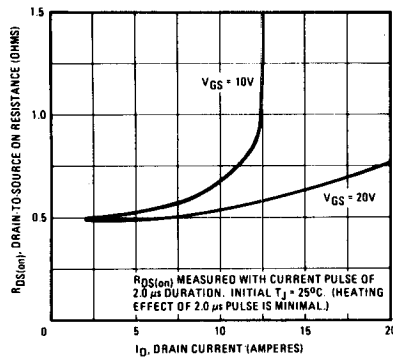


Fig. 12 — Typical On-Resistance Vs. Drain Current

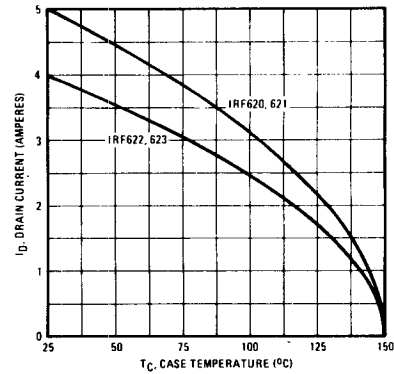


Fig. 13 — Maximum Drain Current Vs. Case Temperature

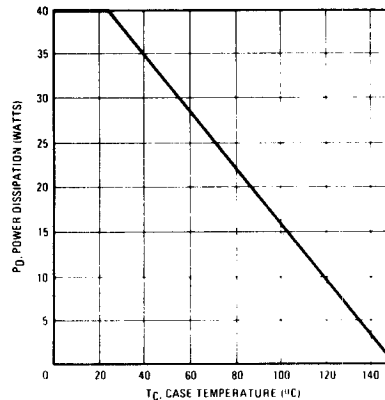


Fig. 14 — Power Vs. Temperature Derating Curve

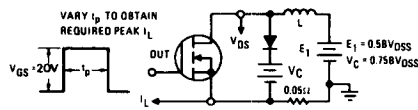


Fig. 15 — Clamped Inductive Test Circuit



Fig. 16 — Clamped Inductive Waveforms

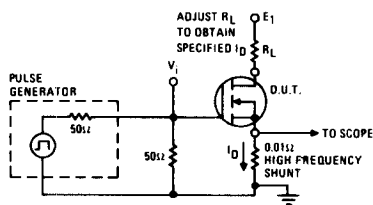


Fig. 17 — Switching Time Test Circuit

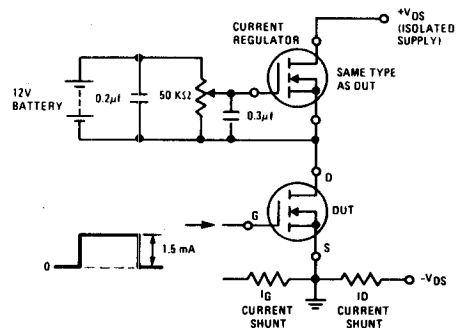


Fig. 18 — Gate Charge Test Circuit