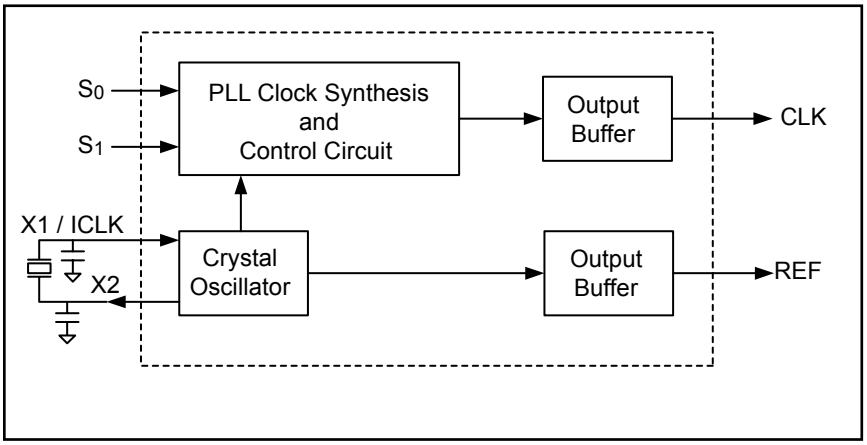
## Features

- Zero ppm multiplication error
- Input crystal frequency range: 5 - 30MHz
- Input clock frequency range: 4 - 50MHz
- Output clock frequencies range ≤ 200MHz
- Period jitter ≤ 100ps (typ)
- 9 Selectable frequencies controlled by $S_0$ and $S_1$ pins
- Supply voltage: 3.3V ±10% or 5.0V ±10%
- Packaging (Pb-Free and Green):
  —8-pin SOIC (W)

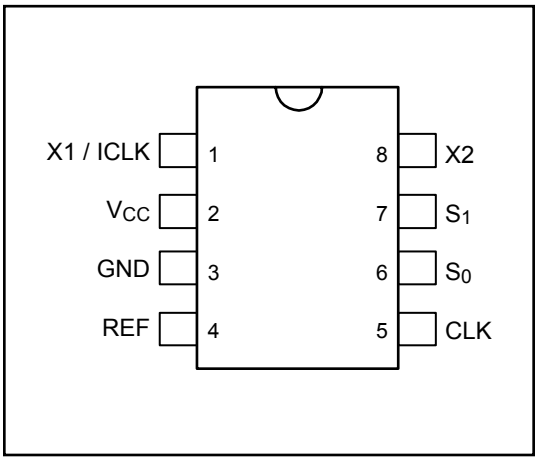
## Description

The PI6C4512 is a precision general-purpose clock synthesizer with fmax≤ 200MHz. The PI6C4512 uses an external low-cost crystal to generate a very accurate rate and stable system clocks.

## Block Diagram




## Pin Configuration




## Clock Output Table(1)

| $S_1$ | $S_0$ | CLK |
|---|---|---|
| 0 | 0 | x 4 |
| 0 | M | x (16/3) |
| 0 | 1 | x 5 |
| M | 0 | x 2.5 |
| M | M | x 2 |
| M | 1 | x (10/3) |
| 1 | 0 | x 6 |
| 1 | M | x 3 |
| 1 | 1 | x 8 |

**Notes:**
1. M = Mid-level (unconnected, biases to $V_{CC}/2$).

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested)

| | |
|---|---|
| Storage temperature | -65°C to +150ºC |
| Ambient Operating Temperature | 0°C to +70ºC |
| Supply Voltage to Ground Potential ($V_{CC}$) | -0.3V to +7.0V |
| Inputs (Referenced to GND) | -0.5V to $V_{CC}$ +0.5V |
| Clock Output (Referenced to GND) | -0.5V to $V_{CC}$ +0.5V |
| Soldering Temperature (Max of 10 seconds) | 260ºC |

**Note:**
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Pin Description

| Name | Pin | Description |
|---|---|---|
| X1/ICLK | 1 | Crystal connection or clock input. |
| $V_{CC}$ | 2 | Supply voltage: 3.3V ±10% or 5.0V ±10% |
| GND | 3 | Connect to GND |
| REF | 4 | Buffered crystal oscillator output clock |
| CLK | 5 | Clock output |
| $S_0$ | 6 | Multiplier select pin 0. Connect to GND or $V_{CC}$ or float (no connection). |
| $S_1$ | 7 | Multiplier select pin 1. Connect to GND or $V_{CC}$ or float (no connection). |
| X2 | 8 | Crystal connection. Leave unconnected for clock input. |

## External Components

The PI6C4512 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.1µF || 0.01µF should be connected between each $V_{DD}$ and GND and placed as close to the chip as possible. A series termination resistor of 33Ω may be used for clock outputs. If a crystal is used, it should be a fundamental mode, parallel resonant crystal. Crystal capacitors should be connected from $X_1$ to ground and from $X_2$ to ground to according to the crystal specifications. The value of capacitors is given by the following equation, where $C_L$ is the crystal load capacitance: Crystal caps (pF) = ($C_L$ -15) x 2.

## Recommended Operation Conditions

| Symbol | Description | Test Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | 3 | | 5.5 | V |
| $T_A$ | Operating Temperature | | 0 | | +70 | °C |

## DC Electrical Characteristics ($V_{CC}$ = 3.3V ± 10% and 5.0V ± 10%, $T_A$ = 0°C to +70°C, unless otherwise noted)

| Symbol | Description | Test Condition | Pin | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | $V_{CC}$ | 3 | | 5.5 | V |
| $I_{CC}$ | Supply current | No load, 20MHz crystal | $V_{CC}$ | ` | 12 | 30 | mA |
| $V_{IH}$ | Input logic HIGH | | ICLK | ($V_{CC}$/2) +1 | $V_{CC}$/2 | | V |
| $V_{IL}$ | Input logic LOW | | ICLK | | $V_{CC}$/2 | ($V_{CC}$/2)-1 | V |
| $V_{IH}$ | Input logic HIGH | | $S_0$, $S_1$ | $V_{CC}$-0.5 | | | V |
| $V_{IM}$ | Input mid-level | | $S_0$, $S_1$ | | $V_{CC}$/2 | | V |
| $V_{IL}$ | Input logic LOW | | $S_0$, $S_1$ | | | 0.5 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = -12mA | CLK, REF | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = +12mA | CLK, REF | | | 0.4 | V |
| $I_S$ | Short circuit current | | CLK | | ±70 | | mA |

## AC Electrical Characteristics ($V_{CC}$ = 3.3V ±10% and 5.0V ± 10%, $T_A$ = 0°C to +70°C, unless noted)

| Symbol | Parameter | Test Condition | Pin | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $F_{IN}$ | Input Frequency | Crystal | ICLK | 5 | | 30 | MHz |
| | | Clock | ICLK | 4 | | 50 | MHz |
| $F_{OUT}$ | Output frequency(1) | $V_{CC}$: 4.5V to 5.5V | CLK | 20 | | 200 | MHz |
| | | $V_{CC}$: 3.0V to 3.6V | CLK | 20 | | 180 | MHz |
| $T_R$ | Output clock rise time | 0.8V to 2.0V, $C_L$ = 15pF load | CLK | | 1 | | ns |
| $T_F$ | Output clock fall time | 2.0V to 0.8V, $C_L$ = 15pF load | CLK | | 1 | | ns |
| $T_{DC}$ | Output clock duty-cycle | At $V_{CC}$/2, f ≤ 150MHz | CLK | 45 | 50 | 55 | % |
| | | At $V_{CC}$/2, f > 150MHz | CLK | 40 | 50 | 60 | |
| BW | PLL bandwidth | f ≤ 150MHz | CLK | 10 | | | kHz |
| $T_{PJ}$ | Period Jitter | 100MHz to 200MHz | CLK | | 100 | 250 | ps |

**Notes:**
1. The phase relationship between input and output clocks can change at power up.

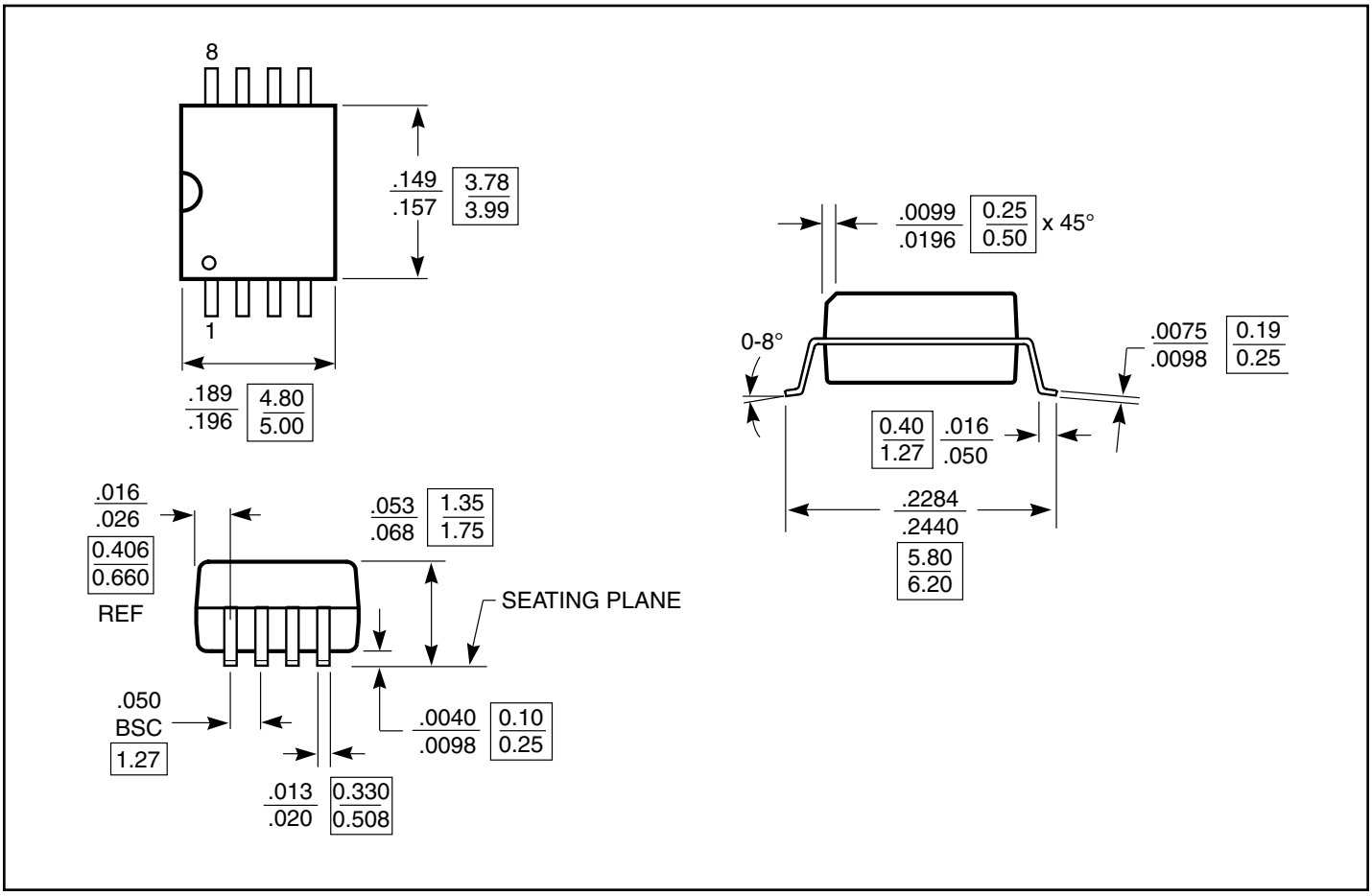
## Recommended Crystal

Pericom recommends the Pericom 49S SMD series crystal, which is a low cost, low profile SMD crystal packaged in a HC-49/u short SMD package.

## Recommended Crystal Specifications

| Parameter | Value | Units |
|---|---|---|
| Mode of Oscillation | Fundamental | AT |
| Frequency | 5 - 30 | MHz |
| Frequency Tolerance | ±50 | PPM |
| Temperature and Aging Stability | ±50 | PPM |
| CO/CI Ratio | 240 | |
| Load Cap | 18 | pF |
| Equivalent Series Resistance | 30 | Ω |

## Packaging Mechanical: 8-Pin SOIC (W)




## Ordering Information[1,2]

| Ordering Code | Package Code | Package Description |
|---|---|---|
| PI6C4512W | W | 8-pin SOIC |
| PI6C4512WE | WE | Pb-Free and Green 8-pin SOIC |

**Note:**
1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green