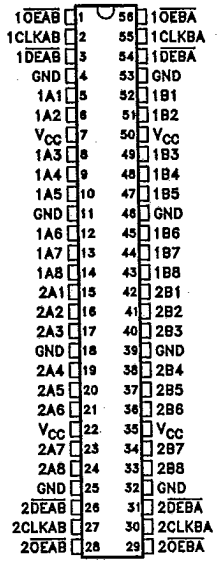
T-52-31

54AC16470, 54ACT16470
74AC16470, 74ACT16470
16-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0246—D3569, JUNE 1990

- **Members of Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16470, 54ACT16470 ... WD PACKAGE
74AC16470, 74ACT16470 ... DL PACKAGE
(TOP VIEW)



description

The 'AC16470 and 'ACT16470 are noninverting 16-bit registered bus transceivers composed of two 8-bit sections with separate control signals. For either 8-bit transceiver section, data flow in the A-to-B mode is controlled by output enable (1$\overline{OEAB}$ or 2$\overline{OEAB}$), direction enable (1$\overline{DEAB}$ or 2$\overline{DEAB}$), and clock (1CLKAB or 2CLKAB) inputs.

When 1$\overline{DEAB}$ (or 2$\overline{DEAB}$) is high, storage of the current A-bus data is inhibited and the corresponding B outputs are in the high-impedance state. When 1$\overline{DEAB}$ (or 2$\overline{DEAB}$) is low, the register contents and the output buffers are controlled by 1CLKAB (or 2CLKAB) and 1$\overline{OEAB}$ (or 2$\overline{OEAB}$). A low level on 1CLKAB (or 2CLKAB) inhibits register loading; a low-to-high transition on 1CLKAB (or 2CLKAB) causes loading of the corresponding registers with the current A-bus data. If 1$\overline{OEAB}$ (or 2$\overline{OEAB}$) is low, the corresponding B outputs reflect the contents of the registers. A high level on 1$\overline{OEAB}$ (or 2$\overline{OEAB}$) causes the B outputs to be in the high-impedance state.

FUNCTION TABLE, EACH SECTION†

INPUTS			LATCH DATA	B OUTPUTS
$\overline{DEAB}$	CLKAB	$\overline{OEAB}$		
H	X	X	Previous A Data	Z
L	L	H	Previous A Data	Z
L	L	L	Previous A Data	Previous A Data
L	↑	H	Current A Data	Z
L	↑	L	Current A Data	Current A Data

† A-to-B data flow is shown. B-to-A data flow is controlled analogously by $\overline{DEBA}$, CLKBA, and $\overline{OEBA}$.

PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

Data flow from B to A is similar, but uses 1$\overline{OEBA}$ and/or 2$\overline{OEBA}$, 1$\overline{DEBA}$ and/or 2$\overline{DEBA}$, and 1CLKBA and/or 2CLKBA.

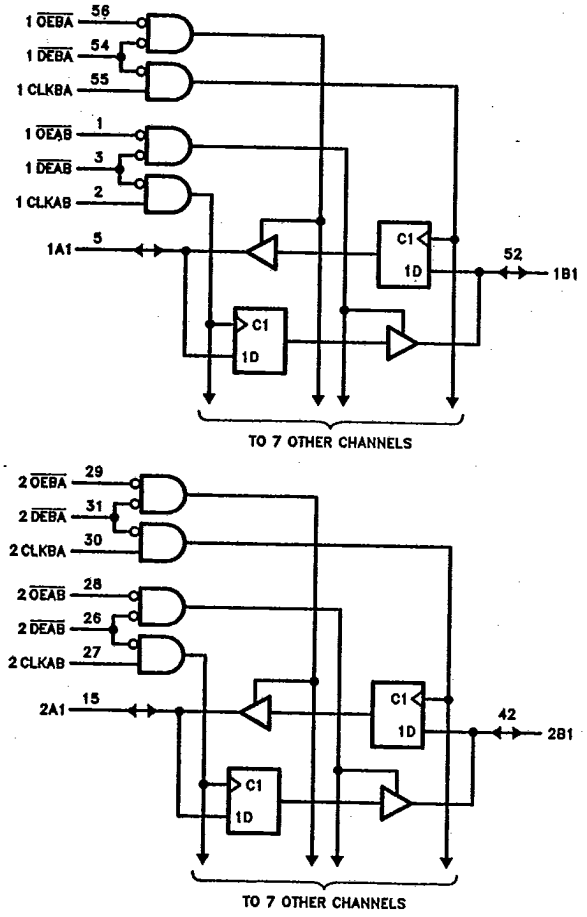
The 74AC16470 and 74ACT16470 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16470 has CMOS-compatible input thresholds. The 'ACT16470 has TTL-compatible input thresholds.

The 54AC16470 and 54ACT16470 are characterized over the full military temperature range of −55°C to 125°C. The 74AC16470 and 74ACT16470 are characterized for operation from −40°C to 85°C.

logic diagram (positive logic)

T-52-31



PRODUCT PREVIEW