❑ MN101C88D, MN101C88F, MN101C88G

Type	MN101C88D	MN101C88F	MN101C88G	MN101CF88G
Internal ROM type	Mask ROM			FLASH
ROM (byte)	64K	96K	128K	
RAM (byte)	2K	4K		10K
Package (Lead-free)	QFP100-P-1818B	QFP100-P-1818B (Under planning)	QFP100-P-1818B	
Minimum Instruction Execution Time	0.1 µs (at 4.5 V to 5.5 V, 20 MHz) 0.24 µs (at 2.7 V to 5.5 V, 8.4 MHz) 0.48 µs (at 2.3 V to 5.5 V, 4.19 MHz)* 1.0 µs (at 2.0 V to 5.5 V, 2.0 MHz)* 62.5 µs (at 2.0 V to 5.5 V, 32 kHz)* * The lower limit for operation guarantee for flash memory built-in type is 2.5 V			

■ Interrupts

RESET, Watchdog, External 0 to 4, Timer 0 to 3, Timer 6, Timer 7 (2 systems), Time base, Serial 0 (2 systems), Serial 1 (2 systems), Serial 2, A/D conversion finish, Automatic transfer finish, FL display key scan, FL display dimmer

■ Timer Counter

Timer counter 0 : 8-bit × 1
(square-wave/8-bit PWM output, event count, generation of remote control carrier, simple pulse width measurement)
Clock source..... 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input
Interrupt source ..... coincidence with compare register 0

Timer counter 1 : 8-bit × 1 (square-wave output, event count, serial transfer clock)
Clock source..... 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input
Interrupt source ..... coincidence with compare register 1

Timer counter 0, 1 can be cascade-connected.

Timer counter 2 : 8-bit × 1
(square-wave output, PWM output, serial transfer clock, event count, simple pulse width measurement)
Clock source..... 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input
Interrupt source ..... coincidence with compare register 2

Timer counter 3 : 8-bit × 1
(square-wave output, event count, generation of remote control carrier, serial transfer clock)
Clock source..... 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input
Interrupt source ..... coincidence with compare register 3

Timer counter 2, 3 can be cascade-connected.

Timer counter 6 : 8-bit freerun timer
Clock source..... 1/1 of system clock frequency; 1/1, 1/128, 1/8192 of OSC oscillation clock frequency; 1/1, 1/128, 1/8192 of XI oscillation clock frequency
Interrupt source ..... coincidence with compare register 6

Timer counter 7 : 16-bit × 1
(square-wave output, 16-bit PWM output (cycle / duty continuous variable), event count, pulse width measurement, input capture)
Clock source..... 1/1, 1/2, 1/4, 1/16 of system clock frequency; 1/1, 1/2, 1/4, 1/16 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency
Interrupt source ..... coincidence with compare register 7 (2 lines)

Time base timer (one-minute count setting)
Clock source..... 1/1 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency
Interrupt source ..... 1/128, 1/256, 1/512, 1/1024, 1/8192, 1/32768, of clock source frequency

Watchdog timer

Interrupt source ..... 1/65536, 1/262144, 1/1048576 of system clock frequency

■ Serial interface

Serial 0 : synchronous type/UART (full-duplex) × 1

Clock source..... 1/2, 1/4 of system clock frequency; pulse output of timer counter 1 or 2; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency, external clock

Serial 1 : synchronous type/UART (full-duplex) × 1

Clock source..... 1/2, 1/4 of system clock frequency; pulse output of timer counter 1 or 2; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency, external clock

Serial 2 : synchronous type/single-master I²C × 1

Clock source..... 1/2, 1/4 of system clock frequency; pulse output of timer counter 2 or 3; 1/2, 1/4, 1/16, 1/32 of OSC oscillation clock frequency, external clock

■ DMA controller

Max. Transfer cycles : 255

Starting factor : external request, various types of interrupt, software

Transfer mode : 1-byte transfer, word transfer, burst transfer

■ I/O Pins

I/O	35	Common use, Specified pull-up resistor available , Input/output selectable (bit unit)
High Voltage	53	Output : 29, I/O : 24, P-ch. open drain (breakdown voltage –40 V) : FL drive : 53 Specified pull-down resistor mask option : 35

■ A/D converter

10-bit × 8-ch. (with S/H)

■ Display control function

FL

(35 to 43) segments × (18 to 10) digits

■ Special Ports

Buzzer output, high-current drive port

■ ROM Correction

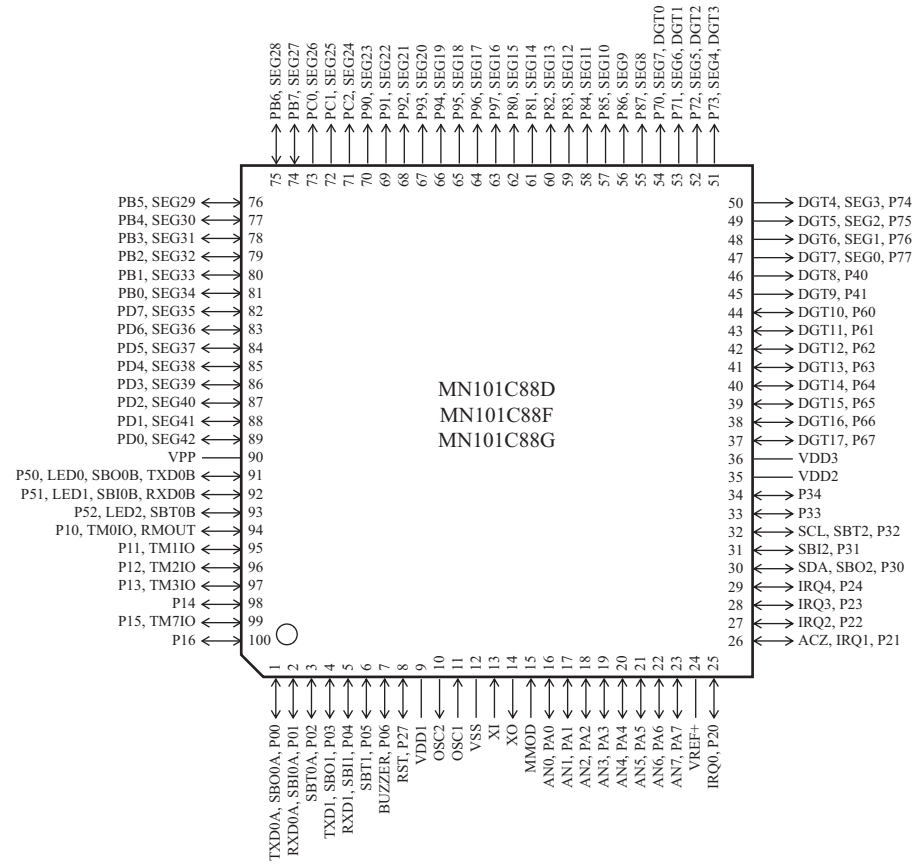
Correcting address designation : up to 3 addresses possible

■ Development tools

In-circuit Emulator

PX-ICE101C/D+PX-PRB101C88-QFP100-P-1818B-M

■ Pin Assignment



QFP100-P-1818B

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