TLE4953
TLE4953C

Differential Two-Wire Hall Effect Sensor IC

Sensors

Never stop thinking

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Previous Version:	V 1.0	

Page	Subjects (major changes since last revision)
	TLE4943 (without C) included

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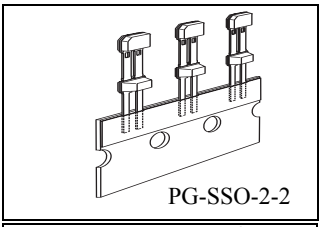
Differential Two-Wire Hall Effect Sensor IC

TLE4953
TLE4953C

Data Sheet V2.0

Features

- Two-wire PWM current interface
- Detection of rotation direction
- Dynamic self-calibration principle & high sensitivity
- Adaptive hysteresis
- Single chip solution - no external components
- Vibration suppression in calibrated mode
- South and north pole pre-induction possible
- High resistance to piezo effects
- Large operating air-gaps
- Wide operating temperature range
- From zero speed up to 12 kHz
- 1.8 nF overmolded capacitor
- For coarse transmission target wheels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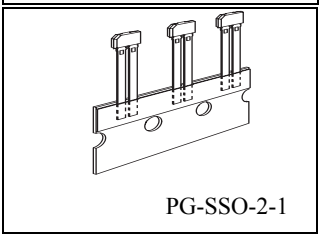
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Type	Marking	Order Code	Package
TLE4953C	53C1R	SP000015141	PG-SSO-2-2
TLE4953	53	SP000278512	PG-SSO-2-1

The differential Hall Effect sensor TLE4953 is designed to provide information about rotational speed and direction of rotation to modern transmission and ABS systems. The output has been designed as a two wire current interface based on a Pulse Width Modulation principle. The sensor operates without external components and combines a fast power-up time with a wide frequency range. Excellent accuracy and sensitivity is specified for harsh automotive requirements as a wide temperature range, high ESD robustness and high EMC resilience. State-of-the-art BiCMOS technology is used for monolithic integration of the active sensor areas and the signal conditioning.

Finally, the optimized piezo compensation and the integrated dynamic offset compensation enable easy manufacturing and elimination of magnetic offsets. Adaptive hysteresis concept increases the noise immunity. The TLE4953C is additionally provided with an overmolded 1.8 nF capacitor for improved EMI performance.

Pin Configuration (top view)

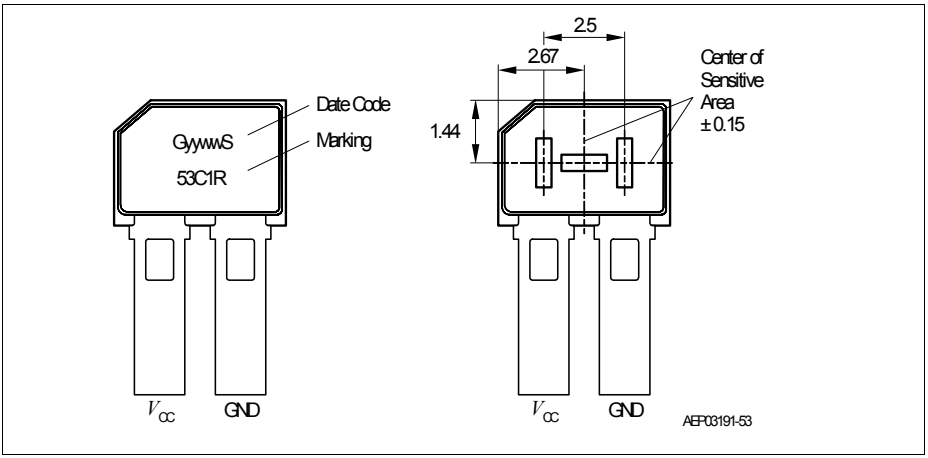


Figure 1

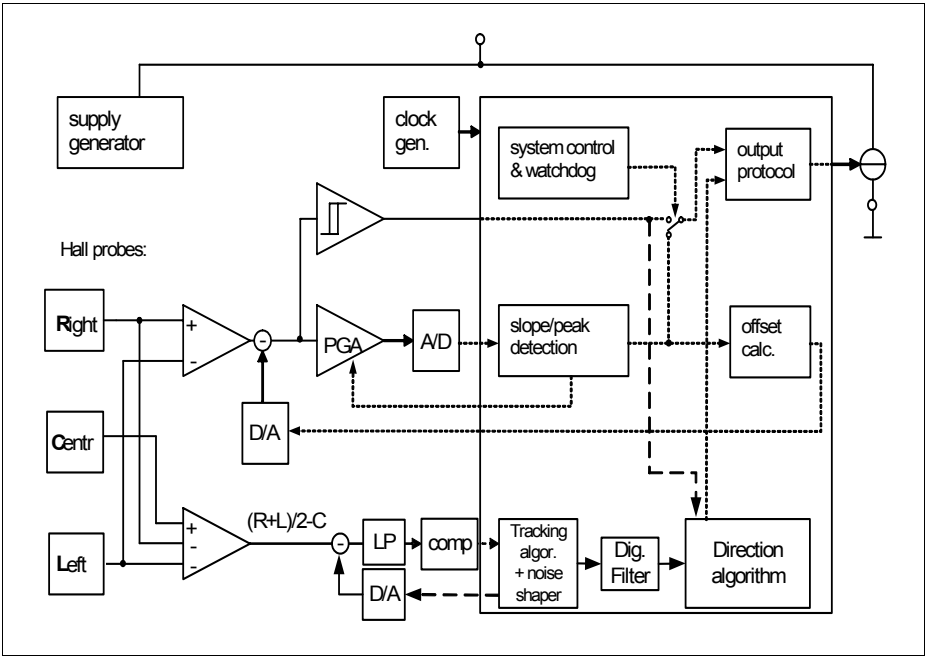


Figure 2 Block Diagram

Functional Description

The differential Hall Effect IC detects the motion of ferromagnetic or permanent magnet structures by measuring the differential flux density of the magnetic field. To detect the motion of ferromagnetic objects the magnetic field must be provided by a backbiasing permanent magnet. Either the South or North pole of the magnet can be attached to the rear, unmarked side (remark: rear side may contain data matrix code) of the IC package.

Magnetic offsets of up to ± 20 mT and mechanical offsets are cancelled out through a self-calibration algorithm. Only 2 transitions are necessary for the self-calibration procedure. After the initial self-calibration sequence switching occurs when the input signal crosses the adaptive threshold on the rising magnetic edge.

The ON and OFF state of the IC are indicated by ***High*** and ***Low*** current consumption. Each rising magnetic edge of the magnetic input signal triggers an output pulse.

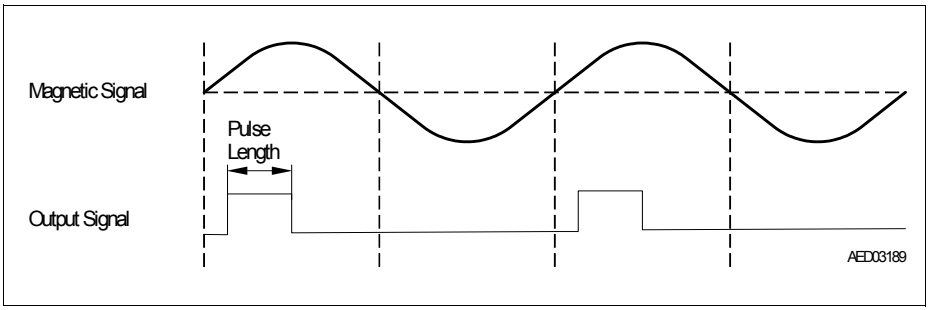


Figure 3 Output Pulses on magnetic rising edge

In addition to the speed signal, the following information is provided by varying the length of the output pulses (PWM modulation):

Speed signal = **S**

The speed signal is issued at the first output pulse after start up and when the magnetic frequency is above 1kHz.

Direction of rotation left = **DR-L**

DR-L information is issued in the output pulse length when the active target wheel in front of the Hall Effect IC moves from the pin V_{CC} to the pin GND.

Direction of rotation right = **DR-R**

DR-R information is issued in the output pulse length when the active target wheel in front of the Hall Effect IC moves from the pin GND to the pin V_{CC}.

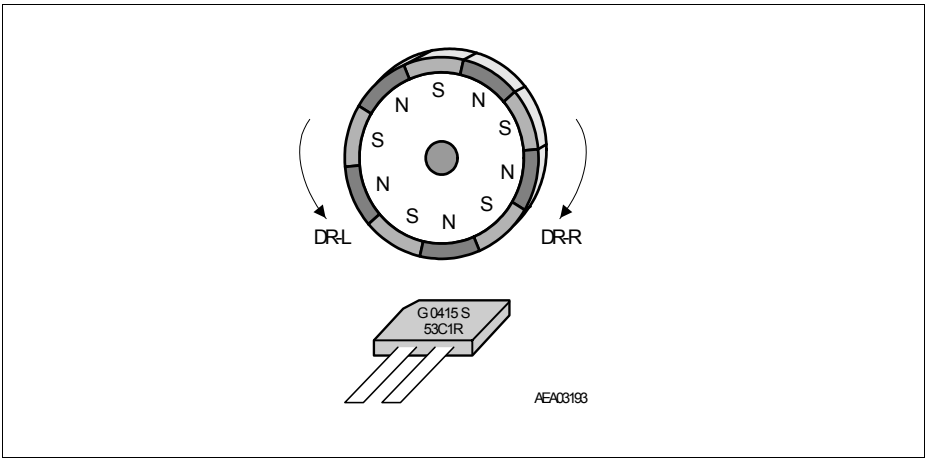


Figure 4 Definition of Rotation Direction

Circuit Description

The circuit internally is supplied by a voltage regulator. A 2 MHz on-chip oscillator serves as a clock generator for the DSP and the output encoder.

Speed signal circuitry

TLE4953 speed signal path comprises a pair of Hall Effect probes, separated from each other by 2.5 mm, a differential amplifier including noise limiting low-pass filter, and a comparator triggering a switched current output stage. An offset cancellation feedback loop is provided through a signal-tracking A/D converter, a digital signal processor (DSP), and an offset cancellation D/A converter.

Uncalibrated Mode

Occasionally a short initial offset settling time $t_{d,input}$ might delay the detection of the input signal. (The sensor is "blind"). During the startup phase (un-calibrated mode) the output is disabled ($I = I_{Low}$). The magnetic input signal is tracked by the speed ADC and monitored within the digital circuit. For detection the signal needs to exceed a threshold (digital noise constant d1). When the signal slope is identified as a rising edge, a trigger pulse is issued to a comparator. A second trigger pulse is issued as soon as the next rising edge is detected.

Between the start-up of the magnetic input signal and the time when its second extreme is reached, the PGA (programmable gain amplifier) will switch to its appropriate position. This value is determined by the signal amplitude and initial offset value. The digital noise constant value is changing accordingly (d1 $\rightarrow$ d2, related to the corresponding PGA

states), leading to a change in phase shift between magnetic input signal and output signal. After that consecutive output edges should have a nominal delay of about 360°. During the uncalibrated mode the offset value is calculated by the peak detection algorithm as described below.

The differential input signal is digitized in the speed A/D converter and fed into the DSP part of the circuit. The minimum and maximum values of the input signal are extracted and their corresponding arithmetic mean value is calculated. The offset of this mean value is determined and fed into the offset cancellation DAC.

The offset update takes place when two valid extremes are found and the direction of the update has the same orientation as the magnetic slope (valid for calibrated mode). For example an positive offset update is only possible on a rising magnetic edge. The offset update is done independant from the output switching.

After successful correction of the offset, the output switching is in calibrated mode. Switching occurs at adaptive threshold-crossover. It is only affected by the propagation delay time of the signal path, which is mainly determined by the noise limiting filter. Signals which are below a predefined threshold $\Delta B_{\mathrm{Limit}}$ are not detected. This prevents unwanted switching.

The adaptive hysteresis is linked to the PGA state. Therefore the system is able to suppress switching if vibration or noise signals are smaller than the adaptive hysteresis.

The switching and direction information is fed into the DSP and the output encoder. The pulse length of the ***High*** output current is generated according to the rotational speed and the direction of rotation.

Direction signal circuitry

The differential signal between a third Hall probe and the mean value of the differential Hall probe pair is obtained from the direction input amplifier. This signal is digitized by the direction ADC and fed into the digital circuitry. There, the phase of the signal referring to the speed signal is analyzed and the direction information is forwarded to the output encoder. The phase is identified by calculating the size of the direction signal at two consecutive zero crossings of the speed signal. This is done by subtracting the current direction signal from the internal stored value which has been taken from the previous magnetic edge.

Depending on the phase shift between the direction signal and the speed signal a positive or a negative value occur. The information if the new direction calculation takes place at a rising or a falling magnetic edge allows together with the algebraic sign of the calculated direction signal a reliable direction detection.

The first pulse after power is always a speed pulse as there is no stored direction information available.

Vibration suppression algorithm:

The magnetic signal amplitude and the direction information is used for detection of parasitic magnetic signals. Unwanted magnetic signals can be caused by angular or airgap vibrations for instance. If an input signal is clearly detected as a vibration signal, the output of pulses will be suppressed.

A magnetic input signal is classified as parasitic vibration signal if

a. the speed signal amplitude is smaller than the internal hysteresis or

b. the direction signal amplitude is smaller than the internal limit or

c. the direction signal consists of alternating left/right information

The quality of vibration suppression (according a & b) depends on the hysteresis limits and on the magnitude of the magnetic signal. The bigger the hysteresis the better the suppression of parasitc signals.

For parasitic signals where items above (a. to c.) are not clearly applicable or at other more rare cases (e.g. IC startup) vibration suppression is not guaranteed. The performance of the direction detection and vibration suppression algorithm depends on the used magnetic circuit and as well on the used target wheel and need to be evaluated.

Please ask for application support if you have questions on the vibration suppresion algorithm.

Package information:

Pure tin covering (green lead plating) is used. Lead frame material is Wieland K62 (UNS: C18090) and contains CuSn1CrNiTi. Product is RoHS (**R**estriction **o**f **H**azardous **S**ubstances) compliant and marked with letter G in front of the data code marking and may contain a data matrix code on the rear side of the package (see also information note 136/03). Please refer to your key account team or regional sales if you need further information.

Absolute Maximum Ratings

T_j = -40 to 155 °C, 4.0V ≤ V_{CC} ≤ 16.5 V

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_{CC}	– 0.3	–	V	T_j ≤ 80 °C
		–	16.5		T_j = 175 °C
		–	20		T_j = 155 °C
		–	22		t = 10 × 5 min
		–	24		t = 10 × 5 min, R_M ≥ 75 Ω included in V_{CC}
		–	27		t = 400 ms, R_M ≥ 75 Ω included in V_{CC}
Reverse polarity current	I_{rev}	–	200	mA	External current limitation required, t ≤4 h[1)]
Junction temperature	T_j	–	155	°C	2000 h, V_{CC} ≤16.5 V
		–	165		1000 h, V_{CC} ≤ 16.5 V (not additive)
		–	175		168 h, V_{CC} ≤ 16.5 V (not additive)
		–	195		3 × 1 h, V_{CC} ≤ 16.5 V
Active lifetime	$t_{B,active}$	10000	–	h	
Storage temperature	T_S	– 40	150	°C	
Thermal resistance PG-SSO-2-2, PG-SSO-2-1	R_{thJA}	–	190	K/W	2)

1) This allows together with an external serial resistor (75 or 100 Ohm) reverse polarity voltage for a short duration. This resistor is usually present in the ECU of the application circuit.
2) Can be improved significantly by further processing like overmolding

Note: Stress in excess of those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Protection

Human Body Model (HBM) tests according to:
Standard EIA/JESD22-A114-B HBM (covers MIL STD 883D)

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
ESD-Protection TLE4953C TLE4953	V_{ESD}	 - -	 ± 12 ± 12	kV	R = 1.5 kΩ, C = 100 pF

Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_{CC}	4.5	20	V	Directly on IC leads excludes the R_M voltage drop
Supply voltage	V_{CC}	4.0	4.5	V	Directly on IC leads excludes the R_M voltage drop [1]
Supply voltage ripple	V_{AC}	–	6	Vpp	V_{CC} = 13 V $0 \le f \le 50$ kHz
Junction temperature	T_j	– 40	150	°C	
			170		168h $V_{CC} \le 16.5$ V [2]
Pre-induction	B_0	– 500	+ 500	mT	
Pre-induction offset between outer probes	$\Delta B_{stat., l/r}$	– 20	+ 20	mT	L-R
Pre-induction offset between mean of outer probes and center probe	$\Delta B_{stat., m/o}$	– 20	+ 20	mT	(L+R)/2-C
Differential Induction	ΔB	– 120	+ 120	mT	

1) Reduced performance possible for jitter/phase accuracy and power supply rejection ratio (EMC). Current levels will typically decrease but will be within specification limits. This voltage range is not recommended for continuos operation and should cover the function during short voltage drops which may occur at cranking of engine / test pulse 4.
2) increased jitter and reduced phase accuracy permissible between 150 and 170°C junction temperature.

Note: Within the operating range the functions given in the circuit description are fulfilled.

AC/DC Characteristics

All values specified at constant amplitude and offset of input signal, over operating range, unless otherwise specified. Typical values correspond to V_{CC}=12V and T_A=25°C

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Supply current	I_{Low}	5.9	7	8.4	mA	
Supply current	I_{High}	11.8	14	16.8	mA	
Supply current ratio	I_{High}/I_{Low}	1.9	–	–		
Output rise/fall slew rate TLE4953	t_r, t_f	12	–	26	mA/µs	R_M = 75 Ω $T_j \leq$ 170 °C See **Figure 5**
Output rise/fall slew rate TLE4953C	t_r, t_f	8	–	26	mA/µs	R_M = 75 Ω $T_j \leq$ 170 °C See **Figure 5**
Current ripple dI_X/dV_{CC}	I_X	–	–	90	µA/V	Only valid for TLE4953
Limit threshold speed 0Hz ≤ f ≤ 2500 Hz 2500 Hz ≤ f ≤ 12000 Hz	ΔB_{Limit}	 0.35	 0.8	 1.5 1.75	mT	[1]
Limit differential direction signal 0Hz ≤ f ≤ 1100 Hz	ΔB_{Dir}		 0.35		mT	Calculated at two consecutive threshold crossings
Initial calibration delay time	$t_{d,input}$	–	300	345	µs	Additional to n_{start}
Magnetic edges required for first output pulse (no previous vibration detected)	n_{start}	–	–	2	magn. edges	pulse occurs only on rising magnetic edge
Number of pulses in uncalibrated mode	$n_{DZ\text{-}Startup}$			2	pulses	3rd pulse calibrated
Number of emitted pulses with invalid direction information[2]	$n_{DR\text{-}Start}$	–	–	2[4]	pulses	3rd pulse correct
Frequency	f	0	–	12000	Hz	[3]

AC/DC Characteristics (cont'd)

All values specified at constant amplitude and offset of input signal, over operating range, unless otherwise specified. Typical values correspond to V_{CC}=12V and T_A=25°C

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Systematic phase error of output edges during start-up and uncalibrated mode		– 88		+ 88	°	Systematical phase error of "uncal" pulse; nth vs. n+1th pulse (does not include jitter)
Phase shift during transition from uncalibrated to calibrated mode	$\Delta\Phi_{switch}$	– 90		+ 90	°	
Phase shift change during PGA switching in calibrated mode		0		80	°	Due to adaptive hysteresis. Depending on signal shape.
Magnetic differential field change required for startup with 1st rising edge $\Delta\hat{B}_{Limit,\ early\ startup}$	$\Delta\hat{B}_{Limit,}$ early startup			3.5	mT	peak to peak value
Jitter, $T_j \leq 150$ °C $T_j \leq 170$ °C f ≤ 2500 Hz	$S_{Jit\text{-}far}$	– –	– –	± 2 ± 3	%	[4] 1 σ value V_{CC} = 12 V $\Delta B \geq 2$ mT
Jitter, $T_j \leq 150$ °C $T_j \leq 170$ °C 2500 Hz < f ≤12000 Hz	$S_{Jit\text{-}far}$	– –	– –	± 3 ± 4.5	%	[4] 1 σ value V_{CC} = 12 V $\Delta B \geq 2$ mT
Jitter at board net ripple	$S_{Jit\text{-}AC}$	–	–	± 2	%	[4] V_{CC} = 13 V±6 Vpp 0 ≤ f ≤50 kHz ΔB = 15 mT

1) magnetic amplitude values, sine magnetic field, Limits refer to the 50% criteria. 50% of pulses are missing.Only valid at lowest PGA stage/highest amplification because of adaptive hysteresis.
2) The first 2 pulses may contain only direction information if the direction signal is above ΔB_{Dir}.The first pulse after starting will be the speed pulse.
3) High frequency behaviour not subject to production test - verified by design/characterization.
4) not subject to production test- verified by design/characterization, magnetic values are amplitude values

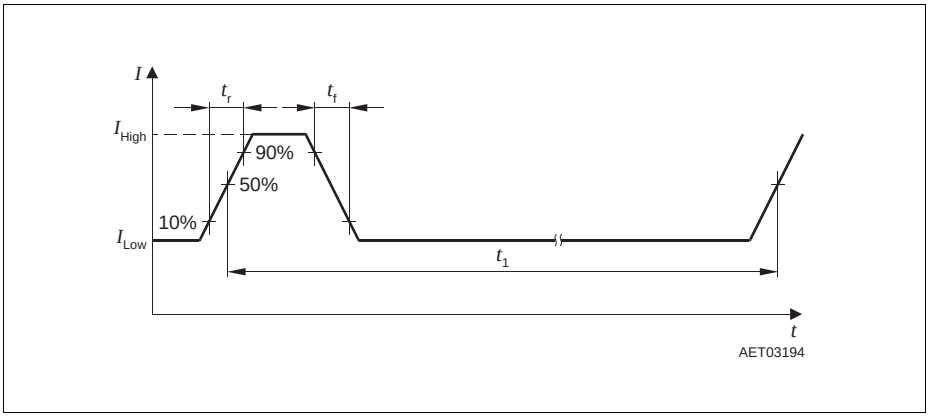


Figure 5 Definition of Rise and Fall Time

Timing Characteristics

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Pre-low length	$t_{\text{pre-low}}$	24	30	36	µs	
Speed signal	t_{S}	24	30	36	µs	
Length of DR-L pulse	$t_{\text{DR-L}}$	50	60	70	µs	
Length of DR-R pulse	$t_{\text{DR-R}}$	102	120	138	µs	
Output of DR-L/R pulse, maximum frequency From low - high frequency From high - low frequency	$f_{\text{DR, max}}$	–	 1100 1000	–	Hz	Internal hysteresis of direction signal

PWM Current Interface

Between each magnetic transition and the rising edge of the corresponding output pulse the output current is ***Low*** for $t_{\text{pre-low}}$ in order to allow reliable internal conveyance. Following the signal pulse (current is ***High***) is output.

If the magnetic direction field exceeds ΔB_{Dir}, the output pulse lengths are 60 µs or 120 µs respectively, depending on the direction of rotation.

If the magnitude of the magnetic direction field is below ΔB_{dir}, the output pulses are suppressed when the frequency is below $f_{\text{DR,max}}$ (see section vibration suppression). For magnitudes of the magnetic differential field below ΔB_{Limit} the signal is lost.

Speed pulse occur only at the first pulse after start up or above $f_{DR,\,max}$.

If no magnetic differential signal change is detected the IC will remain in calibrated mode. No internal reset are generated - therefore a zero speed operation is possible.

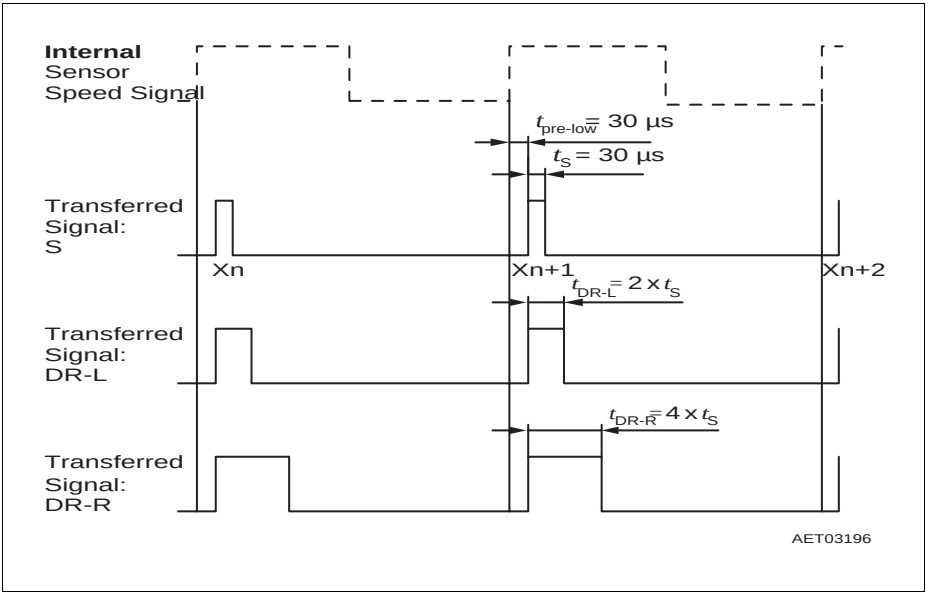


Figure 6 Definition of PWM Current Interface

Electro Magnetic Compatibility (values depend on R_M!)

Parameter	Symbol	Level/Typ	Status
Ref. ISO 7637-1; test circuit 1; ΔB = 2 mT (amplitude of sinus signal); V_{CC} = 13.5 V, f_B = 100 Hz; T = 25 °C; $R_M \geq 75\ \Omega$			
Testpulse 1	V_{EMC}	IV / – 100 V	C[1)]
Testpulse 2		IV / 100 V	C[1)]
Testpulse 3a		IV / – 150 V	A
Testpulse 3b		IV / 100 V	A
Testpulse 4		IV / – 7 V	B[2)]
Testpulse 5		IV / 86.5[3)] V	C

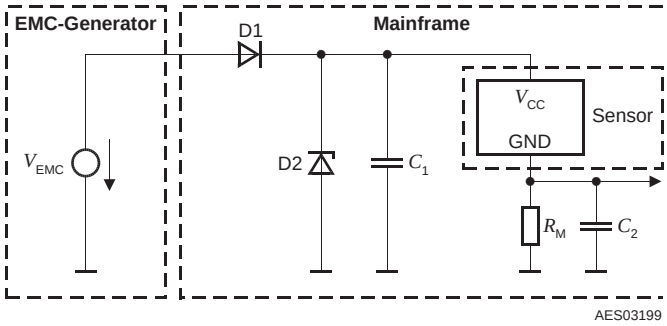
1) According to 7637-1 the supply switched "OFF" for t = 200 ms.
2) According to 7637-1 for test pulse 4 the test voltage shall be 12 V ± 0.2 V. Measured with R_M =75Ω only. Mainly the current consumption will decrease. Status C with test circuit 1.
3) Applying in the board net a suppressor diode with sufficient energy absorption capability.

Ref. ISO 7637-3; test circuit 1;
ΔB = 2 mT (amplitude of sinus signal); V_{CC} = 13.5 V, f_B = 100 Hz; T = 25 °C; $R_M \geq 75\ \Omega$

Testpulse 1	V_{EMC}	IV / – 30 V	A
Testpulse 2		IV / 30 V	A
Testpulse 3a		IV / – 60 V	A
Testpulse 3b		IV / 40 V	A

Ref. ISO 11452-3; test circuit 1; measured in TEM-cell
ΔB = 2 mT; V_{CC} = 13.5 V, f_B = 100 Hz; T= 25 °C

EMC field strength (TLE4953)	$E_{TEM\text{-}Cell}$	IV / 200 V/m	AM = 80%, f = 1 kHz
EMC field strength (TLE4953C)	$E_{TEM\text{-}Cell}$	IV / 250 V/m	AM = 80%, f = 1 kHz



Components: D1: 1N4007
D2: T 5Z27 1J
C_1: 10 µF/35 V
C_2: 1 nF/1000 V
R_M: 75 Ω/5 W

Figure 7 Test Circuit 1

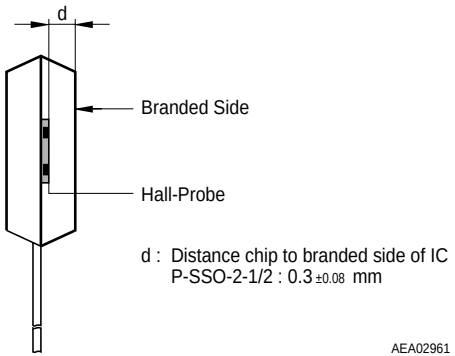
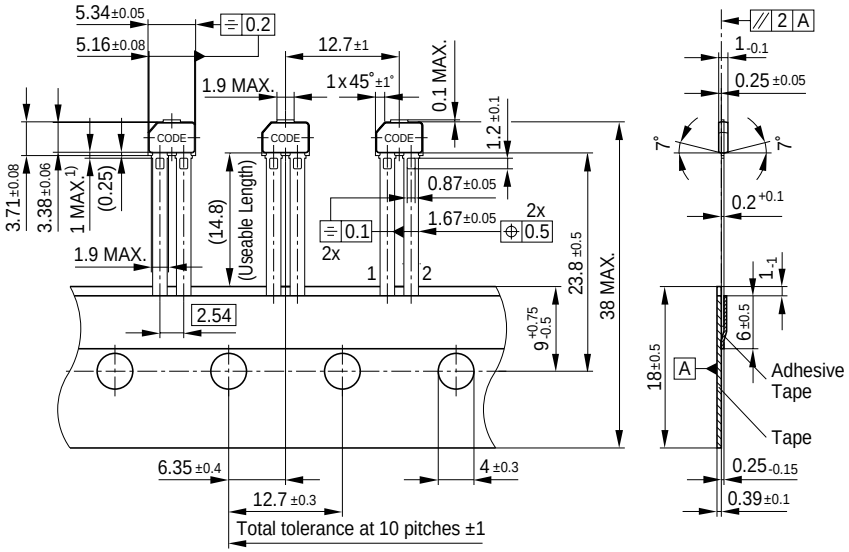


Figure 8 Package Outlines

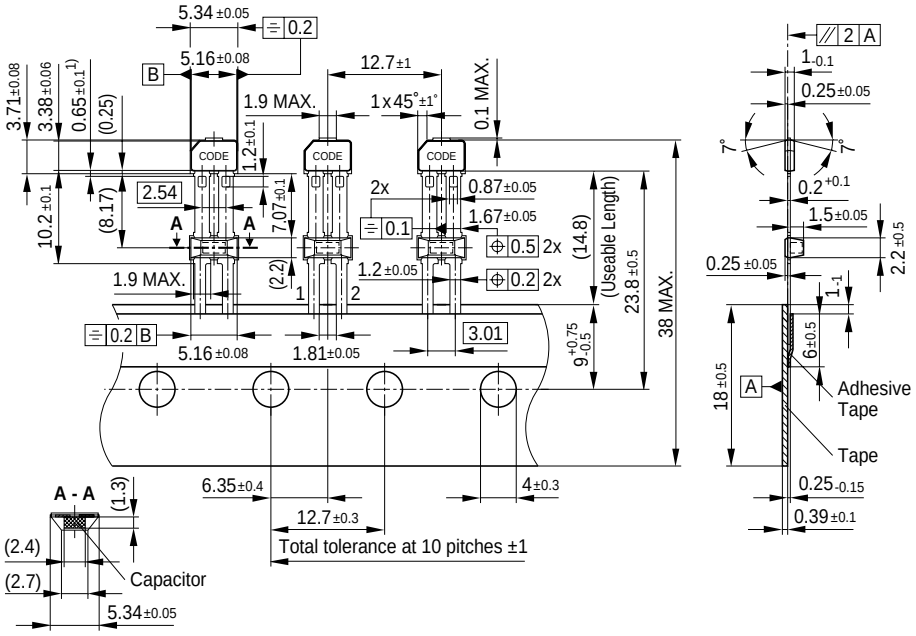
PG-SSO-2-1 (Plastic Single Small Outline Package)



1) No solder function area

Dimensions in mm

PG-SSO-2-2 (Plastic Single Small Outline Package)



1) No solder function area

Dimensions in mm

Note: You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products": http://www.infineon.com/products.

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