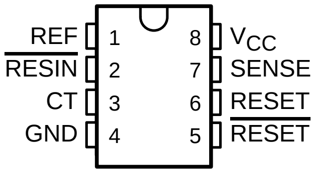
TL7702B, TL7705B, TL7733B
SUPPLY-VOLTAGE SUPERVISORS

The TL7705BM is obsolete and no longer is supplied.

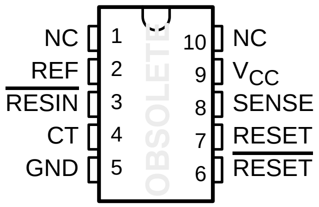
SLVS037M – SEPTEMBER 1989 – REVISED MAY 2003

- **Power-On Reset Generator**
- **Automatic Reset Generation After Voltage Drop**
- **$\overline{\text{RESET}}$ Output Defined From $V_{CC} \geq 1$ V**
- **Precision Voltage Sensor**
- **Temperature-Compensated Voltage Reference**
- **True and Complement Reset Outputs**
- **Externally Adjustable Pulse Duration**

TL77xxBC . . . D OR P PACKAGE
TL7705BM . . . JG PACKAGE
TL7705BQ . . . D PACKAGE
(TOP VIEW)

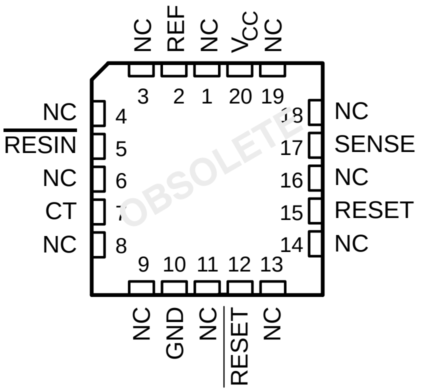


TL7705BM . . . U PACKAGE
(TOP VIEW)



NC – No internal connection

TL7705BM . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The TL7702B, TL7705B, and TL7733B are integrated-circuit supply-voltage supervisors designed for use as reset controllers in microcomputer and microprocessor systems. The supply-voltage supervisor monitors the supply for undervoltage conditions at the SENSE input. During power up, the $\overline{\text{RESET}}$ output becomes active (low) when V_{CC} attains a value approaching 1 V. As V_{CC} approaches 3 V (assuming that SENSE is above V_{T+}), the delay-timer function activates a time delay, after which outputs $\overline{\text{RESET}}$ and RESET go inactive (high and low, respectively). When an undervoltage condition occurs during normal operation, outputs $\overline{\text{RESET}}$ and RESET go active. To ensure that a complete reset occurs, the reset outputs remain active for a time delay after the voltage at the SENSE input exceeds the positive-going threshold value. The time delay is determined by the value of the external capacitor C_T: $t_d \approx 2.6 \times 10^4 \times C_T$, where C_T is in farads (F) and t_d is in seconds (s).

An external capacitor (typically 0.1 µF) must be connected to REF to reduce the influence of fast transients in the supply voltage.

The TL7702BC, TL7705BC, and TL7733BC are characterized for operation from 0°C to 70°C. The TL7702BI, TL7705BI, and TL7733BI are characterized for operation from –40°C to 85°C. The TL7705BQ is characterized for operation from –40°C to 125°C. The TL7705BM is characterized for operation from –55°C to 125°C.

description/ordering information (continued)

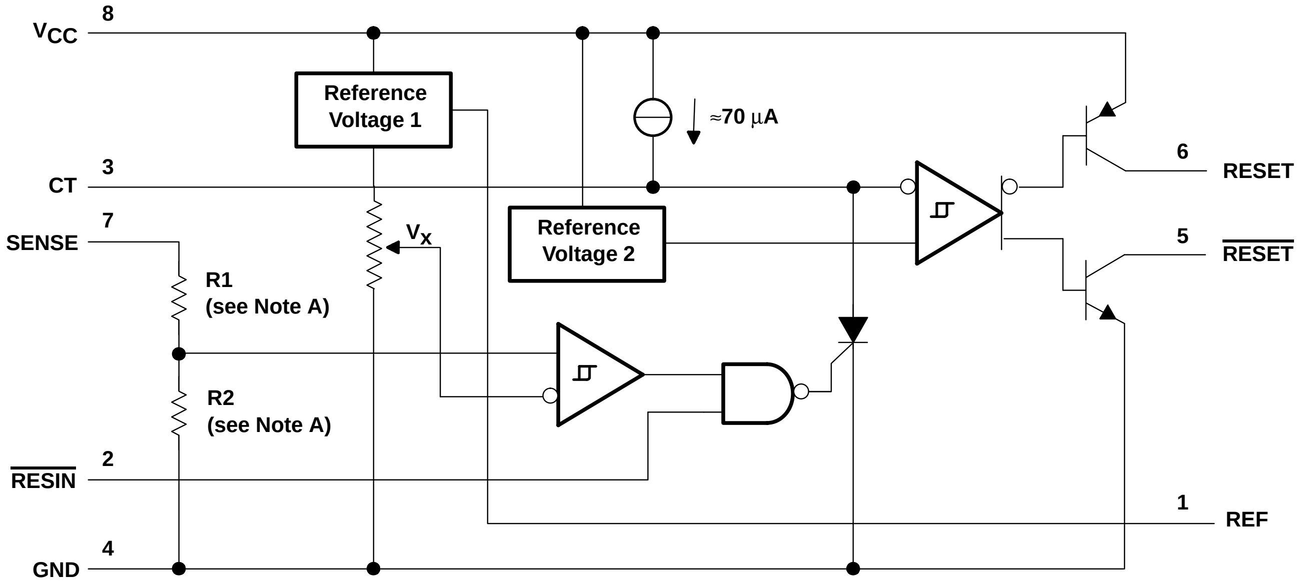
ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (P)	Tube of 50	TL7702BCP	TL7702BCP
	SOIC (D)	Tube of 75	TL7702BCD	7702BC
		Reel of 2500	TL7702BCDR	
	PDIP (P)	Tube of 50	TL7705BCP	TL7705BCP
	SOIC (D)	Tube of 75	TL7705BCD	7705BC
		Reel of 2500	TL7705BCDR	
	PDIP (P)	Tube of 50	TL7733BCP	TL7733BCP
	SOIC (D)	Tube of 75	TL7733BCD	7733BC
		Reel of 2500	TL7733BCDR	
–40°C to 85°C	PDIP (P)	Tube of 50	TL7702BIP	TL7702BIP
	SOIC (D)	Tube of 75	TL7702BID	7702BI
		Reel of 2500	TL7702BIDR	
	PDIP (P)	Tube of 50	TL7705BIP	TL7705BIP
	SOIC (D)	Tube of 75	TL7705BID	7705BI
		Reel of 2500	TL7705BIDR	
	PDIP (P)	Tube of 50	TL7733BIP	TL7705BIP
	SOIC (D)	Tube of 75	TL7733BID	7733BI
		Reel of 2500	TL7733BIDR	
–40°C to 125°C	SOIC (D)	Tube of 75	TL7705BQD	TL7705BQD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional block diagram

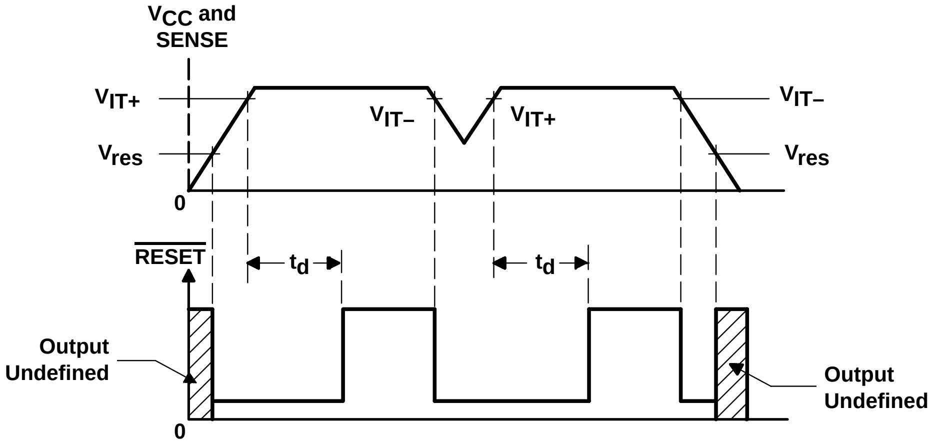
The functional block diagram is shown for illustrative purposes only; the actual circuit includes a trimming network to adjust the reference voltage and sense-comparator trip point.



Pin numbers shown are for the D, JG, and P packages.

NOTE A: TL7702B: R1 = 0 Ω, R2 = open, $V_X = V_{REF1}$
TL7705B: R1 = 23 kΩ, R2 = 10 kΩ, nominal, $V_X \approx 1.43$ V
TL7733B: R1 = 11.3 kΩ, R2 = 10 kΩ, nominal, $V_X \approx 1.43$ V

typical timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	20 V
Input voltage range, V_I: $\overline{\text{RESIN}}$	–0.3 V to 20 V
SENSE	–0.3 V to 20 V
High-level output current, I_{OH} (RESET)	–30 mA
Low-level output current, I_{OL} ($\overline{\text{RESET}}$)	30 mA
Package thermal impedance, θ_{JA} (see Notes 2 and 3): D package	97°C/W
P package	85°C/W
Operating virtual junction temperature, T_J	150°C
Case temperature for 60 seconds, T_C: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or U packages	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P packages	260°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values are with respect to the network ground terminal.
2. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3.6	18	V
V_{IH}	High-level input voltage	$\overline{\text{RESIN}}$	2	18	V
V_{IL}	Low-level input voltage	$\overline{\text{RESIN}}$	0	0.8	V
V_I	Input voltage	SENSE	0	18	V
I_{OH}	High-level output current	RESET		–20	mA
I_{OL}	Low-level output current	$\overline{\text{RESET}}$		20	mA
T_A	Operating free-air temperature range	TL77xxBC	0	70	°C
		TL77xxBI	–40	85	
		TL7705BQ	–40	125	
		TL7705BM	–55	125	

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS[†]		TL77xxBC TL77xxBI TL7705BQ			UNIT
					MIN	TYP	MAX	
V_{OH}	High-level output voltage, RESET		I_{OH} = –16 mA		V_{CC}–1.5			V
V_{OL}	Low-level output voltage, $\overline{\text{RESET}}$		I_{OL} = 16 mA				0.4	V
V_{ref}	Reference voltage, REF		I_{ref} = –500 µA,	T_A = 25°C	2.48	2.53	2.58	V
V_{IT-}	Negative-going input threshold voltage at SENSE input	TL7702B	T_A = 25°C		2.505	2.53	2.555	V
		TL7705B			4.5	4.55	4.6	
		TL7733B			3.03	3.08	3.13	
		TL7702B	T_A = full range[‡]		2.48	2.53	2.58	
		TL7705B			4.45	4.55	4.65	
		TL7733B			3	3.08	3.16	
V_{hys}	Hysteresis, SENSE ($V_{IT+} - V_{IT-}$)	TL7702B	V_{CC} = 3.6 V to 18 V,	T_A = 25°C		10		mV
		TL7705B				30		
		TL7733B				10		
V_{res}[§]	Power-up reset voltage		I_{OL} at $\overline{\text{RESET}}$ = 2 mA,	T_A = 25°C			1	V
I_I	Input current	$\overline{\text{RESIN}}$	V_I = 0.4 V to V_{CC}				–10	µA
		SENSE TL7702B	V_I = V_{ref} to 18 V			–0.1	–2	
I_{OH}	High-level output current, $\overline{\text{RESET}}$		V_O = 18 V,	See Figure 1			50	µA
I_{OL}	Low-level output current, RESET		V_O = 0 V,	See Figure 1			–50	µA
I_{CC}	Supply current		V_{SENSE} = 15 V,	$\overline{\text{RESIN}}$ ≥ 2 V		1.8	3	mA
			V_{CC} = 18 V,	T_A = full range[‡]			3.5	

[†] All electrical characteristics are measured with 0.1-µF capacitors connected at REF, CT, and V_{CC} to GND.
[‡] Full range is 0°C to 70°C for the C-suffix devices, –40°C to 85°C for the I-suffix devices, and –40°C to 125°C for the Q-suffix device.
[§] This is the lowest voltage at which $\overline{\text{RESET}}$ becomes active.

switching characteristics, V_{CC} = 5 V, C_T open, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TL77xxBC TL77xxBI TL7705BQ			UNIT
					MIN	TYP	MAX	
t_{PLH}	Propagation delay time from low- to high-level output	$\overline{\text{RESIN}}$	RESET	See Figures 1, 2, and 3		270	500	ns
t_{PHL}	Propagation delay time from high- to low-level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$	See Figures 1, 2, and 3		270	500	ns
t_w	Effective pulse duration	$\overline{\text{RESIN}}$		See Figure 2		150		ns
		SENSE				100		
t_r	Rise time		RESET	See Figures 1 and 3			75	ns
t_f	Fall time					150	200	
t_r	Rise time		$\overline{\text{RESET}}$	See Figures 1 and 3		75	150	ns
t_f	Fall time						50	

The TL7705BM is obsolete and no longer is supplied.

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER				TEST CONDITIONS[†]	TL7705BM			UNIT
					MIN	TYP	MAX	
V_{OH}	High-level output voltage, RESET			I_{OH} = –16 mA	V_{CC}–1.5			V
V_{OL}	Low-level output voltage, $\overline{\text{RESET}}$			I_{OL} = 16 mA			0.4	V
V_{ref}	Reference voltage, REF			I_{ref} = –500 µA, T_A = 25°C	2.48	2.53	2.58	V
V_{IT-}	Negative-going input threshold voltage at SENSE input		TL7702B	T_A = 25°C	2.505	2.53	2.555	V
			TL7705B		4.5	4.55	4.6	
			TL7702B	T_A = –55°C to 125°C	2.48	2.53	2.58	
			TL7705B		4.45	4.55	4.65	
V_{hys}	Hysteresis, SENSE (V_{IT+} – V_{IT-})		TL7702B	V_{CC} = 3.6 V to 18 V, T_A = 25°C		10		mV
			TL7705B			30		
V_{res}[‡]	Power-up reset voltage			I_{OL} at $\overline{\text{RESET}}$ = 2 mA, T_A = 25°C			1	V
I_I	Input current	$\overline{\text{RESIN}}$		V_I = 0.4 V to V_{CC}			–10	µA
		SENSE	TL7702B	V_I = V_{ref} to V_{CC} – 1.5 V		–0.1	–2	
I_{OH}	High-level output current, $\overline{\text{RESET}}$			V_O = 18 V			50	µA
I_{OL}	Low-level output current, RESET			V_O = 0			–50	µA
I_{CC}	Supply current			V_{SENSE} = 15 V, $\overline{\text{RESIN}}$ ≥ 2 V		1.8	3	mA
				V_{CC} = 18 V, T_A = –55°C to 125°C			4	

[†] All electrical characteristics are measured with 0.1-µF capacitors connected at REF, CT, and V_{CC} to GND.

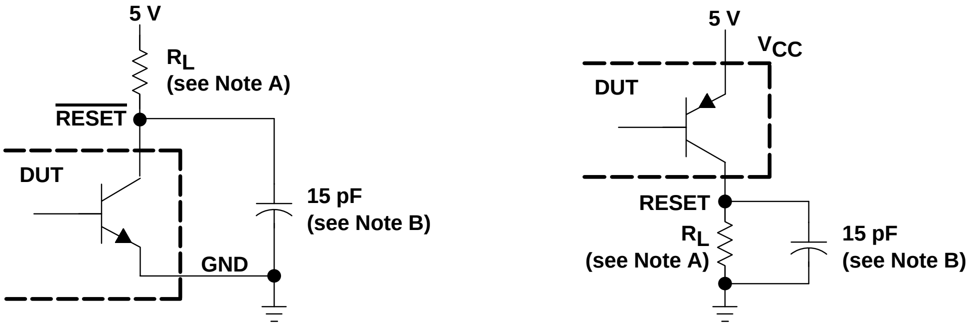
[‡] This is the lowest value at which $\overline{\text{RESET}}$ becomes active.

switching characteristics, V_{CC} = 5 V, C_T open, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TL7705BM			UNIT
					MIN	TYP	MAX	
t_{PLH}	Propagation delay time from low- to high-level output	$\overline{\text{RESIN}}$	RESET	See Figures 1, 2, and 3		270	500*	ns
t_{PHL}	Propagation delay time from high- to low-level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$	See Figures 1, 2, and 3		270	500*	ns
t_w	Effective pulse duration	$\overline{\text{RESIN}}$		See Figure 2	150			ns
		SENSE			100			
t_r	Rise time		RESET	See Figures 1 and 3			75*	ns
t_f	Fall time					150	200*	
t_r	Rise time		$\overline{\text{RESET}}$	See Figures 1 and 3		75	150*	ns
t_f	Fall time						50*	

* On products compliant to MIL-PRF-38535, these parameters are not production tested.

PARAMETER MEASUREMENT INFORMATION



$\overline{\text{RESET}}$ OUTPUT CONFIGURATION

RESET OUTPUT CONFIGURATION

NOTES: A. For I_{OL} and I_{OH}, R_L = 10 kΩ. For all switching characteristics, R_L = 511 Ω.
B. This figure includes jig and probe capacitance.

Figure 1. RESET and $\overline{\text{RESET}}$ Output Configurations

WAVEFORMS

Figure 2. Input Pulse Definition

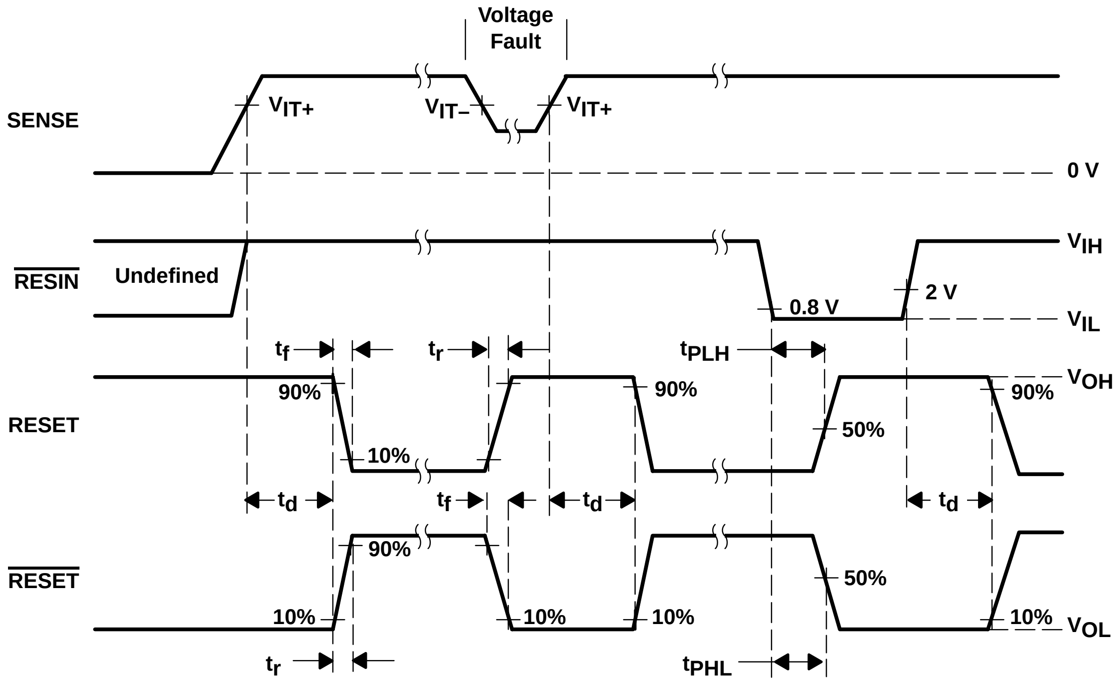


Figure 3. Voltage Waveforms

TYPICAL CHARACTERISTICS†

ASSERTION TIME vs LOAD RESISTANCE

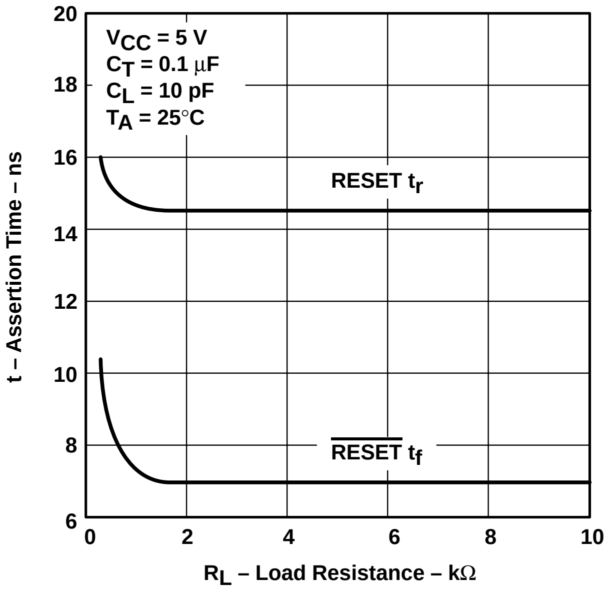


Figure 4

DEASSERTION TIME vs LOAD RESISTANCE

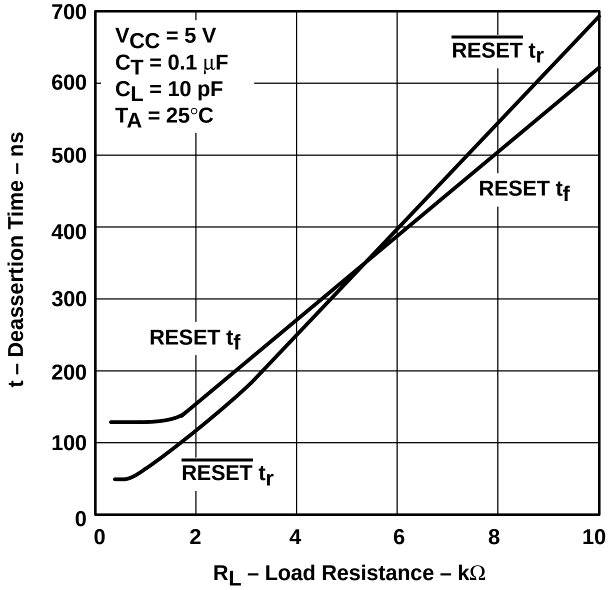


Figure 5

ASSERTION TIME vs LOAD CAPACITANCE

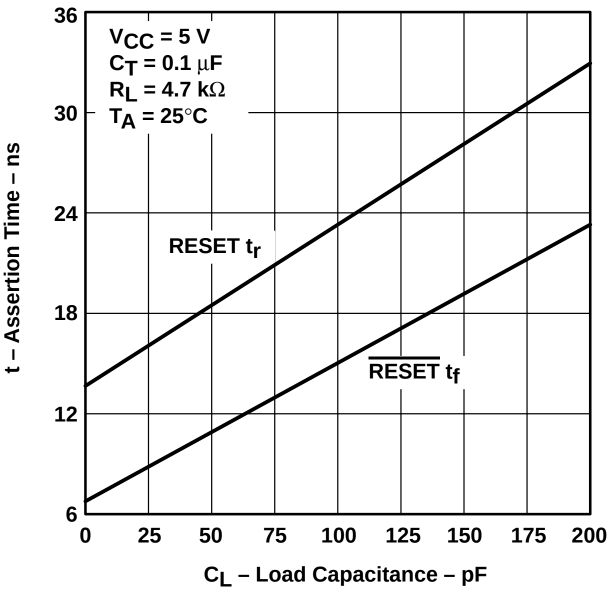


Figure 6

DEASSERTION TIME vs LOAD CAPACITANCE

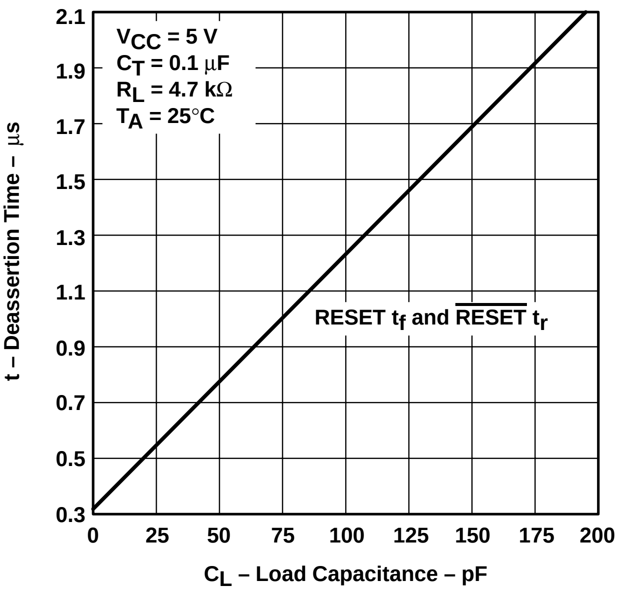


Figure 7

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† For proper operation, both RESET and $\overline{\text{RESET}}$ should be terminated with resistors of similar value. Failure to do so may cause unwanted plateauing in either output waveform during switching.

APPLICATION INFORMATION

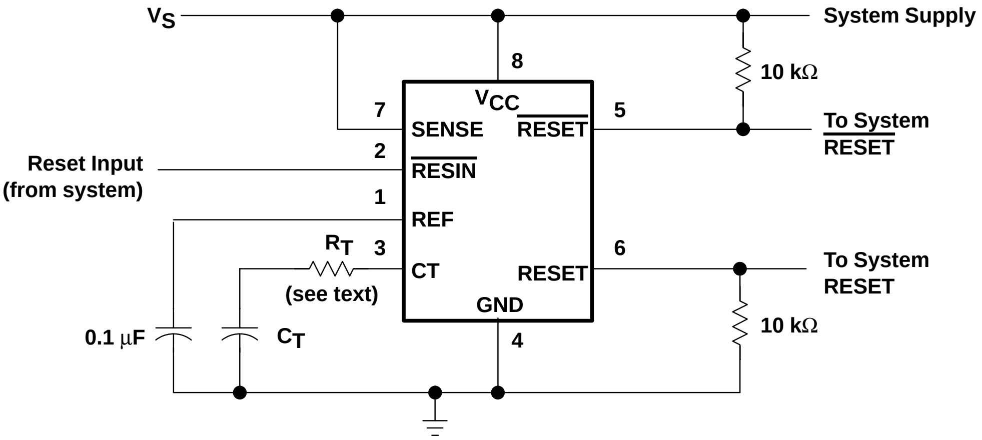

Figure 8. System Reset Controller With Undervoltage Sensing

When the TL770xB SENSE terminal is used to monitor V_{CC}, a current-limiting resistor in series with C_T is recommended. During normal operation, the timing capacitor is charged by the onboard current source to approximately V_{CC} or an internal voltage clamp (≈7.1-V Zener), whichever is less. When the circuit then is subjected to an undervoltage condition during which V_{CC} is rapidly slewed down, the voltage on CT exceeds that on V_{CC}. This forward biases a secondary path internally, which falsely activates the outputs. A fault is indicated when V_{CC} drops below $V_{(CT)}$, not when V_{SENSE} falls below V_{T-}.

Texas Instruments performs a 100% electrical screen to verify that the outputs do not switch with 1 mA forced into the CT terminal. Adding the external resistor, R_T, prevents false triggering. Its value is calculated as follows:

$$\frac{V_{(CT)} - V_{T-}}{R_T}$$

Where:

$V_{(CT)}$ = V_{CC} or 7.1 V, whichever is less
V_{T-} = 4.55 V (nom)
R_T = value of series resistor required

For V_{CC} = 5 V:

$$\frac{5 - 4.55}{R_T} < 1 \text{ mA}$$

Therefore,

$$R_T > 450\ \Omega$$

Using a 20%-tolerance resistor, R_T should be greater than 560 Ω.

Adding this series resistor changes the duration of the reset pulse by no more than 10%. R_T extends the discharge of C_T, but also skews the $V_{(CT)}$ threshold. These effects tend to cancel one another. The precise percentage change can be derived theoretically, but the equation is complicated by this interaction and is dependent upon the duration of the supply-voltage fault condition.

Both outputs of the TL770xB should be terminated with similar value resistors, even when only one is being used. This prevents unwanted plateauing in either output waveform during switching, which may be interpreted as an undefined state or delay system reset.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-88685042A	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
5962-8868504HA	OBSOLETE	CFP	U	10		TBD	Call TI	Call TI	-55 to 125		
5962-88685052A	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
5962-8868505HA	OBSOLETE	CFP	U	10		TBD	Call TI	Call TI	-55 to 125		
5962-8868505PA	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	-55 to 125		
TL7702BCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7702BC	Samples
TL7702BCDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7702BC	Samples
TL7702BCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7702BC	Samples
TL7702BCDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7702BC	Samples
TL7702BCDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7702BC	Samples
TL7702BCP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL7702BCP	Samples
TL7702BCPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL7702BCP	Samples
TL7702BID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7702BI	Samples
TL7702BIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7702BI	Samples
TL7702BIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7702BI	Samples
TL7702BIDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7702BI	Samples
TL7702BIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7702BI	Samples
TL7702BIP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL7702BIP	Samples
TL7702BMFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
TL7702BMJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	-55 to 125		

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL7702BMJGB	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	-55 to 125		
TL7702BMUB	OBSOLETE	CFP	U	10		TBD	Call TI	Call TI	-55 to 125		
TL7702BQD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125		
TL7702BQDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125		
TL7702BQP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	-40 to 125		
TL7705BCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	7705BC	Samples
TL7705BCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	7705BC	Samples
TL7705BCDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	7705BC	Samples
TL7705BCDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	7705BC	Samples
TL7705BCP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL7705BCP	Samples
TL7705BID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	7705BI	Samples
TL7705BIDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	7705BI	Samples
TL7705BIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	7705BI	Samples
TL7705BIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	7705BI	Samples
TL7705BIP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL7705BIP	Samples
TL7705BMFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
TL7705BMJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	-55 to 125		
TL7705BMJGB	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	-55 to 125		
TL7705BMUB	OBSOLETE	CFP	U	10		TBD	Call TI	Call TI	-55 to 125		
TL7705BQD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7705BQ	Samples
TL7705BQDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		7705BQ	Samples
TL7705BQDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7705BQ	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL7705BQDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		7705BQ	Samples
TL7705BQP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	-40 to 125		
TL7733BCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7733BC	Samples
TL7733BCDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7733BC	Samples
TL7733BCDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7733BC	Samples
TL7733BCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7733BC	Samples
TL7733BCDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7733BC	Samples
TL7733BCP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL7733BCP	Samples
TL7733BID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7733BI	Samples
TL7733BIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7733BI	Samples
TL7733BIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7733BI	Samples
TL7733BIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7733BI	Samples
TL7733BIP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL7733BIP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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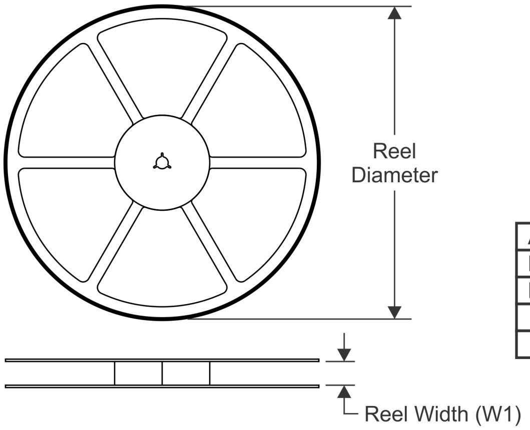
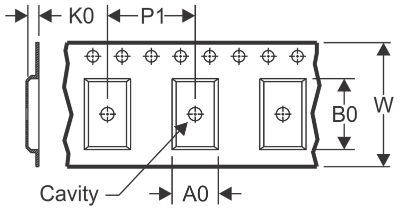
TAPE AND REEL INFORMATION

REEL DIMENSIONS

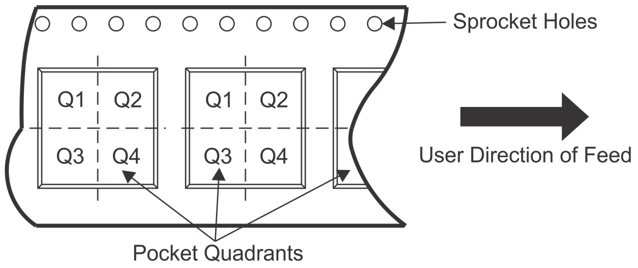


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

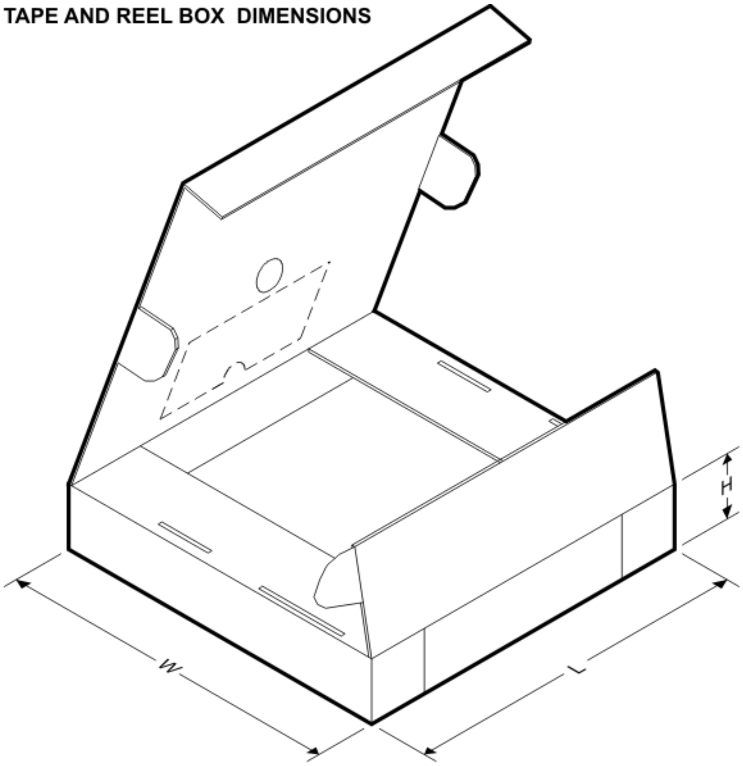
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL7702BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7702BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7705BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7705BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7705BQDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7705BQDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7733BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7733BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

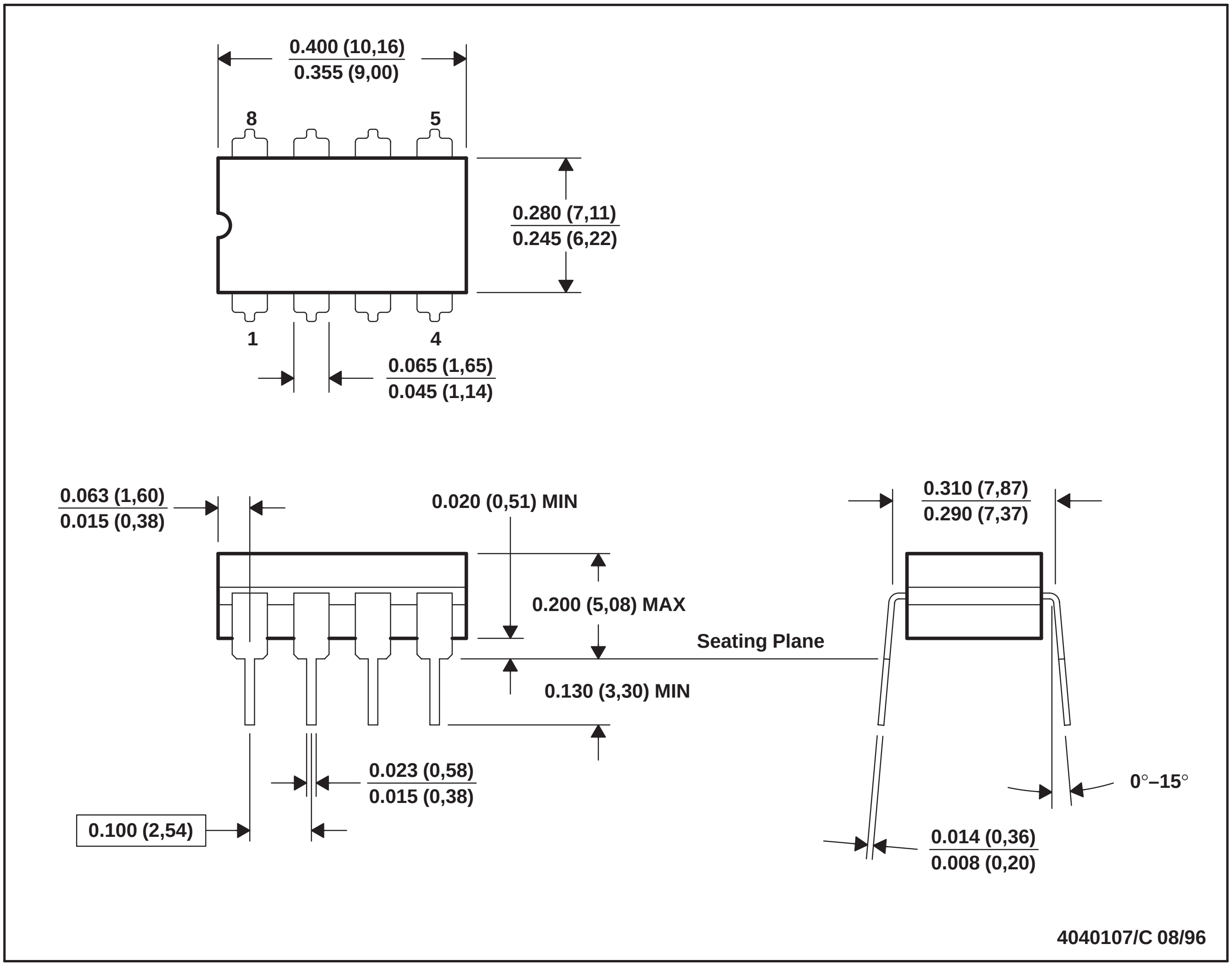
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

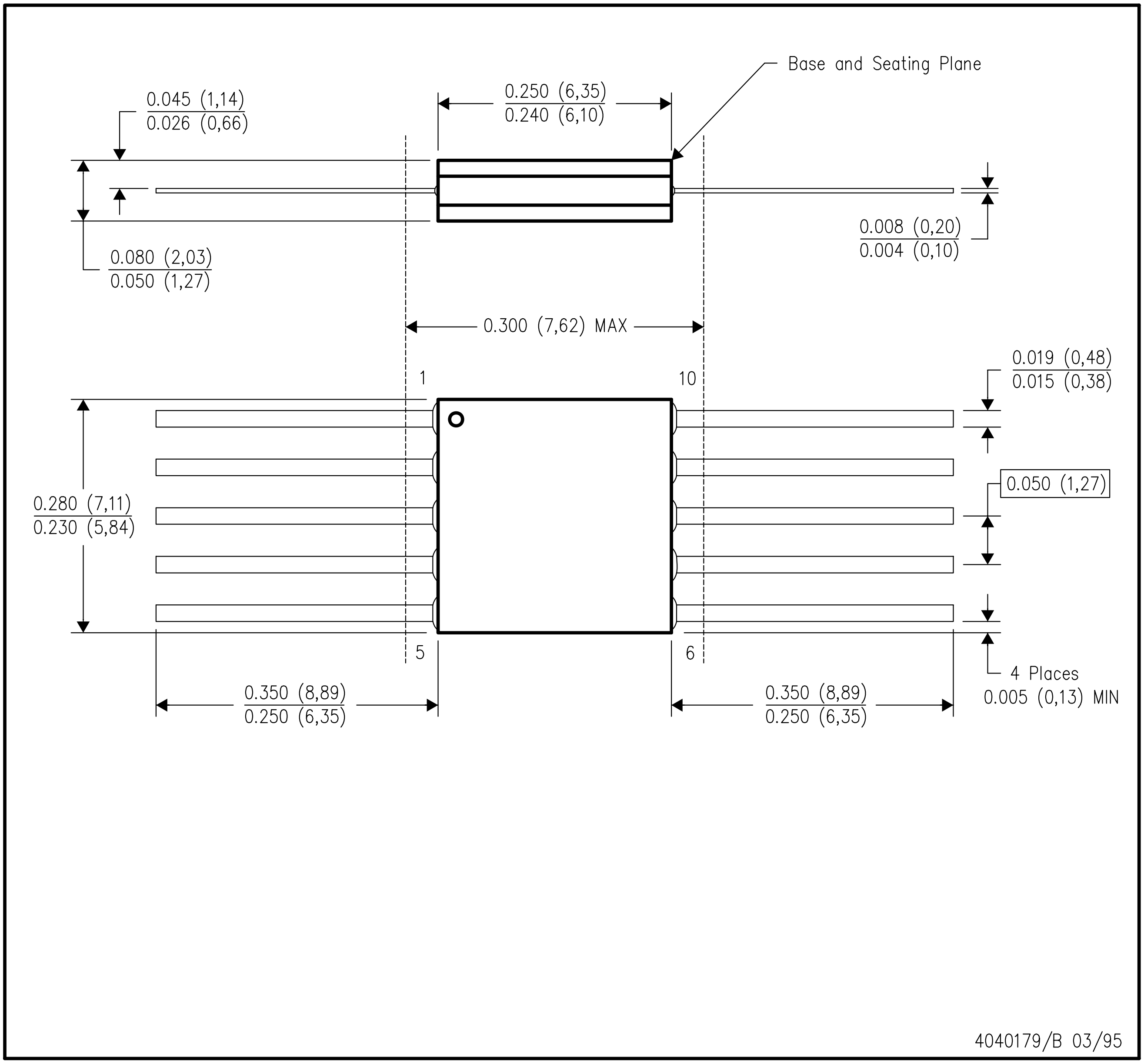
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL7702BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TL7702BIDR	SOIC	D	8	2500	340.5	338.1	20.6
TL7705BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TL7705BIDR	SOIC	D	8	2500	340.5	338.1	20.6
TL7705BQDR	SOIC	D	8	2500	367.0	367.0	35.0
TL7705BQDRG4	SOIC	D	8	2500	367.0	367.0	35.0
TL7733BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TL7733BIDR	SOIC	D	8	2500	340.5	338.1	20.6

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification.
- E. Falls within MIL STD 1835 GDIP1-T8

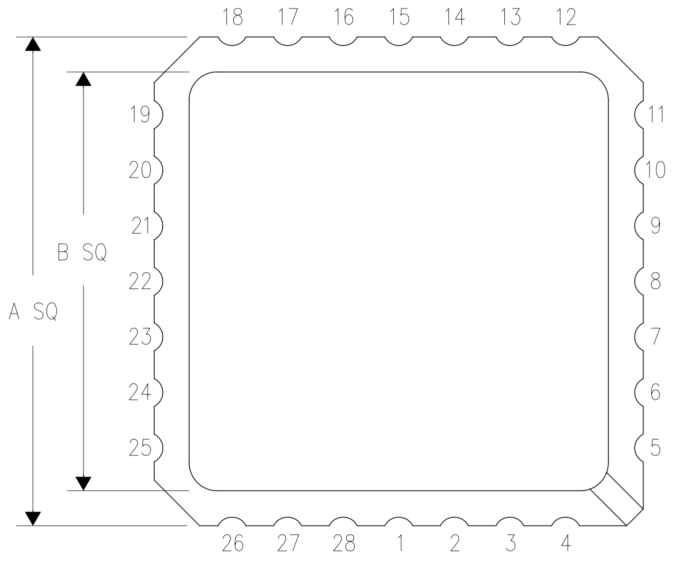
U (S–GDFP–F10) CERAMIC DUAL FLATPACK



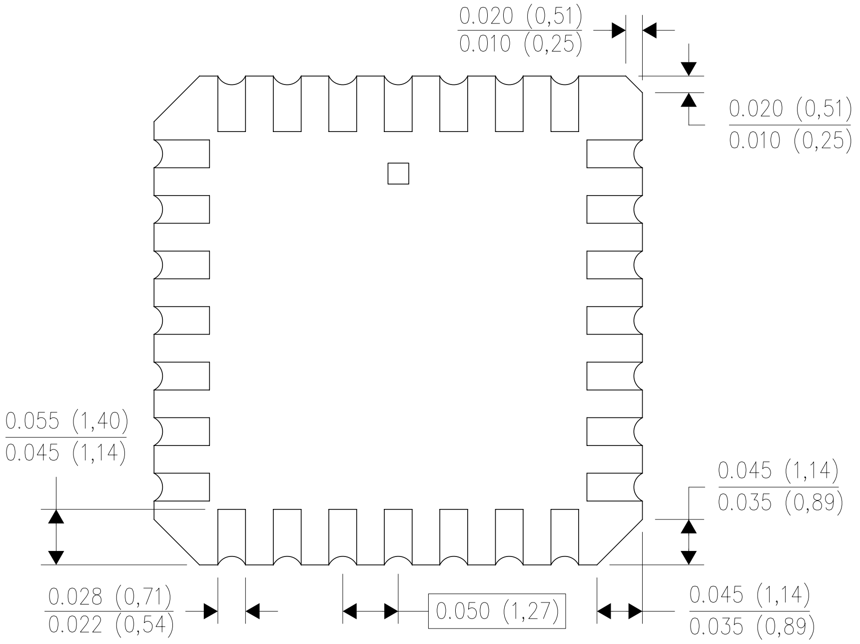
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1–F10 and JEDEC MO–092AA

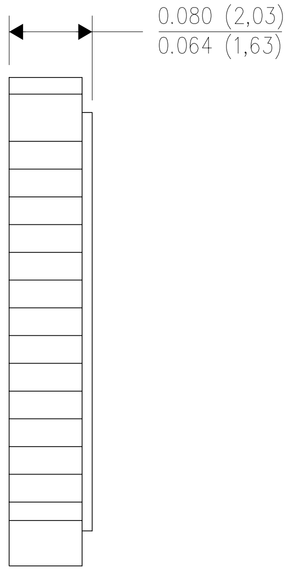
FK (S-CQCC-N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

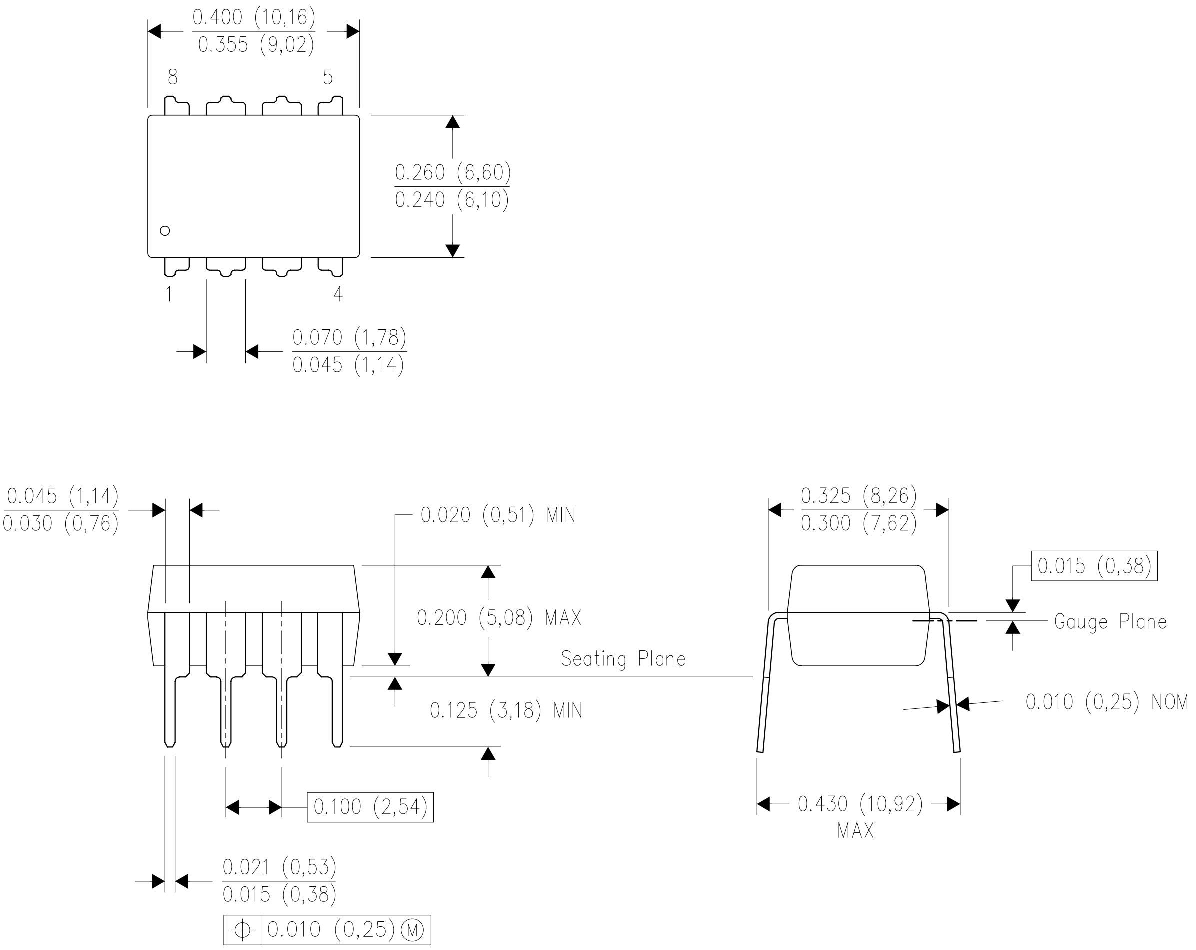




4040140/D 01/11

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

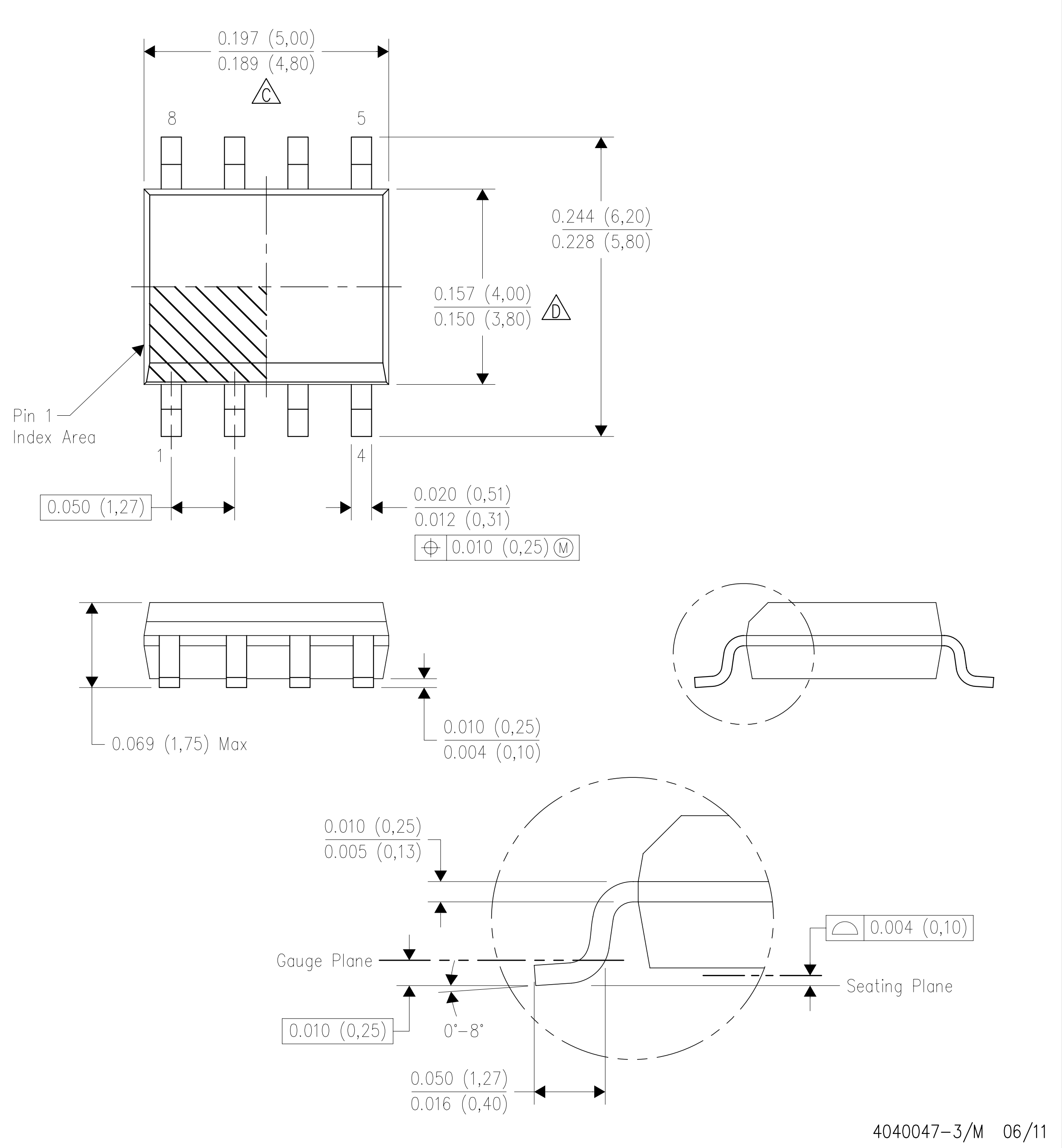
P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



4040082/E 04/2010

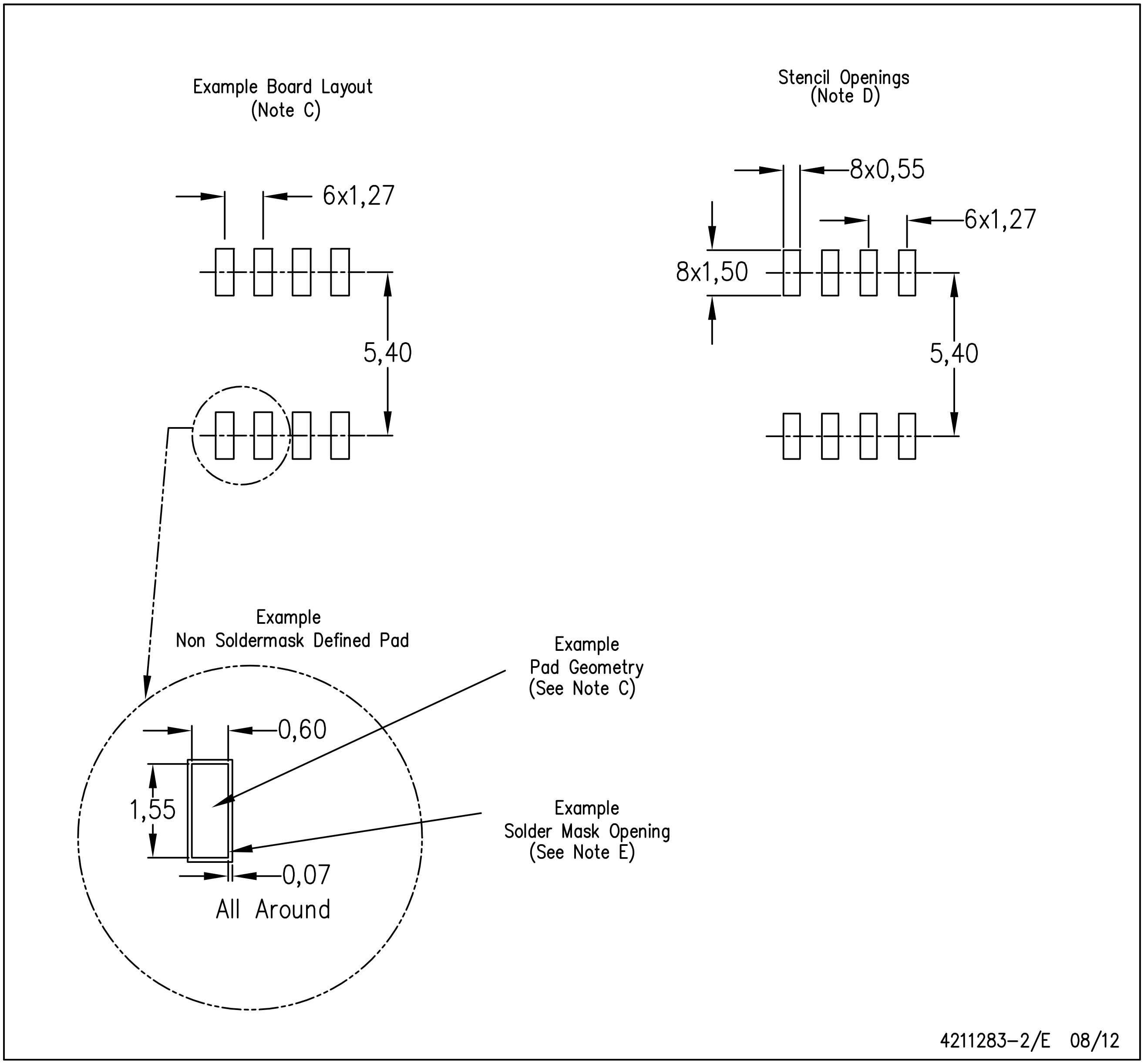
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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