

MX25U12835F

1.8V, 128M-BIT [x 1/x 2/x 4]
CMOS MXSMIO[®] (SERIAL MULTI I/O)
FLASH MEMORY

Key Features

- 1.65 to 2.0 volt for read, erase, and program operations
- Multi I/O Support - Single I/O, Dual I/O and Quad I/O
- Quad Peripheral Interface (QPI) Read / Program Mode
- Program Suspend/Resume & Erase Suspend/Resume
- 23-ball WLCSP (Ball Diameter 0.30mm)

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**1.8V 128M-BIT [x 1/x 2/x 4] CMOS MXSMIO® (SERIAL MULTI I/O)
FLASH MEMORY****1. FEATURES****GENERAL**

- Supports Serial Peripheral Interface -- Mode 0 and Mode 3
- 134,217,728 x 1 bit structure or 67,108,864 x 2 bits (two I/O mode) structure or 33,554,432 x 4 bits (four I/O mode) structure
- Equal Sectors with 4K byte each, or Equal Blocks with 32K byte each or Equal Blocks with 64K byte each
 - Any Block can be erased individually
- Single Power Supply Operation
 - 1.65 to 2.0 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V
- Low Vcc write inhibit is from 1.0V to 1.4V

PERFORMANCE

- High Performance
 - Fast read for SPI mode
 - 1 I/O: 104MHz with 8 dummy cycles
 - 2 I/O: 84MHz with 4 dummy cycles, equivalent to 168MHz
 - 4 I/O: 104MHz with 2+4 dummy cycles, equivalent to 416MHz
 - 4 I/O: 133MHz with 2+6 dummy cycles, equivalent to 532MHz (for MX25U12835FZNI-08G only)
 - Fast read for QPI mode
 - 4 I/O: 84MHz with 2+2 dummy cycles, equivalent to 336MHz
 - 4 I/O: 104MHz with 2+4 dummy cycles, equivalent to 416MHz
 - 4 I/O: 133MHz with 2+6 dummy cycles, equivalent to 532MHz (for MX25U12835FZNI-08G only)
 - Fast program time:
0.5ms(typ.) and 3ms(max.)/page (256-byte per page)
 - Byte program time: 12us (typical)
 - 8/16/32/64 byte Wrap-Around Burst Read Mode
 - Fast erase time:
 - 35ms (typ.)/sector (4K-byte per sector);
 - 200ms(typ.)/block (32K-byte per block),
 - 350ms(typ.) /block (64K-byte per block)
- Low Power Consumption
 - Low active read current:
 - 20mA(typ.) at 104MHz,
 - 15mA(typ.) at 84MHz,
 - 27mA(typ.) at 133MHz(for MX25U12835FZNI-08G only)
 - Low active erase current:
 - 18mA (typ.)
 - at Sector Erase, Block Erase (32KB/64KB);
 - 20mA at Chip Erase
 - Low active programming current: 20mA (typ.)
 - Standby current: 15uA (typ.)

- Deep Power Down: 1.5uA(typ.)
- Typical 100,000 erase/program cycles
- 20 years data retention

SOFTWARE FEATURES

- Input Data Format
 - 1-byte Command code
- Advanced Security Features
 - Block lock protection
 - The BP0-BP3 status bit defines the size of the area to be software protection against program and erase instructions
 - Additional 4k-bit secured OTP for unique identifier
- Auto Erase and Auto Program Algorithm
 - Automatically erases and verifies data at selected sector or block
 - Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse widths (Any page to be programmed should have page in the erased state first)
- Status Register Feature
- Command Reset
- Program/Erase Suspend
- Electronic Identification
 - JEDEC 1-byte manufacturer ID and 2-byte device ID
 - RES command for 1-byte Device ID
 - REMS command for 1-byte manufacturer ID and 1-byte device ID
- Support Serial Flash Discoverable Parameters (SFDP) mode

HARDWARE FEATURES

- SCLK Input - Serial clock input
- SI/SIO0 - Serial Data Input or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- SO/SIO1 - Serial Data Output or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- WP#/SIO2 - Hardware write protection or serial data Input/Output for 4 x I/O read mode
- RESET#/SIO3 - Hardware Reset pin or Serial input & Output for 4 x I/O read mode

- PACKAGE
 - 16-pin SOP (300mil)
 - 8-land WSON (6x5mm)
 - 8-land WSON (8x6mm)
 - 23-ball WLCSP (Ball Diameter 0.30mm)
 - 8-pin SOP (200mil)
 - 24-Ball BGA (5x5 ball array)

All devices are RoHS Compliant and Halogen-free

2. GENERAL DESCRIPTION

MX25U12835F is 128Mb bits Serial NOR Flash memory, which is configured as 16,777,216 x 8 internally. When it is in two or four I/O mode, the structure becomes 67,108,864 bits x 2 or 33,554,432 bits x 4.

MX25U12835F features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

When it is in two I/O read mode, the SI pin and SO pin become SIO0 pin and SIO1 pin for address/dummy bits input and data output. When it is in four I/O read mode, the SI pin, SO pin, WP# pin and RESET# pin become SIO0 pin, SIO1 pin, SIO2 pin and SIO3 pin for address/dummy bits input and data output.

The MX25U12835F MXSMIO® (Serial Multi I/O) provides sequential read operation on the whole chip.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, or word basis. Erase command is executed on 4K-byte sector, 32K-byte block, or 64K-byte block, or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

Advanced security features enhance the protection and security functions, please refer to security features section for more details.

The MX25U12835F utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

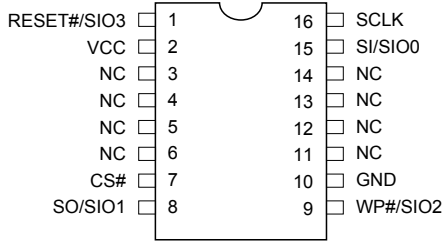
Table 1. Read Performance

| MX25U12835F | Read Performance | | | | | | | | |
|-------------|------------------|--------|--------|--------|---------|----------|--------|---------|----------|
| | SPI | | | | | | QPI | | |
| I/O | 1 I/O | 1I /2O | 2 I/O | 1I/4O | 4 I/O | 4 I/O | 4 I/O | 4 I/O | 4 I/O |
| Dummy Cycle | 8 | 8 | 4 | 8 | 6 | 8 | 4 | 6 | 8 |
| MHz | 104 MHz | 104MHz | 84 MHz | 104MHz | 104 MHz | 133 MHz* | 84 MHz | 104 MHz | 133 MHz* |

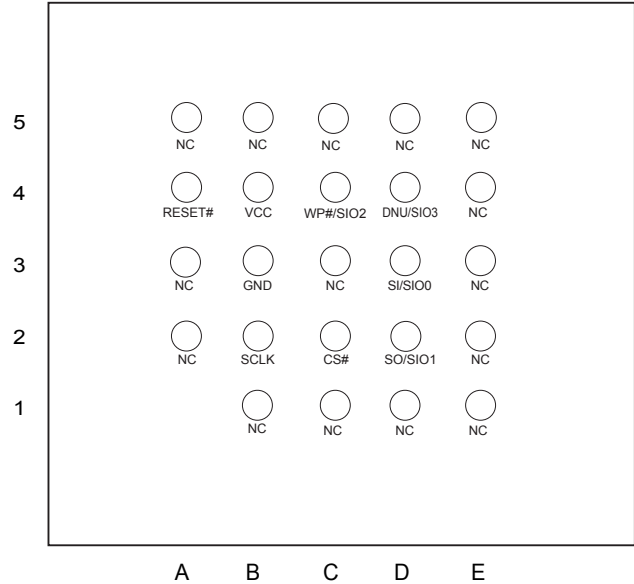
* For MX25U12835FZNI-08G only

3. PIN CONFIGURATIONS

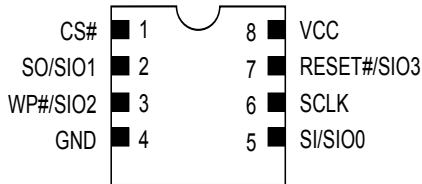
16-PIN SOP (300mil)



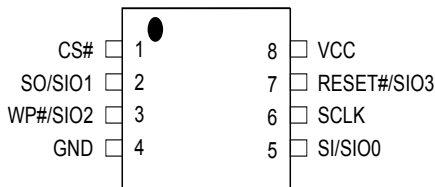
24-BALL BGA (5x5 ball array)



8-WSON (6x5mm, 8x6mm)



8-PIN SOP (200mil)



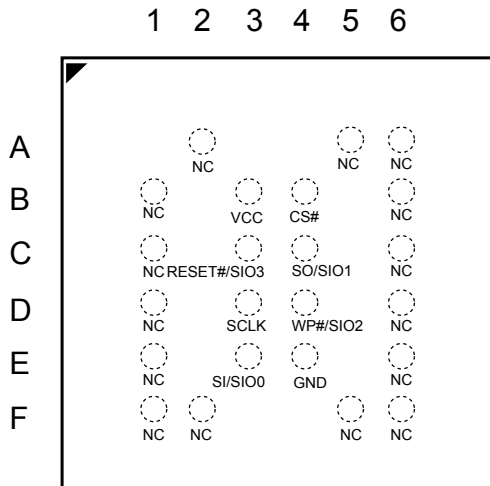
4. PIN DESCRIPTION

| Symbol | Description |
|------------------------------------|---|
| CS# | Chip Select |
| SI/SIO0 | Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode) |
| SO/SIO1 | Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode) |
| SCLK | Clock Input |
| WP#/SIO2 | Write Protection Active low or Serial Data Input & Output (for 4xI/O read mode) ^{Note 1} |
| RESET#/SIO3 | Hardware Reset Pin Active low or Serial Data Input & Output (for 4xI/O read mode) ^{Note 1} |
| DNU/SIO3 ^{Note 2} (24BGA) | Do Not Use or Serial Data Input & Output (for 4xI/O read mode) |
| VCC | + 1.8V Power Supply |
| GND | Ground |

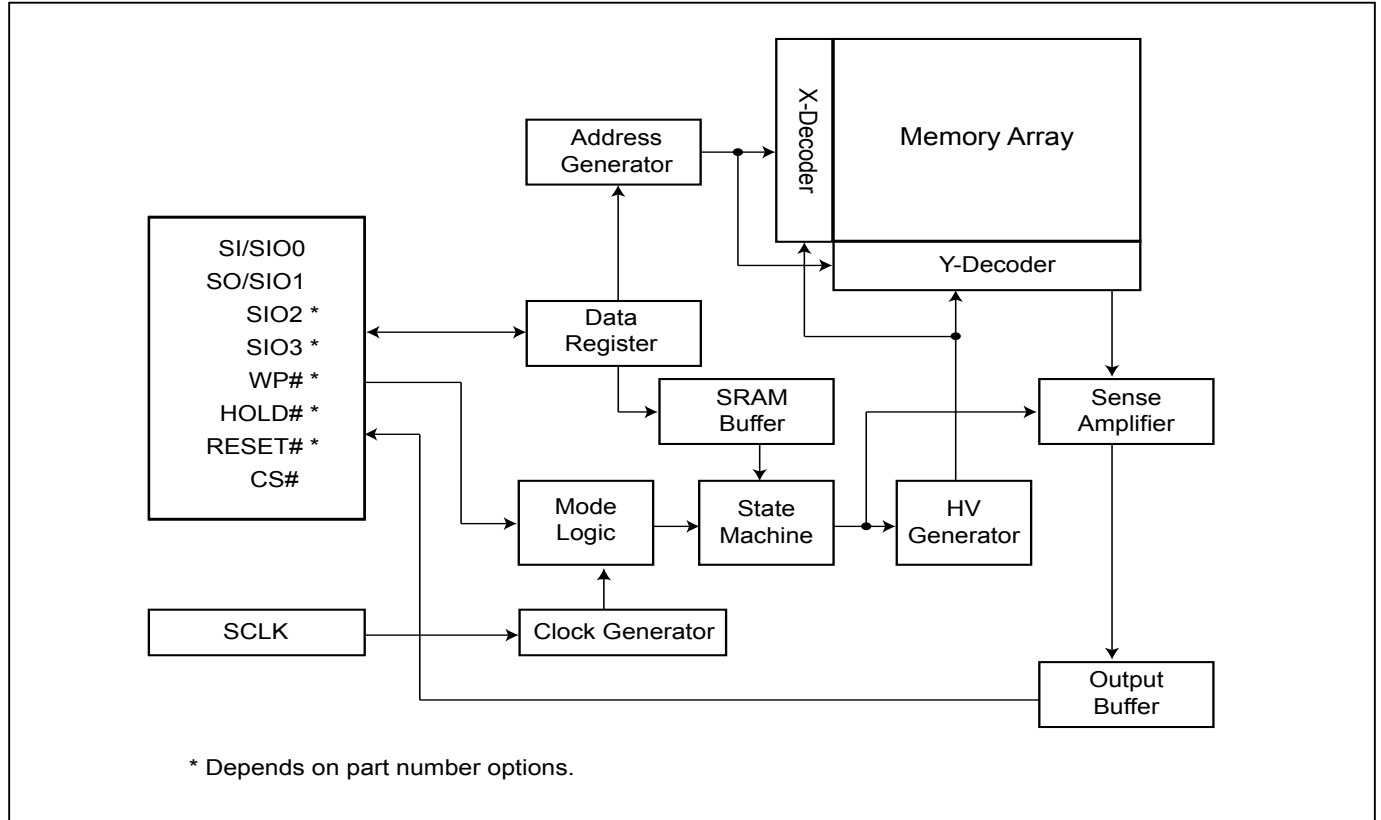
Notes:

- When using 1 I/O or 2 I/O (QE bit not enabled), the DNU/SIO3 pin of 24BGA can not connect to GND. We suggest user to connect this pin to VCC or floating.
- The pin of RESET#/SIO3 or WP#/SIO2 will remain internal pull up function while this pin is not physically connected in system configuration. However, the internal pull up function will be disabled if the system has physical connection to RESET#/SIO3 or WP#/SIO2 pin.

23-BALL BGA (WLCSP) TOP View



5. BLOCK DIAGRAM



6. DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.
- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before other command to change data.
- Deep Power Down Mode: By entering deep power down mode, the flash device is under protected from writing all commands except Release from deep power down mode command (RDP) and Read Electronic Signature command (RES) and softreset command.
- Advanced Security Features: there are some protection and security features which protect content from inadvertent write and hostile access.

I. Block lock protection

- The Software Protected Mode (SPM) use (BP3, BP2, BP1, BP0) bits to allow part of memory to be protected as read only. The protected area definition is shown as "[Table 2. Protected Area Sizes](#)", the protected areas are more flexible which may protect various area by setting value of BP0-BP3 bits.
- The Hardware Protected Mode (HPM) use WP#/SIO2 to protect the (BP3, BP2, BP1, BP0) bits and Status Register Write Protect bit.
- In four I/O and QPI mode, the feature of HPM will be disabled.

Table 2. Protected Area Sizes

Protected Area Sizes (T/B bit = 0)

| Status bit | | | | Protect Level |
|------------|-----|-----|-----|---|
| BP3 | BP2 | BP1 | BP0 | 128Mb |
| 0 | 0 | 0 | 0 | 0 (none) |
| 0 | 0 | 0 | 1 | 1 (1 block, protected block 255 th) |
| 0 | 0 | 1 | 0 | 2 (2 blocks, protected block 254 th -255 th) |
| 0 | 0 | 1 | 1 | 3 (4 blocks, protected block 252 nd -255 th) |
| 0 | 1 | 0 | 0 | 4 (8 blocks, protected block 248 th -255 th) |
| 0 | 1 | 0 | 1 | 5 (16 blocks, protected block 240 th -255 th) |
| 0 | 1 | 1 | 0 | 6 (32 blocks, protected block 224 th -255 th) |
| 0 | 1 | 1 | 1 | 7 (64 blocks, protected block 192 nd -255 th) |
| 1 | 0 | 0 | 0 | 8 (128 blocks, protected block 128 th -255 th) |
| 1 | 0 | 0 | 1 | 9 (256 blocks, protected all) |
| 1 | 0 | 1 | 0 | 10 (256 blocks, protected all) |
| 1 | 0 | 1 | 1 | 11 (256 blocks, protected all) |
| 1 | 1 | 0 | 0 | 12 (256 blocks, protected all) |
| 1 | 1 | 0 | 1 | 13 (256 blocks, protected all) |
| 1 | 1 | 1 | 0 | 14 (256 blocks, protected all) |
| 1 | 1 | 1 | 1 | 15 (256 blocks, protected all) |

Protected Area Sizes (T/B bit = 1)

| Status bit | | | | Protect Level |
|------------|-----|-----|-----|---|
| BP3 | BP2 | BP1 | BP0 | 128Mb |
| 0 | 0 | 0 | 0 | 0 (none) |
| 0 | 0 | 0 | 1 | 1 (1 block, protected block 0 th) |
| 0 | 0 | 1 | 0 | 2 (2 blocks, protected block 0 th -1 st) |
| 0 | 0 | 1 | 1 | 3 (4 blocks, protected block 0 th -3 rd) |
| 0 | 1 | 0 | 0 | 4 (8 blocks, protected block 0 th -7 th) |
| 0 | 1 | 0 | 1 | 5 (16 blocks, protected block 0 th -15 th) |
| 0 | 1 | 1 | 0 | 6 (32 blocks, protected block 0 th -31 st) |
| 0 | 1 | 1 | 1 | 7 (64 blocks, protected block 0 th -63 rd) |
| 1 | 0 | 0 | 0 | 8 (128 blocks, protected block 0 th -127 th) |
| 1 | 0 | 0 | 1 | 9 (256 blocks, protected all) |
| 1 | 0 | 1 | 0 | 10 (256 blocks, protected all) |
| 1 | 0 | 1 | 1 | 11 (256 blocks, protected all) |
| 1 | 1 | 0 | 0 | 12 (256 blocks, protected all) |
| 1 | 1 | 0 | 1 | 13 (256 blocks, protected all) |
| 1 | 1 | 1 | 0 | 14 (256 blocks, protected all) |
| 1 | 1 | 1 | 1 | 15 (256 blocks, protected all) |

II. Additional 4K-bit secured OTP for unique identifier: to provide 4K-bit one-time program area for setting device unique serial number - Which may be set by factory or system customer.

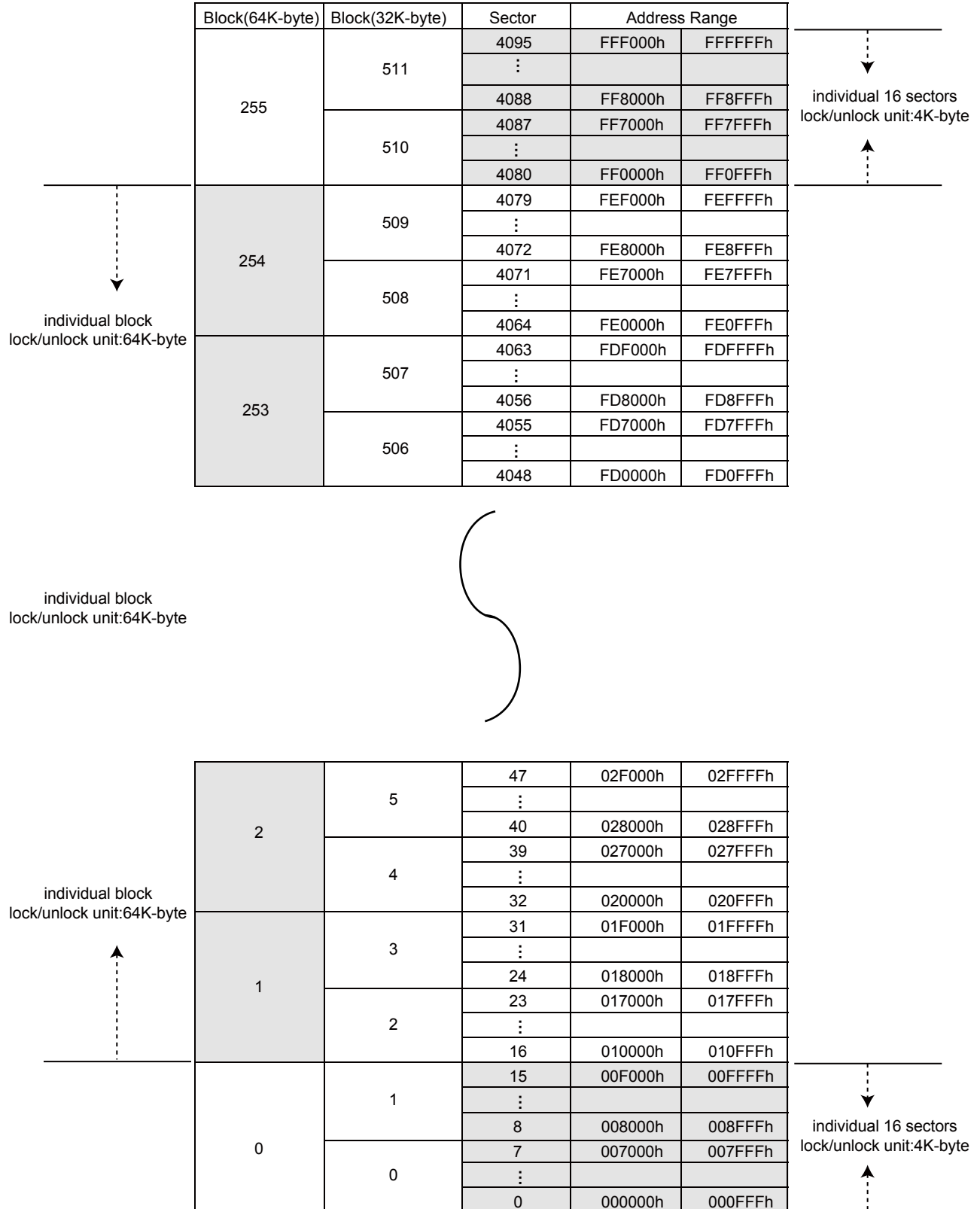
- Security register bit 0 indicates whether the secured OTP area is locked by factory or not.
- To program the 4K-bit secured OTP by entering 4K-bit secured OTP mode (with Enter Security OTP command), and going through normal program procedure, and then exiting 4K-bit secured OTP mode by writing Exit Security OTP command.
- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to "[Table 9. Security Register Definition](#)" for security register bit definition and "[Table 3. 4K-bit Secured OTP Definition](#)" for address range definition.
- Note: Once lock-down whatever by factory or customer, it cannot be changed any more. While in 4K-bit secured OTP mode, array access is not allowed.

Table 3. 4K-bit Secured OTP Definition

| Address range | Size | Standard Factory Lock | Customer Lock |
|-----------------|----------|--------------------------------|------------------------|
| xxx000 - xxx00F | 128-bit | ESN (electrical serial number) | Determined by customer |
| xxx010 - xxx1FF | 3968-bit | N/A | |

7. Memory Organization

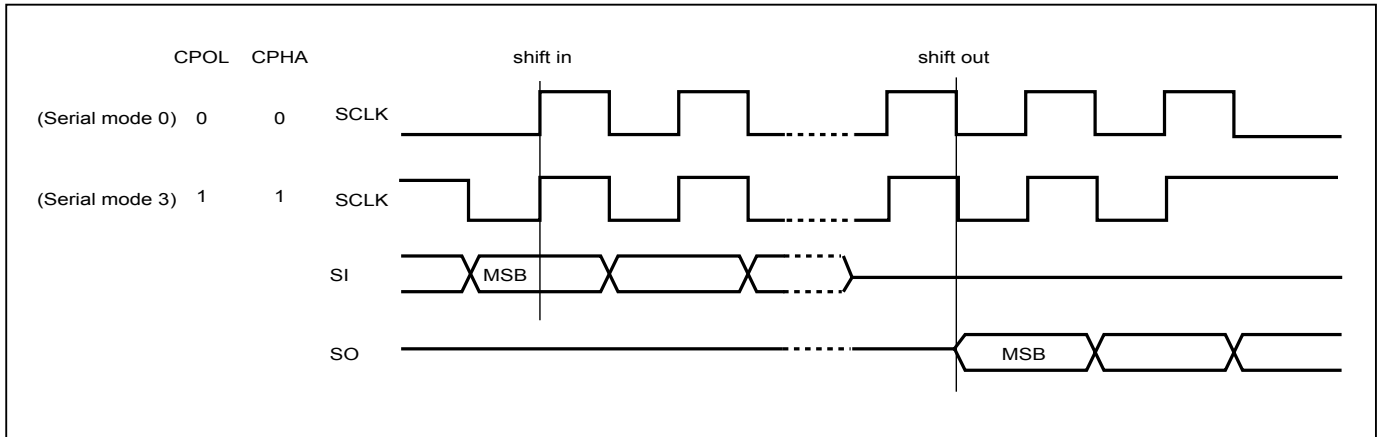
Table 4. Memory Organization



8. DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.
2. When incorrect command is inputted to this device, this device becomes standby mode and keeps the standby mode until next CS# falling edge. In standby mode, SO pin of this device should be High-Z.
3. When correct command is inputted to this device, this device becomes active mode and keeps the active mode until next CS# rising edge.
4. Input data is latched on the rising edge of Serial Clock (SCLK) and data shifts out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as "Figure 1. Serial Modes Supported".
5. For the following instructions: RDID, RDSR, RDSCUR, READ, FAST_READ, DREAD, 2READ, QREAD, 4READ, W4READ, RDSFDP, RES, REMS, QPIID, RDBLOCK, the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE32K, BE, CE, PP, 4PP, DP, ENSO, EXSO, WRSCUR, WPSEL, SBLK, SBULK, GBULK, SUSPEND, RESUME, NOP, RSTEN, RST, EQIO, RSTQIO the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.
6. During the progress of Write Status Register, Program, Erase operation, to access the memory array is neglected and not affect the current operation of Write Status Register, Program, Erase.

Figure 1. Serial Modes Supported



Note:

CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

Figure 2. Serial Input Timing

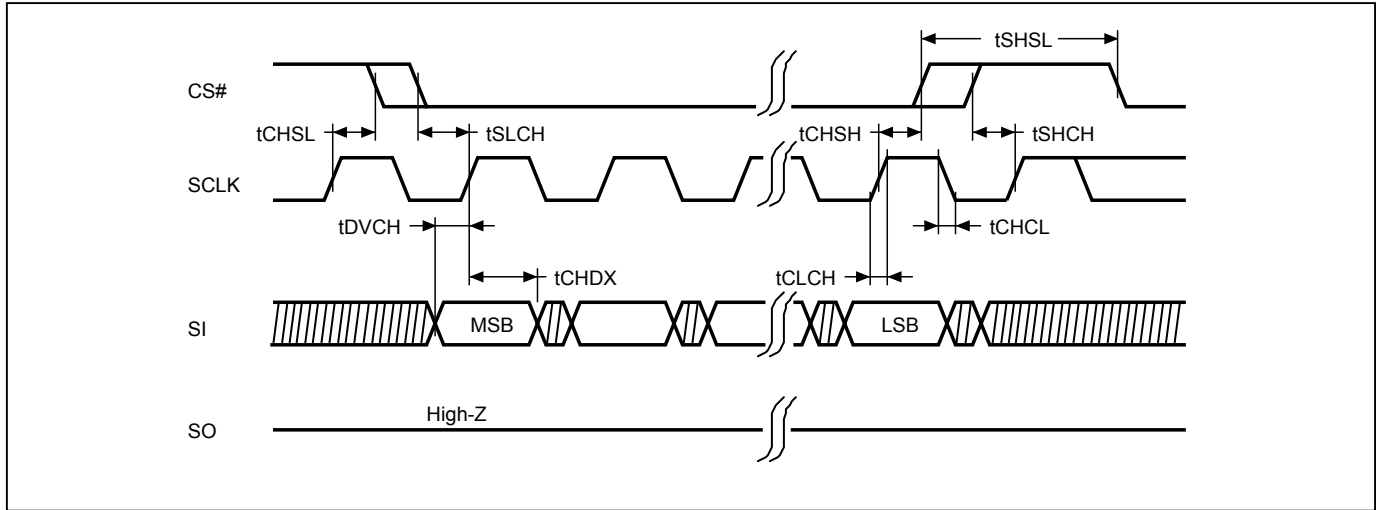
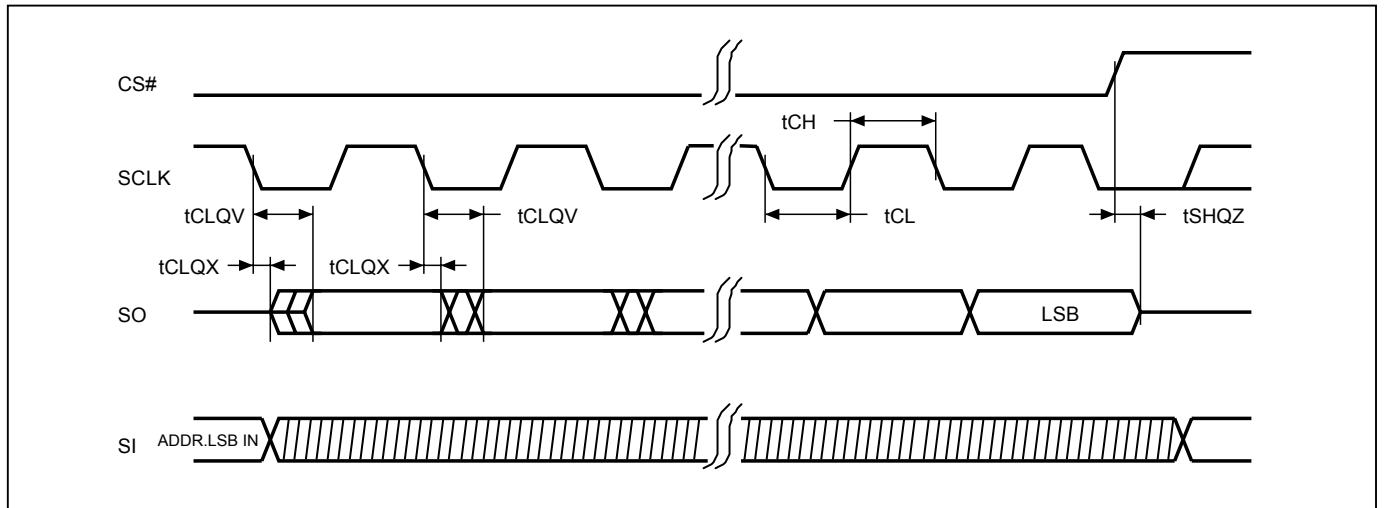


Figure 3. Output Timing



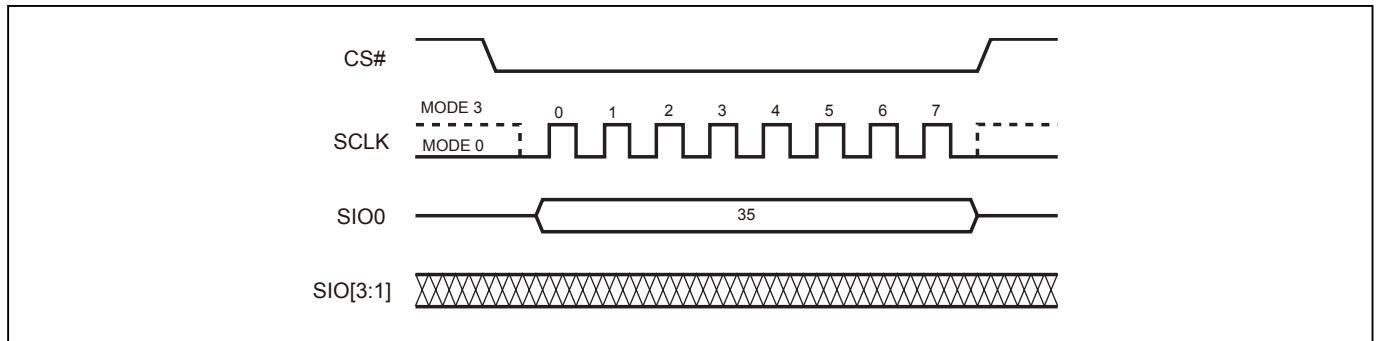
8-1. Quad Peripheral Interface (QPI) Read Mode

QPI protocol enables user to take full advantage of Quad I/O Serial NOR Flash by providing the Quad I/O interface in command cycles, address cycles and as well as data output cycles.

Enable QPI mode

By issuing EQIO command (35h), the QPI mode is enabled.

Figure 4. Enable QPI Sequence (Command 35h)



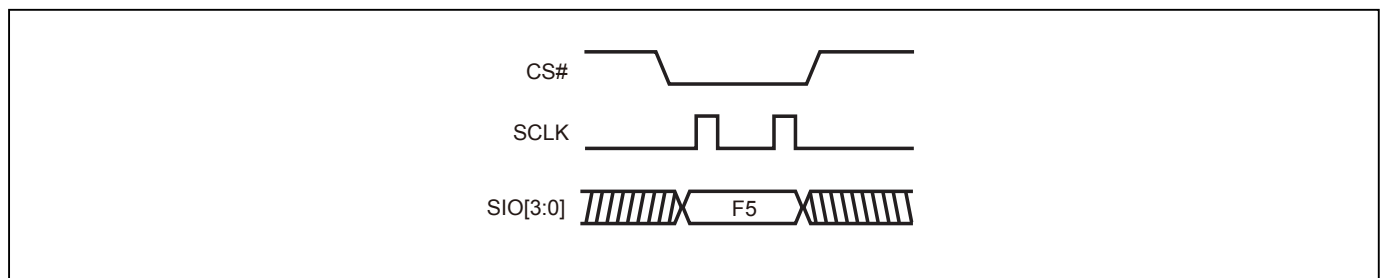
Reset QPI (RSTQIO)

To reset the QPI mode, the RSTQIO (F5h) command is required. After the RSTQIO command is issued, the device returns from QPI mode (4 I/O interface in command cycles) to SPI mode (1 I/O interface in command cycles).

Note:

For EQIO and RSTQIO commands, CS# high width has to follow "write spec" tSHSL (as defined in ["Table 19. AC Characteristics"](#)) for next instruction.

Figure 5. Reset QPI Mode (Command F5h)



9. COMMAND DESCRIPTION

Table 5. Command Set

Read/Write Array Commands

| Mode | SPI | SPI/QPI | SPI | SPI | SPI/QPI | SPI/QPI |
|----------------------|--|--|--|---|---|--|
| Command (byte) | READ (normal read) | FAST READ (fast read data) | DREAD (1I / 2O read command) | 2READ (2 x I/O read command) | 4READ (4 x I/O read) | 4READ (4 x I/O read) |
| 1 st byte | 03 (hex) | 0B (hex) | 3B (hex) | BB (hex) | EB (hex) | EB (hex) |
| 2 nd byte | ADD1(8) ^(Note 4) | ADD1(8) | ADD1(8) | ADD1(4) | ADD1(2) | ADD1(2) |
| 3 rd byte | ADD2(8) | ADD2(8) | ADD2(8) | ADD2(4) | ADD2(2) | ADD2(2) |
| 4 th byte | ADD3(8) | ADD3(8) | ADD3(8) | ADD3(4) | ADD3(2) | ADD3(2) |
| 5 th byte | | Dummy(8)/(4) <i>(Note 1)</i> | Dummy(8) | Dummy(4) ^(Note 3) | Dummy(6) | Dummy ^(Note 2) |
| Action | n bytes read out until CS# goes high | n bytes read out until CS# goes high | n bytes read out by Dual Output until CS# goes high | n bytes read out by 2 x I/O until CS# goes high | Quad I/O read with 6 dummy cycles | Quad I/O read with configurable dummy cycles |

| Mode | SPI | SPI | SPI/QPI | SPI | SPI/QPI | SPI/QPI |
|----------------------|---|--|---------------------------------|---|---------------------------------|---------------------------------------|
| Command (byte) | W4READ | QREAD (1I/4O read) | PP (page program) | 4PP (quad page program) | SE (sector erase) | BE 32K (block erase 32KB) |
| 1 st byte | E7 (hex) | 6B (hex) | 02 (hex) | 38 (hex) | 20 (hex) | 52 (hex) |
| 2 nd byte | ADD1(2) | ADD1(8) | ADD1 | ADD1 | ADD1 | ADD1 |
| 3 rd byte | ADD2(2) | ADD2(8) | ADD2 | ADD2 | ADD2 | ADD2 |
| 4 th byte | ADD3(2) | ADD3(8) | ADD3 | ADD3 | ADD3 | ADD3 |
| 5 th byte | Dummy(4) | Dummy(8) | | | | |
| Action | Quad I/O read for with 4 dummy cycles | n bytes read out by Quad output until CS# goes high | to program the selected page | quad input to program the selected page | to erase the selected sector | to erase the selected 32K block |

| Mode | SPI/QPI | SPI/QPI |
|----------------------|--------------------------------|------------------------|
| Command (byte) | BE (block erase 64KB) | CE (chip erase) |
| 1 st byte | D8 (hex) | 60 or C7 (hex) |
| 2 nd byte | ADD1 | |
| 3 rd byte | ADD2 | |
| 4 th byte | ADD3 | |
| 5 th byte | | |
| Action | to erase the selected block | to erase whole chip |

Note 1: The fast read command (0Bh) when under QPI mode, the dummy cycle is 4 clocks.

Note 2: Dummy cycle number will be different, depending on the bit7 (DC) setting of Configuration Register. Please refer to "[Configuration Register](#)" Table. Only MX25U12835FZNI-08G supports 4READ with 8 dummy cycles.

Note 3: The count base is 4-bit for ADD(2) and Dummy(2) because of 2 x I/O. And the MSB is on SO/SIO1, which is different from 1 x I/O condition.

Note 4: The number in parentheses after "ADD" or "Data" stands for how many clock cycles it has. For example, "Data(8)" represents there are 8 clock cycles for the data in.

Register/Setting Commands

| Command (byte) | WREN (write enable) | WRDI (write disable) | RDSR (read status register) | RDCR (read configuration register) | WRSR (write status/configuration register) | WPSEL (Write Protect Selection) | EQIO (Enable QPI) |
|----------------------|---------------------------------------|---|---|--|--|---|-----------------------|
| Mode | SPI/QPI | SPI/QPI | SPI/QPI | SPI/QPI | SPI/QPI | SPI/QPI | SPI |
| 1 st byte | 06 (hex) | 04 (hex) | 05 (hex) | 15 (hex) | 01 (hex) | 68 (hex) | 35 (hex) |
| 2 nd byte | | | | | Values | | |
| 3 rd byte | | | | | Values | | |
| 4 th byte | | | | | | | |
| 5 th byte | | | | | | | |
| Action | sets the (WEL) write enable latch bit | resets the (WEL) write enable latch bit | to read out the values of the status register | to read out the values of the configuration register | to write new values of the status/configuration register | to enter and enable individual block protect mode | Entering the QPI mode |

| Command (byte) | RSTQIO (Reset QPI) | PGM/ERS Suspend (Suspends Program/Erase) | PGM/ERS Resume (Resumes Program/Erase) | DP (Deep power down) | RDP (Release from deep power down) | SBL (Set Burst Length) |
|----------------------|----------------------|--|--|-----------------------------|------------------------------------|------------------------|
| Mode | QPI | SPI/QPI | SPI/QPI | SPI/QPI | SPI/QPI | SPI/QPI |
| 1 st byte | F5 (hex) | B0 (hex) | 30 (hex) | B9 (hex) | AB (hex) | C0 (hex) |
| 2 nd byte | | | | | | Value |
| 3 rd byte | | | | | | |
| 4 th byte | | | | | | |
| 5 th byte | | | | | | |
| Action | Exiting the QPI mode | | | enters deep power down mode | release from deep power down mode | to set Burst length |

ID/Security Commands

| Command (byte) | RDID (read identification) | RES (read electronic ID) | REMS (read electronic manufacturer & device ID) | QPIID (QPI ID Read) | RDSFDP | ENSO (enter secured OTP) | EXSO (exit secured OTP) |
|----------------------|---|------------------------------|---|---------------------|--------------------------------------|--------------------------------------|-------------------------------------|
| Mode | SPI | SPI/QPI | SPI | QPI | SPI/QPI | SPI/QPI | SPI/QPI |
| 1 st byte | 9F (hex) | AB (hex) | 90 (hex) | AF (hex) | 5A (hex) | B1 (hex) | C1 (hex) |
| 2 nd byte | | x | x | | ADD1(8) | | |
| 3 rd byte | | x | x | | ADD2(8) | | |
| 4 th byte | | x | ADD ^(Note 5) | | ADD3(8) | | |
| 5 th byte | | | | | Dummy(8) | | |
| Action | outputs JEDEC ID: 1-byte Manufacturer ID & 2-byte Device ID | to read out 1-byte Device ID | output the Manufacturer ID & Device ID | ID in QPI interface | n bytes read out until CS# goes high | to enter the 4K-bit secured OTP mode | to exit the 4K-bit secured OTP mode |

| COMMAND (byte) | RDSCUR (read security register) | WRSCUR (write security register) | SBLK (single block lock) | SBULK (single block unlock) | RDBLOCK (block protect read) | GBLK (gang block lock) | GBULK (gang block unlock) |
|----------------------|------------------------------------|--|---|---|--|--------------------------|---------------------------|
| Mode | SPI/QPI | SPI/QPI | SPI/QPI | SPI/QPI | SPI/QPI | SPI/QPI | SPI/QPI |
| 1 st byte | 2B (hex) | 2F (hex) | 36 (hex) | 39 (hex) | 3C (hex) | 7E (hex) | 98 (hex) |
| 2 nd byte | | | ADD1 | ADD1 | ADD1 | | |
| 3 rd byte | | | ADD2 | ADD2 | ADD2 | | |
| 4 th byte | | | ADD3 | ADD3 | ADD3 | | |
| 5 th byte | | | | | | | |
| Action | to read value of security register | to set the lock-down bit as "1" (once lock-down, cannot be update) | individual block (64K-byte) or sector (4K-byte) write protect | individual block (64K-byte) or sector (4K-byte) unprotect | read individual block or sector write protect status | whole chip write protect | whole chip unprotect |

Note 5: ADD=00H will output the manufacturer ID first and ADD=01H will output device ID first.

Reset Commands

| COMMAND (byte) | NOP (No Operation) | RSTEN (Reset Enable) | RST (Reset Memory) |
|----------------------|-----------------------|-------------------------|--------------------------|
| Mode | SPI/QPI | SPI/QPI | SPI/QPI |
| 1 st byte | 00 (hex) | 66 (hex) | 99 (hex) |
| 2 nd byte | | | |
| 3 rd byte | | | |
| 4 th byte | | | |
| 5 th byte | | | |
| Action | | | <i>(Note 6)</i> |

Note 5: It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.

Note 6: The RSTEN command must be executed before executing the RST command. If any other command is issued in-between RSTEN and RST, the RST command will be ignored.

9-1. Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, 4PP, SE, BE32K, BE, CE, and WRSR, which are intended to change the device content WEL bit should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→sending WREN instruction code→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are "don't care" in SPI mode.

Figure 6. Write Enable (WREN) Sequence (SPI Mode)

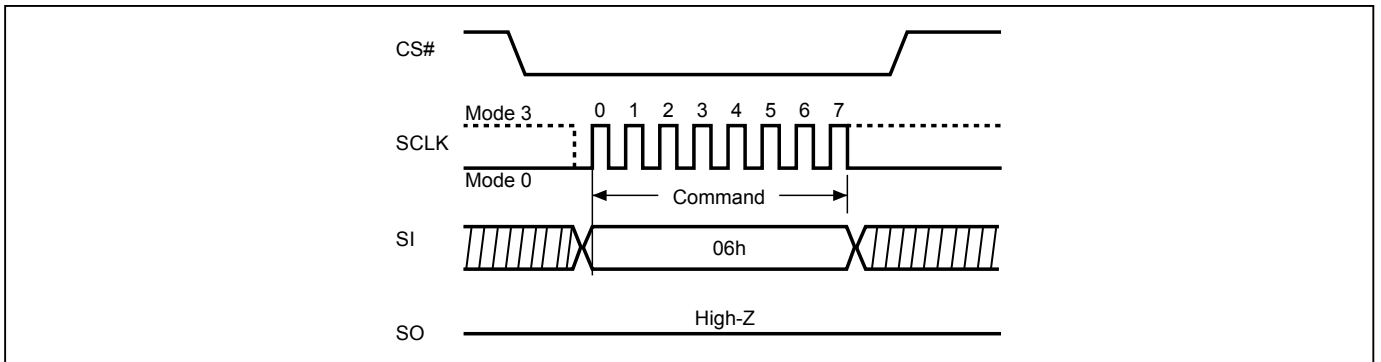
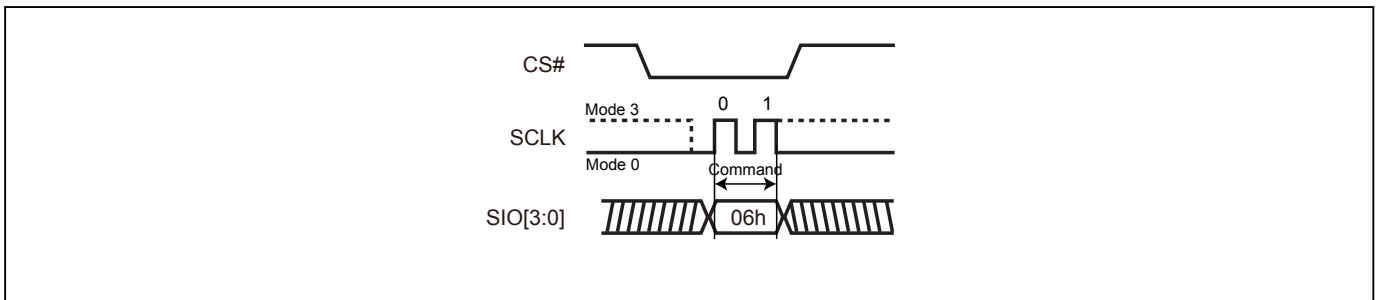


Figure 7. Write Enable (WREN) Sequence (QPI Mode)



9-2. Write Disable (WRDI)

The Write Disable (WRDI) instruction is to reset Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→sending WRDI instruction code→CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are "don't care" in SPI mode.

The WEL bit is reset by following situations:

- Power-up
- Reset# pin driven low
- WRDI command completion
- WRSR command completion
- PP command completion
- 4PP command completion
- SE command completion
- BE32K command completion
- BE command completion
- CE command completion
- PGM/ERS Suspend command completion
- Softreset command completion
- WRSCUR command completion
- WPSEL command completion
- GBLK command completion
- GBULK command completion

Figure 8. Write Disable (WRDI) Sequence (SPI Mode)

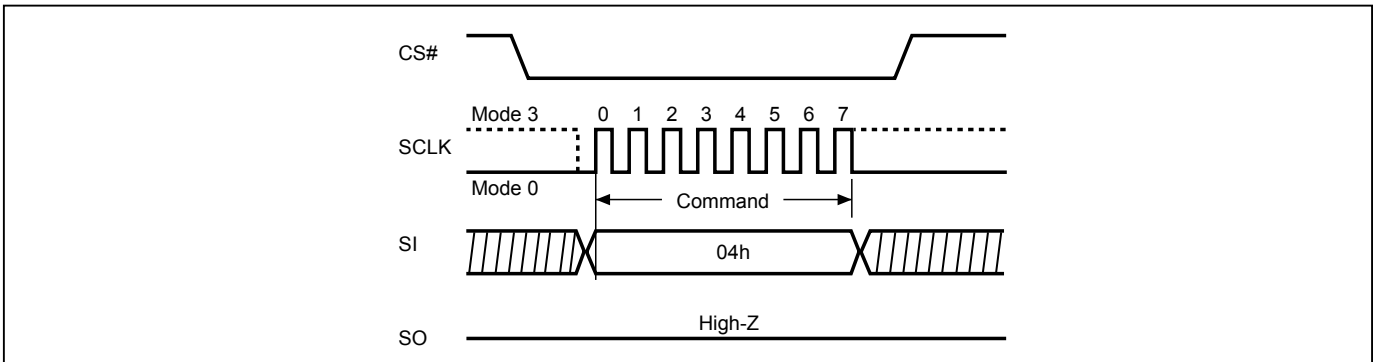
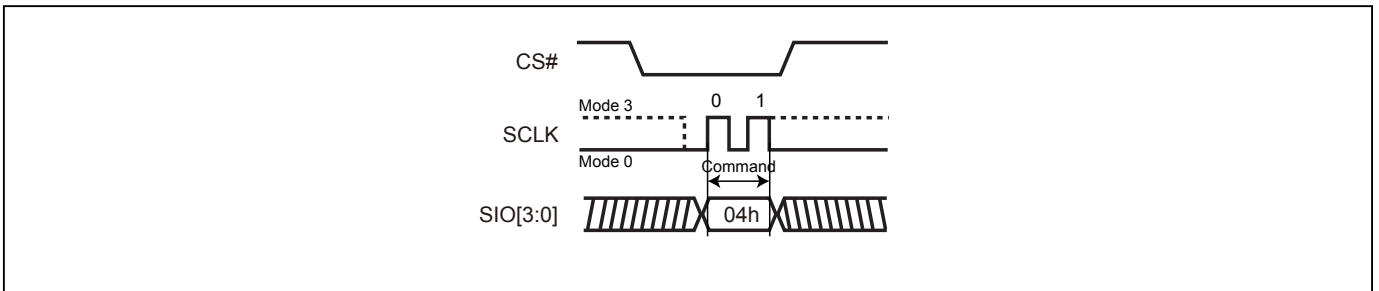


Figure 9. Write Disable (WRDI) Sequence (QPI Mode)



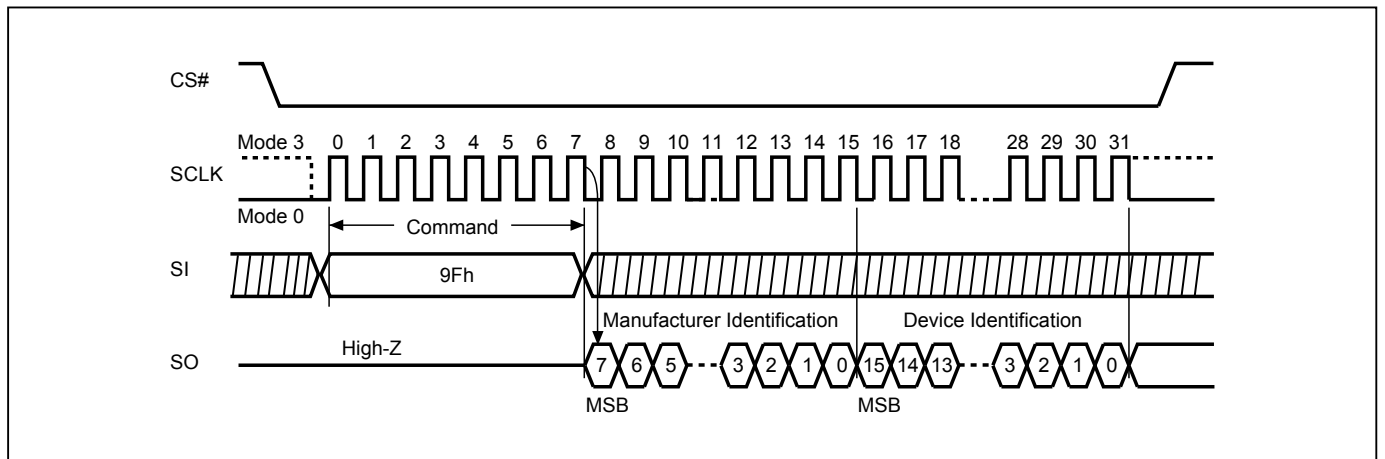
9-3. Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The Macro-nix Manufacturer ID and Device ID are listed as "Table 6. ID Definitions".

The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code→24-bits ID data out on SO→ to end RDID operation can drive CS# to high at any time during data out.

While Program/Erase operation is in progress, it will not decode the RDID instruction, therefore there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

Figure 10. Read Identification (RDID) Sequence (SPI mode only)



9-4. Release from Deep Power-down (RDP), Read Electronic Signature (RES)

The Release from Deep Power-down (RDP) instruction is terminated by driving Chip Select (CS#) High. When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, the transition to the Stand-by Power mode is delayed by t_{RES2} , and Chip Select (CS#) must remain High for at least $t_{RES2}(max)$, as specified in "Table 19. AC Characteristics". AC Characteristics. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions. The RDP instruction is only for releasing from Deep Power Down Mode. Reset# pin goes low will release the Flash from deep power down mode.

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as "Table 6. ID Definitions". This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction.

Even in Deep power-down mode, the RDP and RES are also allowed to be executed, only except the device is in progress of program/erase/write cycle; there's no effect on the current program/erase/write cycle in progress.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are "don't care" in SPI mode.

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of t_{RES2} to transit to standby mode, and CS# must remain to high at least $t_{RES2}(max)$. Once in the standby mode, the device waits to be selected, so it can be receive, decode, and execute instruction.

Figure 11. Read Electronic Signature (RES) Sequence (SPI Mode)

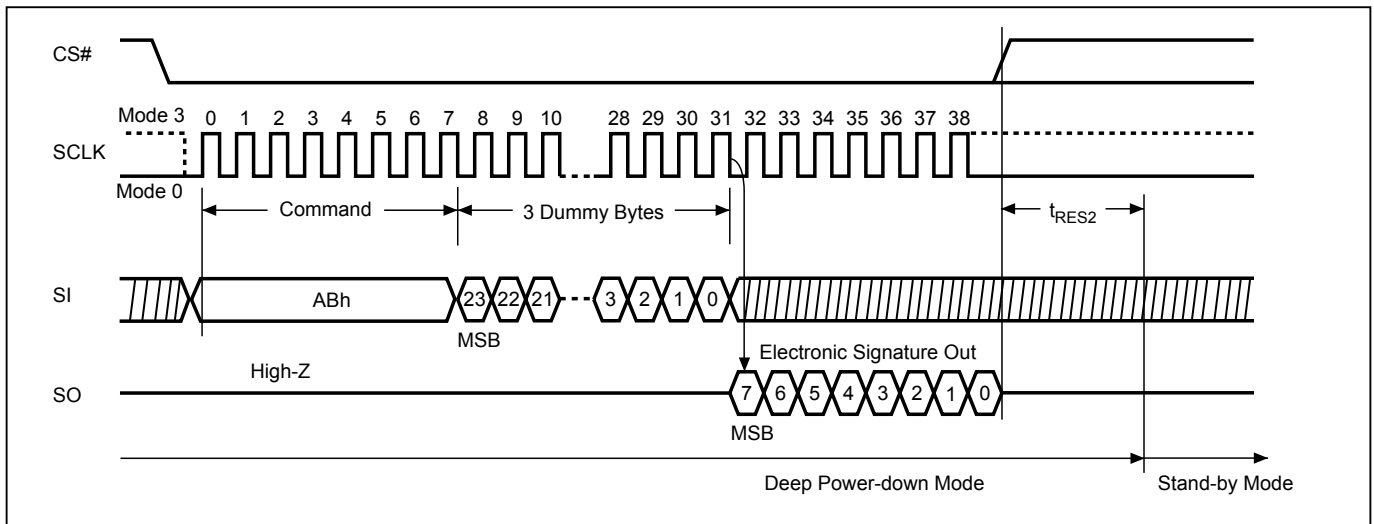


Figure 12. Read Electronic Signature (RES) Sequence (QPI Mode)

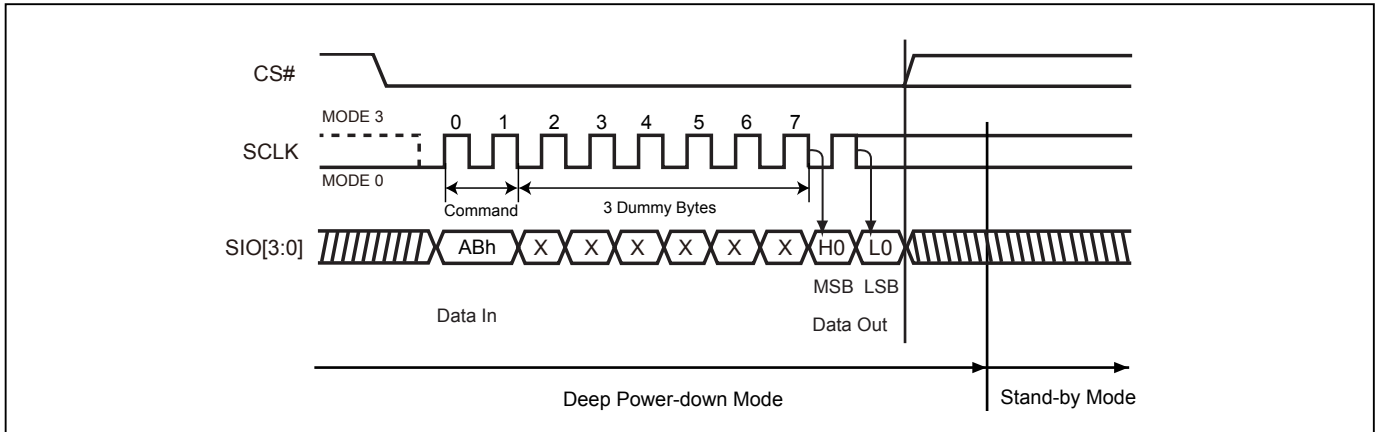


Figure 13. Release from Deep Power-down (RDP) Sequence (SPI Mode)

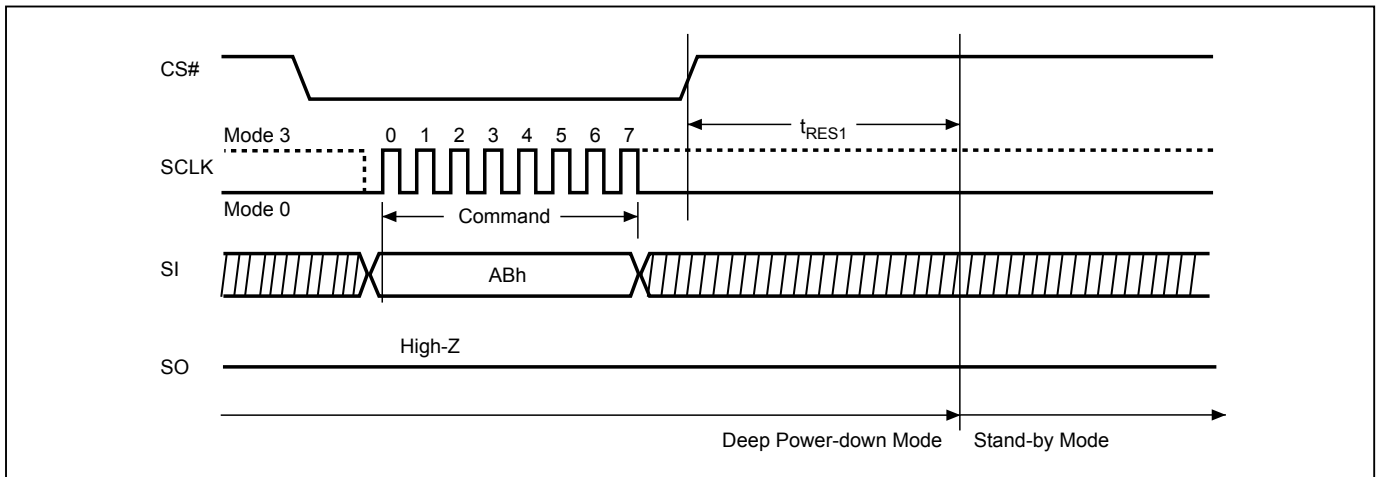
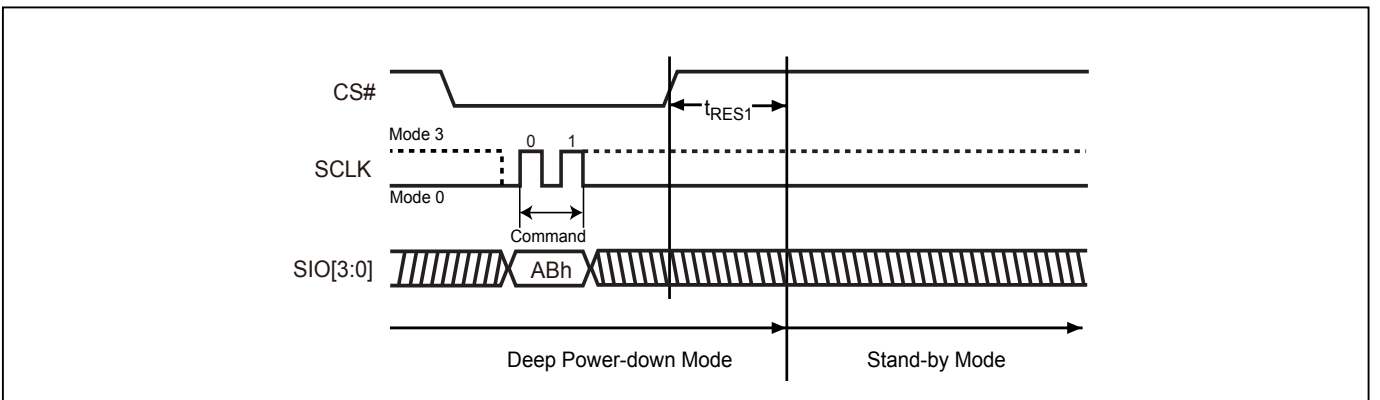


Figure 14. Release from Deep Power-down (RDP) Sequence (QPI Mode)

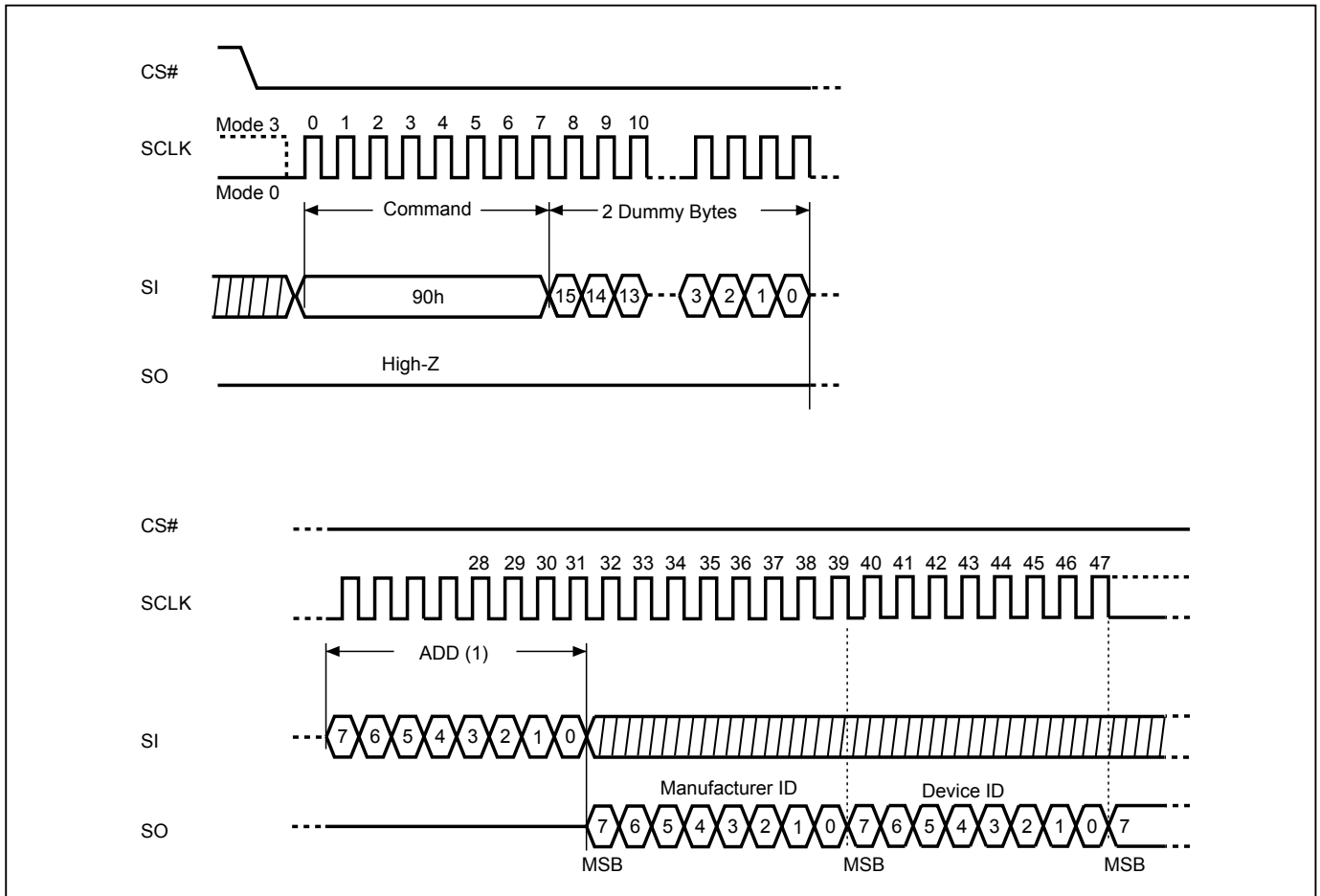


9-5. Read Electronic Manufacturer ID & Device ID (REMS)

The REMS instruction returns both the JEDEC assigned manufacturer ID and the device ID. The Device ID values are listed in "Table 6. ID Definitions".

The REMS instruction is initiated by driving the CS# pin low and sending the instruction code "90h" followed by two dummy bytes and one address byte (A7-A0). After which the manufacturer ID for Macronix (C2h) and the device ID are shifted out on the falling edge of SCLK with the most significant bit (MSB) first. If the address byte is 00h, the manufacturer ID will be output first, followed by the device ID. If the address byte is 01h, then the device ID will be output first, followed by the manufacturer ID. While CS# is low, the manufacturer and device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

Figure 15. Read Electronic Manufacturer & Device ID (REMS) Sequence (SPI Mode only)



Notes:

- (1) ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first.
- (2) Instruction is 90h (hex).

9-6. QPI ID Read (QPIID)

User can execute this ID Read instruction to identify the Device ID and Manufacturer ID. The sequence of issue QPIID instruction is CS# goes low→sending QPI ID instruction→Data out on SO→CS# goes high. Most significant bit (MSB) first.

After the command cycle, the device will immediately output data on the falling edge of SCLK. The manufacturer ID, memory type, and device ID data byte will be output continuously, until the CS# goes high.

Table 6. ID Definitions

| Command Type | Command | MX25U12835F | | |
|--------------|-----------|-----------------|-------------|----------------|
| RDID / QPIID | 9Fh / AFh | Manufacturer ID | Memory Type | Memory Density |
| | | C2 | 25 | 38 |
| RES | ABh | Electronic ID | | |
| | | 38 | | |
| REMS | 90h | Manufacturer ID | Device ID | |
| | | C2 | 38 | |

9-7. Read Status Register (RDSR)

The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase/write status register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low → sending RDSR instruction code → Status Register data out on SO.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are "don't care" in SPI mode.

Figure 16. Read Status Register (RDSR) Sequence (SPI Mode)

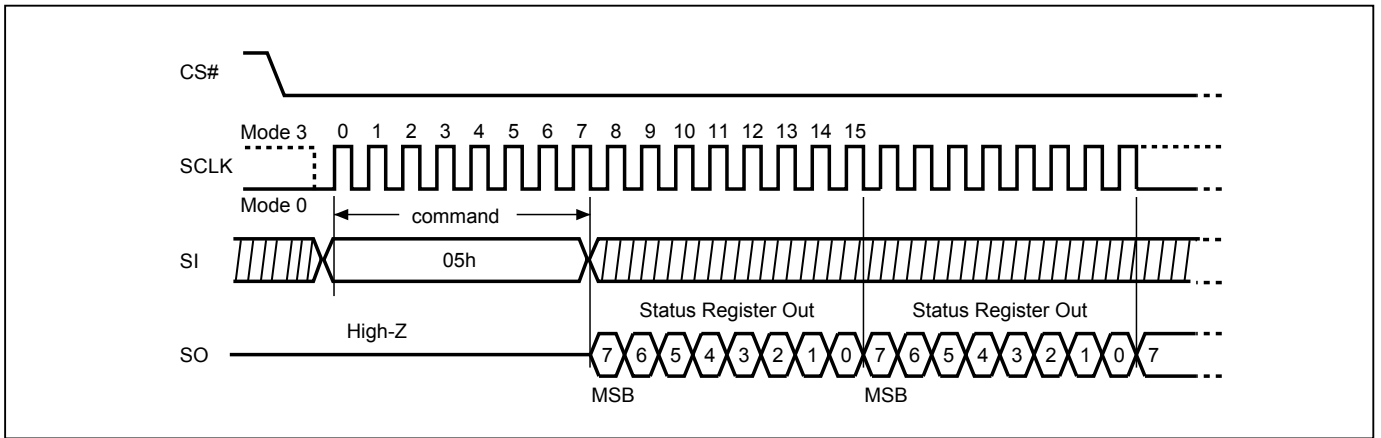
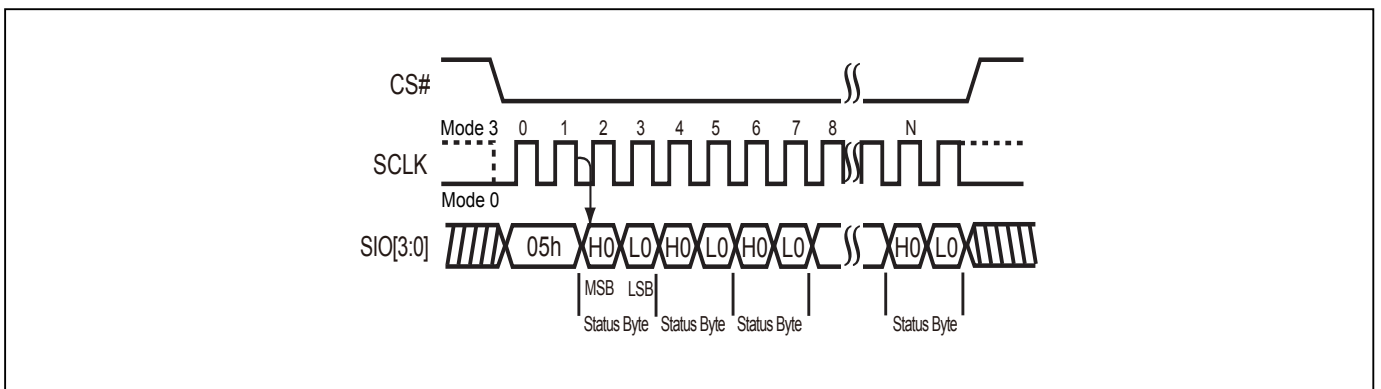


Figure 17. Read Status Register (RDSR) Sequence (QPI Mode)



9-8. Read Configuration Register (RDCR)

The RDCR instruction is for reading Configuration Register Bits. The Read Configuration Register can be read at any time (even in program/erase/write configuration register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write configuration register operation is in progress.

The sequence of issuing RDCR instruction is: CS# goes low → sending RDCR instruction code → Configuration Register data out on SO.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are "don't care" in SPI mode.

Figure 18. Read Configuration Register (RDCR) Sequence (SPI Mode)

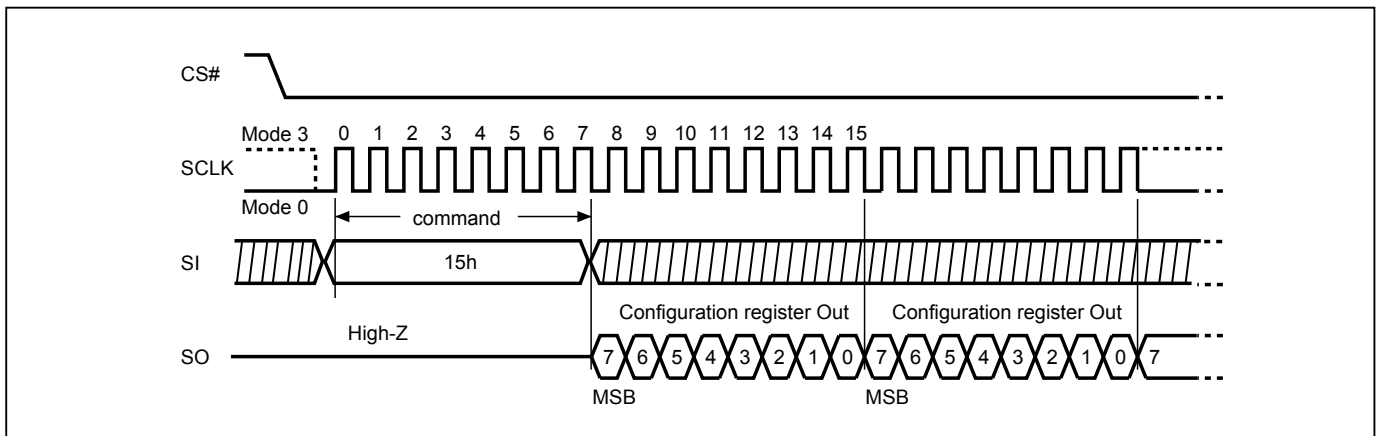
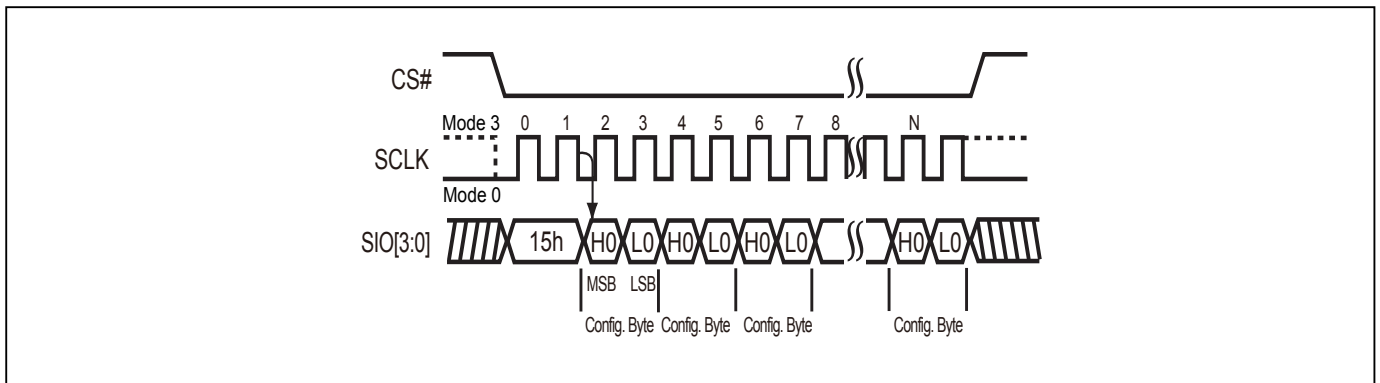


Figure 19. Read Configuration Register (RDCR) Sequence (QPI Mode)



For user to check if Program/Erase operation is finished or not, RDSR instruction flow are shown as follows:

Figure 20. Program/Erase flow with read array data

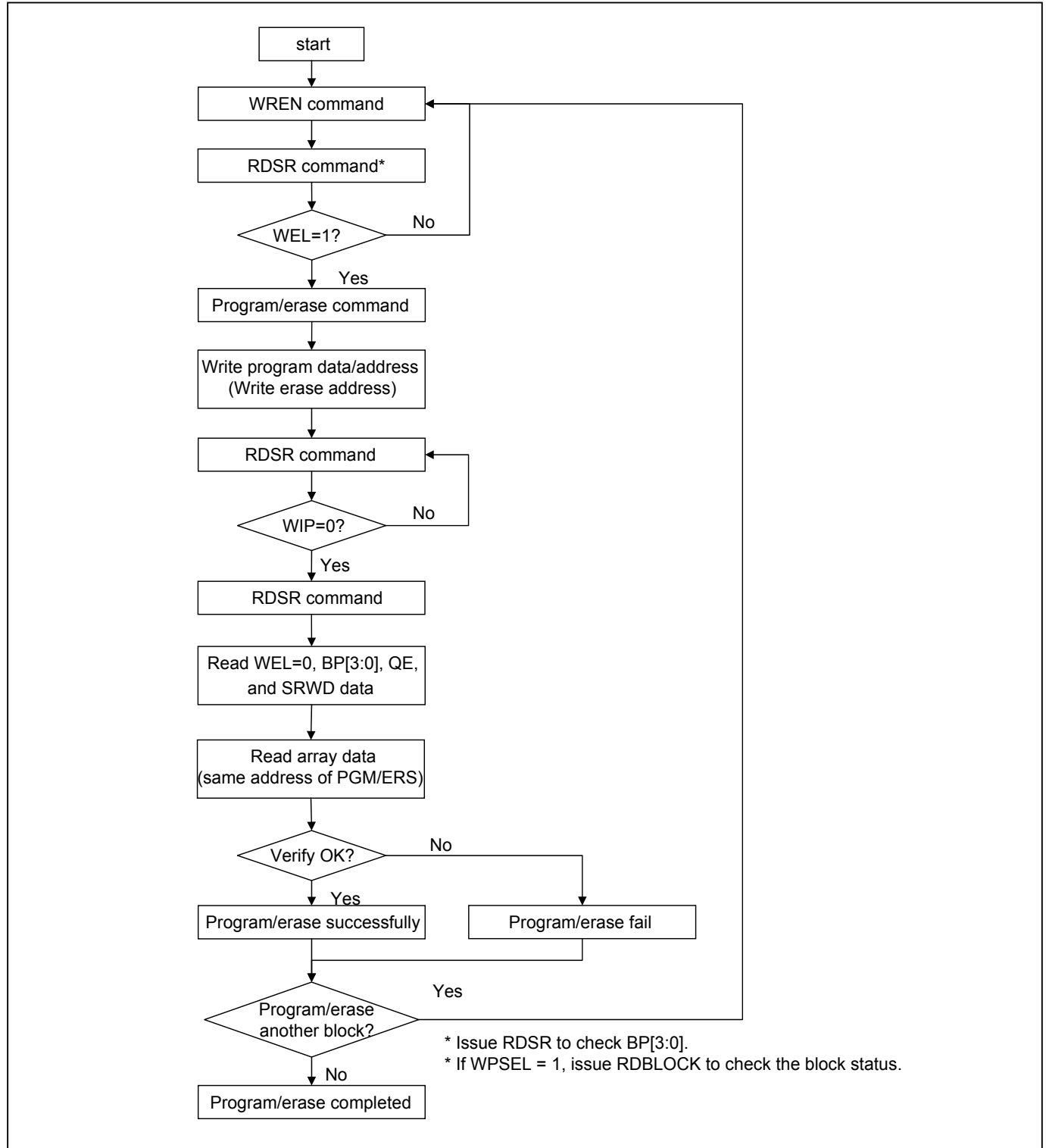
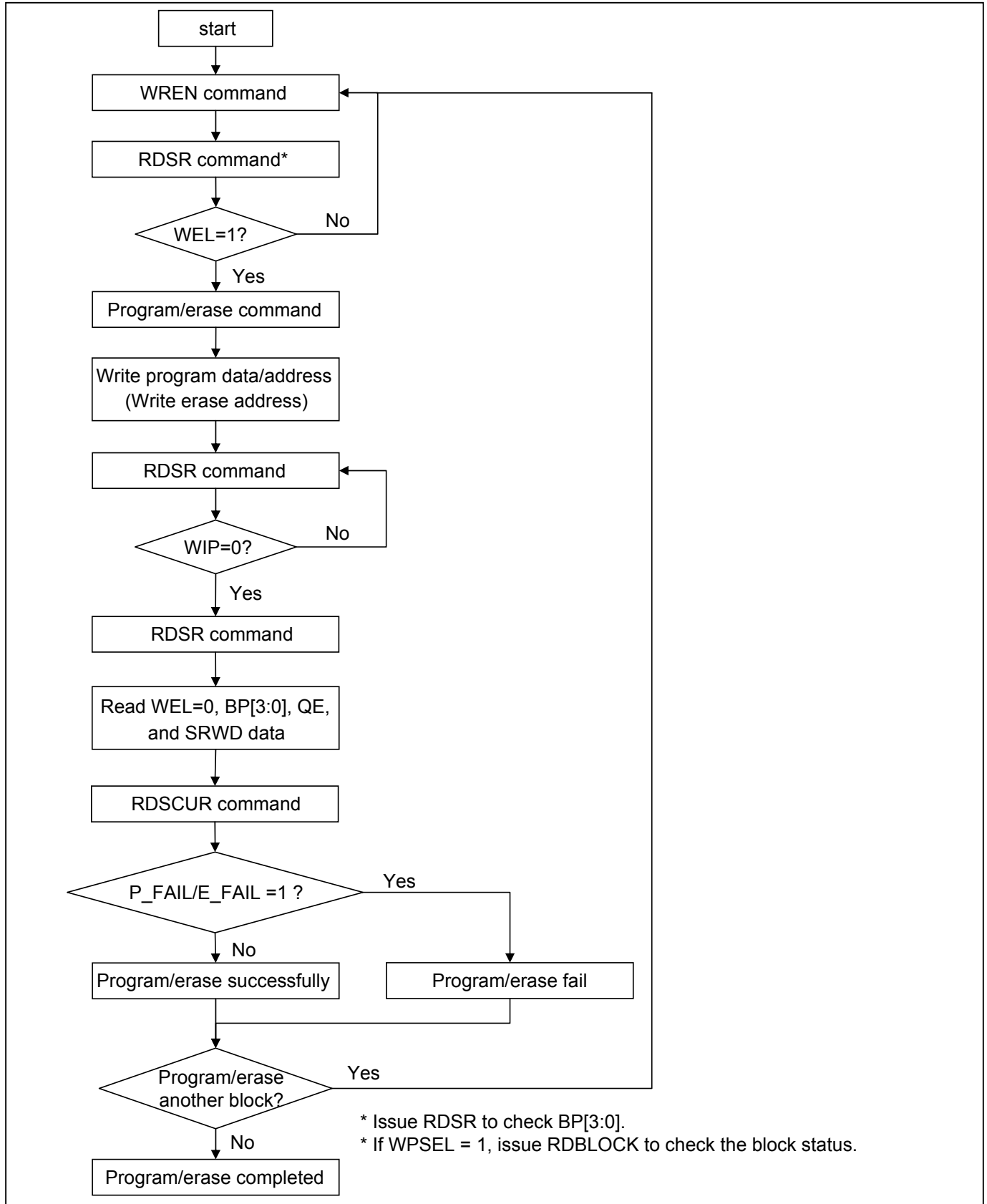


Figure 21. Program/Erase flow without read array data (read P_FAIL/E_FAIL flag)



Status Register

The definition of the status register bits is as below:

WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

WEL bit. The Write Enable Latch (WEL) bit is a volatile bit that is set to "1" by the WREN instruction. WEL needs to be set to "1" before the device can accept program and erase instructions, otherwise the program and erase instructions are ignored. WEL automatically clears to "0" when a program or erase operation completes. To ensure that both WIP and WEL are "0" and the device is ready for the next program or erase operation, it is recommended that WIP be confirmed to be "0" before checking that WEL is also "0" (Please refer to "Figure 24. WRSR flow"). If a program or erase instruction is applied to a protected memory area, the instruction will be ignored and WEL will clear to "0".

BP3, BP2, BP1, BP0 bits. The Block Protect (BP3, BP2, BP1, BP0) bits, non-volatile bits, indicate the protected area (as defined in "Table 2. Protected Area Sizes") of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP3, BP2, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase 32KB (BE32K), Block Erase (BE) and Chip Erase (CE) instructions (only if Block Protect bits (BP3:BP0) set to 0, the CE instruction can be executed). The BP3, BP2, BP1, BP0 bits are "0" as default, which is unprotected.

QE bit. The Quad Enable (QE) bit, non-volatile bit, while it is "0" (factory default), it performs non-Quad and WP#, RESET# are enable. While QE is "1", it performs Quad I/O mode and WP#, RESET# are disabled. In the other word, if the system goes into four I/O mode (QE=1), the feature of HPM and RESET will be disabled.

SRWD bit. The Status Register Write Disable (SRWD) bit, non-volatile bit, is operated together with Write Protection (WP#/SIO2) pin for providing hardware protection mode. The hardware protection mode requires SRWD sets to 1 and WP#/SIO2 pin signal is low stage. In the hardware protection mode, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP3, BP2, BP1, BP0) are read only. The SRWD bit defaults to be "0".

Table 7. Status Register

| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---|------------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------------|---|
| SRWD (status register write protect) | QE (Quad Enable) | BP3 (level of protected block) | BP2 (level of protected block) | BP1 (level of protected block) | BP0 (level of protected block) | WEL (write enable latch) | WIP (write in progress bit) |
| 1=status register write disabled 0=status register write enabled | 1=Quad Enable 0=not Quad Enable | (note 1) | (note 1) | (note 1) | (note 1) | 1=write enable 0=not write enable | 1=write operation 0=not in write operation |
| Non-volatile bit | Non-volatile bit | Non-volatile bit | Non-volatile bit | Non-volatile bit | Non-volatile bit | volatile bit | volatile bit |

Note 1: Please refer to the "Table 2. Protected Area Sizes".

Configuration Register

The Configuration Register is able to change the default status of Flash memory. Flash memory will be configured after the CR bit is set.

ODS bit

The output driver strength (ODS2, ODS1, ODS0) bits are volatile bits, which indicate the output driver level (as defined in *Output Driver Strength Table*) of the device. The Output Driver Strength is defaulted as 30 Ohms when delivered from factory. To write the ODS bits requires the Write Status Register (WRSR) instruction to be executed.

TB bit

The Top/Bottom (TB) bit is a non-volatile OTP bit. The Top/Bottom (TB) bit is used to configure the Block Protect area by BP bit (BP3, BP2, BP1, BP0), starting from TOP or Bottom of the memory array. The TB bit is defaulted as "0", which means Top area protect. When it is set as "1", the protect area will change to Bottom area of the memory device. To write the TB bits requires the Write Status Register (WRSR) instruction to be executed.

Configuration Register

| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|------------------------|----------|----------|----------|--|--------------------------------------|--------------------------------------|--------------------------------------|
| DC (Dummy Cycle) | Reserved | Reserved | Reserved | TB (top/bottom selected) | ODS 2 (output driver strength) | ODS 1 (output driver strength) | ODS 0 (output driver strength) |
| <i>(note 2)</i> | x | x | x | 0=Top area protect 1=Bottom area protect (Default=0) | <i>(note 1)</i> | <i>(note 1)</i> | <i>(note 1)</i> |
| Volatile bit | x | x | x | OTP | volatile bit | volatile bit | volatile bit |

Note 1: Please refer to "[Output Driver Strength Table](#)"

Note 2: For 4READ command on MX25U12835FZNI-08G (f=133MHz) only. Please refer to "[Dummy Cycle and Frequency Table](#)" for details.

Output Driver Strength Table

| ODS2 | ODS1 | ODS0 | Description | Note |
|------|------|------|-------------------|--------------------|
| 0 | 0 | 0 | Reserved | Impedance at VCC/2 |
| 0 | 0 | 1 | 90 Ohms | |
| 0 | 1 | 0 | 60 Ohms | |
| 0 | 1 | 1 | 45 Ohms | |
| 1 | 0 | 0 | Reserved | |
| 1 | 0 | 1 | 20 Ohms | |
| 1 | 1 | 0 | 15 Ohms | |
| 1 | 1 | 1 | 30 Ohms (Default) | |

Dummy Cycle and Frequency Table

| DC | Numbers of Dummy clock cycles | Quad I/O Read |
|-------------|----------------------------------|---------------|
| 1 | 8 | 133 |
| 0 (default) | 6 | 104 |

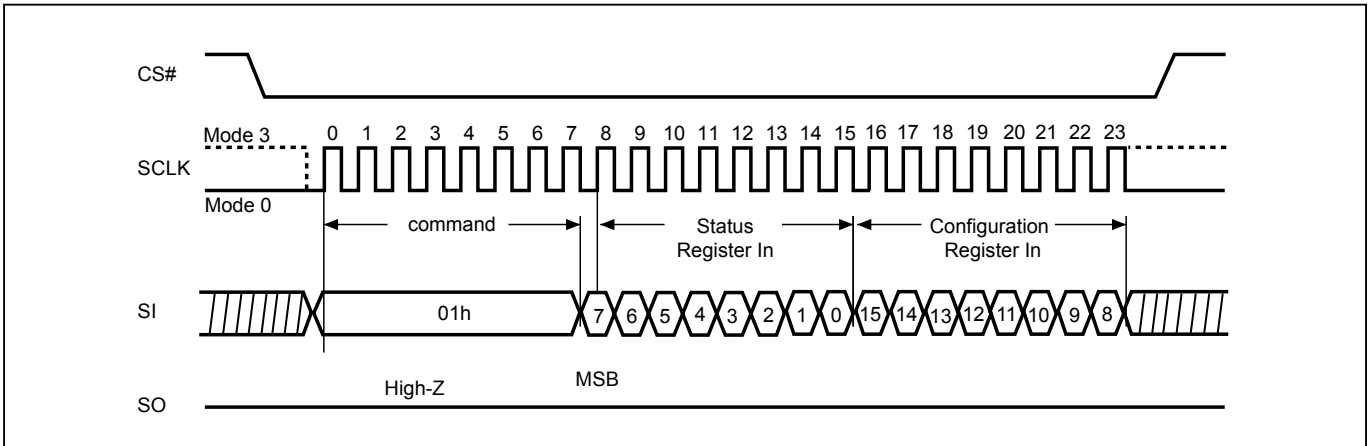
9-9. Write Status Register (WRSR)

The WRSR instruction is for changing the values of Status Register Bits and Configuration Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP3, BP2, BP1, BP0) bits to define the protected area of memory (as shown in "Table 2. Protected Area Sizes"). The WRSR also can set or reset the Quad enable (QE) bit and set or reset the Status Register Write Disable (SRWD) bit in accordance with Write Protection (WP#/SIO2) pin signal, but has no effect on bit1(WEL) and bit0 (WIP) of the status register. The WRSR instruction cannot be executed once the Hardware Protected Mode (HPM) is entered.

The sequence of issuing WRSR instruction is: CS# goes low→ sending WRSR instruction code→ Status Register data on SI→CS# goes high.

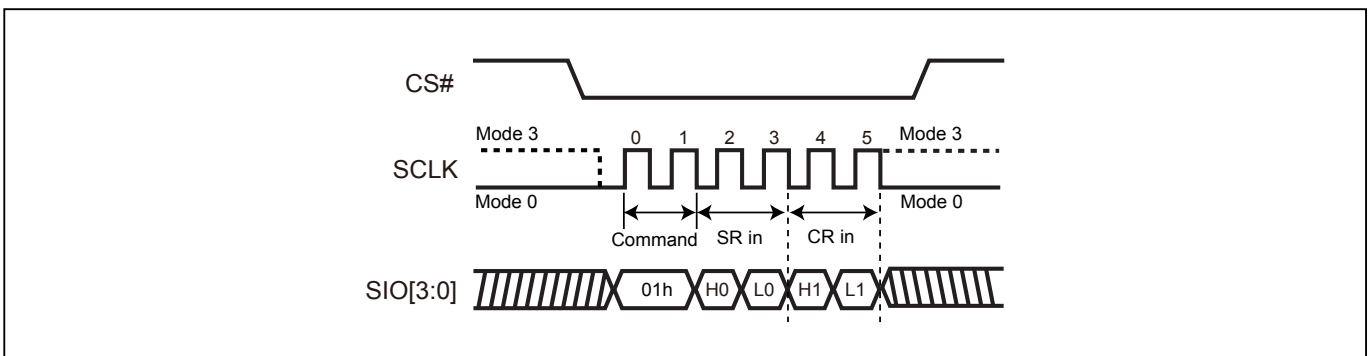
The CS# must go high exactly at the 8 bits or 16 bits data boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Figure 22. Write Status Register (WRSR) Sequence (SPI Mode)



Note: The CS# must go high exactly at 8 bits or 16 bits data boundary to completed the write register command.

Figure 23. Write Status Register (WRSR) Sequence (QPI Mode)



Software Protected Mode (SPM):

- When SRWD bit=0, no matter WP#/SIO2 is low or high, the WREN instruction may set the WEL bit and can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM).
- When SRWD bit=1 and WP#/SIO2 is high, the WREN instruction may set the WEL bit can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM)

Note:

If SRWD bit=1 but WP#/SIO2 is low, it is impossible to write the Status Register even if the WEL bit has previously been set. It is rejected to write the Status Register and not be executed.

Hardware Protected Mode (HPM):

- When SRWD bit=1, and then WP#/SIO2 is low (or WP#/SIO2 is low before SRWD bit=1), it enters the hardware protected mode (HPM). The data of the protected area is protected by software protected mode by BP3, BP2, BP1, BP0 and hardware protected mode by the WP#/SIO2 to against data modification.

Note:

To exit the hardware protected mode requires WP#/SIO2 driving high once the hardware protected mode is entered. If the WP#/SIO2 pin is permanently connected to high, the hardware protected mode can never be entered; only can use software protected mode via BP3, BP2, BP1, BP0.

If the system enter QPI or set QE=1, the feature of HPM will be disabled.

Table 8. Protection Modes

| Mode | Status register condition | WP# and SRWD bit status | Memory |
|--------------------------------|---|--|--|
| Software protection mode (SPM) | Status register can be written in (WEL bit is set to "1") and the SRWD, BP0-BP3 bits can be changed | WP#=1 and SRWD bit=0, or WP#=0 and SRWD bit=0, or WP#=1 and SRWD=1 | The protected area cannot be program or erase. |
| Hardware protection mode (HPM) | The SRWD, BP0-BP3 of status register bits cannot be changed | WP#=0, SRWD bit=1 | The protected area cannot be program or erase. |

Note: As defined by the values in the Block Protect (BP3, BP2, BP1, BP0) bits of the Status Register, as shown in ["Table 2. Protected Area Sizes"](#).

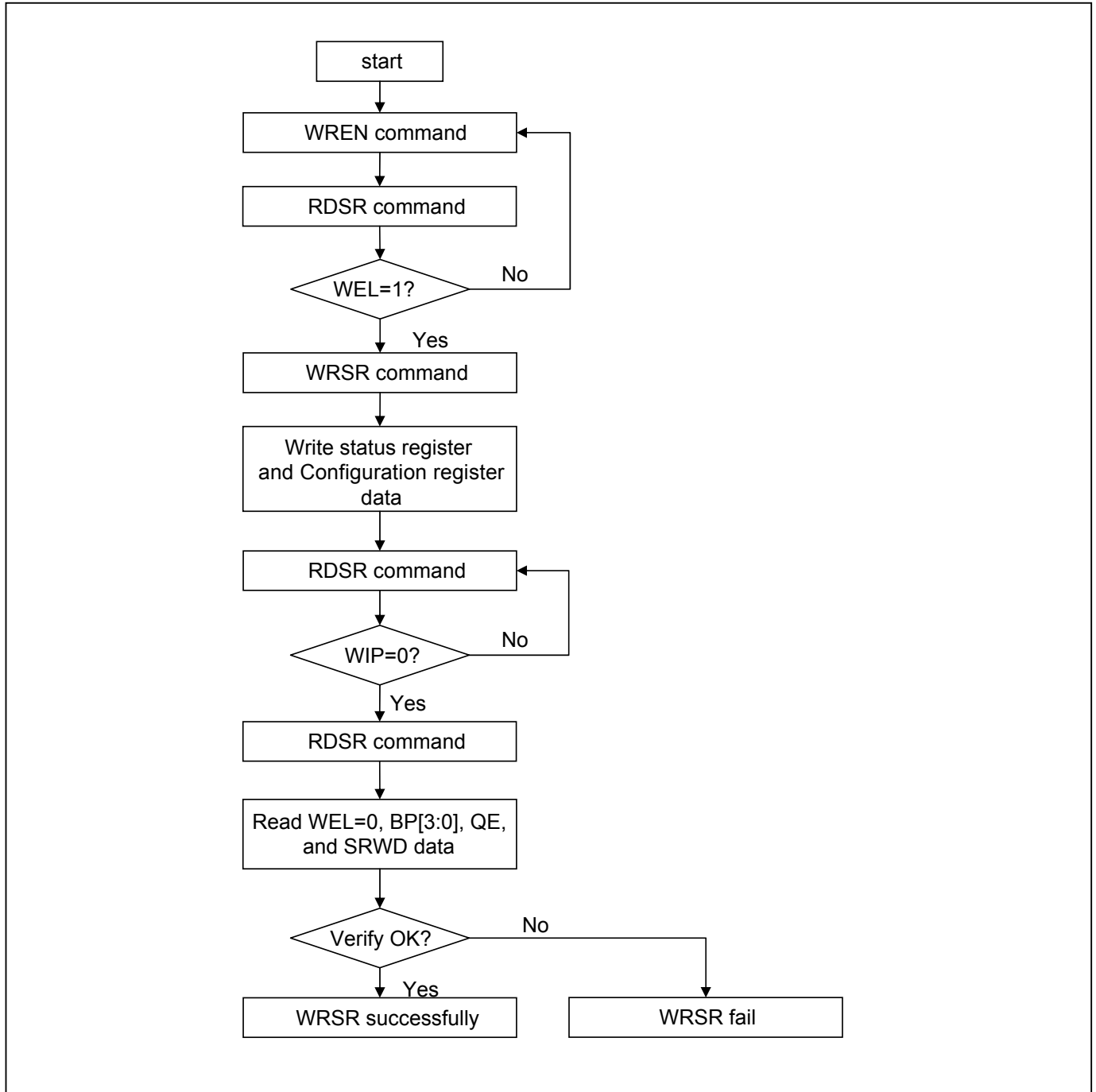
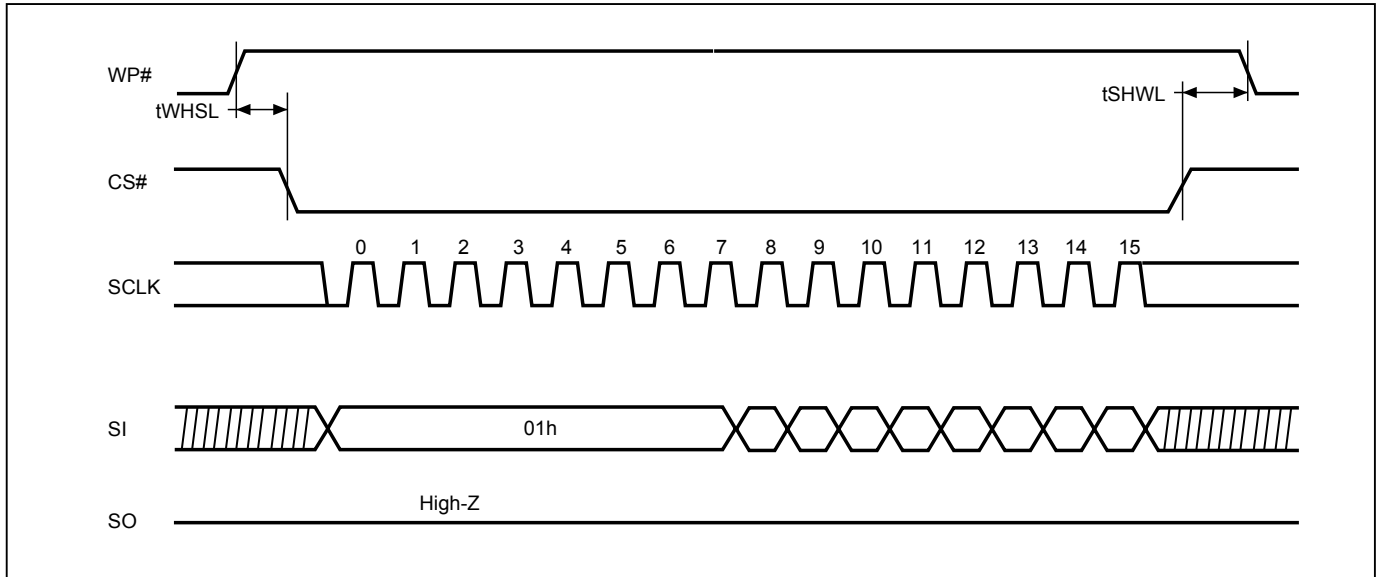
Figure 24. WRSR flow

Figure 25. WP# Setup Timing and Hold Timing during WRSR when SRWD=1

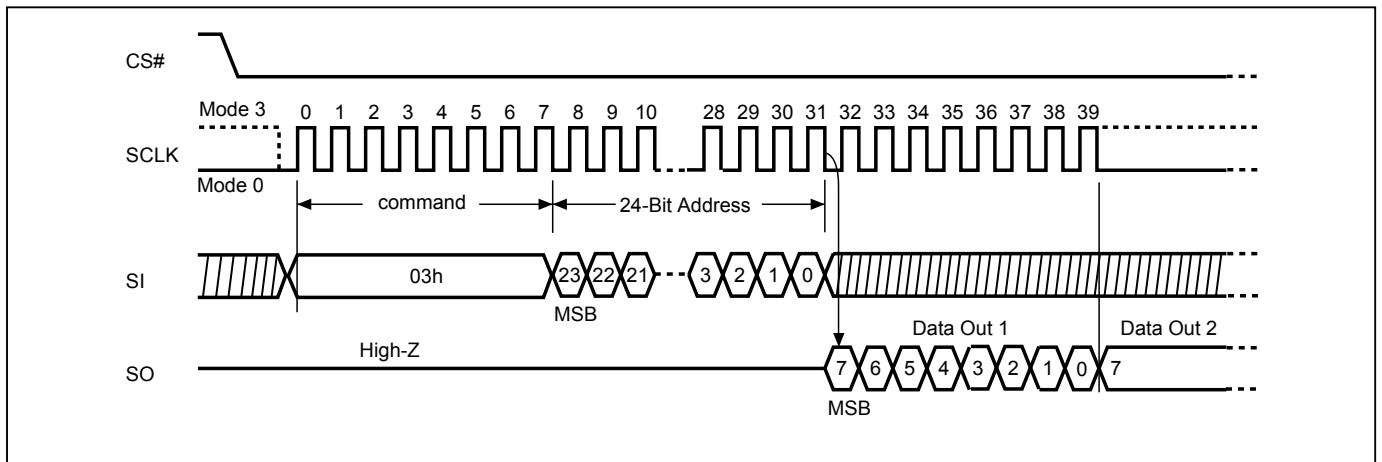


9-10. Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency f_R . The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing READ instruction is: CS# goes low→sending READ instruction code→ 3-byte address on SI→ data out on SO→to end READ operation can use CS# to high at any time during data out.

Figure 26. Read Data Bytes (READ) Sequence (SPI Mode only)



9-11. Read Data Bytes at Higher Speed (FAST_READ)

The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

Read on SPI Mode The sequence of issuing FAST_READ instruction is: CS# goes low→ sending FAST_READ instruction code→ 3-byte address on SI→1-dummy byte (default) address on SI→ data out on SO→ to end FAST_READ operation can use CS# to high at any time during data out.

Read on QPI Mode The sequence of issuing FAST_READ instruction in QPI mode is: CS# goes low→ sending FAST_READ instruction, 2 cycles→ 24-bit address interleave on SIO3, SIO2, SIO1 & SIO0→4 dummy cycles→data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end QPI FAST_READ operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 27. Read at Higher Speed (FAST_READ) Sequence (SPI Mode)

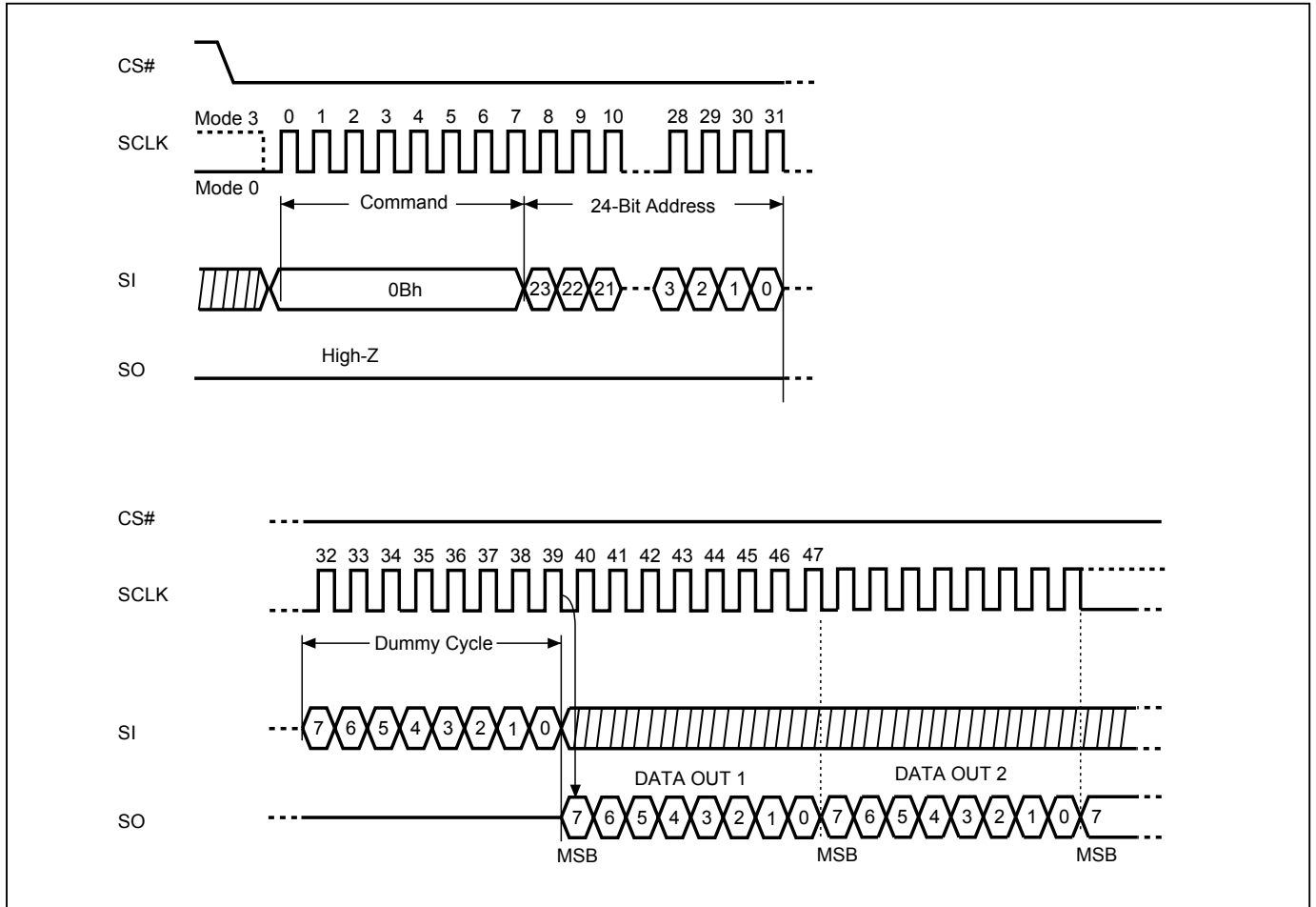
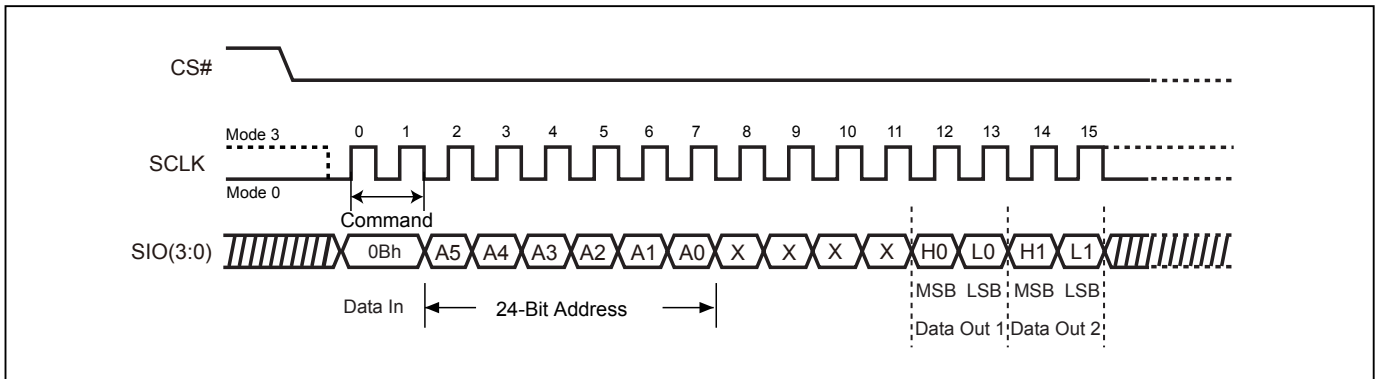


Figure 28. Read at Higher Speed (FAST_READ) Sequence (QPI Mode)



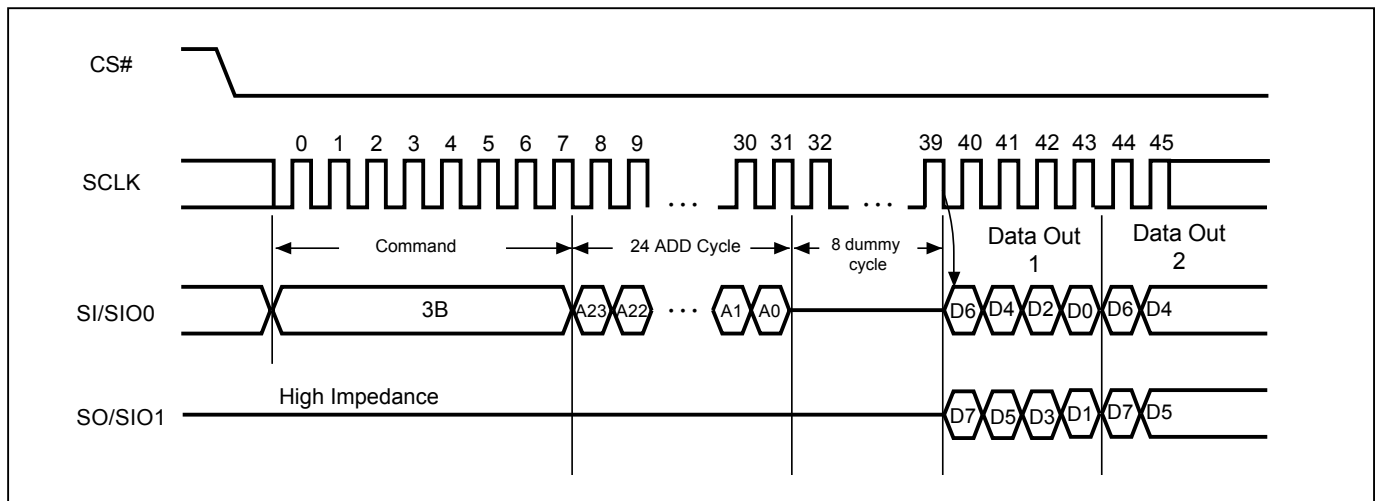
9-12. Dual Read Mode (DREAD)

The DREAD instruction enable double throughput of Serial NOR Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency f_T . The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single DREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing DREAD instruction, the following data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing DREAD instruction is: CS# goes low → sending DREAD instruction → 3-byte address on SI → 8-bit dummy cycle → data out interleave on SIO1 & SIO0 → to end DREAD operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, DREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 29. Dual Read Mode Sequence (Command 3B)



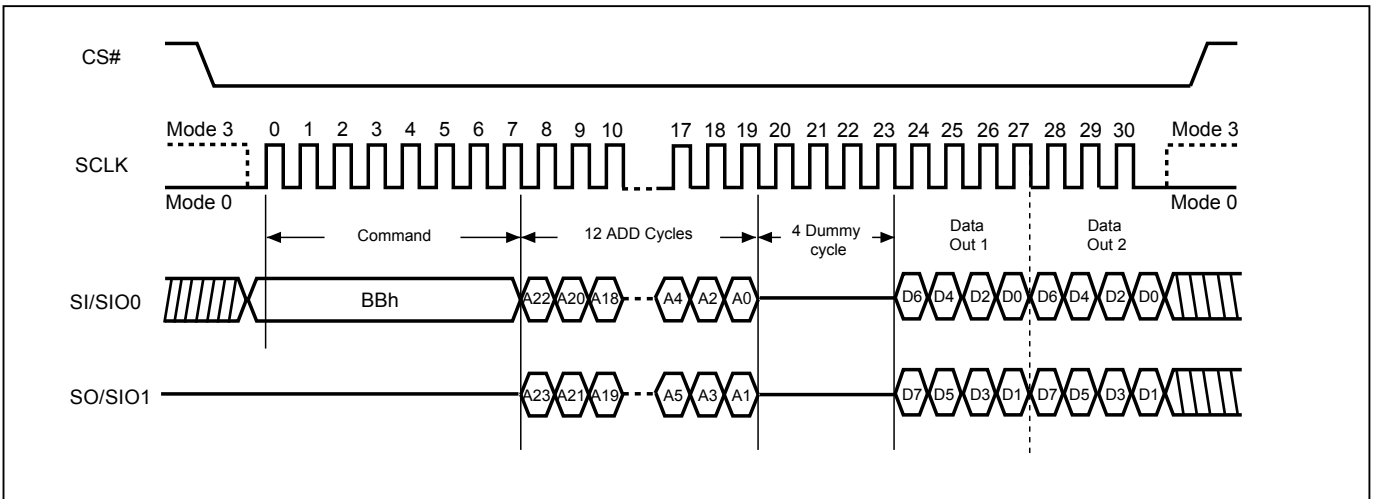
9-13. 2 x I/O Read Mode (2READ)

The 2READ instruction enable double throughput of Serial NOR Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 2READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 2READ instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing 2READ instruction is: CS# goes low→ sending 2READ instruction→ 24-bit address interleave on SIO1 & SIO0→ 4 dummy cycles on SIO1 & SIO0→ data out interleave on SIO1 & SIO0→ to end 2READ operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, 2READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 30. 2 x I/O Read Mode Sequence (SPI Mode only)



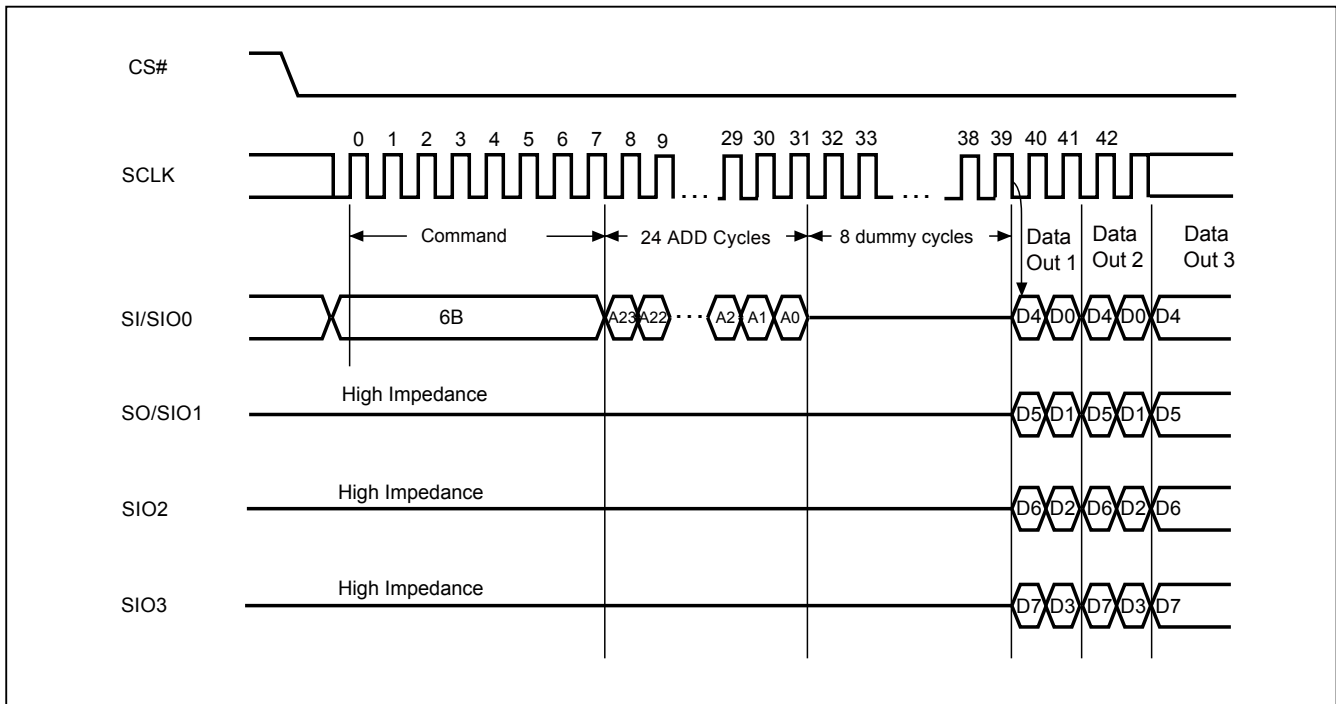
9-14. Quad Read Mode (QREAD)

The QREAD instruction enable quad throughput of Serial NOR Flash in read mode. A Quad Enable (QE) bit of status Register must be set to "1" before sending the QREAD instruction. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single QREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing QREAD instruction, the following data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing QREAD instruction is: CS# goes low → sending QREAD instruction → 3-byte address on SI → 8-bit dummy cycle → data out interleave on SIO3, SIO2, SIO1 & SIO0 → to end QREAD operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, QREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 31. Quad Read Mode Sequence (Command 6B)



9-15. 4 x I/O Read Mode (4READ)

The 4READ instruction enable quad throughput of Serial NOR Flash in read mode. A Quad Enable (QE) bit of status Register must be set to "1" before sending the 4READ instruction. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 4READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 4READ instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

4 x I/O Read on SPI Mode (4READ) The sequence of issuing 4READ instruction is: CS# goes low→ sending 4READ instruction→ 24-bit address interleave on SIO3, SIO2, SIO1 & SIO0→2+4 dummy cycles→data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end 4READ operation can use CS# to high at any time during data out.

4 x I/O Read on QPI Mode (4READ) The 4READ instruction also support on QPI command mode. The sequence of issuing 4READ instruction QPI mode is: CS# goes low→ sending 4READ instruction→ 24-bit address interleave on SIO3, SIO2, SIO1 & SIO0→2+4 dummy cycles (default) →data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end 4READ operation can use CS# to high at any time during data out.

Another sequence of issuing 4READ instruction especially useful in random access is : CS# goes low→sending 4 READ instruction→3-bytes address interleave on SIO3, SIO2, SIO1 & SIO0 →performance enhance toggling bit P[7:0]→ 4 dummy cycles →data out still CS# goes high → CS# goes low (reduce 4READ instruction) →24-bit random access address.

In the performance-enhancing mode, P[7:4] must be toggling with P[3:0] ; likewise P[7:0]=A5h, 5Ah, F0h or 0Fh can make this mode continue and reduce the next 4READ instruction. Once P[7:4] is no longer toggling with P[3:0]; likewise P[7:0]=FFh,00h,AAh or 55h and afterwards CS# is raised and then lowered, the system then will escape from performance enhance mode and return to normal operation.

While Program/Erase/Write Status Register cycle is in progress, 4READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

W4READ instruction (E7h) is also available for 4 I/O read. Please refer to "[Figure 36. W4READ \(Quad Read with 4 dummy cycles\) Sequence](#)".

Figure 32. 4 x I/O Read Mode Sequence (SPI Mode)

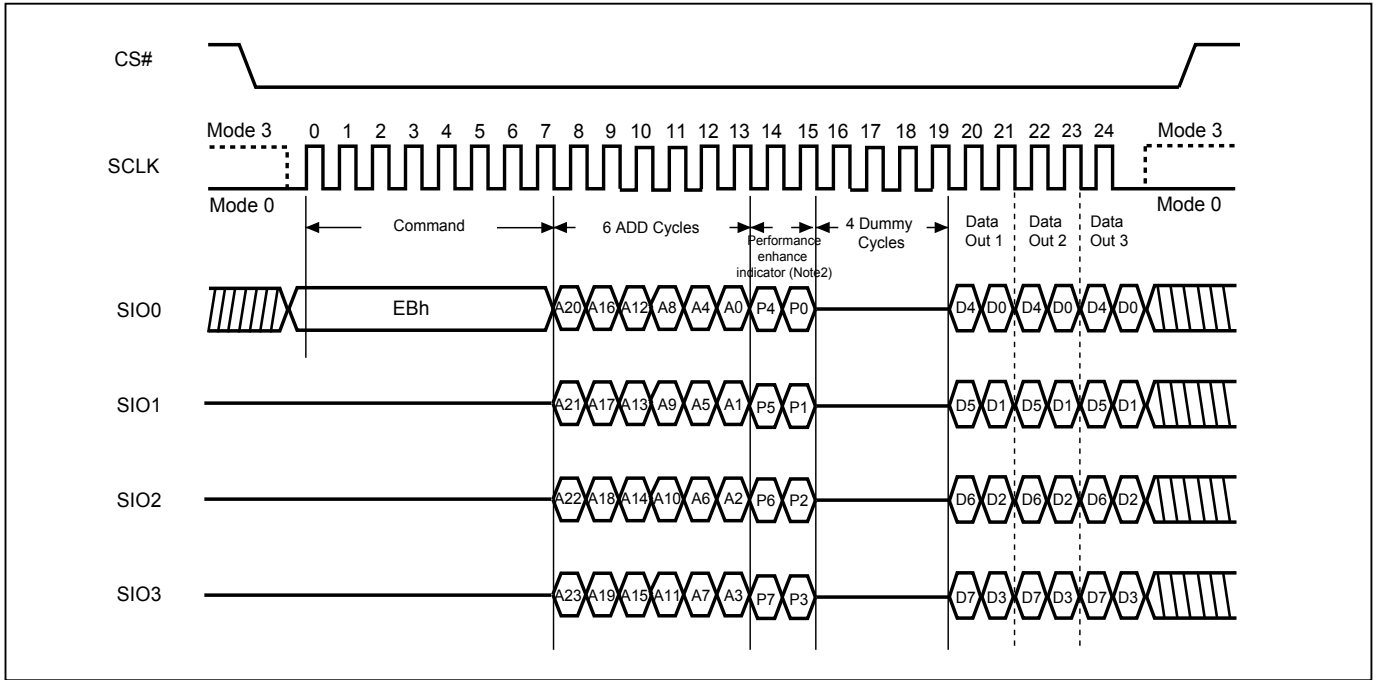
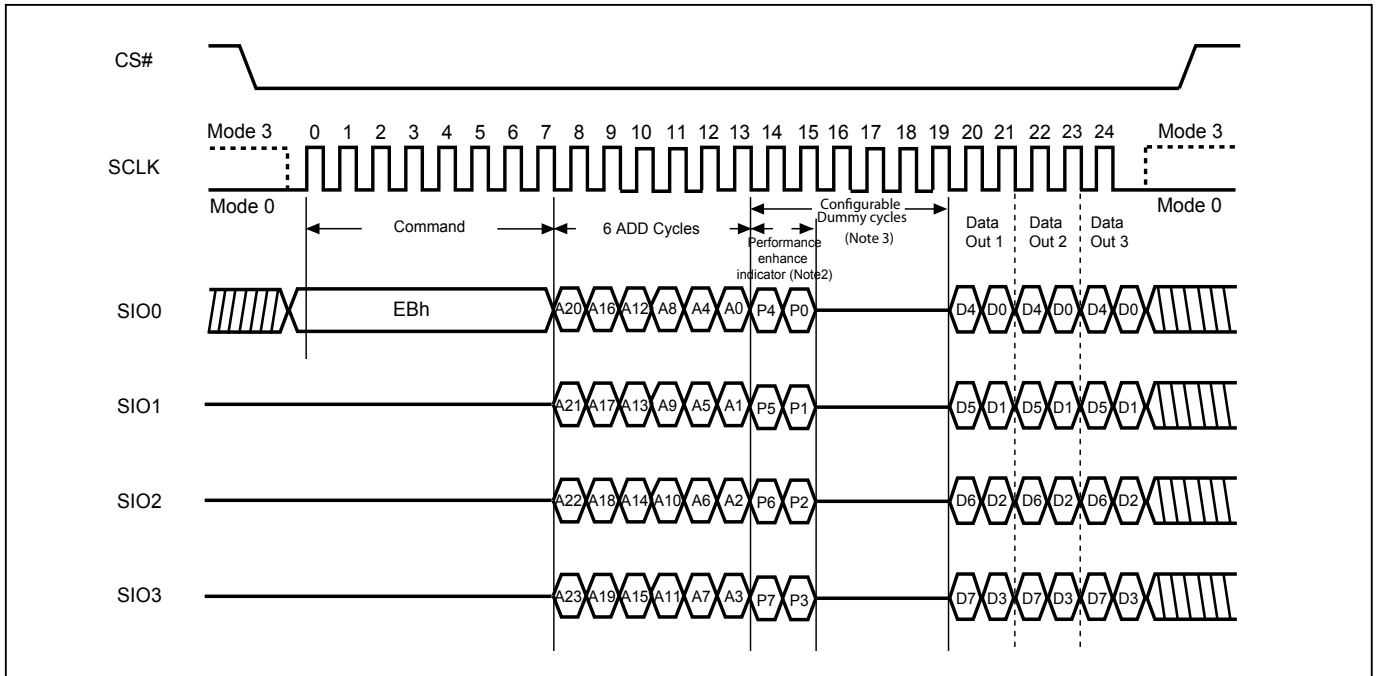


Figure 33. 4 x I/O Read Mode Sequence (SPI Mode), for MX25U12835FZNI-08G only



Note:

1. Hi-impedance is inhibited for the two clock cycles.
2. P7≠P3, P6≠P2, P5≠P1 & P4≠P0 (Toggling) is inhibited.
3. The Configurable Dummy Cycle (default = 6) is set by Configuration Register Bit . Please check ["Dummy Cycle and Frequency Table"](#) for details.

Figure 34. 4 x I/O Read Mode Sequence (QPI Mode)

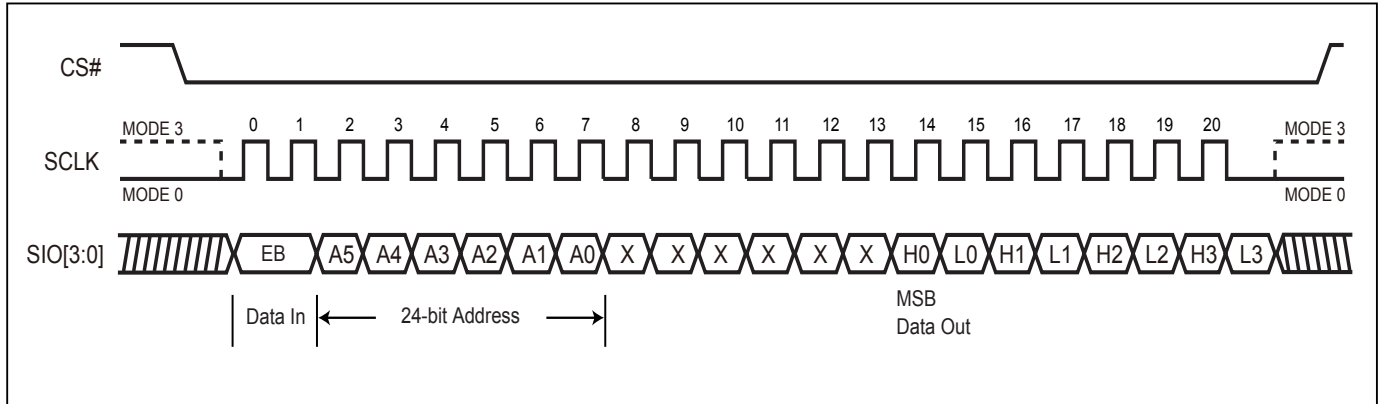
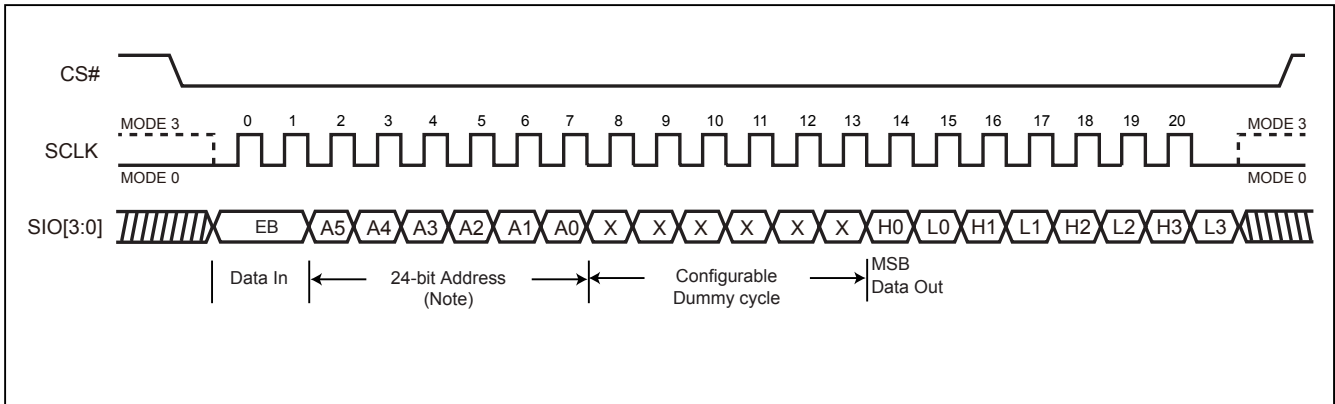
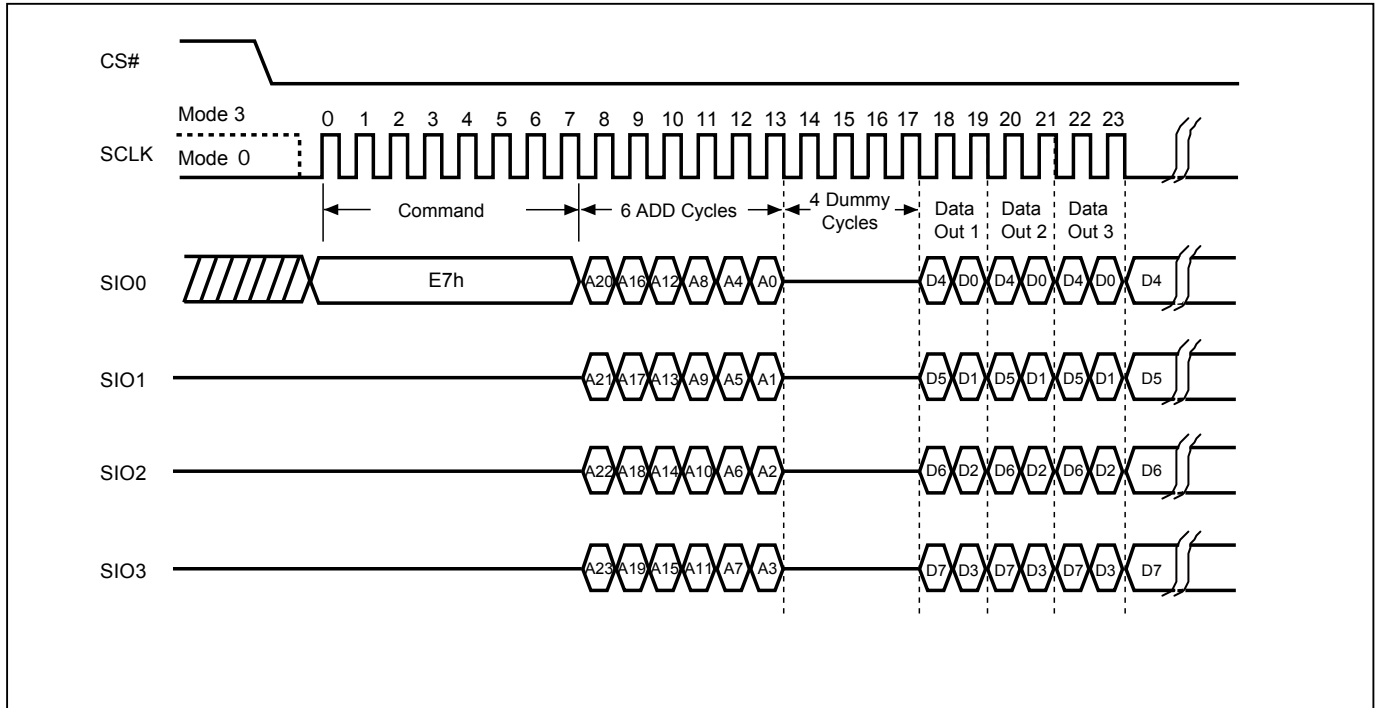


Figure 35. 4 x I/O Read Mode Sequence (QPI Mode), for MX25U12835FZNI-08G only



Note: The Configurable Dummy Cycle (default = 6) is set by Configuration Register Bit. Please check ["Dummy Cycle and Frequency Table"](#) for details.

Figure 36. W4READ (Quad Read with 4 dummy cycles) Sequence



9-16. Burst Read

This device supports Burst Read in both SPI and QPI mode.

To set the Burst length, following command operation is required

Issuing command: “C0h” in the first Byte (8-clocks), following 4 clocks defining wrap around enable with “0h” and disable with “1h”.

Next 4 clocks is to define wrap around depth. Definition as following table:

| Data | Wrap Around | Wrap Depth |
|------|-------------|------------|
| 00h | Yes | 8-byte |
| 01h | Yes | 16-byte |
| 02h | Yes | 32-byte |
| 03h | Yes | 64-byte |
| 1xh | No | X |

The wrap around unit is defined within the 256Byte page, with random initial address. It’s defined as “wrap-around mode disable” for the default state of the device. To exit wrap around, it is required to issue another “C0h” command in which data=‘1xh’. Otherwise, wrap around status will be retained until power down or reset command. To change wrap around depth, it is required to issue another “C0h” command in which data=“0xh”. QPI “0Bh” “EBh” and SPI “EBh” “E7h” support wrap around feature after wrap around enable. However, the RDID command is default without Burst read.

Figure 37. Burst Read (SPI Mode)

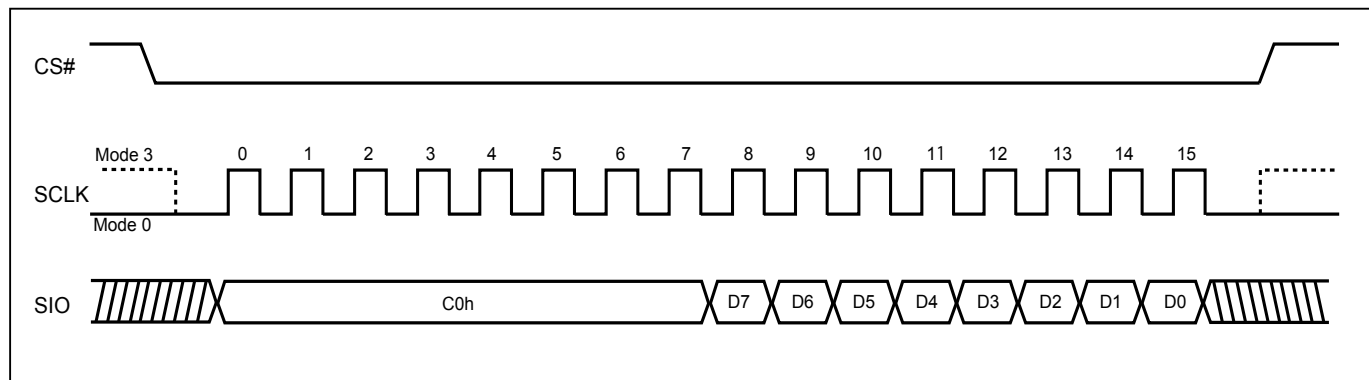
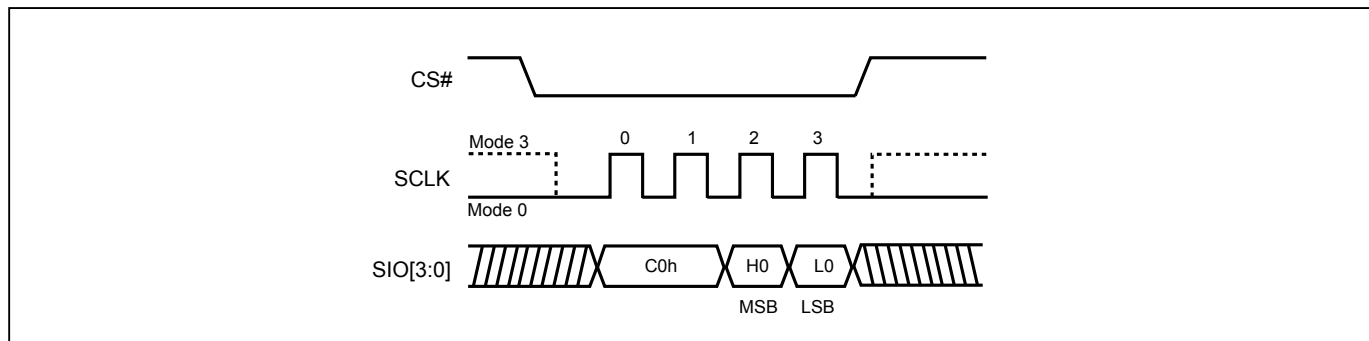


Figure 38. Burst Read (QPI Mode)



Note: MSB=Most Significant Bit
LSB=Least Significant Bit

9-17. Performance Enhance Mode

The device could waive the command cycle bits if the two cycle bits after address cycle toggles.

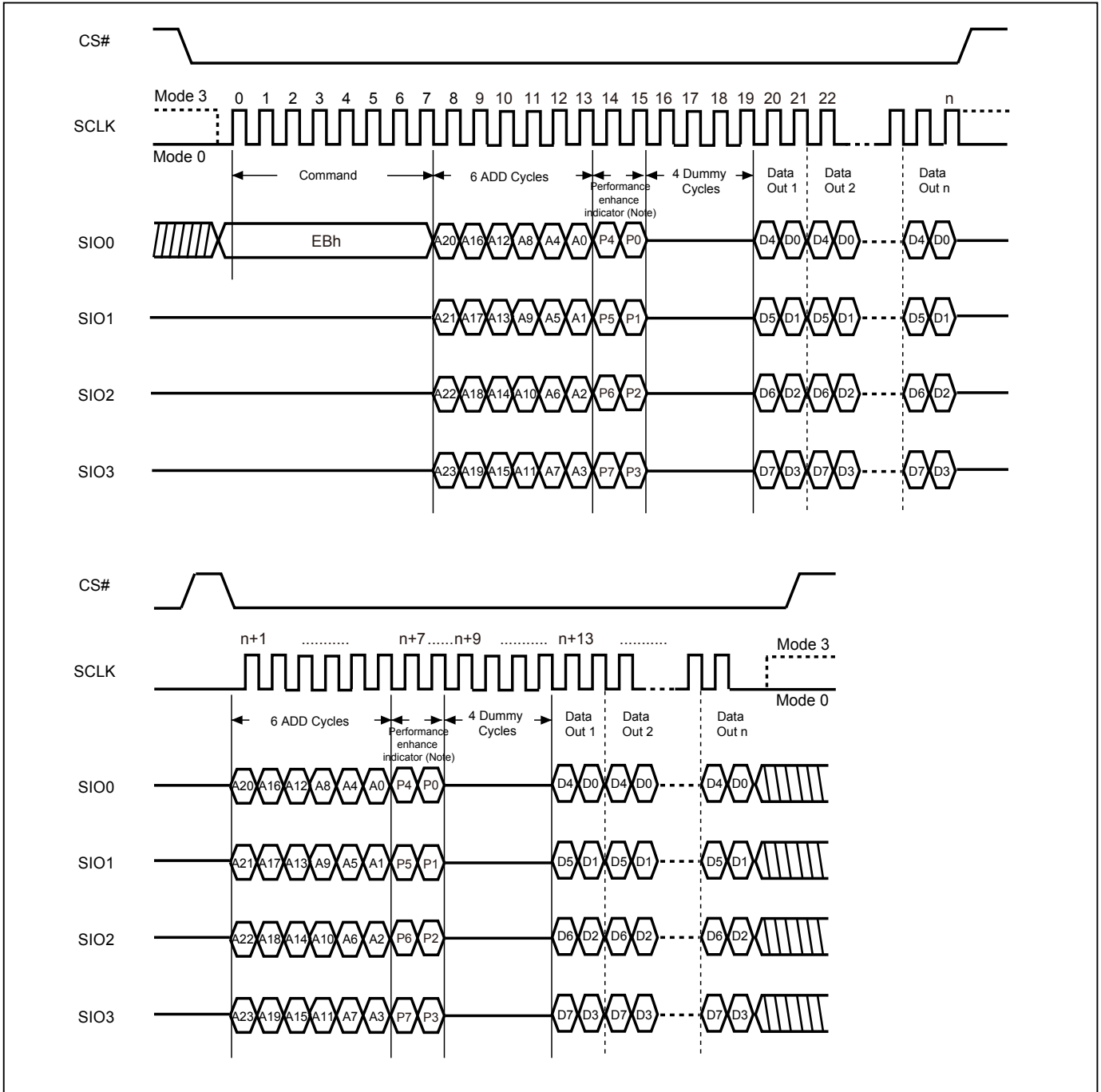
Performance enhance mode is supported in both SPI and QPI mode.

In QPI mode, "EBh" "0Bh" and SPI "EBh" "E7h" commands support enhance mode. The performance enhance mode is not supported in dual I/O mode.

After entering enhance mode, following CS# go high, the device will stay in the read mode and treat CS# go low of the first clock as address instead of command cycle.

To exit enhance mode, a new fast read command whose first two dummy cycles is not toggle then exit. Or issue "FFh" data cycle to exit enhance mode.

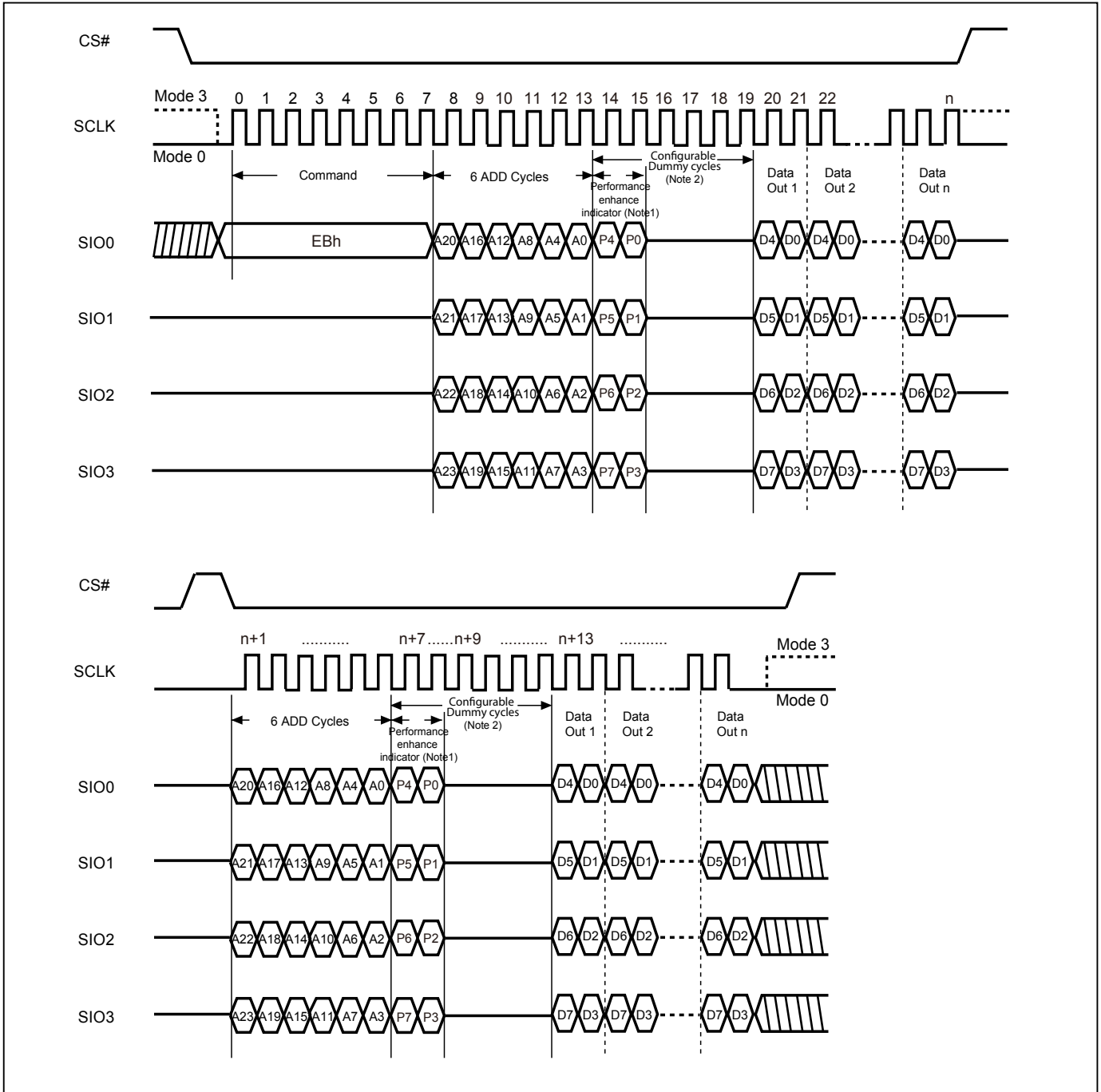
Figure 39. 4 x I/O Read Performance Enhance Mode Sequence (SPI Mode)



Note:

1. Performance enhance mode, if $P7 \neq P3$ & $P6 \neq P2$ & $P5 \neq P1$ & $P4 \neq P0$ (Toggling), ex: A5, 5A, 0F, if not using performance enhance recommend to keep 1 or 0 in performance enhance indicator.
2. Reset the performance enhance mode, if $P7 = P3$ or $P6 = P2$ or $P5 = P1$ or $P4 = P0$, ex: AA, 00, FF.

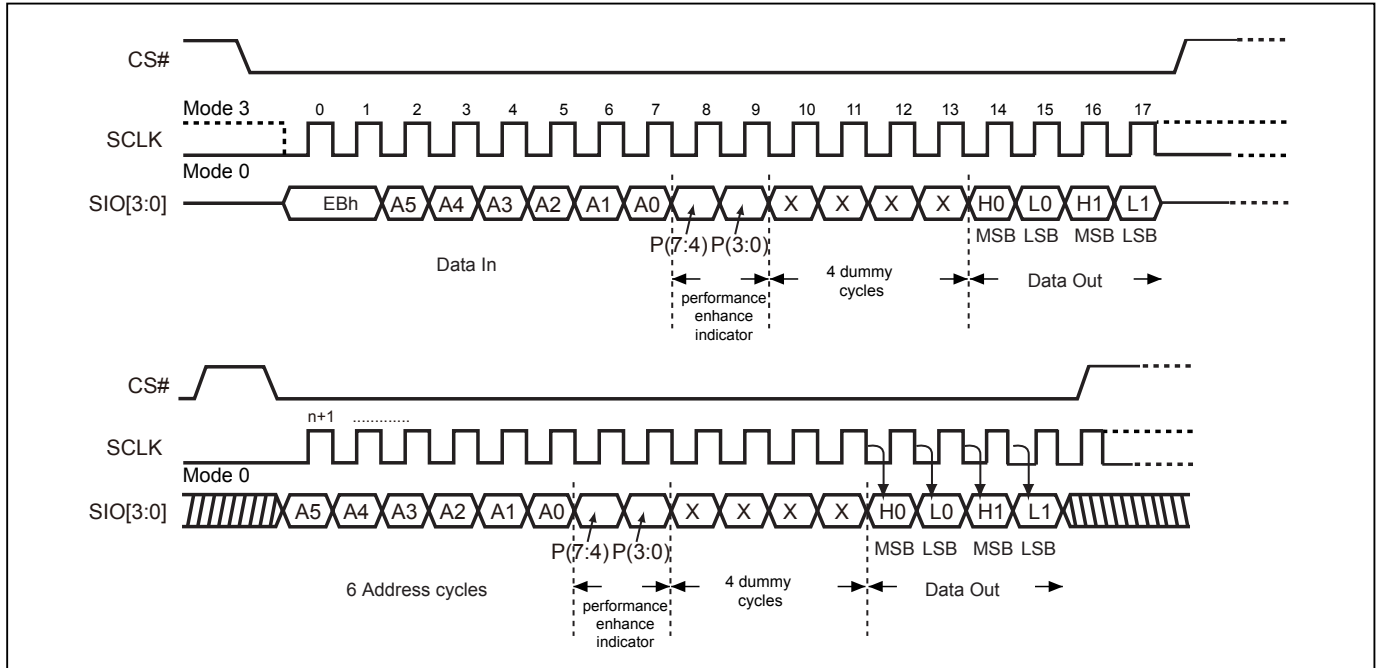
Figure 40. 4 x I/O Read Performance Enhance Mode Sequence (SPI Mode), for MX25U12835FZNI-08G only



Note:

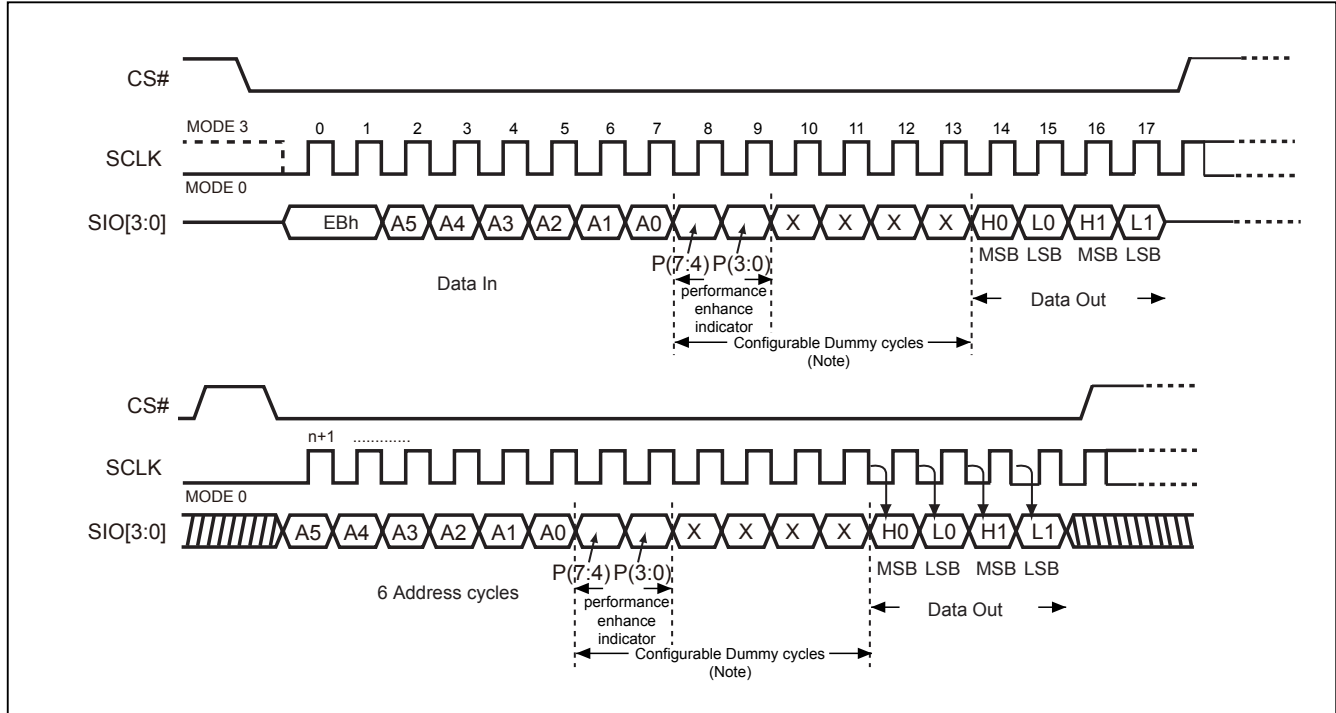
1. Performance enhance mode, if $P7 \neq P3$ & $P6 \neq P2$ & $P5 \neq P1$ & $P4 \neq P0$ (Toggling), ex: A5, 5A, 0F, if not using performance enhance recommend to keep 1 or 0 in performance enhance indicator.
Reset the performance enhance mode, if $P7 = P3$ or $P6 = P2$ or $P5 = P1$ or $P4 = P0$, ex: AA, 00, FF.
2. The Configurable Dummy Cycle (default = 6) is set by Configuration Register Bit. Please refer to ["Dummy Cycle and Frequency Table"](#) for details.

Figure 41. 4 x I/O Read Performance Enhance Mode Sequence (QPI Mode)



Note: Reset the performance enhance mode, if P7=P3 or P6=P2 or P5=P1 or P4=P0, ex: AA, 00, FF.

Figure 42. 4 x I/O Read Performance Enhance Mode Sequence (QPI Mode), for MX25U12835FZNI-08G only



Note:

1. The Configurable Dummy Cycle (default = 6) is set by Configuration Register Bit . Please refer to ["Dummy Cycle and Frequency Table"](#) for details.
2. Reset the performance enhance mode, if P7=P3 or P6=P2 or P5=P1 or P4=P0, ex: AA, 00, FF.

9-18. Sector Erase (SE)

The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". The instruction is used for any 4K-byte sector. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector (Please refer to "Table 4. Memory Organization") is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of the address been latched-in); otherwise, the instruction will be rejected and not executed.

Address bits [Am-A12] (Am is the most significant address) select the sector address.

The sequence of issuing SE instruction is: CS# goes low→ sending SE instruction code→ 3-byte address on SI→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are "don't care" in SPI mode.

The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Sector Erase cycle is in progress. The WIP sets during the tSE timing, and clears when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the sector is protected by BP3, BP2, BP1, BP0 bits, the Sector Erase (SE) instruction will not be executed on the sector.

Figure 43. Sector Erase (SE) Sequence (SPI Mode)

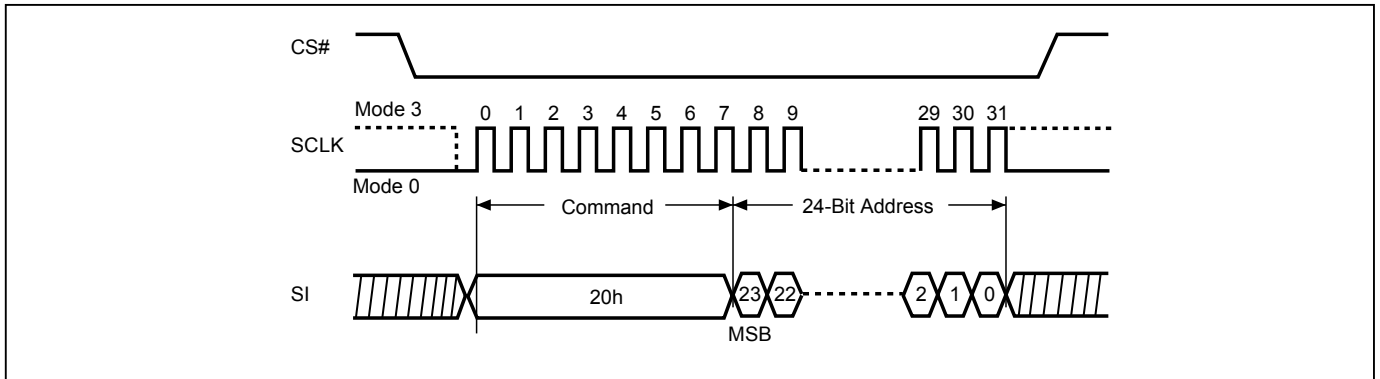
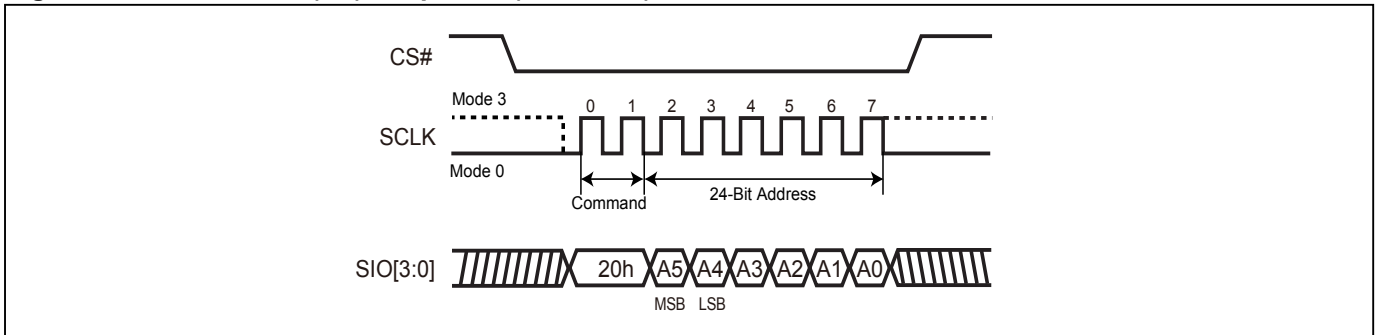


Figure 44. Sector Erase (SE) Sequence (QPI Mode)



9-19. Block Erase (BE32K)

The Block Erase (BE32K) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 32K-byte block erase operation. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE32K). Any address of the block (Please refer to "Table 4. Memory Organization") is a valid address for Block Erase (BE32K) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE32K instruction is: CS# goes low→ sending BE32K instruction code→ 3-byte address on SI→CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are "don't care" in SPI mode.

The self-timed Block Erase Cycle time (tBE32K) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Block Erase cycle is in progress. The WIP sets 1 during the tBE32K timing, and sets 0 when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the block is protected by BP3, BP2, BP1, BP0 bits, the Block Erase (tBE32K) instruction will not be executed on the block.

Figure 45. Block Erase 32KB (BE32K) Sequence (SPI Mode)

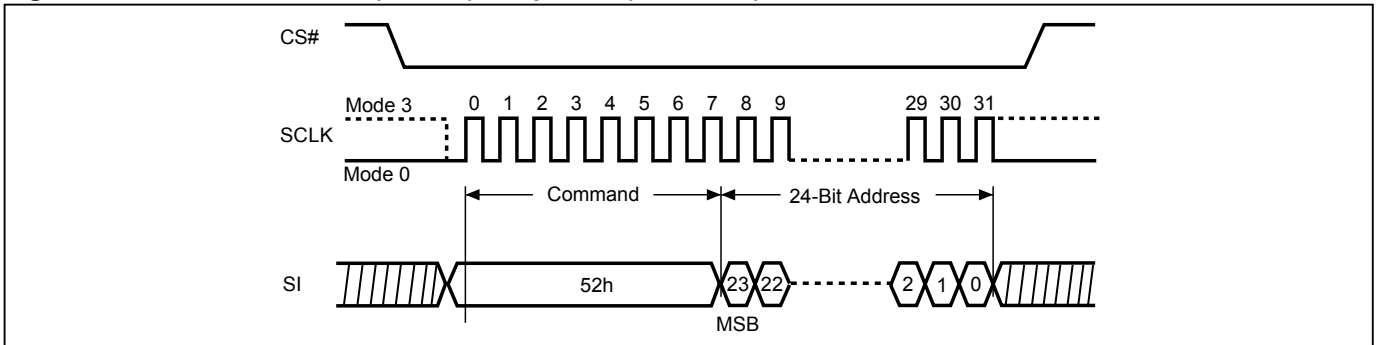
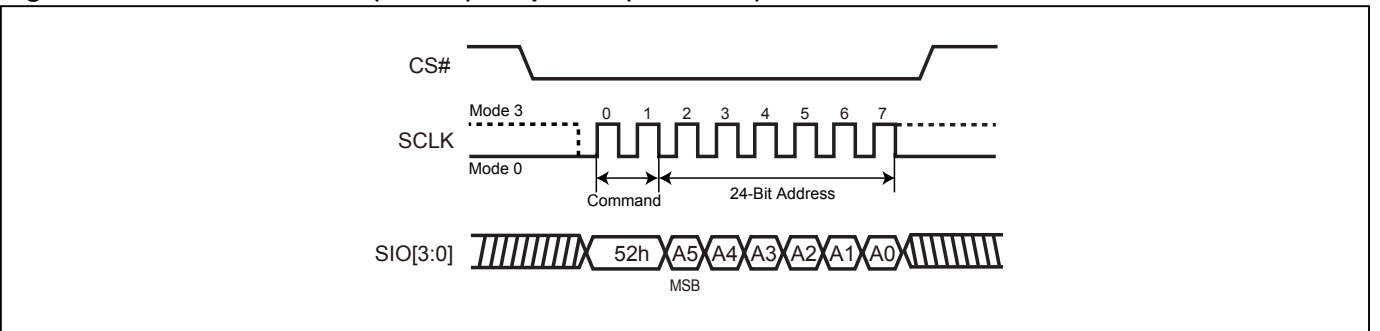


Figure 46. Block Erase 32KB (BE32K) Sequence (QPI Mode)



9-20. Block Erase (BE)

The Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte block erase operation. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any address of the block (Please refer to "Table 4. Memory Organization") is a valid address for Block Erase (BE) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE instruction is: CS# goes low → sending BE instruction code → 3-byte address on SI → CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are "don't care" in SPI mode.

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Block Erase cycle is in progress. The WIP sets during the tBE timing, and clears when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the block is protected by BP3, BP2, BP1, BP0 bits, the Block Erase (BE) instruction will not be executed on the block.

Figure 47. Block Erase (BE) Sequence (SPI Mode)

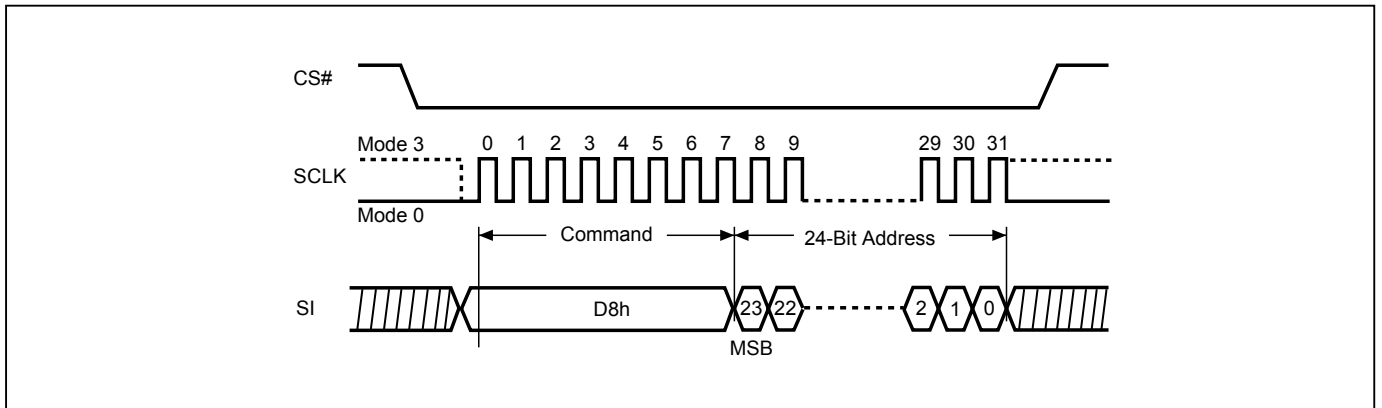
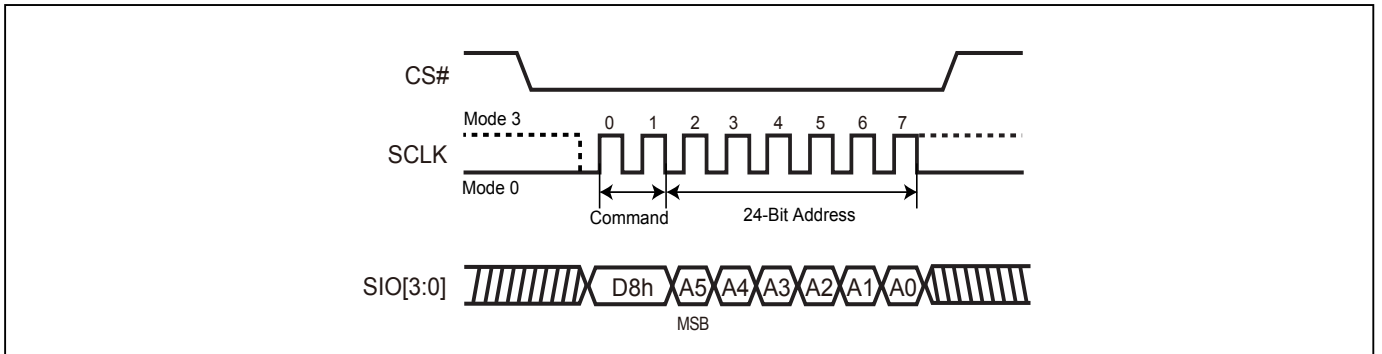


Figure 48. Block Erase (BE) Sequence (QPI Mode)



9-21. Chip Erase (CE)

The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). The CS# must go high exactly at the byte boundary, otherwise the instruction will be rejected and not executed.

The sequence of issuing CE instruction is: CS# goes low→sending CE instruction code→CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are "don't care" in SPI mode.

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Chip Erase cycle is in progress. The WIP sets during the tCE timing, and clears when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the chip is protected by BP3, BP2, BP1, BP0 bits, the Chip Erase (CE) instruction will not be executed. It will be only executed when BP3, BP2, BP1, BP0 all set to "0".

Figure 49. Chip Erase (CE) Sequence (SPI Mode)

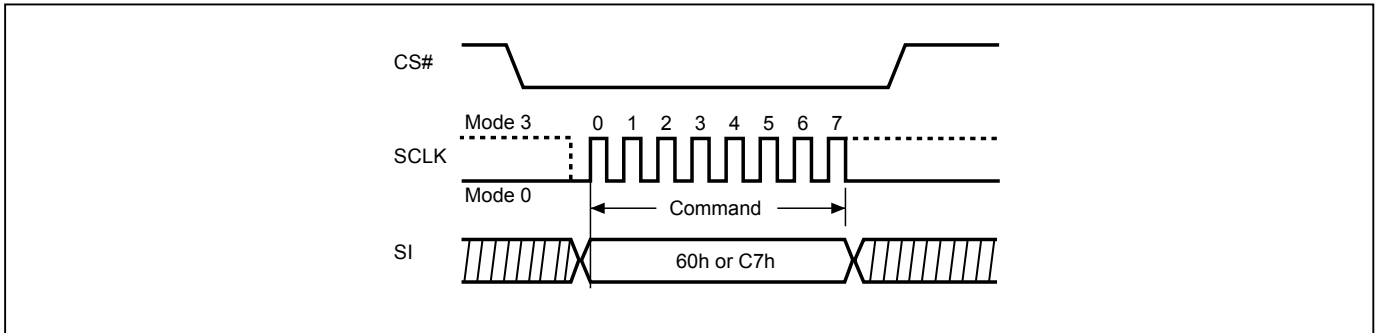
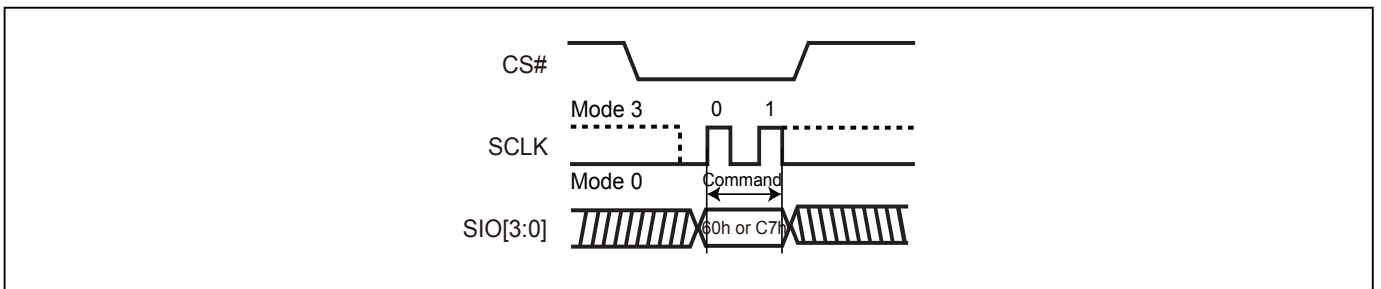


Figure 50. Chip Erase (CE) Sequence (QPI Mode)



9-22. Page Program (PP)

The Page Program (PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). The device programs only the last 256 data bytes sent to the device. The last address byte (the 8 least significant address bits, A7-A0) should be set to 0 for 256 bytes page program. If A7-A0 are not all zero, transmitted data that exceed page length are programmed from the starting address (24-bit address that last 8 bit are all 0) of currently selected page. If the data bytes sent to the device exceeds 256, the last 256 data byte is programmed at the request page and previous data will be disregarded. If the data bytes sent to the device has not exceeded 256, the data will be programmed at the request address of the page. There will be no effort on the other data bytes of the same page.

The sequence of issuing PP instruction is: CS# goes low→ sending PP instruction code→ 3-byte address on SI→ at least 1-byte on data on SI→ CS# goes high.

The CS# must be kept low during the whole Page Program cycle; The CS# must go high exactly at the byte boundary (the latest eighth bit of data being latched in), otherwise the instruction will be rejected and will not be executed.

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Page Program cycle is in progress. The WIP sets 1 during the tPP timing, and sets 0 when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP3, BP2, BP1, BP0 bits, the Page Program (PP) instruction will not be executed.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are "don't care" in SPI mode.

Figure 51. Page Program (PP) Sequence (SPI Mode)

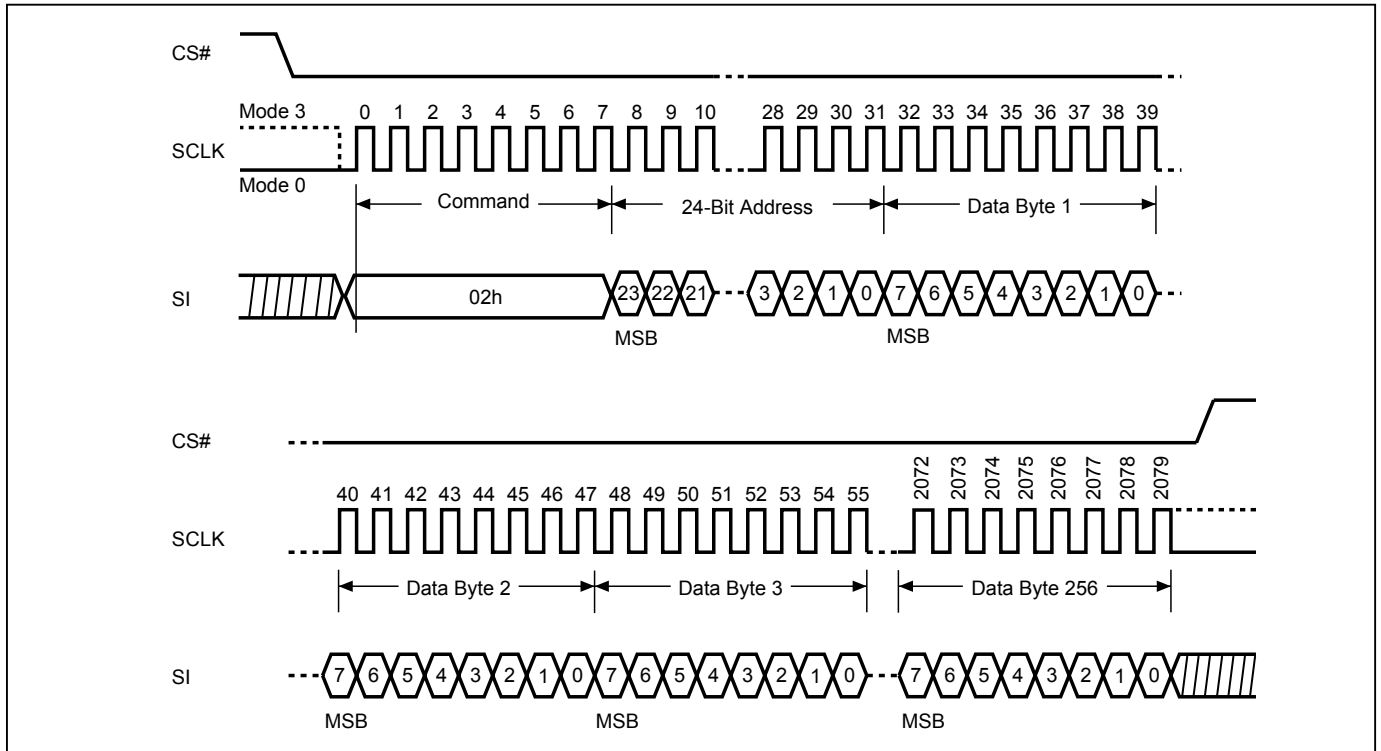
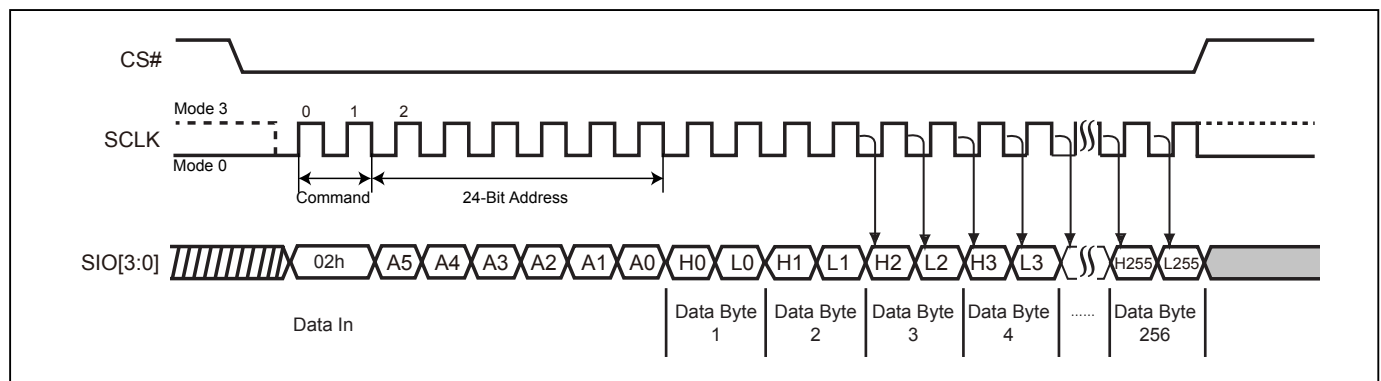


Figure 52. Page Program (PP) Sequence (QPI Mode)

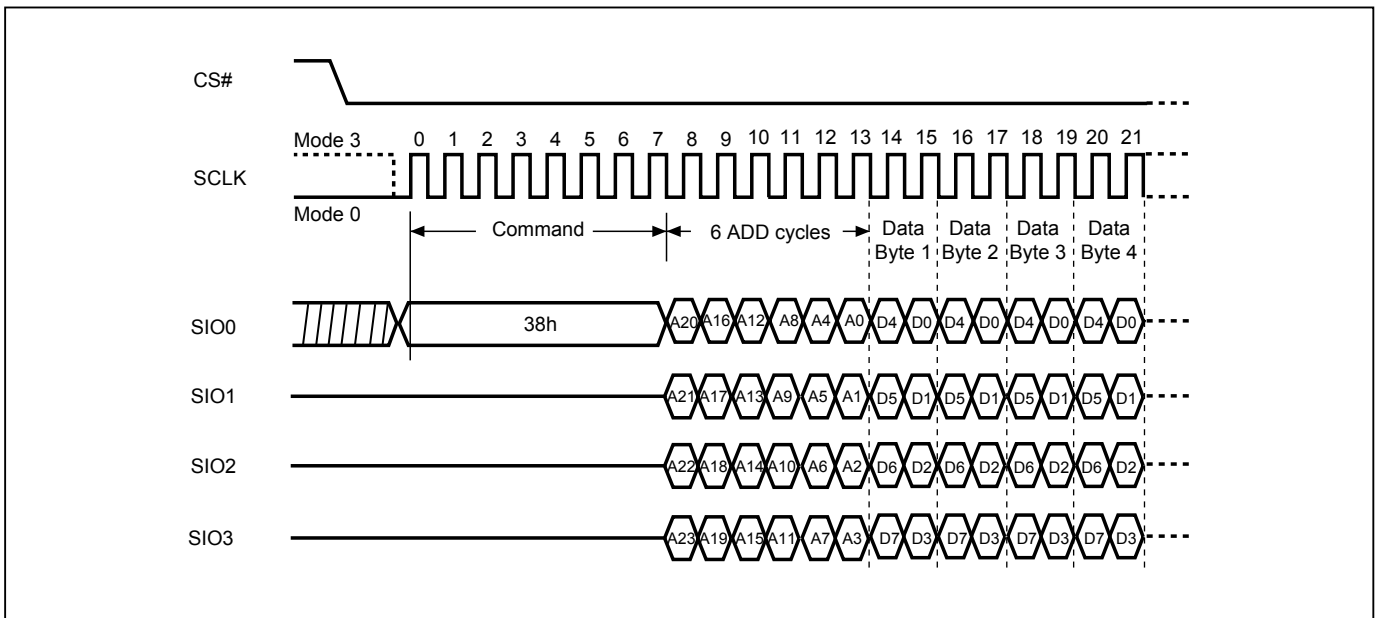


9-23. 4 x I/O Page Program (4PP)

The Quad Page Program (4PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit and Quad Enable (QE) bit must be set to "1" before sending the Quad Page Program (4PP). The Quad Page Programming takes four pins: SIO0, SIO1, SIO2, and SIO3 as address and data input, which can improve programmer performance and the effectiveness of application. The 4PP operation frequency supports as fast as 104MHz. The other function descriptions are as same as standard page program.

The sequence of issuing 4PP instruction is: CS# goes low→ sending 4PP instruction code→ 3-byte address on SIO[3:0]→ at least 1-byte on data on SIO[3:0]→CS# goes high.

Figure 53. 4 x I/O Page Program (4PP) Sequence (SPI Mode only)



9-24. Deep Power-down (DP)

The Deep Power-down (DP) instruction is for setting the device on the minimizing the power consumption (to entering the Deep Power-down mode), the standby current is reduced from ISB1 to ISB2). The Deep Power-down mode requires the Deep Power-down (DP) instruction to enter, during the Deep Power-down mode, the device is not active and all Write/Program/Erase instruction are ignored. When CS# goes high, it's only in deep power-down mode not standby mode. It's different from Standby mode.

The sequence of issuing DP instruction is: CS# goes low→sending DP instruction code→CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are "don't care" in SPI mode.

Once the DP instruction is set, all instructions will be ignored except the Release from Deep Power-down mode (RDP) and Read Electronic Signature (RES) instruction and softreset command. (those instructions allow the ID being reading out). When Power-down, or software reset command the deep power-down mode automatically stops, and when power-up, the device automatically is in standby mode. For DP instruction the CS# must go high exactly at the byte boundary (the latest eighth bit of instruction code been latched-in); otherwise, the instruction will not be executed. As soon as Chip Select (CS#) goes high, a delay of t_{DP} is required before entering the Deep Power-down mode.

Figure 54. Deep Power-down (DP) Sequence (SPI Mode)

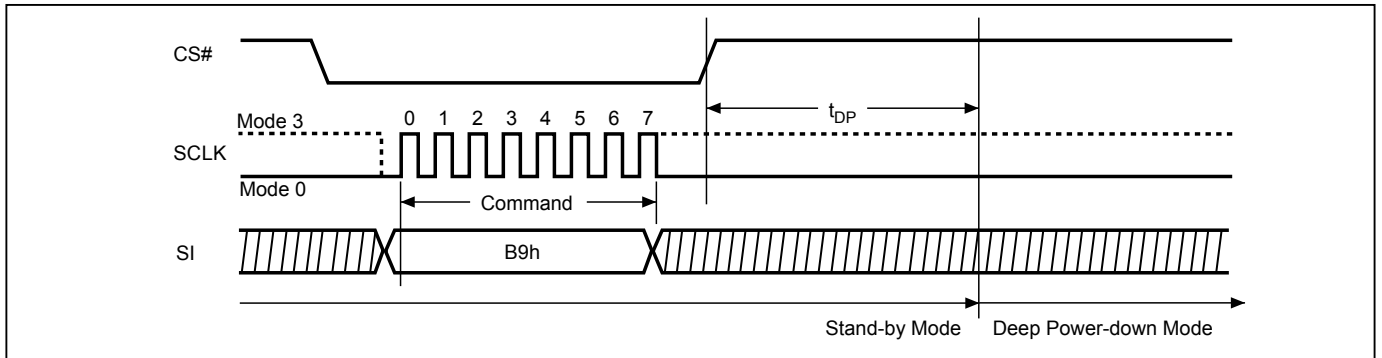
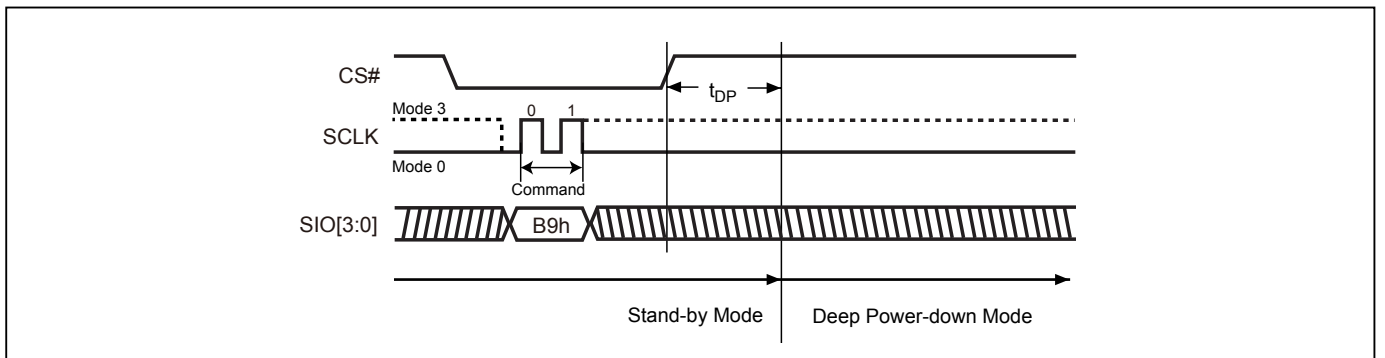


Figure 55. Deep Power-down (DP) Sequence (QPI Mode)



9-25. Enter Secured OTP (ENSO)

The ENSO instruction is for entering the additional 4K-bit secured OTP mode. The additional 4K-bit secured OTP is independent from main array, which may use to store unique serial number for system identifier. After entering the Secured OTP mode, and then follow standard read or program procedure to read out the data or update data. The Secured OTP data cannot be updated again once it is lock-down.

The sequence of issuing ENSO instruction is: CS# goes low→ sending ENSO instruction to enter Secured OTP mode→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are "don't care" in SPI mode.

Please note that WRSR/WRSCUR commands are not acceptable during the access of secure OTP region, once security OTP is lock down, only read related commands are valid.

9-26. Exit Secured OTP (EXSO)

The EXSO instruction is for exiting the additional 4K-bit secured OTP mode.

The sequence of issuing EXSO instruction is: CS# goes low→ sending EXSO instruction to exit Secured OTP mode→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are "don't care" in SPI mode.

9-27. Read Security Register (RDSCUR)

The RDSCUR instruction is for reading the value of Security Register bits. The Read Security Register can be read at any time (even in program/erase/write status register/write security register condition) and continuously.

The sequence of issuing RDSCUR instruction is : CS# goes low→sending RDSCUR instruction→Security Register data out on SO→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are "don't care" in SPI mode.

The definition of the Security Register bits is as below:

Secured OTP Indicator bit. The Secured OTP indicator bit shows the secured OTP area is locked by factory before exit factory or not. When it is "0", it indicates non-factory lock; "1" indicates factory-lock.

Lock-down Secured OTP (LDSO) bit. By writing WRSCUR instruction, the LDSO bit may be set to "1" for customer lock-down purpose. However, once the bit is set to "1" (lock-down), the LDSO bit and the 4K-bit Secured OTP area cannot be update any more. While it is in 4K-bit secured OTP mode, main array access is not allowed.

Table 9. Security Register Definition

| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---|---|---|--------------|--|--|---|--|
| WPSEL | E_FAIL | P_FAIL | Reserved | ESB (Erase Suspend bit) | PSB (Program Suspend bit) | LDSO (indicate if lock-down) | Secured OTP indicator bit |
| 0=BP protection mode 1=individual mode (default=0) | 0=normal Erase succeed 1=individual Erase failed (default=0) | 0=normal Program succeed 1=indicate Program failed (default=0) | - | 0=Erase is not suspended 1= Erase suspended (default=0) | 0=Program is not suspended 1= Program suspended (default=0) | 0 = not lock-down 1 = lock-down (cannot program/erase OTP) | 0 = non-factory lock 1 = factory lock |
| Non-volatile bit (OTP) | Volatile bit | Volatile bit | Volatile bit | Volatile bit | Volatile bit | Non-volatile bit (OTP) | Non-volatile bit (OTP) |

9-28. Write Security Register (WRSCUR)

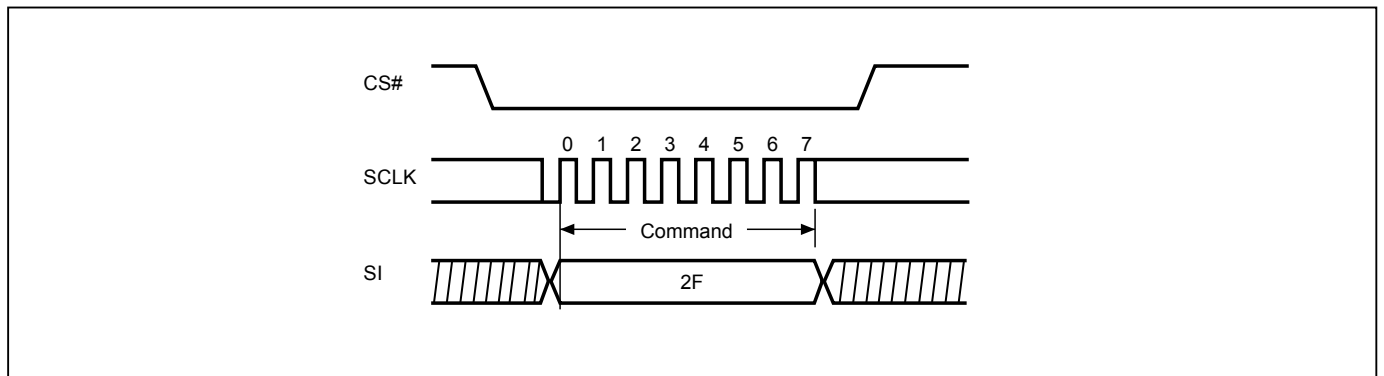
The WRSCUR instruction is for setting the values of Security Register Bits. The WREN (Write Enable) instruction is required before issuing WRSCUR instruction. The WRSCUR instruction may change the values of bit1 (LDSO bit) for customer to lock-down the 4K-bit Secured OTP area. Once the LDSO bit is set to "1", the Secured OTP area cannot be updated any more. The LDSO bit is an OTP bit. Once the LDSO bit is set, the value of LDSO bit can not be altered any more.

The sequence of issuing WRSCUR instruction is :CS# goes low→ sending WRSCUR instruction → CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are "don't care" in SPI mode.

The CS# must go high exactly at the boundary; otherwise, the instruction will be rejected and not executed.

Figure 56. Write Security Register (WRSCUR) Sequence (Command 2F)



9-29. Write Protection Selection (WPSEL)

There are two write protection methods, (1) BP protection mode (2) individual block protection mode. If WPSEL=0, flash is under BP protection mode. If WPSEL=1, flash is under individual block protection mode. The default value of WPSEL is “0”. WPSEL command can be used to set WPSEL=1. **Please note that WPSEL is an OTP bit. Once WPSEL is set to 1, there is no chance to recover WPSEL bit back to “0”.** If the flash is under BP mode, the individual block protection mode is disabled. Contrarily, if flash is on the individual block protection mode, the BP mode is disabled.

Every time after the system is powered-on, and the Security Register bit 7 is checked to be WPSEL=1, all the blocks or sectors will be write protected by default. User may only unlock the blocks or sectors via SBULK and GBULK instruction. Program or erase functions can only be operated after the Unlock instruction is conducted.

BP protection mode, WPSEL=0:

ARRAY is protected by BP3-BP0 and BP3-BP0 bits are protected by “SRWD=1 and WP#=0”, where SRWD is bit 7 of status register that can be set by WRSR command.

Individual block protection mode, WPSEL=1:

Blocks are individually protected by their own SRAM lock bits which are set to “1” after power up. SBULK and SBLK command can set SRAM lock bit to “0” and “1”. When the system accepts and executes WPSEL instruction, the bit 7 in security register will be set. It will activate SBLK, SBULK, RDBLOCK, GBLK, GBULK etc instructions to conduct block lock protection and replace the original Software Protect Mode (SPM) use (BP3-BP0) indicated block methods. Under the individual block protection mode (WPSEL=1), hardware protection is performed by driving WP#=0. Once WP#=0 all array blocks/sectors are protected regardless of the contents of SRAM lock bits.

The sequence of issuing WPSEL instruction is: CS# goes low → sending WPSEL instruction to enter the individual block protect mode → CS# goes high. Please refer to *"Figure 59. Write Protection Selection (WPSEL) Sequence (Command 68)"*.

WPSEL instruction function flow is as follows:

Figure 57. BP and SRWD if WPSEL=0

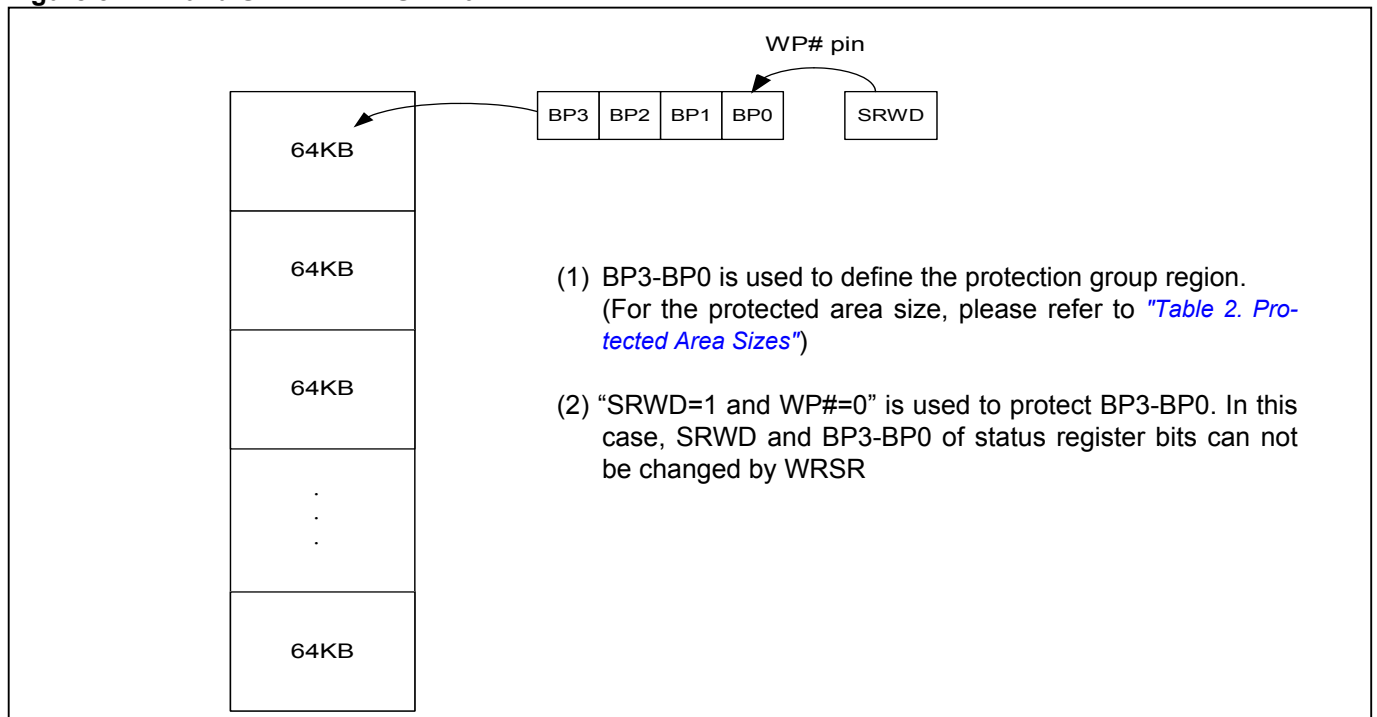


Figure 58. The individual block lock mode is effective after setting WPSEL=1

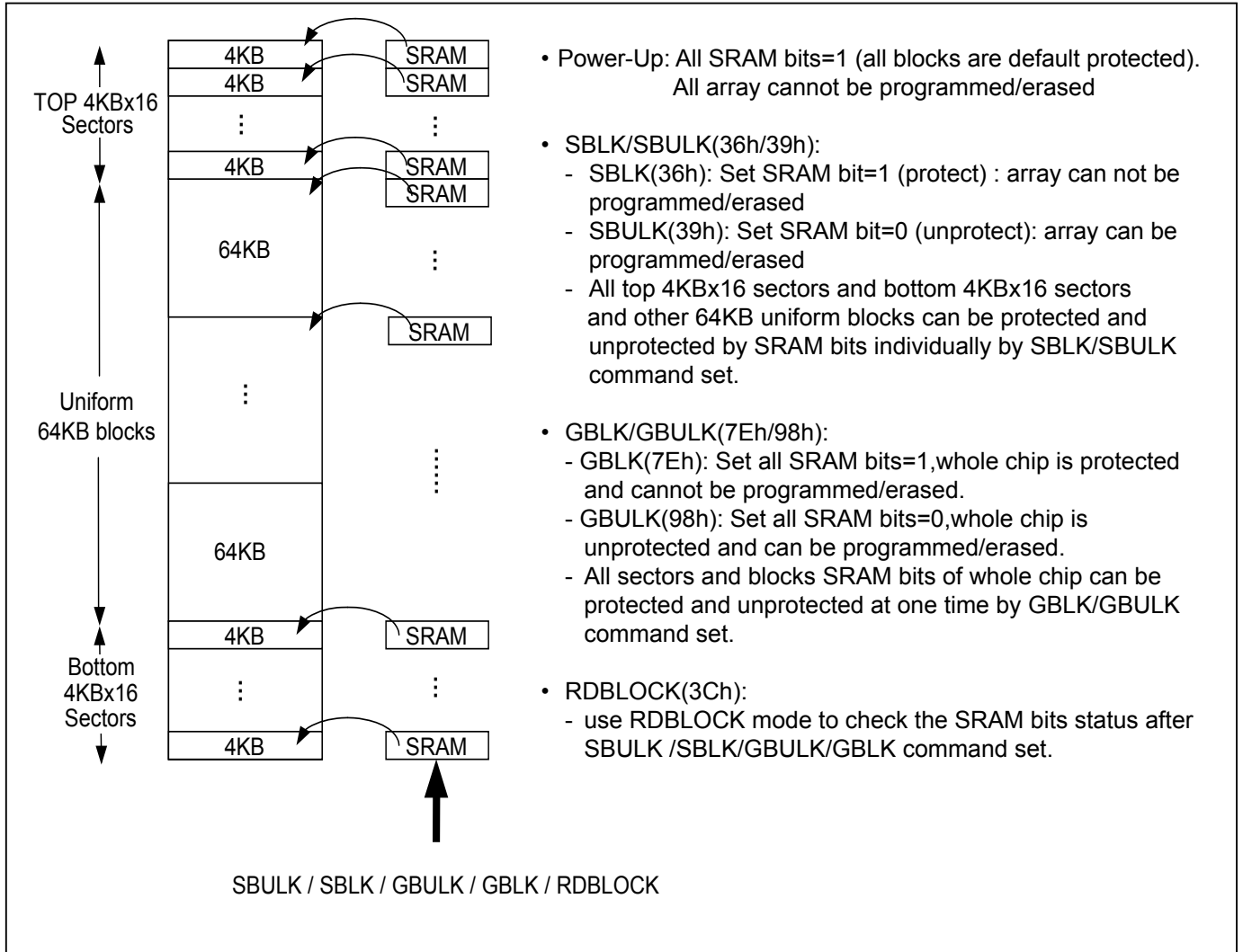


Figure 59. Write Protection Selection (WPSEL) Sequence (Command 68)

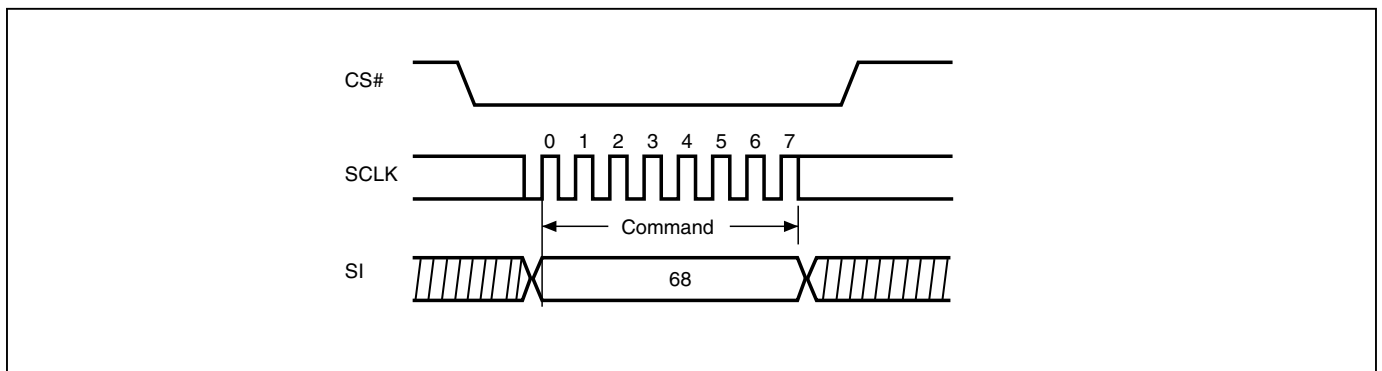
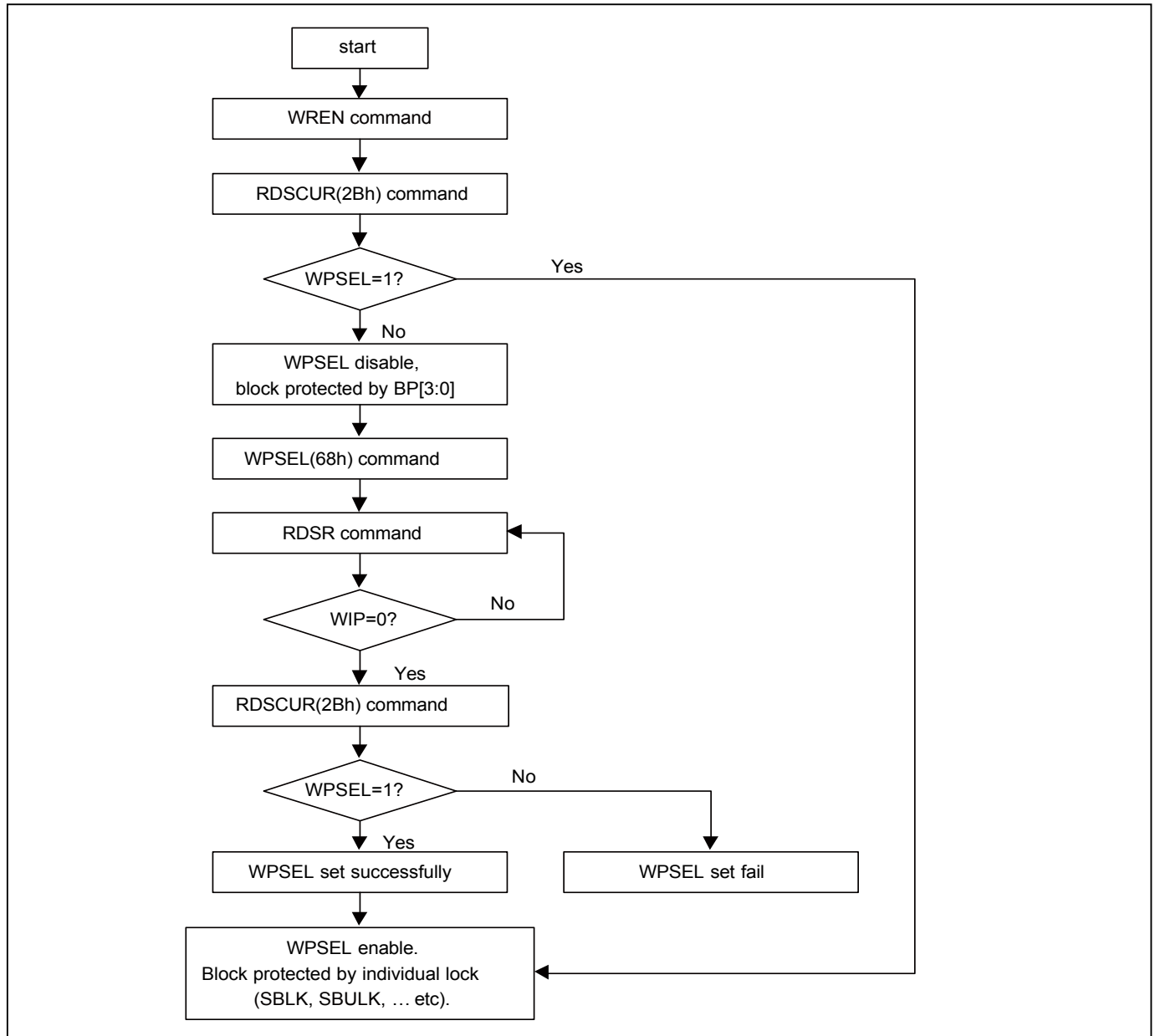


Figure 60. WPSEL Flow

9-30. Single Block Lock/Unlock Protection (SBLK/SBULK)

These instructions are only effective after WPSEL was executed. The SBLK instruction is for write protection a specified block (or sector) of memory, using $A_{MAX}-A16$ or ($A_{MAX}-A12$) address bits to assign a 64Kbyte block (or 4K bytes sector) to be protected as read only. The SBULK instruction will cancel the block (or sector) write protection state. This feature allows user to stop protecting the entire block (or sector) through the chip unprotect command (GBULK).

The WREN (Write Enable) instruction is required before issuing SBLK/SBULK instruction.

The sequence of issuing SBLK/SBULK instruction is: CS# goes low → send SBLK/SBULK (36h/39h) instruction → send 3-byte address assign one block (or sector) to be protected on SI pin → CS# goes high. The CS# must go high exactly at the byte boundary, otherwise the instruction will be rejected and not be executed.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are "don't care" in SPI mode.

SBLK/SBULK instruction function flow is as follows:

Figure 61. Block Lock Flow

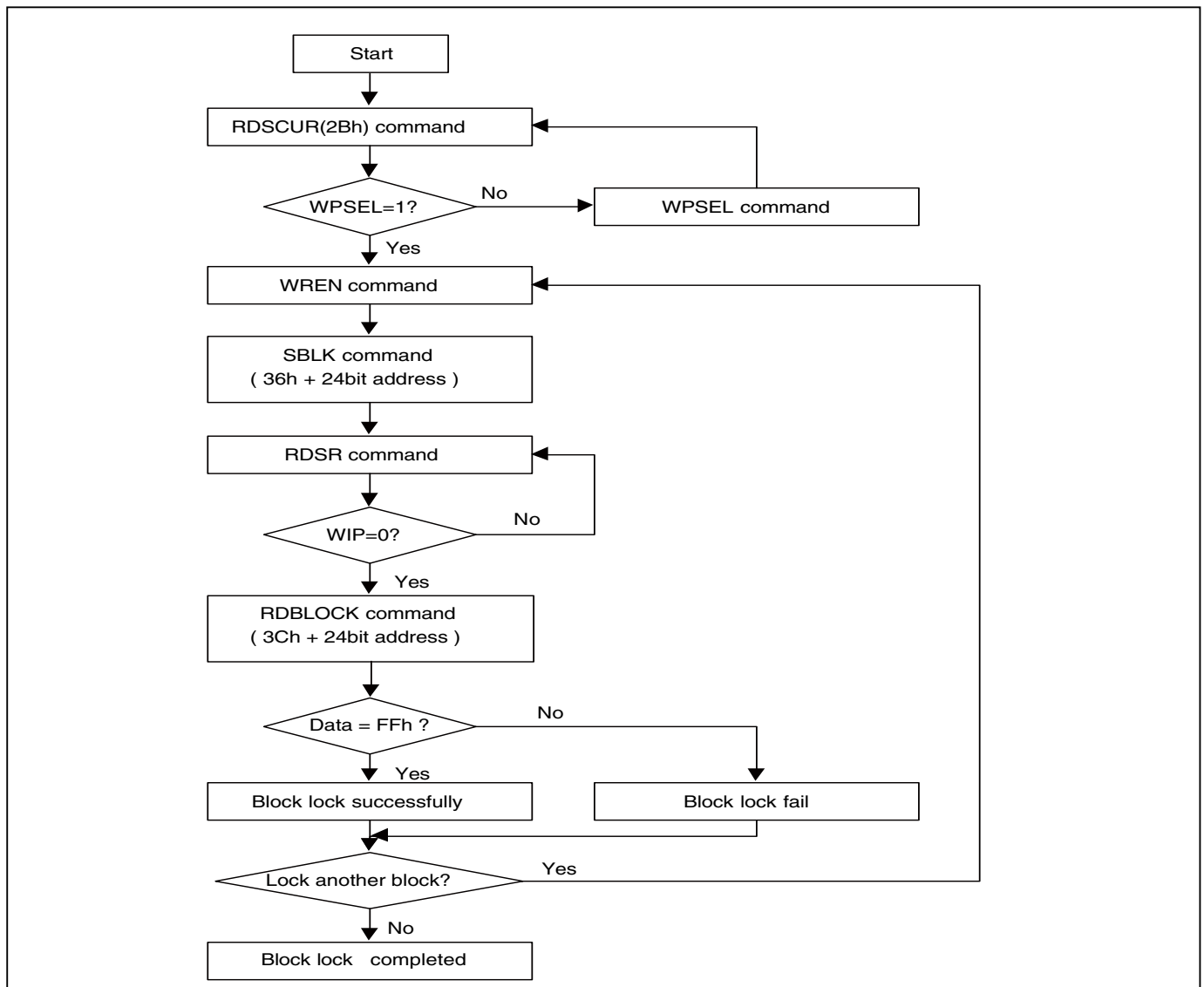
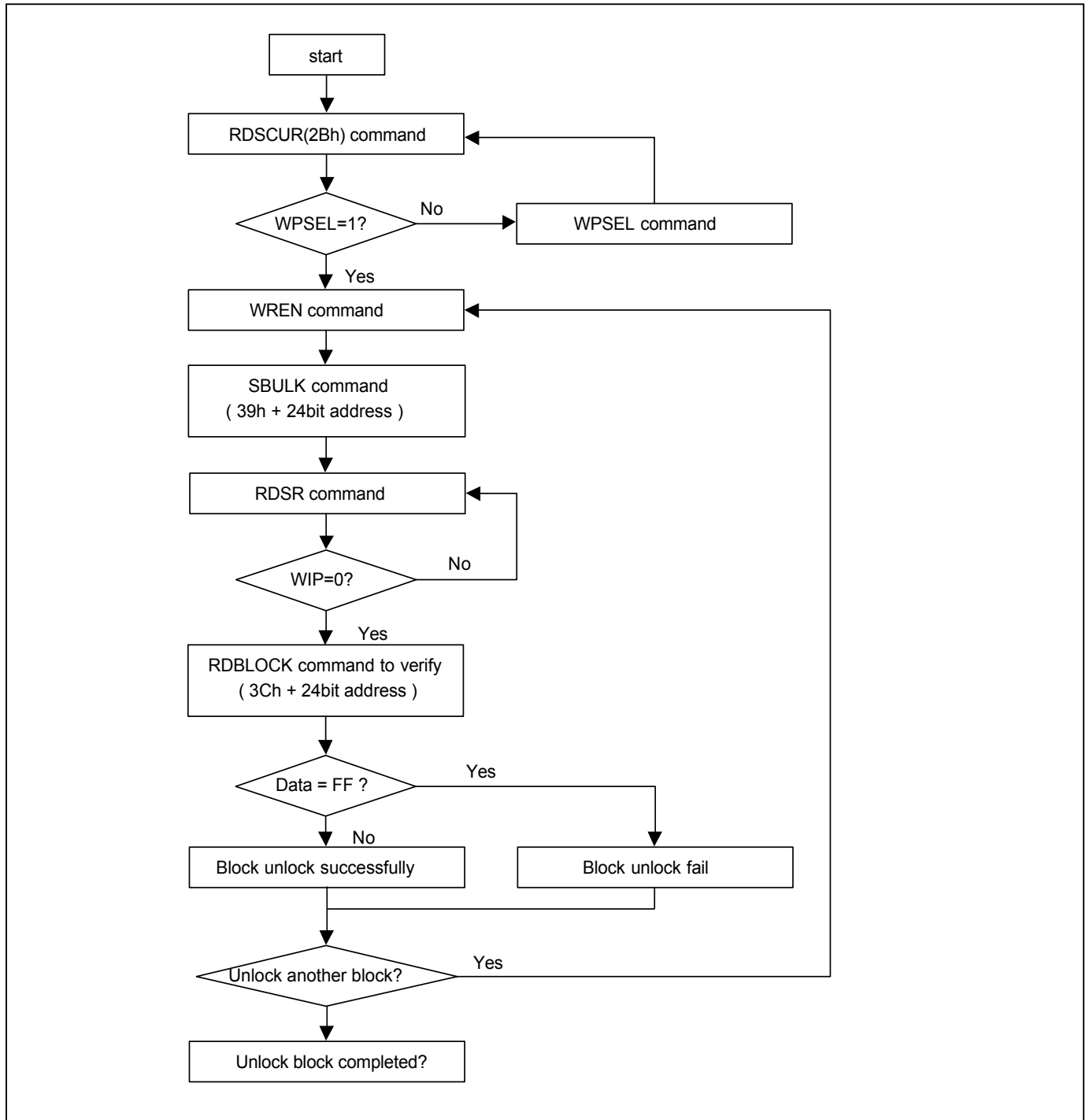


Figure 62. Block Unlock Flow



9-31. Read Block Lock Status (RDBLOCK)

This instruction is only effective after WPSEL was executed. The RDBLOCK instruction is for reading the status of protection lock of a specified block (or sector), using $A_{MAX-A16}$ (or $A_{MAX-A12}$) address bits to assign a 64K bytes block (4K bytes sector) and read protection lock status bit which the first byte of Read-out cycle. The status bit is "1" to indicate that this block has be protected, that user can read only but cannot write/program /erase this block. The status bit is "0" to indicate that this block hasn't be protected, and user can read and write this block.

The sequence of issuing RDBLOCK instruction is: CS# goes low → send RDBLOCK (3Ch) instruction → send 3-byte address to assign one block on SI pin → read block's protection lock status bit on SO pin → CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are "don't care" in SPI mode.

9-32. Gang Block Lock/Unlock (GBLK/GBULK)

These instructions are only effective after WPSEL was executed. The GBLK/GBULK instruction is for enable/disable the lock protection block of the whole chip.

The WREN (Write Enable) instruction is required before issuing GBLK/GBULK instruction.

The sequence of issuing GBLK/GBULK instruction is: CS# goes low → send GBLK/GBULK (7Eh/98h) instruction → CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are "don't care" in SPI mode.

The CS# must go high exactly at the byte boundary, otherwise, the instruction will be rejected and not be executed.

9-33. Program Suspend and Erase Suspend

The Suspend instruction interrupts a Page Program, Sector Erase, or Block Erase operation to allow access to the memory array.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

After the program or erase operation has entered the suspended state, the memory array can be read except for the page being programmed or the sector or block being erased (*"Table 10. Readable Area of Memory While a Program or Erase Operation is Suspended"*).

Table 10. Readable Area of Memory While a Program or Erase Operation is Suspended

| Suspended Operation | Readable Region of Memory Array |
|---------------------|-------------------------------------|
| Page Program | All but the Page being programmed |
| Sector Erase (4KB) | All but the 4KB Sector being erased |
| Block Erase (32KB) | All but the 32KB Block being erased |
| Block Erase (64KB) | All but the 64KB Block being erased |

When the Serial NOR Flash receives the Suspend instruction, there is a latency of tPSL or tESL (*"Figure 63. Suspend to Read Latency"*) before the Write Enable Latch (WEL) bit clears to "0" and the PSB or ESB sets to "1", after which the device is ready to accept one of the commands listed in *"Table 11. Acceptable Commands During Program/Erase Suspend after tPSL/tESL"* (e.g. FAST READ). Refer to *"Table 19. AC Characteristics"* for tPSL and tESL timings.

"Table 12. Acceptable Commands During Suspend (tPSL/tESL not required)" lists the commands for which the tPSL and tESL latencies do not apply. For example, RDSR, RDSCUR, RSTEN, and RST can be issued at any time after the Suspend instruction.

Security Register bit 2 (PSB) and bit 3 (ESB) can be read to check the suspend status (please refer to *"Table 9. Security Register Definition"*). The PSB (Program Suspend Bit) sets to "1" when a program operation is suspended. The ESB (Erase Suspend Bit) sets to "1" when an erase operation is suspended. The PSB or ESB clears to "0" when the program or erase operation is resumed.

Figure 63. Suspend to Read Latency

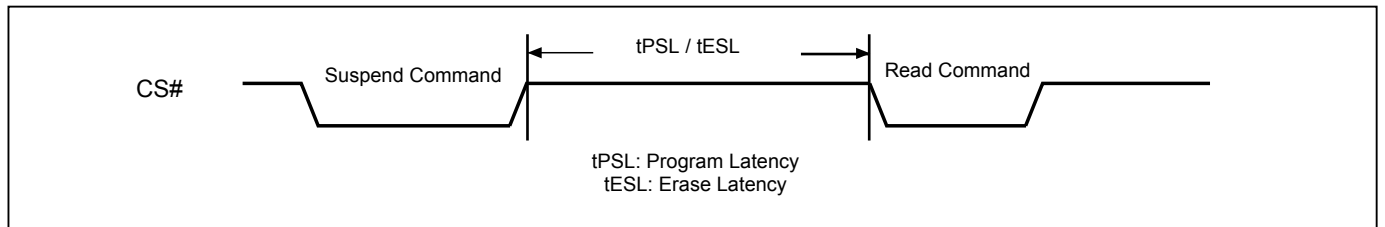


Table 11. Acceptable Commands During Program/Erase Suspend after tPSL/tESL

| Command Name | Command Code | Suspend Type | |
|--------------|--------------|-----------------|---------------|
| | | Program Suspend | Erase Suspend |
| READ | 03h | • | • |
| FAST READ | 0Bh | • | • |
| DREAD | 3Bh | • | • |
| QREAD | 6Bh | • | • |
| 2READ | BBh | • | • |
| 4READ | EBh | • | • |
| W4READ | E7h | • | • |
| RDSFDP | 5Ah | • | • |
| RDID | 9Fh | • | • |
| QPIID | AFh | • | • |
| REMS | 90h | • | • |
| ENSO | B1h | • | • |
| EXSO | C1h | • | • |
| WREN | 06h | | • |
| EQIO | 35h | • | • |
| RSTQIO | F5h | • | • |
| RESUME | 30h | • | • |
| SBL | C0h | • | • |
| PP | 02h | | • |
| 4PP | 38h | | • |

Table 12. Acceptable Commands During Suspend (tPSL/tESL not required)

| Command Name | Command Code | Suspend Type | |
|--------------|--------------|-----------------|---------------|
| | | Program Suspend | Erase Suspend |
| WRDI | 04h | | • |
| RDSR | 05h | • | • |
| RDCR | 15h | • | |
| RDSCUR | 2Bh | • | • |
| RES | ABh | • | • |
| RSTEN | 66h | • | • |
| RST | 99h | • | • |
| NOP | 00h | • | • |

Figure 64. Resume to Suspend Latency

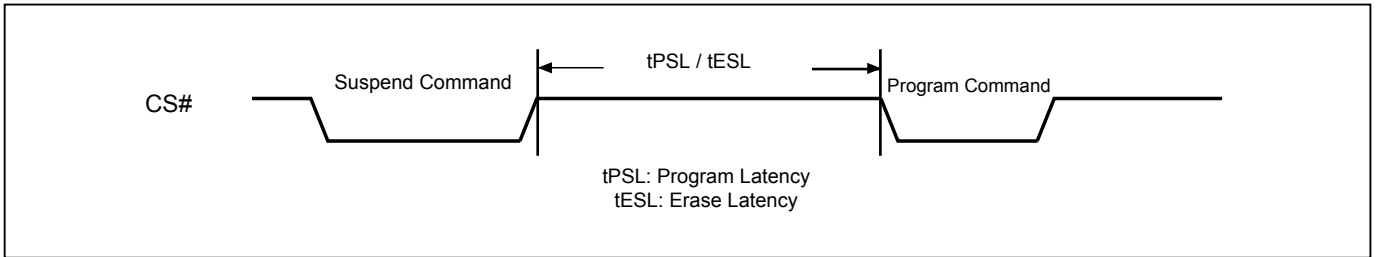


9-33-1. Erase Suspend to Program

The “Erase Suspend to Program” feature allows Page Programming while an erase operation is suspended. Page Programming is permitted in any unprotected memory except within the sector of a suspended Sector Erase operation or within the block of a suspended Block Erase operation. The Write Enable (WREN) instruction must be issued before any Page Program instruction.

A Page Program operation initiated within a suspended erase cannot itself be suspended and must be allowed to finish before the suspended erase can be resumed. The Status Register can be polled to determine the status of the Page Program operation. The WEL and WIP bits of the Status Register will remain “1” while the Page Program operation is in progress and will both clear to “0” when the Page Program operation completes.

Figure 65. Suspend to Program Latency



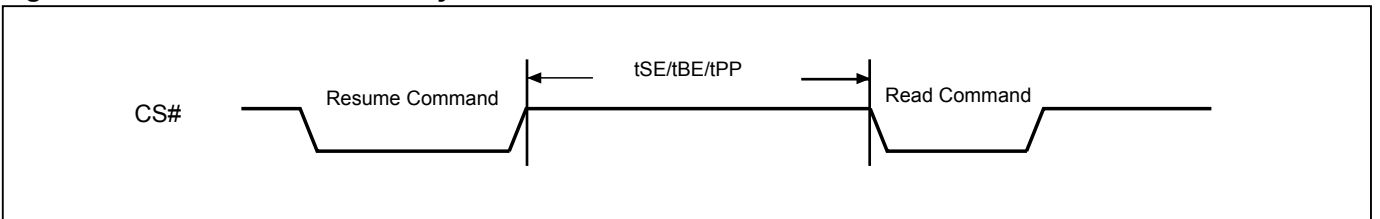
9-34. Program Resume and Erase Resume

The Resume instruction resumes a suspended Page Program, Sector Erase, or Block Erase operation. Before issuing the Resume instruction to restart a suspended erase operation, make sure that there is no Page Program operation in progress.

Immediately after the Serial NOR Flash receives the Resume instruction, the WEL and WIP bits are set to “1” and the PSB or ESB is cleared to “0”. The program or erase operation will continue until finished (“[Figure 66. Resume to Read Latency](#)”) or until another Suspend instruction is received. A resume-to-suspend latency of tPRS or tERS must be observed before issuing another Suspend instruction (“[Figure 64. Resume to Suspend Latency](#)”).

Please note that the Resume instruction will be ignored if the Serial NOR Flash is in “Performance Enhance Mode”. Make sure the Serial NOR Flash is not in “Performance Enhance Mode” before issuing the Resume instruction.

Figure 66. Resume to Read Latency



9-35. No Operation (NOP)

The "No Operation" command is only able to terminate the Reset Enable (RSTEN) command and will not affect any other command.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are "don't care" in SPI mode.

9-36. Software Reset (Reset-Enable (RSTEN) and Reset (RST))

The Software Reset operation combines two instructions: Reset-Enable (RSTEN) command and Reset (RST) command. It returns the device to standby mode. All the volatile bits and settings will be cleared then, which makes the device return to the default status as power on.

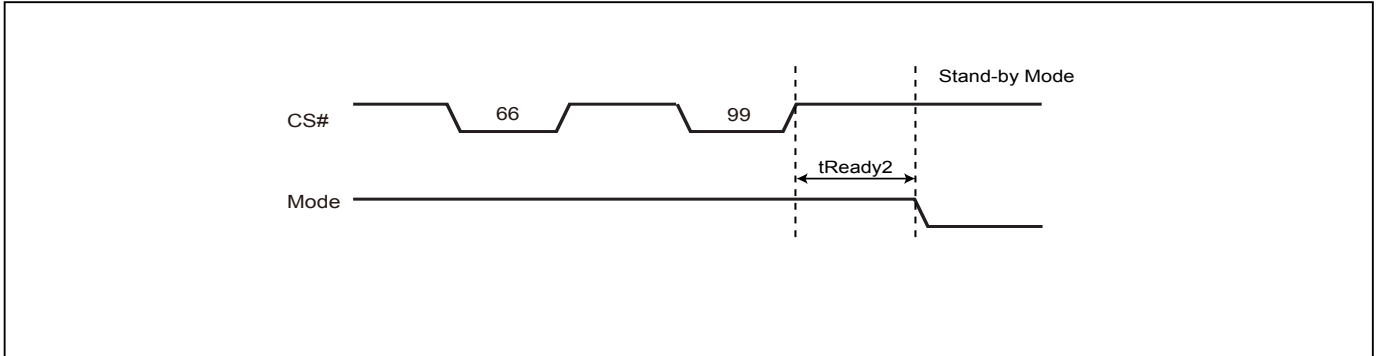
To execute Reset command (RST), the Reset-Enable (RSTEN) command must be executed first to perform the Reset operation. If there is any other command to interrupt after the Reset-Enable command, the Reset-Enable will be invalid.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

If the Reset command is executed during program or erase operation, the operation will be disabled, the data under processing could be damaged or lost.

The reset time is different depending on the last operation. For details, please refer to "[Table 15-2. Reset Timing-\(Other Operation\)](#)" for tREADY2.

Figure 67. Software Reset Recovery



Note: Refer to "Table 15-2. Reset Timing-(Other Operation)" for tREADY2 data.

Figure 68. Reset Sequence (SPI mode)

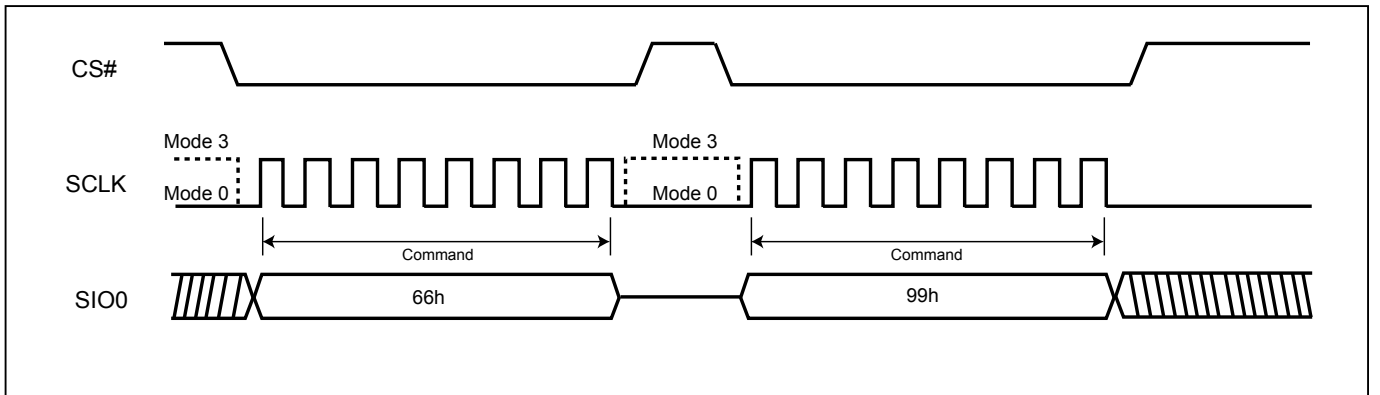
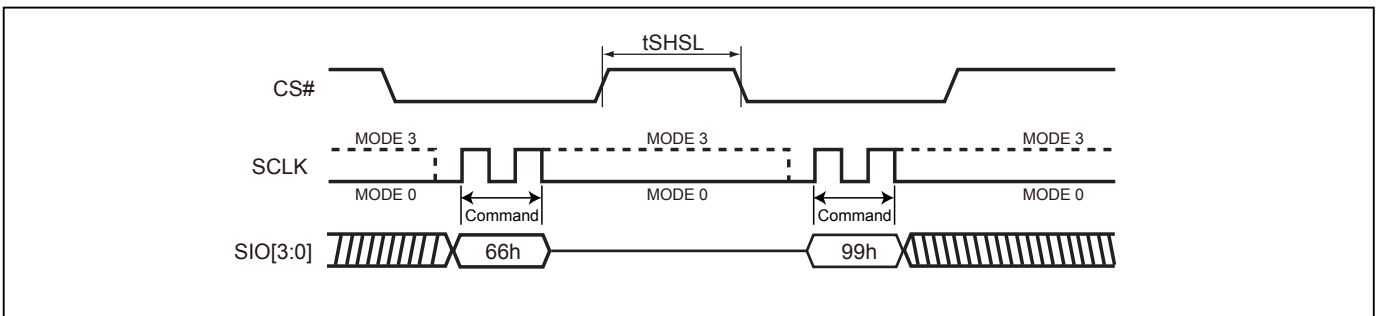


Figure 69. Reset Sequence (QPI mode)



9-37. Read SFDP Mode (RDSFDP)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI.

The sequence of issuing RDSFDP instruction is same as CS# goes low→send RDSFDP instruction (5Ah)→send 3 address bytes on SI pin→send 1 dummy byte on SI pin→read SFDP code on SO→to end RDSFDP operation can use CS# to high at any time during data out.

SFDP is a JEDEC Standard, JESD216.

Figure 70. Read Serial Flash Discoverable Parameter (RDSFDP) Sequence

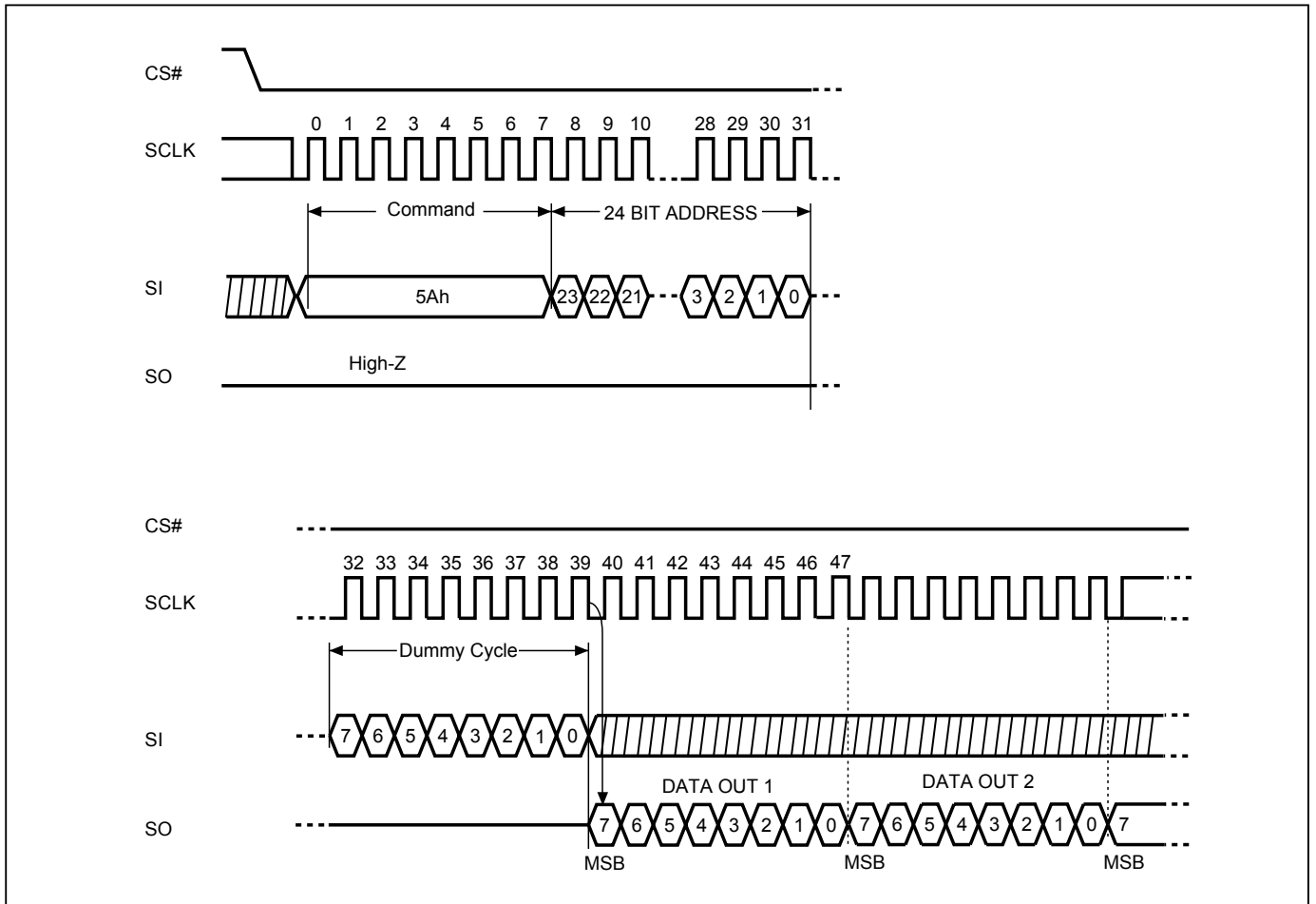


Table 12. Signature and Parameter Identification Data Values

SFDP Table (JESD216) below is for MX25U12835FZNI-10G, MX25U12835FZ2I-10G, MX25U12835FZNI-08G, MX25U12835FMI-10G and MX25U12835FM2I-10G

| Description | Comment | Add (h) (Byte) | DW Add (Bit) | Data (h/b) (Note1) | Data (h) |
|--|--|-------------------|-----------------|-----------------------|-------------|
| SFDP Signature | Fixed: 50444653h | 00h | 07:00 | 53h | 53h |
| | | 01h | 15:08 | 46h | 46h |
| | | 02h | 23:16 | 44h | 44h |
| | | 03h | 31:24 | 50h | 50h |
| SFDP Minor Revision Number | Start from 00h | 04h | 07:00 | 00h | 00h |
| SFDP Major Revision Number | Start from 01h | 05h | 15:08 | 01h | 01h |
| Number of Parameter Headers | This number is 0-based. Therefore, 0 indicates 1 parameter header. | 06h | 23:16 | 01h | 01h |
| Unused | | 07h | 31:24 | FFh | FFh |
| ID number (JEDEC) | 00h: it indicates a JEDEC specified header. | 08h | 07:00 | 00h | 00h |
| Parameter Table Minor Revision Number | Start from 00h | 09h | 15:08 | 00h | 00h |
| Parameter Table Major Revision Number | Start from 01h | 0Ah | 23:16 | 01h | 01h |
| Parameter Table Length (in double word) | How many DWORDs in the Parameter table | 0Bh | 31:24 | 09h | 09h |
| Parameter Table Pointer (PTP) | First address of JEDEC Flash Parameter table | 0Ch | 07:00 | 30h | 30h |
| | | 0Dh | 15:08 | 00h | 00h |
| | | 0Eh | 23:16 | 00h | 00h |
| Unused | | 0Fh | 31:24 | FFh | FFh |
| ID number (Macronix manufacturer ID) | it indicates Macronix manufacturer ID | 10h | 07:00 | C2h | C2h |
| Parameter Table Minor Revision Number | Start from 00h | 11h | 15:08 | 00h | 00h |
| Parameter Table Major Revision Number | Start from 01h | 12h | 23:16 | 01h | 01h |
| Parameter Table Length (in double word) | How many DWORDs in the Parameter table | 13h | 31:24 | 04h | 04h |
| Parameter Table Pointer (PTP) | First address of Macronix Flash Parameter table | 14h | 07:00 | 60h | 60h |
| | | 15h | 15:08 | 00h | 00h |
| | | 16h | 23:16 | 00h | 00h |
| Unused | | 17h | 31:24 | FFh | FFh |

Table 13. Parameter Table (0): JEDEC Flash Parameter Tables

SFDP Table below is for MX25U12835FZNI-10G, MX25U12835FZ2I-10G, MX25U12835FZNI-08G, MX25U12835FMI-10G and MX25U12835FM2I-10G

| Description | Comment | Add (h) (Byte) | DW Add (Bit) | Data (h/b) (Note1) | Data (h) |
|--|--|-------------------|-----------------|-----------------------|-------------|
| Block/Sector Erase sizes | 00: Reserved, 01: 4KB erase, 10: Reserved, 11: not support 4KB erase | 30h | 01:00 | 01b | E5h |
| Write Granularity | 0: 1Byte, 1: 64Byte or larger | | 02 | 1b | |
| Write Enable Instruction Required for Writing to Volatile Status Registers | 0: not required 1: required 00h to be written to the status register | | 03 | 0b | |
| Write Enable Opcode Select for Writing to Volatile Status Registers | 0: use 50h opcode, 1: use 06h opcode Note: If target flash status register is nonvolatile, then bits 3 and 4 must be set to 00b. | | 04 | 0b | |
| Unused | Contains 111b and can never be changed | | 07:05 | 111b | |
| 4KB Erase Opcode | | 31h | 15:08 | 20h | 20h |
| (1-1-2) Fast Read (Note2) | 0=not support 1=support | 32h | 16 | 1b | F1h |
| Address Bytes Number used in addressing flash array | 00: 3Byte only, 01: 3 or 4Byte, 10: 4Byte only, 11: Reserved | | 18:17 | 00b | |
| Double Transfer Rate (DTR) Clocking | 0=not support 1=support | | 19 | 0b | |
| (1-2-2) Fast Read | 0=not support 1=support | | 20 | 1b | |
| (1-4-4) Fast Read | 0=not support 1=support | | 21 | 1b | |
| (1-1-4) Fast Read | 0=not support 1=support | | 22 | 1b | |
| Unused | | | 23 | 1b | |
| Unused | | 33h | 31:24 | FFh | FFh |
| Flash Memory Density | | 37h:34h | 31:00 | 07FF FFFFh | |
| (1-4-4) Fast Read Number of Wait states (Note3) | 0 0000b: Not supported; 0 0100b: 4 0 0110b: 6; 0 1000b: 8 | 38h | 04:00 | 0 0100b | 44h |
| (1-4-4) Fast Read Number of Mode Bits (Note4) | Mode Bits: 000b: Not supported; 010b: 2 bits | | 07:05 | 010b | |
| (1-4-4) Fast Read Opcode | | 39h | 15:08 | EBh | EBh |
| (1-1-4) Fast Read Number of Wait states | 0 0000b: Not supported; 0 0100b: 4 0 0110b: 6; 0 1000b: 8 | 3Ah | 20:16 | 0 1000b | 08h |
| (1-1-4) Fast Read Number of Mode Bits | Mode Bits: 000b: Not supported; 010b: 2 bits | | 23:21 | 000b | |
| (1-1-4) Fast Read Opcode | | 3Bh | 31:24 | 6Bh | 6Bh |



SFDP Table below is for MX25U12835FZNI-10G, MX25U12835FZ2I-10G, MX25U12835FZNI-08G, MX25U12835FMI-10G and MX25U12835FM2I-10G

| Description | Comment | Add (h) (Byte) | DW Add (Bit) | Data (h/b) (Note1) | Data (h) |
|---|--|-------------------|-----------------|-----------------------|-------------|
| (1-1-2) Fast Read Number of Wait states | 0 0000b: Not supported; 0 0100b: 4 0 0110b: 6; 0 1000b: 8 | 3Ch | 04:00 | 0 1000b | 08h |
| (1-1-2) Fast Read Number of Mode Bits | Mode Bits: 000b: Not supported; 010b: 2 bits | | 07:05 | 000b | |
| (1-1-2) Fast Read Opcode | | 3Dh | 15:08 | 3Bh | 3Bh |
| (1-2-2) Fast Read Number of Wait states | 0 0000b: Not supported; 0 0100b: 4 0 0110b: 6; 0 1000b: 8 | 3Eh | 20:16 | 0 0100b | 04h |
| (1-2-2) Fast Read Number of Mode Bits | Mode Bits: 000b: Not supported; 010b: 2 bits | | 23:21 | 000b | |
| (1-2-2) Fast Read Opcode | | 3Fh | 31:24 | BBh | BBh |
| (2-2-2) Fast Read | 0=not support 1=support | 40h | 00 | 0b | FEh |
| Unused | | | 03:01 | 111b | |
| (4-4-4) Fast Read | 0=not support 1=support | | 04 | 1b | |
| Unused | | | 07:05 | 111b | |
| Unused | | 43h:41h | 31:08 | FFh | FFh |
| Unused | | 45h:44h | 15:00 | FFh | FFh |
| (2-2-2) Fast Read Number of Wait states | 0 0000b: Not supported; 0 0100b: 4 0 0110b: 6; 0 1000b: 8 | 46h | 20:16 | 0 0000b | 00h |
| (2-2-2) Fast Read Number of Mode Bits | Mode Bits: 000b: Not supported; 010b: 2 bits | | 23:21 | 000b | |
| (2-2-2) Fast Read Opcode | | 47h | 31:24 | FFh | FFh |
| Unused | | 49h:48h | 15:00 | FFh | FFh |
| (4-4-4) Fast Read Number of Wait states | 0 0000b: Not supported; 0 0100b: 4 0 0110b: 6; 0 1000b: 8 | 4Ah | 20:16 | 0 0100b | 44h |
| (4-4-4) Fast Read Number of Mode Bits | Mode Bits: 000b: Not supported; 010b: 2 bits | | 23:21 | 010b | |
| (4-4-4) Fast Read Opcode | | 4Bh | 31:24 | EBh | EBh |
| Sector Type 1 Size | Sector/block size = 2 ^N bytes (Note5) 0Ch: 4KB; 0Fh: 32KB; 10h: 64KB | 4Ch | 07:00 | 0Ch | 0Ch |
| Sector Type 1 erase Opcode | | 4Dh | 15:08 | 20h | 20h |
| Sector Type 2 Size | Sector/block size = 2 ^N bytes 00h: N/A; 0Fh: 32KB; 10h: 64KB | 4Eh | 23:16 | 0Fh | 0Fh |
| Sector Type 2 erase Opcode | | 4Fh | 31:24 | 52h | 52h |
| Sector Type 3 Size | Sector/block size = 2 ^N bytes 00h: N/A; 0Fh: 32KB; 10h: 64KB | 50h | 07:00 | 10h | 10h |
| Sector Type 3 erase Opcode | | 51h | 15:08 | D8h | D8h |
| Sector Type 4 Size | 00h: N/A, This sector type doesn't exist | 52h | 23:16 | 00h | 00h |
| Sector Type 4 erase Opcode | | 53h | 31:24 | FFh | FFh |

Table 14. Parameter Table (1): Macronix Flash Parameter Tables

SFDP Table below is for MX25U12835FZNI-10G, MX25U12835FZ2I-10G, MX25U12835FZNI-08G, MX25U12835FMI-10G and MX25U12835FM2I-10G

| Description | Comment | Add (h) (Byte) | DW Add (Bit) | Data (h/b) (Note1) | Data (h) | |
|---|--|-------------------|-----------------|-----------------------|-------------|-----|
| Vcc Supply Maximum Voltage | 2000h=2.000V 2700h=2.700V 3600h=3.600V | 61h:60h | 07:00 15:08 | 00h 20h | 00h 20h | |
| Vcc Supply Minimum Voltage | 1650h=1.650V, 1750h=1.750V 2250h=2.250V, 2300h=2.300V 2350h=2.350V, 2650h=2.650V 2700h=2.700V | 63h:62h | 23:16 31:24 | 50h 16h | 50h 16h | |
| H/W Reset# pin | 0=not support 1=support | 65h:64h | 00 | 1b | F99Dh | |
| H/W Hold# pin | 0=not support 1=support | | 01 | 0b | | |
| Deep Power Down Mode | 0=not support 1=support | | 02 | 1b | | |
| S/W Reset | 0=not support 1=support | | 03 | 1b | | |
| S/W Reset Opcode | Reset Enable (66h) should be issued before Reset Opcode | | 11:04 | 1001 1001b (99h) | | |
| Program Suspend/Resume | 0=not support 1=support | | 12 | 1b | | |
| Erase Suspend/Resume | 0=not support 1=support | | 13 | 1b | | |
| Unused | | | 14 | 1b | | |
| Wrap-Around Read mode | 0=not support 1=support | | 15 | 1b | | |
| Wrap-Around Read mode Opcode | | | 66h | 23:16 | | C0h |
| Wrap-Around Read data length | 08h:support 8B wrap-around read 16h:8B&16B 32h:8B&16B&32B 64h:8B&16B&32B&64B | 67h | 31:24 | 64h | 64h | |
| Individual block lock | 0=not support 1=support | 6Bh:68h | 00 | 1b | C8D9h | |
| Individual block lock bit (Volatile/Nonvolatile) | 0=Volatile 1=Nonvolatile | | 01 | 0b | | |
| Individual block lock Opcode | | | 09:02 | 0011 0110b (36h) | | |
| Individual block lock Volatile protect bit default protect status | 0=protect 1=unprotect | | 10 | 0b | | |
| Secured OTP | 0=not support 1=support | | 11 | 1b | | |
| Read Lock | 0=not support 1=support | | 12 | 0b | | |
| Permanent Lock | 0=not support 1=support | | 13 | 0b | | |
| Unused | | | 15:14 | 11b | | |
| Unused | | | 31:16 | FFh | | FFh |
| Unused | | | 6Fh:6Ch | 31:00 | | FFh |

Note 1: h/b is hexadecimal or binary.

Note 2: **(x-y-z)** means I/O mode nomenclature used to indicate the number of active pins used for the opcode (x), address (y), and data (z). At the present time, the only valid Read SFDP instruction modes are: (1-1-1), (2-2-2), and (4-4-4)

Note 3: **Wait States** is required dummy clock cycles after the address bits or optional mode bits.

Note 4: **Mode Bits** is optional control bits that follow the address bits. These bits are driven by the system controller if they are specified. (eg, read performance enhance toggling bits)

Note 5: 4KB=2⁰Ch, 32KB=2⁰Fh, 64KB=2¹0h

Note 6: All unused and undefined area data is blank FFh for SFDP Tables that are defined in Parameter Identification Header. All other areas beyond defined SFDP Table are reserved by Macronix.

10. RESET

Driving the RESET# pin low for a period of tRLRH or longer will reset the device. After reset cycle, the device is at the following states:

- Standby mode
- All the volatile bits such as WEL/WIP/SRAM lock bit will return to the default status as power on.

If the device is under programming or erasing, driving the RESET# pin low will also terminate the operation and data could be lost. During the resetting cycle, the SO data becomes high impedance and the current will be reduced to minimum.

Figure 71. RESET Timing

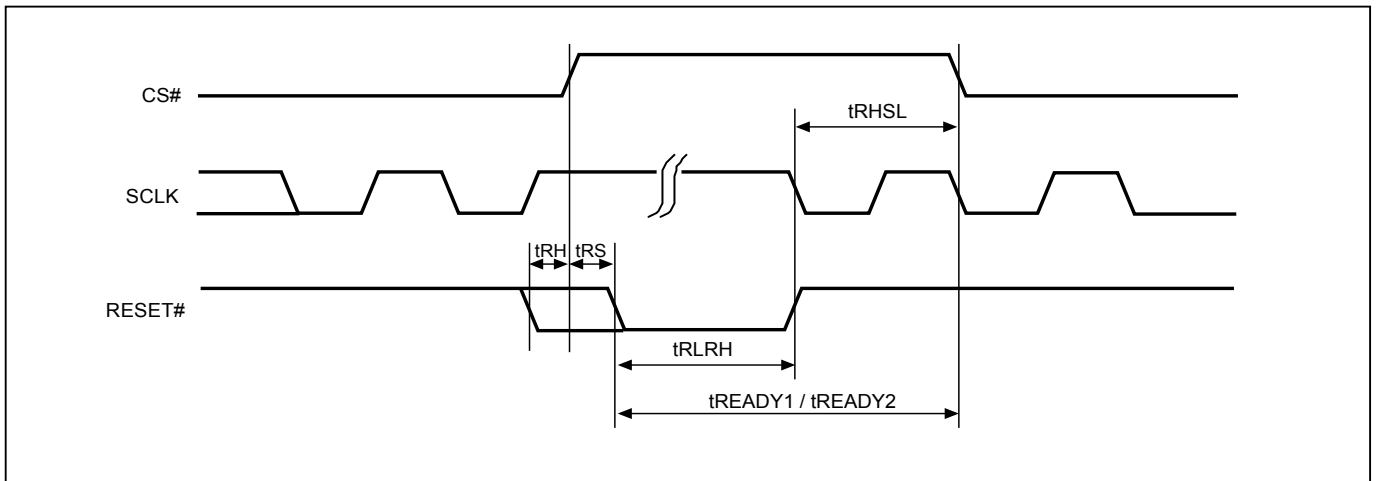


Table 15-1. Reset Timing-(Power On)

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---------|----------------------------|------|------|------|------|
| tRHSL | Reset# high before CS# low | 10 | | | us |
| tRS | Reset# setup time | 15 | | | ns |
| tRH | Reset# hold time | 15 | | | ns |
| tRLRH | Reset# low pulse width | 10 | | | us |
| tREADY1 | Reset Recovery time | 35 | | | us |

Table 15-2. Reset Timing-(Other Operation)

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---------|---|------|------|------|------|
| tRHSL | Reset# high before CS# low | 10 | | | us |
| tRS | Reset# setup time | 15 | | | ns |
| tRH | Reset# hold time | 15 | | | ns |
| tRLRH | Reset# low pulse width | 10 | | | us |
| tREADY2 | Reset Recovery time (During instruction decoding) | 40 | | | us |
| | Reset Recovery time (for read operation) | 40 | | | us |
| | Reset Recovery time (for program operation) | 310 | | | us |
| | Reset Recovery time (for SE operation) | 12 | | | ms |
| | Reset Recovery time (for BE64KB/BE32KB operation) | 25 | | | ms |
| | Reset Recovery time (for Chip Erase operation) | 100 | | | ms |
| | Reset Recovery time (for WRSR operation) | 40 | | | ms |

11. POWER-ON STATE

The device is at the following states after power-up:

- Standby mode (please note it is not deep power-down mode)
- Write Enable Latch (WEL) bit is reset

The device must not be selected during power-up and power-down stage until the VCC reaches the following levels:

- VCC minimum at power-up stage and then after a delay of tVSL
- GND at power-down

Please note that a pull-up resistor on CS# may ensure a safe and proper power-up/down level.

An internal power-on reset (POR) circuit may protect the device from data corruption and inadvertent data change during power up state. When VCC is lower than VWI (POR threshold voltage value), the internal logic is reset and the flash device has no response to any command.

For further protection on the device, if the VCC does not reach the VCC minimum level, the correct operation is not guaranteed. The write, erase, and program command should be sent after the below time delay:

- tVSL after VCC reached VCC minimum level

The device can accept read command after VCC reached VCC minimum and a time delay of tVSL.

Please refer to the ["Figure 79. Power-up Timing"](#).

Note:

- To stabilize the VCC level, the VCC rail decoupled by a suitable capacitor close to package pins is recommended. (generally around 0.1uF)
- At power-down stage, the VCC drops below VWI level, all operations are disabled and device has no response to any command. The data corruption might occur during this stage if a write, program, erase cycle is in progress.

12. ELECTRICAL SPECIFICATIONS

Table 16. Absolute Maximum Ratings

| Rating | | Value |
|-------------------------------|------------------|-------------------|
| Ambient Operating Temperature | Industrial grade | -40°C to 85°C |
| Storage Temperature | | -65°C to 150°C |
| Applied Input Voltage | | -0.5V to VCC+0.5V |
| Applied Output Voltage | | -0.5V to VCC+0.5V |
| VCC to Ground Potential | | -0.5V to 2.5V |

NOTICE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Specifications contained within the following tables are subject to change.
3. During voltage transitions, all pins may overshoot to VCC+1.0V or -1.0V for period up to 20ns.

Figure 72. Maximum Negative Overshoot Waveform

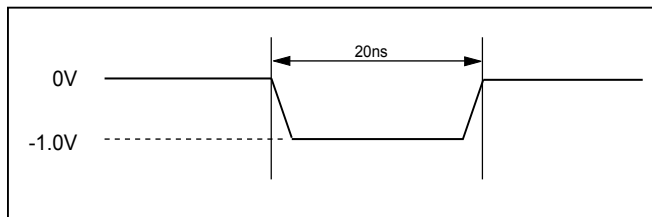


Figure 73. Maximum Positive Overshoot Waveform

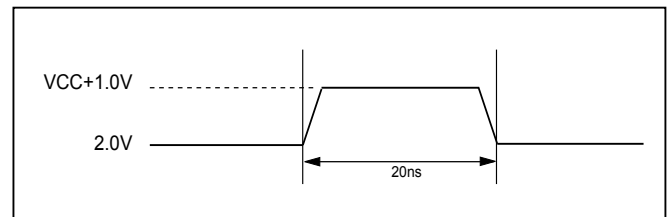


Table 17. Capacitance TA = 25°C, f = 1.0 MHz

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|--------|--------------------|------|------|------|------|------------|
| CIN | Input Capacitance | | | 6 | pF | VIN = 0V |
| COUT | Output Capacitance | | | 8 | pF | VOUT = 0V |

Figure 74. Input Test Waveforms and Measurement Level

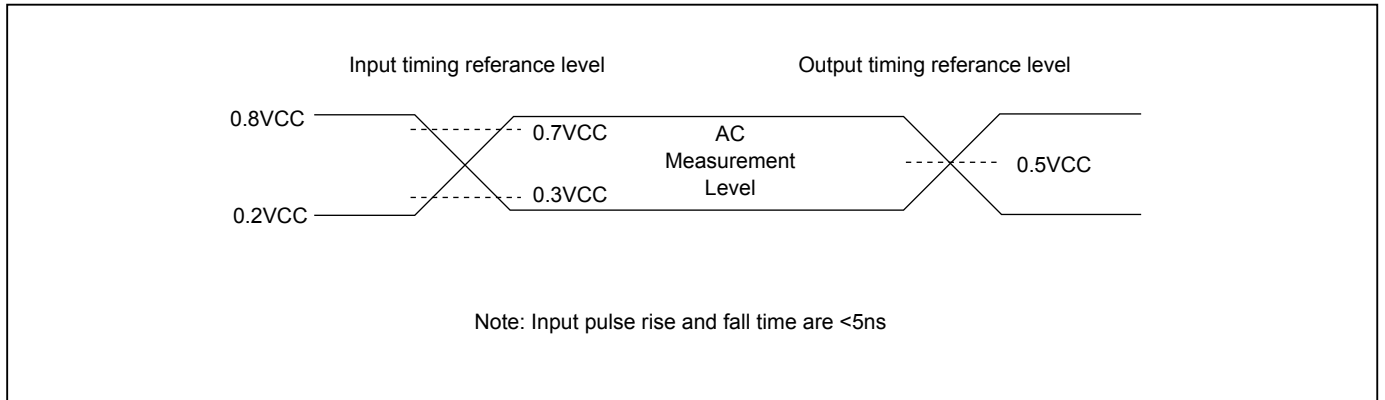


Figure 75. Output Loading

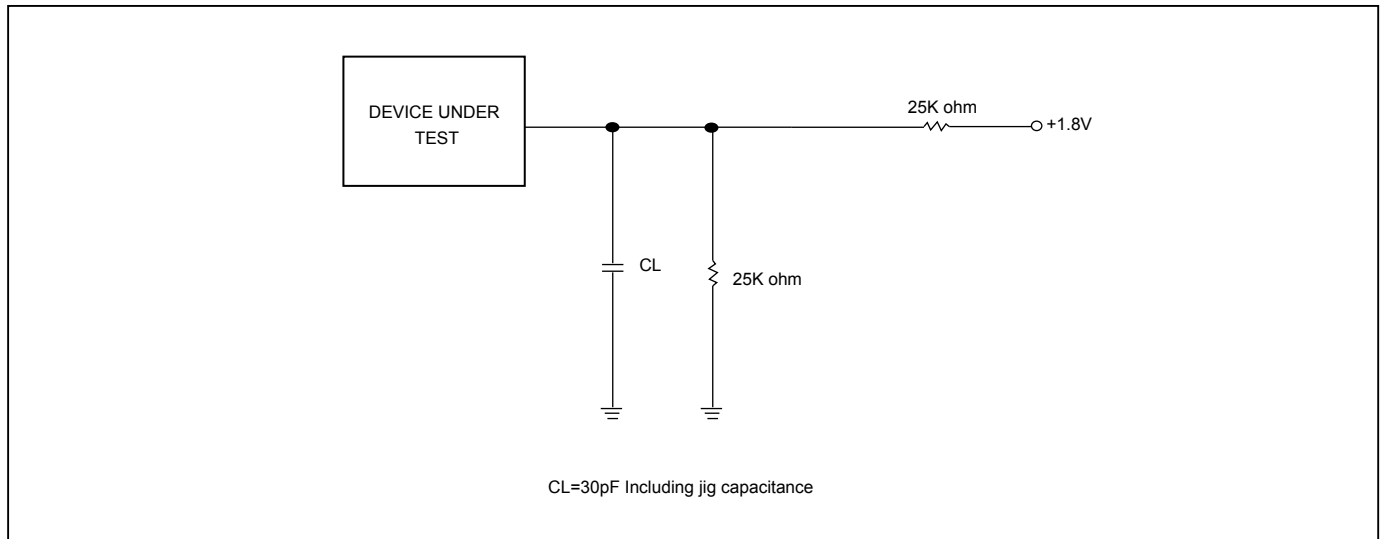


Figure 76. SCLK TIMING DEFINITION

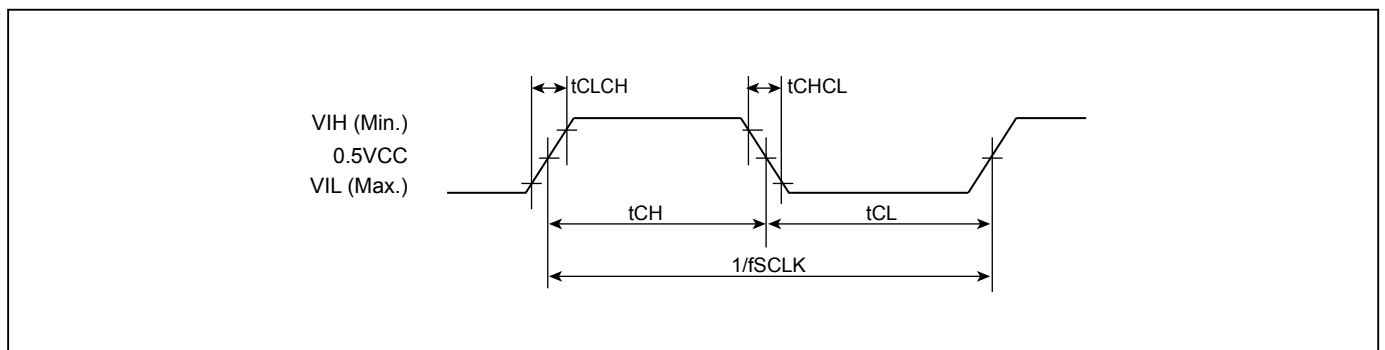


Table 18. DC Characteristics

Temperature = -40°C to 85°C, VCC = 1.65V - 2.0V

| Symbol | Parameter | Notes | Min. | Typ. | Max. | Units | Test Conditions |
|--------|---|-------|---------|------|---------|-------|---|
| ILI | Input Load Current | 1 | | | ±2 | uA | VCC = VCC Max, VIN = VCC or GND |
| ILO | Output Leakage Current | 1 | | | ±2 | uA | VCC = VCC Max, VOUT = VCC or GND |
| ISB1 | VCC Standby Current | 1 | | 15 | 50 | uA | VIN = VCC or GND, CS# = VCC |
| ISB2 | Deep Power-down Current | | | 1.5 | 15 | uA | VIN = VCC or GND, CS# = VCC |
| ICC1 | VCC Read | 1 | | | 27 | mA | f=133MHz, (4 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open (for MX25U12835FZNI-08G only) |
| | | | | | 20 | mA | f=104MHz, (4 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open |
| | | | | | 15 | mA | f=84MHz, SCLK=0.1VCC/0.9VCC, SO=Open |
| ICC2 | VCC Program Current (PP) | 1 | | 20 | 25 | mA | Program in Progress, CS# = VCC |
| ICC3 | VCC Write Status Register (WRSR) Current | | | 10 | 20 | mA | Program status register in progress, CS#=VCC |
| ICC4 | VCC Sector/Block (32K, 64K) Erase Current (SE/BE/BE32K) | 1 | | 18 | 25 | mA | Erase in Progress, CS#=VCC |
| ICC5 | VCC Chip Erase Current (CE) | 1 | | 20 | 25 | mA | Erase in Progress, CS#=VCC |
| VIL | Input Low Voltage | | -0.5 | | 0.2VCC | V | |
| VIH | Input High Voltage | | 0.7VCC | | VCC+0.4 | V | |
| VOL | Output Low Voltage | | | | 0.2 | V | IOL = 100uA |
| VOH | Output High Voltage | | VCC-0.2 | | | V | IOH = -100uA |

Notes:

1. Typical values at VCC = 1.8V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. Typical value is calculated by simulation.

Table 19. AC Characteristics

Temperature = -40°C to 85°C, VCC = 1.65V - 2.0V

| Symbol | Alt. | Parameter | Min. | Typ. ⁽²⁾ | Max. | Unit |
|----------------------|------|---|---|------------------------------------|------------|------|
| fSCLK | fC | Clock Frequency for the following instructions: FAST_READ, PP, SE, BE, CE, DP, RES, RDP, WREN, WRDI, RDID, RDSR, WRSR | D.C. | | 104 | MHz |
| fRSCLK | fR | Clock Frequency for READ instructions ⁽⁶⁾ | | | 55 | MHz |
| fTSCLK | fT | Clock Frequency for 2READ instructions | | | 84 | MHz |
| | fQ | Clock Frequency for 4READ instructions ⁽⁵⁾ | | | 84/104/133 | MHz |
| tCH ⁽⁷⁾ | tCLH | Clock High Time | Others (fSCLK) | 4.5 | | ns |
| | | | Normal Read (fRSCLK) | 7 | | ns |
| tCL ⁽⁷⁾ | tCLL | Clock Low Time | Others (fSCLK) | 4.5 | | ns |
| | | | Normal Read (fRSCLK) | 7 | | ns |
| tCLCH ⁽²⁾ | | Clock Rise Time (peak to peak) | 0.1 | | | V/ns |
| tCHCL ⁽²⁾ | | Clock Fall Time (peak to peak) | 0.1 | | | V/ns |
| tSLCH | tCSS | CS# Active Setup Time (relative to SCLK) | 5 | | | ns |
| tCHSL | | CS# Not Active Hold Time (relative to SCLK) | 5 | | | ns |
| tDVCH | tDSU | Data In Setup Time | MX25U12835FZNI-08G | 1.5 | | ns |
| | | | Others | 2 | | ns |
| tCHDX | tDH | Data In Hold Time | MX25U12835FZNI-08G | 2 | | ns |
| | | | Others | 3 | | ns |
| tCHSH | | CS# Active Hold Time (relative to SCLK) | MX25U12835FZNI-08G | 1.5 | | ns |
| | | | Others | 2 | | ns |
| tSHCH | | CS# Not Active Setup Time (relative to SCLK) | MX25U12835FZNI-08G | 2 | | ns |
| | | | Others | 3 | | ns |
| tSHSL | tCSH | CS# Deselect Time | From Read to next Read | 5 | | ns |
| | | | From Write/Erase/Program to Read Status Register | 30 | | ns |
| tSHQZ ⁽²⁾ | tDIS | Output Disable Time | | | 8 | ns |
| tCLQV | tV | Clock Low to Output Valid Loading: 30pF/15pF/10pF | Loading: 30pF | | 7 | ns |
| | | | Loading: 15pF | | 6 | ns |
| | | | Loading: 10pF (only for MX25U12835FZNI-08G) | | 5.1 | ns |
| tCLQX | tHO | Output Hold Time | 0 | | | ns |
| tWHSL ⁽³⁾ | | Write Protect Setup Time | 10 | | | ns |
| tSHWL ⁽³⁾ | | Write Protect Hold Time | 10 | | | ns |
| tDP ⁽²⁾ | | CS# High to Deep Power-down Mode | | | 10 | us |
| tRES1 ⁽²⁾ | | CS# High to Standby Mode without Electronic Signature Read | | | 30 | us |
| tRES2 ⁽²⁾ | | CS# High to Standby Mode with Electronic Signature Read | | | 30 | us |
| tW | | Write Status/Configuration Register Cycle Time | | | 40 | ms |
| tBP | | Byte-Program | | 12 | 30 | us |
| tPP | | Page Program Cycle Time | | 0.5 | 3 | ms |
| tPP ⁽⁷⁾ | | Page Program Cycle Time (n bytes) | | 0.008+ (nx0.004) ⁽⁸⁾ | 3 | ms |

| Symbol | Alt. | Parameter | Min. | Typ. ⁽²⁾ | Max. | Unit |
|----------------------|------|---|------|---------------------|------|------|
| tESL ⁽⁹⁾ | | Erase Suspend Latency | | | 20 | us |
| tPSL ⁽⁹⁾ | | Program Suspend Latency | | | 20 | us |
| tPRS ⁽¹⁰⁾ | | Latency between Program Resume and next Suspend | 0.3 | 100 | | us |
| tERS ⁽¹¹⁾ | | Latency between Erase Resume and next Suspend | 0.3 | 400 | | us |
| tSE | | Sector Erase Cycle Time | | 35 | 200 | ms |
| tBE32 | | Block Erase (32KB) Cycle Time | | 0.2 | 1 | s |
| tBE | | Block Erase (64KB) Cycle Time | | 0.35 | 2 | s |
| tCE | | Chip Erase Cycle Time | | 100 | 150 | s |

Notes:

- tCH + tCL must be greater than or equal to 1/ Frequency.
- Typical values given for TA=25°C. Not 100% tested.
- Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.
- Test condition is shown as "Figure 74. Input Test Waveforms and Measurement Level", "Figure 75. Output Loading".
- When dummy cycle=4 (In both QPI & SPI mode), maximum clock rate=84MHz; when dummy cycle=6 (In both QPI & SPI mode), maximum clock rate=104MHz.
When dummy cycle=8 (In both QPI & SPI mode), maximum clock rate=133MHz (for MX25U12835FZNI-08G only).
- The maximum clock rate=33MHz when reading secured OTP area.
- While programming consecutive bytes, Page Program instruction provides optimized timings by selecting to program the whole 256 bytes or only a few bytes between 1-256 bytes.
- "n"=how many bytes to program. In the formula, while n=1, byte program time=12us.
- Latency time is required to complete Erase/Program Suspend operation until WIP bit is "0".
- For tPRS, minimum timing must be observed before issuing the next program suspend command. However, a period equal to or longer than the typical timing is required in order for the program operation to make progress. (The flash memory can accept another suspend command just after 0.3us from suspend resume. However, if the timing is less than 100us from Program Suspend Resume, the content of flash memory might not be changed before the suspend command has been issued.) Not 100% tested.
- For tERS, minimum timing must be observed before issuing the next erase suspend command. However, a period equal to or longer than the typical timing is required in order for the erase operation to make progress. (The flash memory can accept another suspend command just after 0.3us from suspend resume. However, if the timing is less than 400us from Erase Suspend Resume, the content of flash memory might not be changed before the suspend command has been issued.) Not 100% tested.

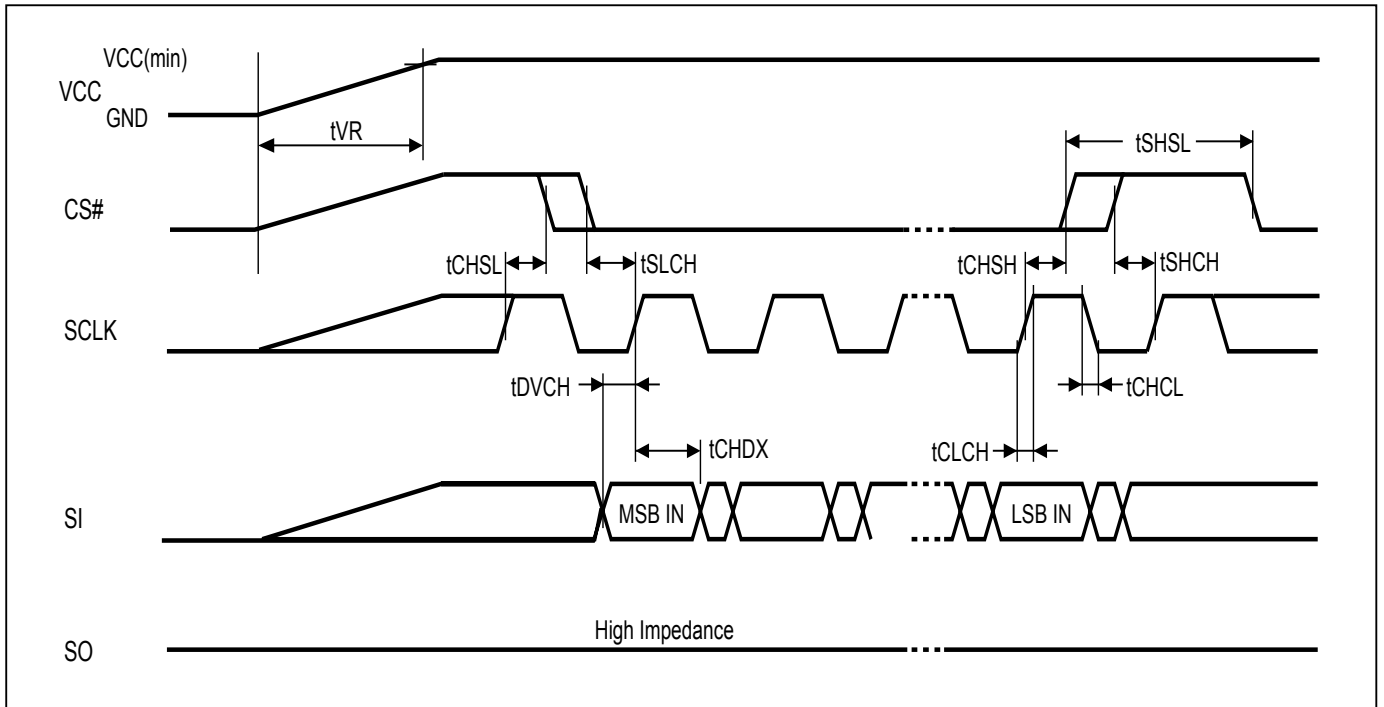
13. OPERATING CONDITIONS

At Device Power-Up and Power-Down

AC timing illustrated in "Figure 77. AC Timing at Device Power-Up" and "Figure 78. Power-Down Sequence" are for the supply voltages and the control signals at device power-up and power-down. If the timing in the figures is ignored, the device will not operate correctly.

During power-up and power-down, CS# needs to follow the voltage applied on VCC to keep the device not to be selected. The CS# can be driven low when VCC reach $V_{cc(min)}$ and wait a period of t_{VSL} .

Figure 77. AC Timing at Device Power-Up



| Symbol | Parameter | Notes | Min. | Max. | Unit |
|--------|---------------|-------|------|--------|------|
| tVR | VCC Rise Time | 1 | | 500000 | us/V |

Notes :

1. Sampled, not 100% tested.
2. For AC spec tCHSL, tSLCH, tDVCH, tCHDX, tSHSL, tCHSH, tSHCH, tCHCL, tCLCH in the figure, please refer to "Table 19. AC Characteristics".

Figure 78. Power-Down Sequence

During power-down, CS# needs to follow the voltage drop on VCC to avoid mis-operation.

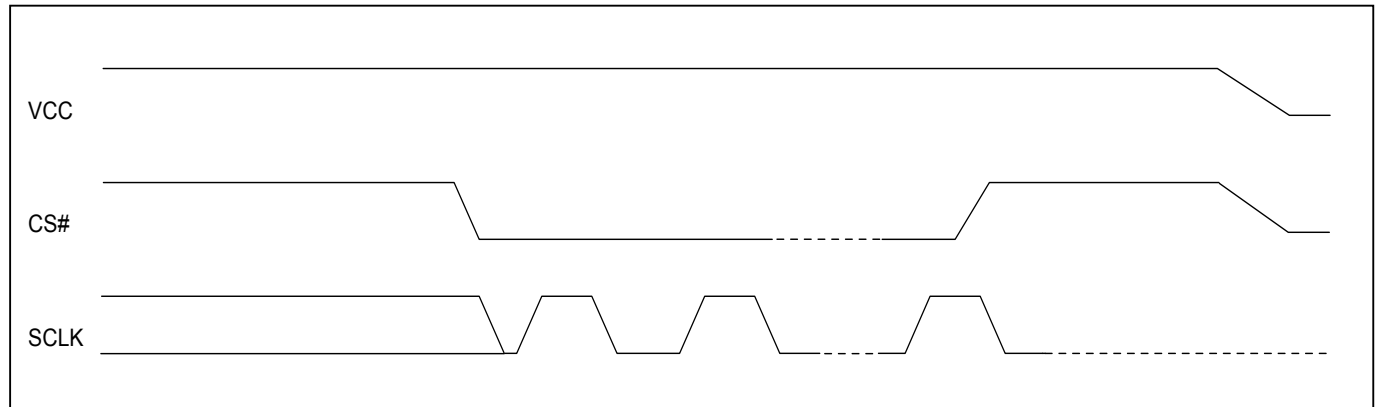
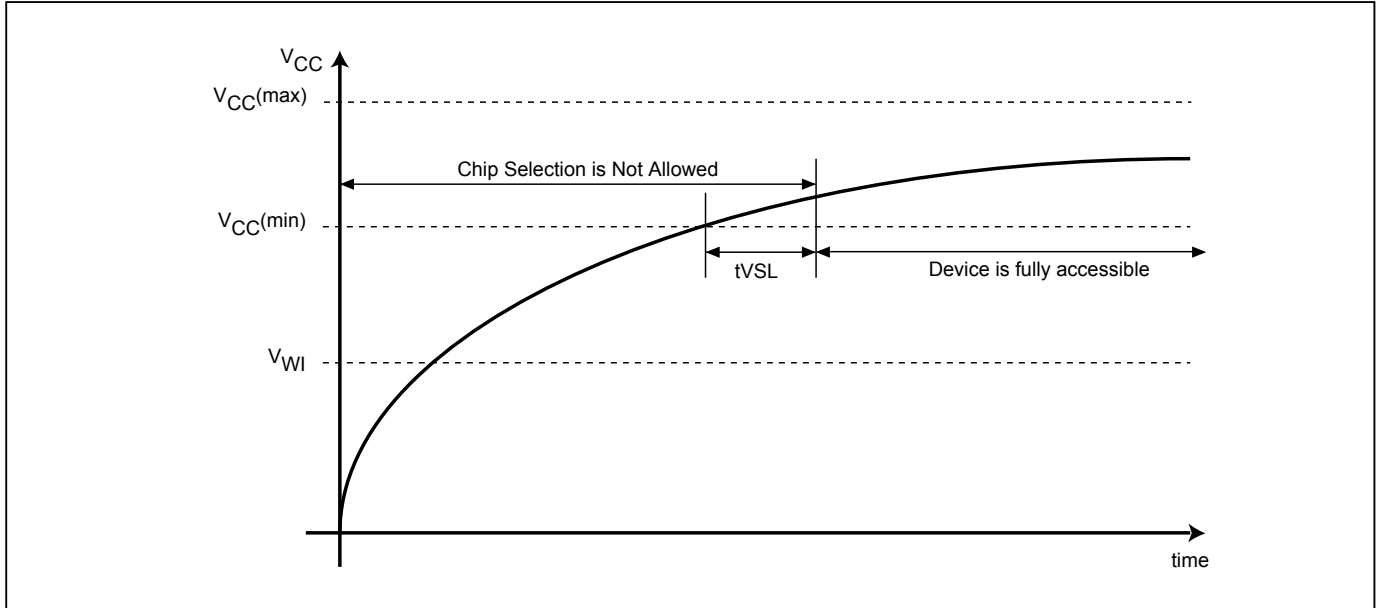


Figure 79. Power-up Timing



Note: VCC (max.) is 2.0V and VCC (min.) is 1.65V.

Table 20. Power-Up Timing and VWI Threshold

| Symbol | Parameter | Min. | Max. | Unit |
|---------------------|-------------------------------------|------|------|------|
| tVSL ⁽¹⁾ | VCC(min) to CS# low (VCC Rise Time) | 800 | | us |
| VWI ⁽¹⁾ | Write Inhibit Voltage | 1.0 | 1.4 | V |

Note: 1. These parameters are characterized only.

Figure 80. Power Up/Down and Voltage Drop

For Power-down to Power-up operation, the VCC of flash device must descend to be lower than V_{PVD} for the least tPVD timing, to ensure the flash memory to initialize correctly. Please check ["Table 21. Power-Up/Down and Voltage Drop"](#) for more detail.

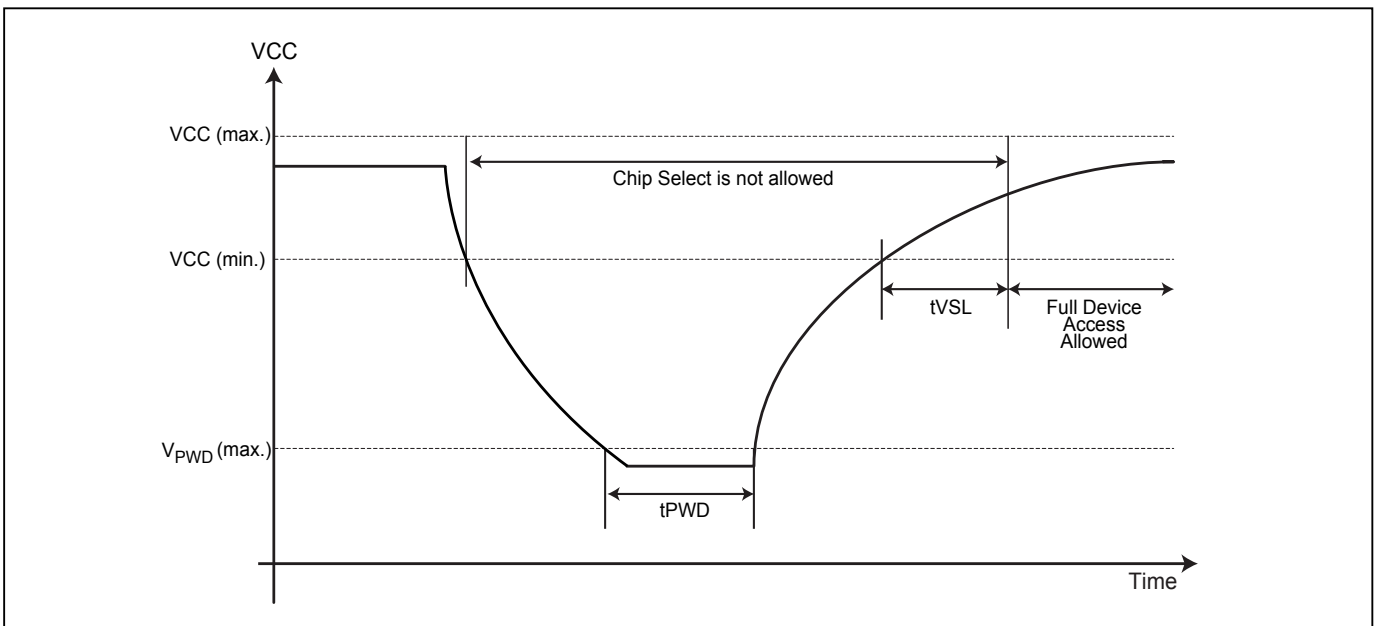


Table 21. Power-Up/Down and Voltage Drop

| Symbol | Parameter | Min. | Max. | Unit |
|------------------|---|------|------|------|
| V _{PWD} | VCC voltage needed to below V _{PWD} for ensuring initialization will occur | | 0.9 | V |
| tPWD | The minimum duration for ensuring initialization will occur | 300 | | us |
| tVSL | VCC(min) to CS# low (VCC Rise Time) | 800 | | us |
| VCC | VCC Power Supply | 1.65 | 2.0 | V |

13-1. Initial Delivery State

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

14. ERASE AND PROGRAMMING PERFORMANCE

| Parameter | Min. | Typ. ⁽¹⁾ | Max. ⁽²⁾ | Unit |
|--|------|---------------------|---------------------|--------|
| Write Status Register Cycle Time | | | 40 | ms |
| Sector Erase Cycle Time (4KB) | | 35 | 200 | ms |
| Block Erase Cycle Time (32KB) | | 0.2 | 1 | s |
| Block Erase Cycle Time (64KB) | | 0.35 | 2 | s |
| Chip Erase Cycle Time | | 100 | 150 | s |
| Byte Program Time (via page program command) | | 12 ⁽⁵⁾ | 30 | us |
| Page Program Time | | 0.5 ⁽⁵⁾ | 3 | ms |
| Erase/Program Cycle | | 100,000 | | cycles |

Note:

1. Typical erase assumes the following conditions: 25°C, 1.8V, and all zero pattern.
2. Under worst conditions of 85°C and 1.65V.
3. System-level overhead is the time required to execute the first-bus-cycle sequence for the programming command.
4. The maximum chip programming time is evaluated under the worst conditions of 0°C, VCC=1.8V, and 100K cycle with 90% confidence level.
5. Typical program assumes the following conditions: 25°C, 1.8V, and checkerboard pattern.

15. LATCH-UP CHARACTERISTICS

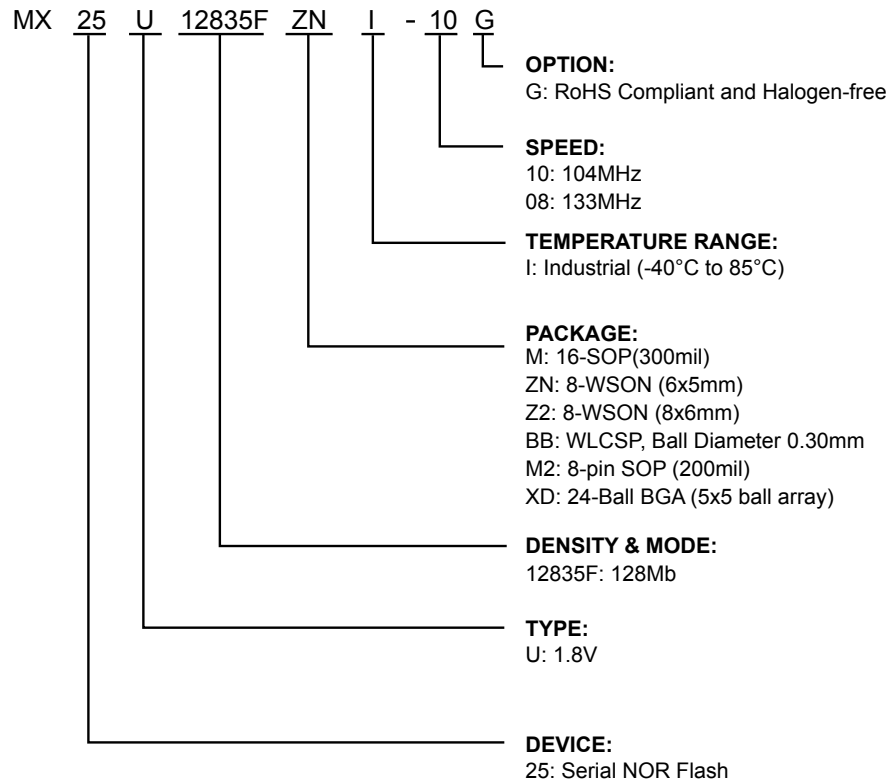
| | Min. | Max. |
|---|--------|------------|
| Input Voltage with respect to GND on all power pins, SI, CS# | -1.0V | 2 VCCmax |
| Input Voltage with respect to GND on SO | -1.0V | VCC + 1.0V |
| Current | -100mA | +100mA |
| Includes all pins except VCC. Test conditions: VCC = 1.8V, one pin at a time. | | |

16. ORDERING INFORMATION

Please contact Macronix regional sales for the latest product selection and available form factors.

| PART NO. | CLOCK (MHz) | TEMPERATURE | PACKAGE | Remark |
|--------------------|--------------------|--------------------|---------------------------------|----------------------|
| MX25U12835FMI-10G | 104 | -40°C to 85°C | 16-SOP (300mil) | |
| MX25U12835FZNI-10G | 104 | -40°C to 85°C | 8-WSON (6x5mm) | |
| MX25U12835FZ2I-10G | 104 | -40°C to 85°C | 8-WSON (8x6mm) | |
| MX25U12835FZNI-08G | 133 | -40°C to 85°C | 8-WSON (6x5mm) | |
| MX25U12835FBBI-10G | 104 | -40°C to 85°C | 23-Ball WLCSP | Ball Diameter 0.30mm |
| MX25U12835FM2I-10G | 104 | -40°C to 85°C | 8-SOP (200mil) | |
| MX25U12835FXDI-10G | 104 | -40°C to 85°C | 24-Ball BGA (5x5 ball array) | |

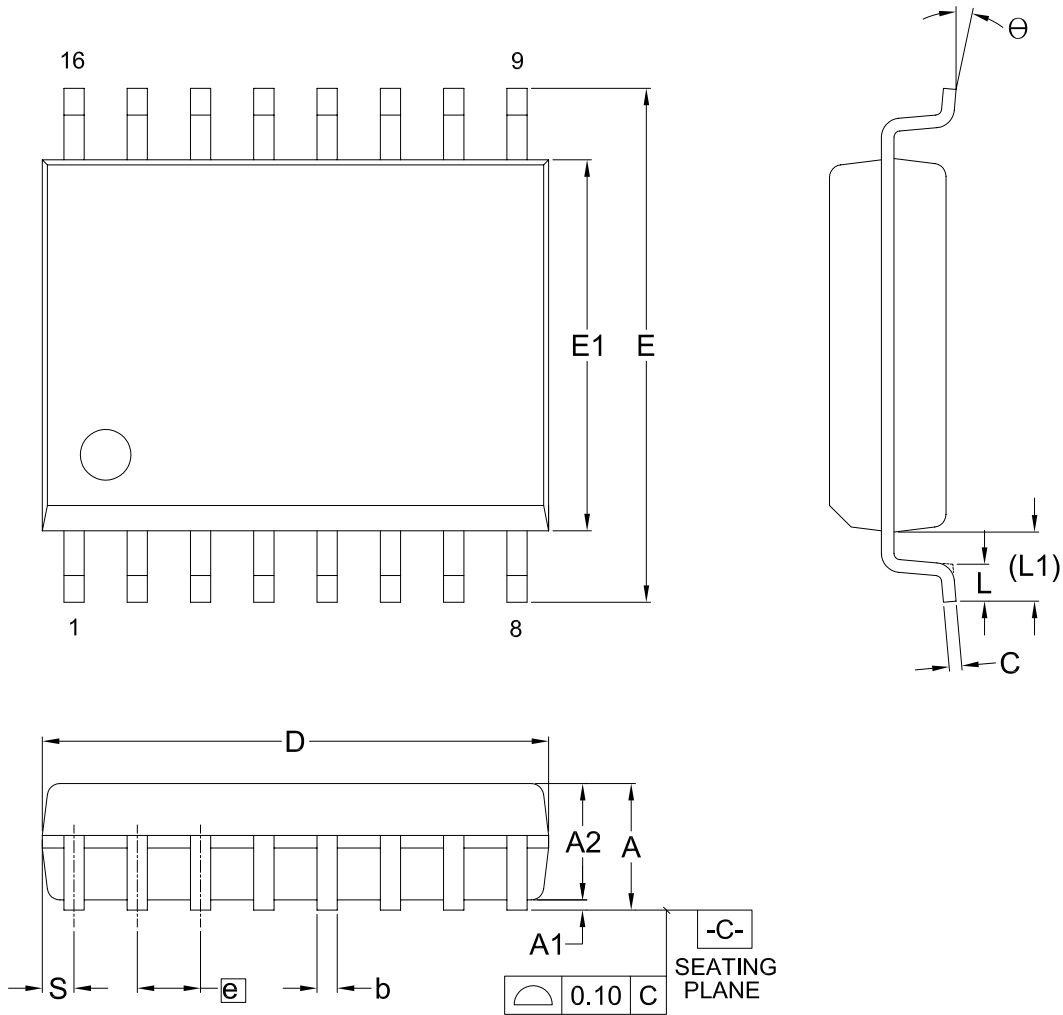
17. PART NAME DESCRIPTION



18. PACKAGE INFORMATION

18-1. 16-pin SOP (300mil)

Doc. Title: Package Outline for SOP 16L (300MIL)



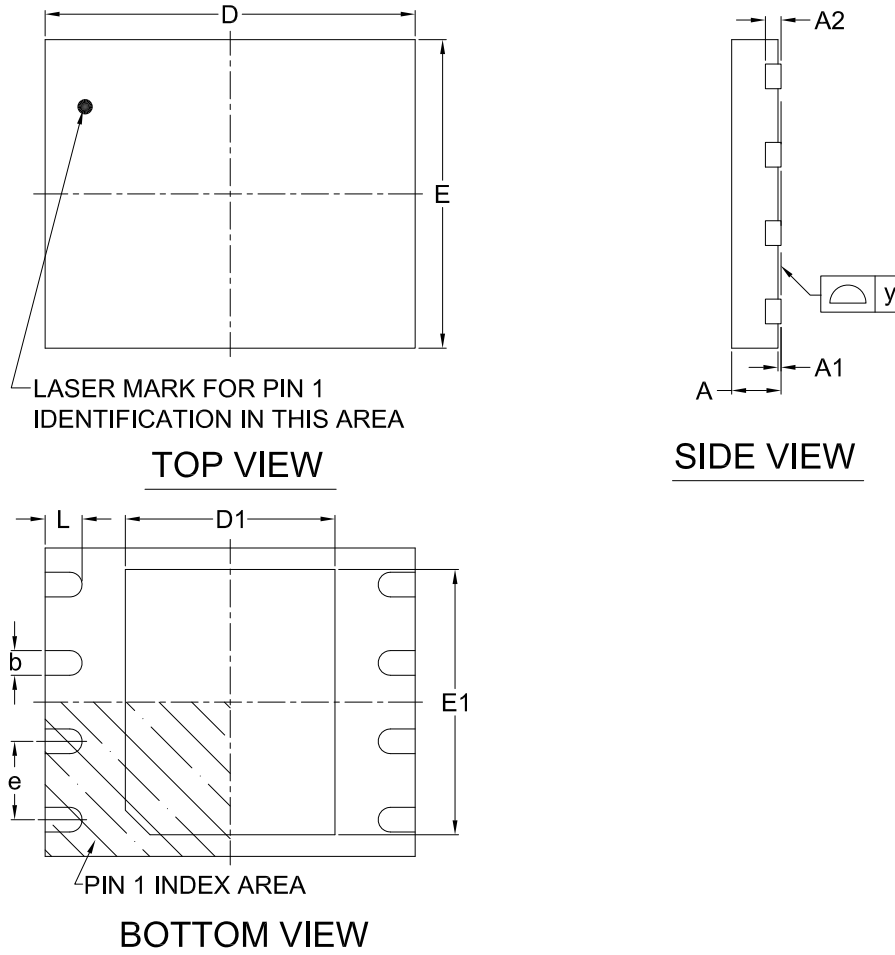
Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL | | A | A1 | A2 | b | C | D | E | E1 | e | L | L1 | S | θ |
|--------|------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|----|
| UNIT | | | | | | | | | | | | | | |
| mm | Min. | -- | 0.10 | 2.25 | 0.31 | 0.20 | 10.10 | 10.10 | 7.42 | -- | 0.40 | 1.31 | 0.51 | 0° |
| | Nom. | -- | 0.20 | 2.35 | 0.41 | 0.25 | 10.30 | 10.30 | 7.52 | 1.27 | 0.84 | 1.44 | 0.64 | 5° |
| | Max. | 2.65 | 0.30 | 2.45 | 0.51 | 0.30 | 10.50 | 10.50 | 7.60 | -- | 1.27 | 1.57 | 0.77 | 8° |
| Inch | Min. | -- | 0.004 | 0.089 | 0.012 | 0.008 | 0.397 | 0.397 | 0.292 | -- | 0.016 | 0.052 | 0.020 | 0° |
| | Nom. | -- | 0.008 | 0.093 | 0.016 | 0.010 | 0.405 | 0.405 | 0.296 | 0.050 | 0.033 | 0.057 | 0.025 | 5° |
| | Max. | 0.104 | 0.012 | 0.096 | 0.020 | 0.012 | 0.413 | 0.413 | 0.299 | -- | 0.050 | 0.062 | 0.030 | 8° |

| Dwg. No. | Revision | Reference | | |
|-----------|----------|-----------|------|--|
| | | JEDEC | EIAJ | |
| 6110-1402 | 13 | MS-013 | | |

18-2. 8-land WSON (6x5mm)

Doc. Title: Package Outline for WSON 8L (6x5x0.8MM, LEAD PITCH 1.27MM)



Note:

This package has an exposed metal pad underneath the package. It is recommended to leave the metal pad floating or to connect it to the same ground as the GND pin of the package. Do not connect the metal pad to any other voltage or signal line on the PCB. Avoid placing vias or traces underneath the metal pad. Connection of this metal pad to any other voltage or signal line can result in shorts and/or electrical malfunction of the device.

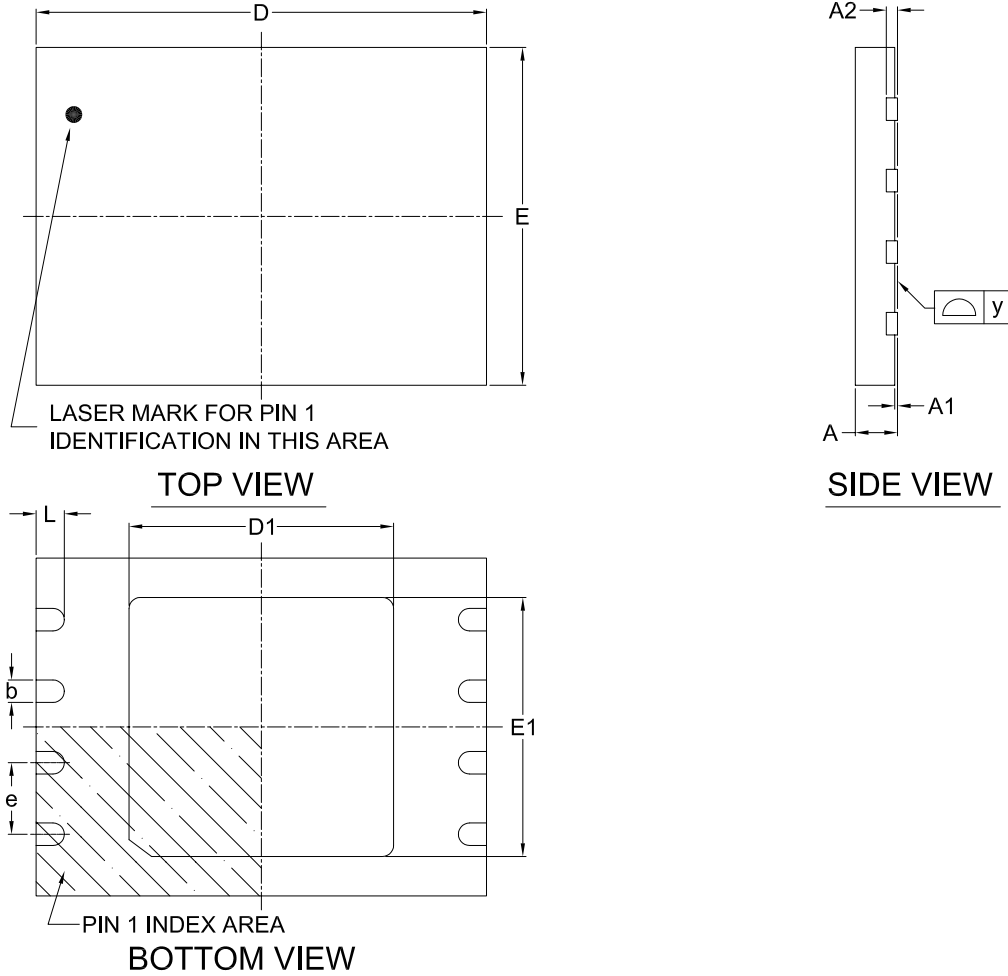
Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL | | A | A1 | A2 | b | D | D1 | E | E1 | L | e | y |
|--------|------|-------|-------|-------|-------|-------|-------|-------|-------|-------|------|-------|
| UNIT | | | | | | | | | | | | |
| mm | Min. | 0.70 | -- | -- | 0.35 | 5.90 | 3.30 | 4.90 | 3.90 | 0.50 | -- | 0.00 |
| | Nom. | -- | -- | 0.20 | 0.40 | 6.00 | 3.40 | 5.00 | 4.00 | 0.60 | 1.27 | -- |
| | Max. | 0.80 | 0.05 | -- | 0.48 | 6.10 | 3.50 | 5.10 | 4.10 | 0.75 | -- | 0.05 |
| Inch | Min. | 0.028 | -- | -- | 0.014 | 0.232 | 0.129 | 0.193 | 0.154 | 0.020 | -- | 0.00 |
| | Nom. | -- | -- | 0.008 | 0.016 | 0.236 | 0.134 | 0.197 | 0.157 | 0.024 | 0.05 | -- |
| | Max. | 0.032 | 0.002 | -- | 0.019 | 0.240 | 0.138 | 0.201 | 0.161 | 0.030 | -- | 0.002 |

| Dwg. No. | Revision | Reference | | | |
|-----------|----------|-----------|------|--|--|
| | | JEDEC | EIAJ | | |
| 6110-3401 | 8 | MO-220 | | | |

18-3. 8-land WSON (8x6mm)

Doc. Title: Package Outline for WSON 8L (8x6x0.8MM, LEAD PITCH 1.27MM)



Note:

This package has an exposed metal pad underneath the package. It is recommended to leave the metal pad floating or to connect it to the same ground as the GND pin of the package. Do not connect the metal pad to any other voltage or signal line on the PCB. Avoid placing vias or traces underneath the metal pad. Connection of this metal pad to any other voltage or signal line can result in shorts and/or electrical malfunction of the device.

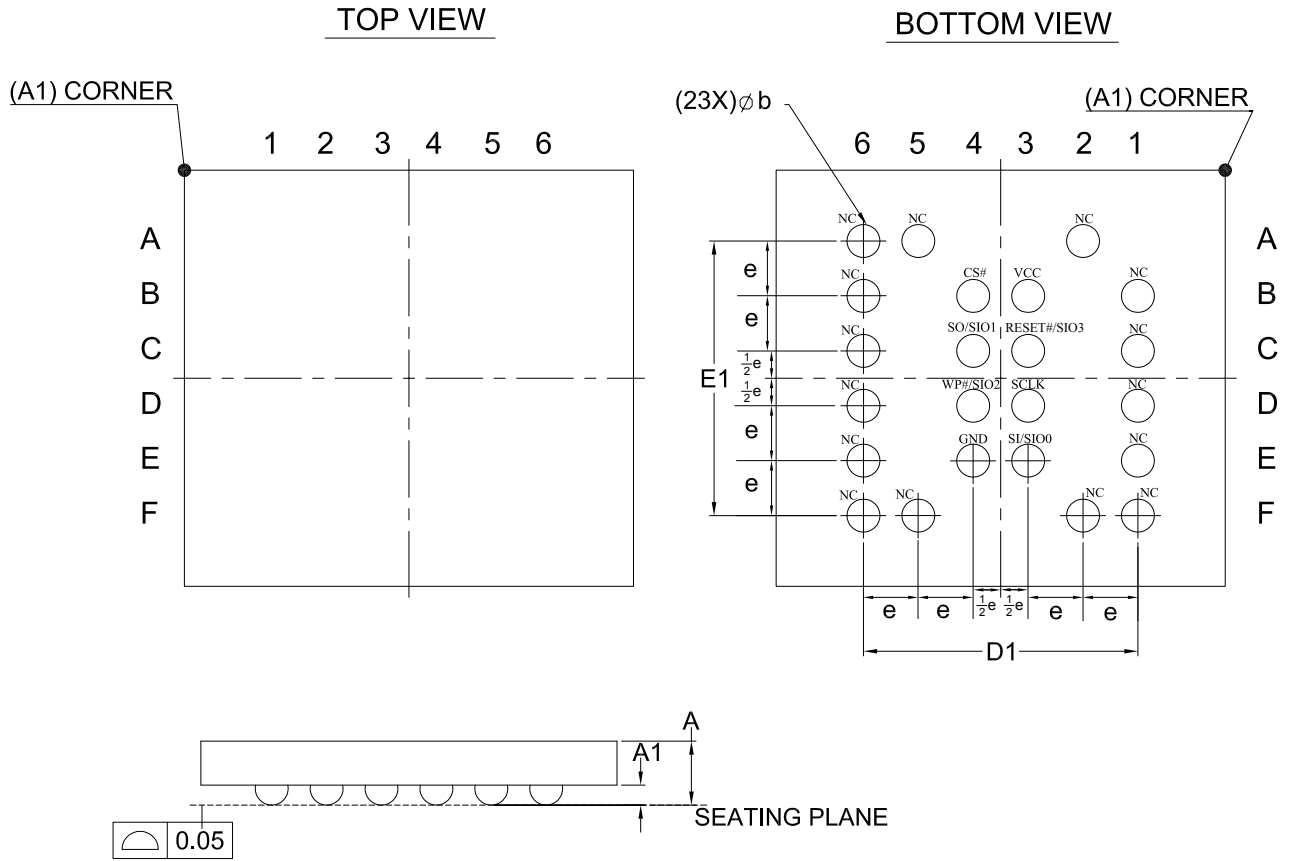
Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL | | A | A1 | A2 | b | D | D1 | E | E1 | L | e | y |
|--------|------|-------|-------|-------|-------|-------|-------|-------|-------|-------|------|-------|
| UNIT | | | | | | | | | | | | |
| mm | Min. | 0.70 | --- | --- | 0.35 | 7.90 | 4.60 | 5.90 | 4.50 | 0.40 | --- | 0.00 |
| | Nom. | --- | --- | 0.20 | 0.40 | 8.00 | 4.70 | 6.00 | 4.60 | 0.50 | 1.27 | --- |
| | Max. | 0.80 | 0.05 | --- | 0.48 | 8.10 | 4.80 | 6.10 | 4.70 | 0.60 | --- | 0.05 |
| Inch | Min. | 0.028 | --- | --- | 0.014 | 0.311 | 0.181 | 0.232 | 0.177 | 0.016 | --- | 0.00 |
| | Nom. | --- | --- | 0.008 | 0.016 | 0.315 | 0.185 | 0.236 | 0.181 | 0.020 | 0.05 | --- |
| | Max. | 0.032 | 0.002 | --- | 0.019 | 0.319 | 0.189 | 0.240 | 0.185 | 0.024 | --- | 0.002 |

| Dwg. No. | Revision | Reference | | |
|-----------|----------|-----------|------|--|
| | | JEDEC | EIAJ | |
| 6110-3402 | 9 | MO-220 | | |

18-4. 23-ball WLCSP (Ball Diameter 0.30mm)

Title: Package Outline for 23Ball WLCSP (BALL DIAMETER 0.30MM)



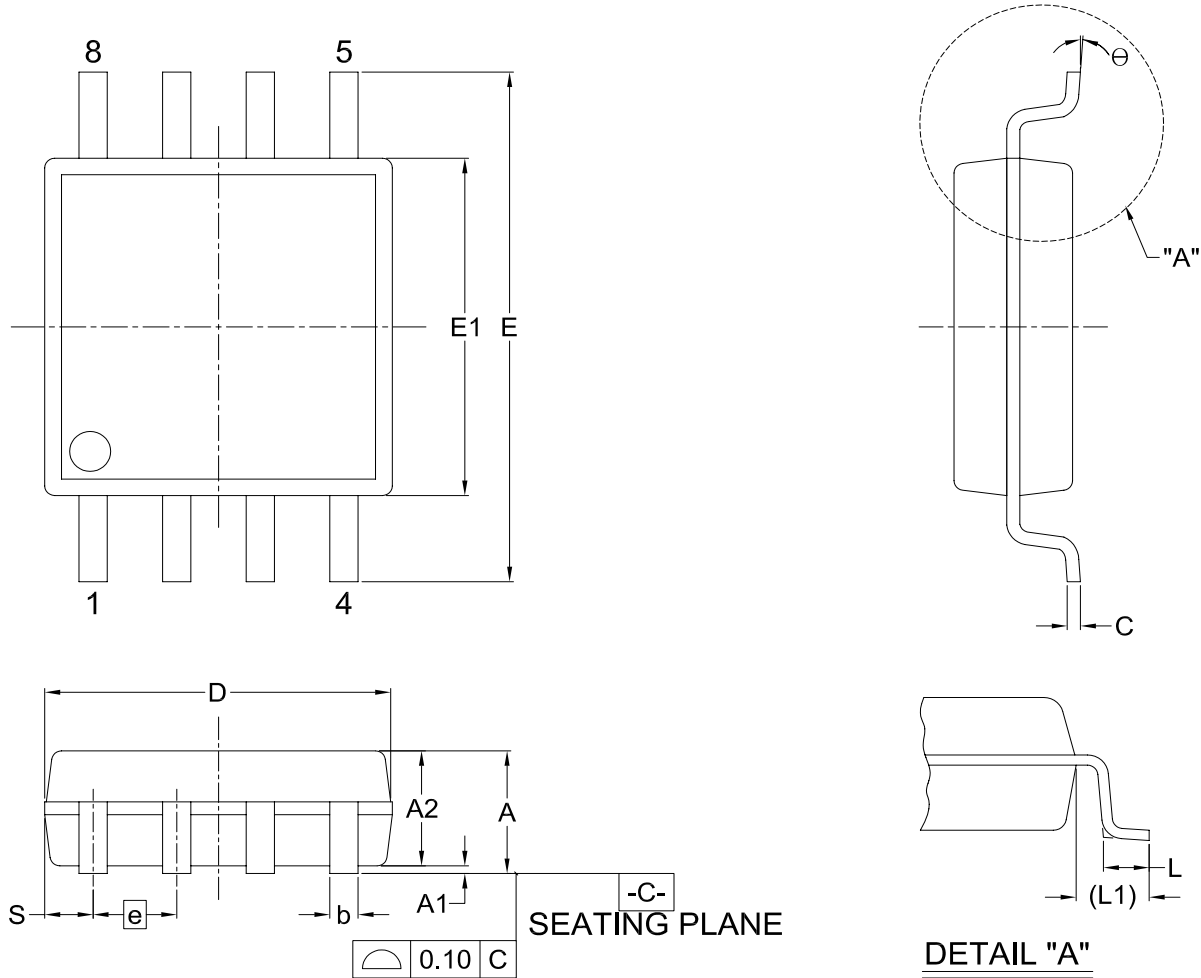
Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL | | A | A1 | b | D1 | E1 | e |
|--------|------|-------|--------|-------|-------|-------|-----------|
| mm | Min. | 0.42 | 0.152 | 0.24 | --- | --- | --- |
| | Nom. | 0.47 | 0.167 | 0.30 | 2.50 | 2.50 | 0.50 BSC |
| | Max. | 0.52 | 0.182 | 0.36 | --- | --- | --- |
| Inch | Min. | 0.017 | 0.0060 | 0.009 | --- | --- | --- |
| | Nom. | 0.019 | 0.0066 | 0.012 | 0.098 | 0.098 | 0.020 BSC |
| | Max. | 0.021 | 0.0072 | 0.014 | --- | --- | --- |

Please contact local Macronix sales channel for complete package dimensions.

18-5. 8-pin SOP (200mil)

Doc. Title: Package Outline for SOP 8L 200MIL (official name - 209MIL)



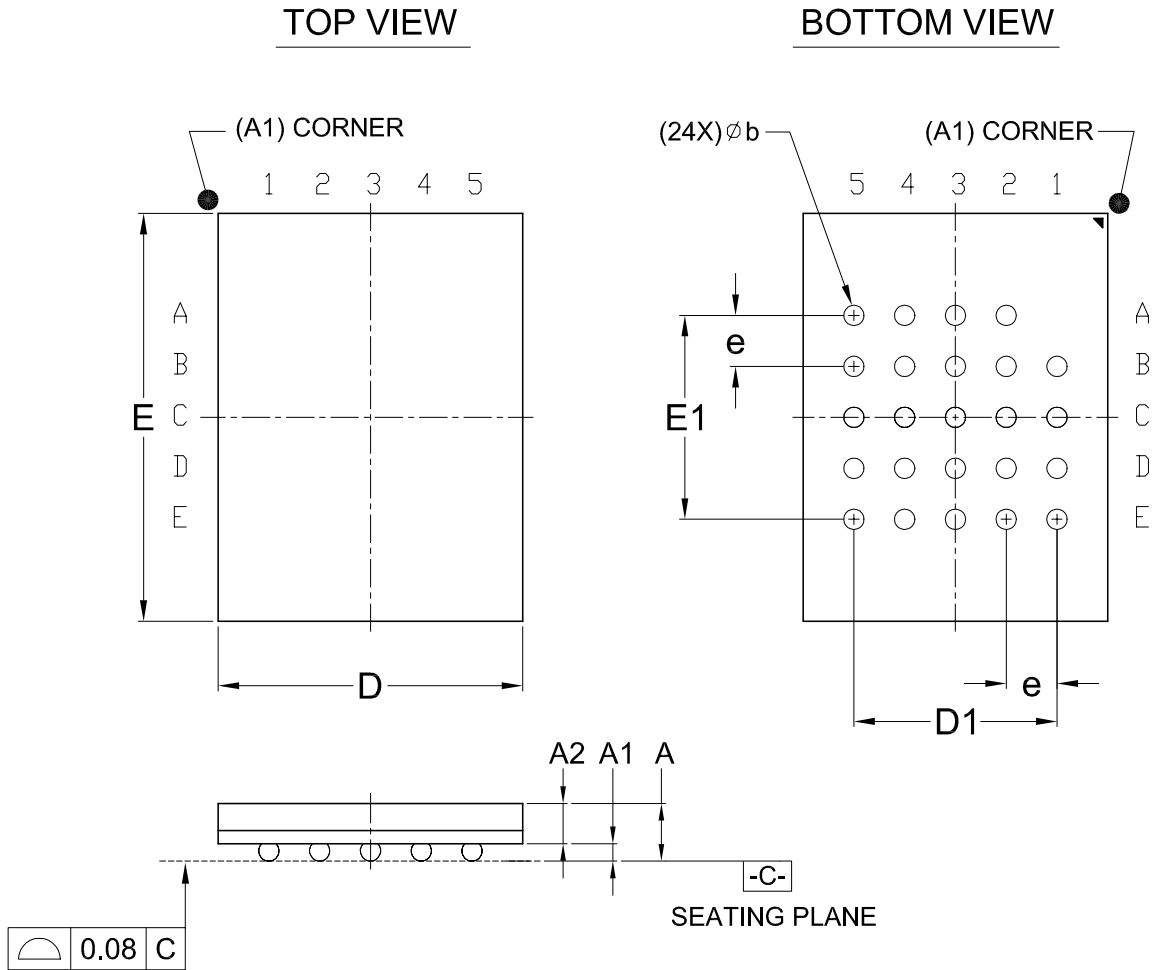
Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL | | A | A1 | A2 | b | C | D | E | E1 | e | L | L1 | S | θ |
|--------|------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|----------|
| UNIT | | | | | | | | | | | | | | |
| mm | Min. | 1.75 | 0.05 | 1.70 | 0.36 | 0.19 | 5.13 | 7.70 | 5.18 | -- | 0.50 | 1.21 | 0.62 | 0° |
| | Nom. | 1.95 | 0.15 | 1.80 | 0.41 | 0.20 | 5.23 | 7.90 | 5.28 | 1.27 | 0.65 | 1.31 | 0.74 | 5° |
| | Max. | 2.16 | 0.20 | 1.91 | 0.51 | 0.25 | 5.33 | 8.10 | 5.38 | -- | 0.80 | 1.41 | 0.88 | 8° |
| Inch | Min. | 0.069 | 0.002 | 0.067 | 0.014 | 0.007 | 0.202 | 0.303 | 0.204 | -- | 0.020 | 0.048 | 0.024 | 0° |
| | Nom. | 0.077 | 0.006 | 0.071 | 0.016 | 0.008 | 0.206 | 0.311 | 0.208 | 0.050 | 0.026 | 0.052 | 0.029 | 5° |
| | Max. | 0.085 | 0.008 | 0.075 | 0.020 | 0.010 | 0.210 | 0.319 | 0.212 | -- | 0.031 | 0.056 | 0.035 | 8° |

| Dwg. No. | Revision | Reference | | | |
|-----------|----------|-----------|------|--|--|
| | | JEDEC | EIAJ | | |
| 6110-1406 | 5 | | | | |

18-6. 24-Ball BGA (5x5 ball array)

Doc. Title: Package Outline for CSP 24BALL (6x8x1.2MM, BALL PITCH 1.0MM, BALL DIAMETER 0.4MM, 5x5 BALL ARRAY)



Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL | | A | A1 | A2 | b | D | D1 | E | E1 | e |
|--------|------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| UNIT | | | | | | | | | | |
| mm | Min. | --- | 0.25 | 0.65 | 0.35 | 5.90 | --- | 7.90 | --- | --- |
| | Nom. | --- | 0.30 | --- | 0.40 | 6.00 | 4.00 | 8.00 | 4.00 | 1.00 |
| | Max. | 1.20 | 0.35 | --- | 0.45 | 6.10 | --- | 8.10 | --- | --- |
| Inch | Min. | --- | 0.010 | 0.026 | 0.014 | 0.232 | --- | 0.311 | --- | --- |
| | Nom. | --- | 0.012 | --- | 0.016 | 0.236 | 0.157 | 0.315 | 0.157 | 0.039 |
| | Max. | 0.047 | 0.014 | --- | 0.018 | 0.240 | --- | 0.319 | --- | --- |

| Dwg. No. | Revision | Reference | | |
|-------------|----------|-----------|------|--|
| | | JEDEC | EIAJ | |
| 6110-4257.1 | 1 | | | |

19. REVISION HISTORY

| Revision No. | Description | Page | Date |
|--|---|--|-------------|
| 0.01 | 1. Changed title from "Advanced Information" to "Preliminary" | P4 | OCT/14/2011 |
| | 2. Modified Chip Erase Cycle Time | P80,85 | |
| | 3. Modified tVSL(min.) from 500us to 800us | P84 | |
| | 4. Modified Write Protection Selection (WPSEL) description | P59,60 | |
| | 5. Modified Power-up Timing | P84 | |
| | 6. Changed EPN of 8WSON(8x6mm) | P86,87 | |
| 1.0 | 1. Modified tCE from 100 to 72 sec.(typ.), 200 to 160 sec.(max.) | P80,85 | FEB/03/2012 |
| | 2. Modified tVSL(min.) in Power-Up Timing Table | P84 | |
| | 3. Modified value of tWHSL, tSHWL, tCHDX, tCHSH, tSHCH, tSHSL and ISB1(max.) in CHARACTERISTICS Table | P79,80 | |
| | 4. Added Reset# description for write/erase execution | P33,49,50-53,58,75 | |
| 1.1 | 1. Modified Normal READ (fRSCLK) to 55MHz | P80 | AUG/31/2012 |
| | 2. Modified Normal Read (fRSCLK) Clock High/Low Time | P80 | |
| | 3. Modified content | P27-28 | |
| 1.2 | 1. Added ICC1: 27mA (typ.) at 133 MHz for MX25U12835FZNI-08G | P4,81 | DEC/17/2012 |
| | 2. Added Configurable Dummy Cycle for MX25U12835FZNI-08G | P16,32,42,43,48,49 | |
| | 3. Modified tCLQV value at 30pF Loading condition | P82 | |
| 1.3 | 1. Added DREAD function | P6,13,16,40 | OCT/23/2013 |
| | 2. Added QREAD function | P6,13,16,42 | |
| | 3. Updated DREAD(1-1-2) / QREAD(1-1-4) in SFDP Table | P75,76 | |
| | 4. Modified tVSL value | P88 | |
| | 5. Modified accepted commands after Erase Suspend | P69 | |
| | 6. Modified VCC to Ground Potential | P81 | |
| | 7. Updated Erase/Page Program time, Consumption current | P4 | |
| | 8. Updated ISB1, ISB2, ICC3 and ICC4 in DC Table | P83 | |
| | 9. Updated tPP, tSE, tBE32, tBE and tCE in AC Table | P84 | |
| | 10. Updated Erase time and Page Program time | P89 | |
| | 11. Modified Data Retention value | P4 | |
| 1.4 | 1. Removed Advanced Information status of MX25U12835FZNI-08G | P90 | FEB/12/2014 |
| 1.5 | 1. Modified AC Characteristics for MX25U12835FZNI-08G | P84 | SEP/29/2014 |
| 1.6 | 1. Updated Package Outline of SOP 16L (300mil) | P92 | DEC/21/2015 |
| | 2. Updated SFDP Table and notes (No. 6) | P74-78 | |
| | 3. Added parameters name for Suspend/Resume and updated Suspend/Resume descriptions | P85 P68-70 | |
| | 5. Added 23-ball WLCSP and 8-pin SOP (200mil) package & part number: MX25U12835FM2I-10G as Advanced Information | P5,7,90-91,95-96 | |
| | 6. Updated BLOCK DIAGRAM | P8 | |
| | 7. Added "Figure 56. Write Security Register (WRSCUR) Sequence (Command 2F)". | P61 | |
| | 8. Added "Figure 59. Write Protection Selection (WPSEL) Sequence (Command 68)" | P63 | |
| | 9. Removed the tRCR / tRCP / tRCE parameters and updated "10. RESET": "Figure 71. RESET Timing", "Table 15-1. Reset Timing-(Power On)", "Table 15-2. Reset Timing-(Other Operation)" and "Figure 67. Software Reset Recovery" | P84 P71-72,79 | |
| | 10. Removed Performance Enhance Mode Reset figures and modified the related descriptions | P19,51 | |
| | 11. Modified W4READ and Burst Read descriptions | P16,43,47 | |
| | 1.7 | 1. Added 24-Ball BGA product information | |
| 2. Added parameters and waveforms for Power Up/Down operations | | P88,89 | |
| 3. Added a statement for product ordering information. | | P90 | |
| 4. Updated the minimum VIH (Input High Voltage). | | P83 | |



| Revision No. | Description | Page | Date |
|--------------|---|---------|-------------|
| 1.8 | 1. Updated Package Outline of 23-ball WLCSP | P95 | MAY/03/2017 |
| | 2. Updated <i>"18-3. 8-land WSON (8x6mm)"</i> | P94 | |
| | 3. Updated <i>"18-6. 24-Ball BGA (5x5 ball array)"</i> | P97 | |
| | 4. Updated the note for the internal pull up status of RESET#/SIO3 and WP#/SIO2 | P7 | |
| | 5. Updated tVR values | P86, 89 | |
| | 6. Added <i>"Figure 76. SCLK TIMING DEFINITION"</i> | P82 | |
| | 7. Content modification | P11, 31 | |



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