

PRELIMINARY
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MITSUBISHI SEMICONDUCTOR <TRANSISTOR ARRAY>

M63850P/FP

4-UNIT 1.5A DMOS ARRAY WITH CLAMP DIODE

DESCRIPTION

The M63850P/FP is a inverter input power DMOS transistor array that consists of 4 independent output N-channel DMOS transistors.

FEATURES

- 4 circuits of N-channels DMOS
- High breakdown voltage ($V_{DS} \geq 80V$)
- High-current driving ($I_{DS(max)} = 1.5A$)
- With clamping diodes
- Drain-source on-state low resistance ($R_{ON} = 0.72\Omega$, @ $= 1.25A$)
- Wide operating temperature range ($T_a = -40$ to $+85^\circ C$)

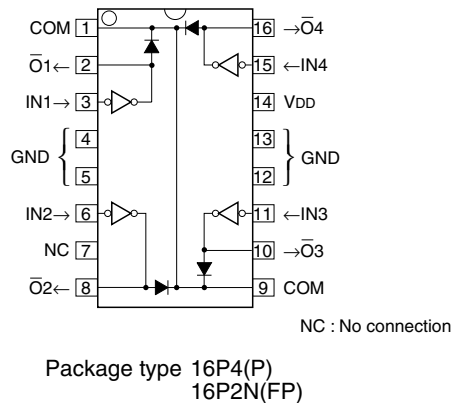
APPLICATION

Drives of relays and printers, digit drives of indication elements (LEDs and lamps)

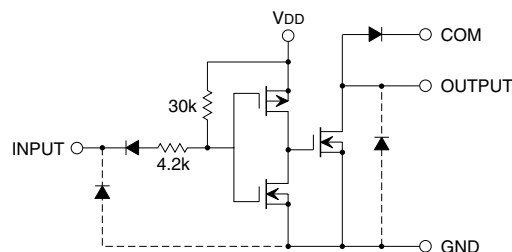
FUNCTION

The M63850P/FP is consists of 4 independent N-channel DMOS transistors. Each DMOS transistor is connected in a common-source with GND PIN. The clamp diodes for spike killers are connected between the output pin and the COM pin of each DMOS transistor. The maximum of Drain current is 1.5A. The maximum Drain-Source voltage is 80V.

PIN CONFIGURATION



CIRCUIT DIAGRAM



The four circuits share the COM and GND.
 The diode, indicated with the dotted line, is parasitic, and cannot be used.

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (Unless otherwise noted, $T_a = -40 \sim +85^\circ C$)

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}	Supply voltage		7	V
V_{DS}	Drain-source voltage	Output, H	$-0.5 \sim +80$	V
I_{DS}	Drain current	Current per circuit output, L	1.5	A
V_I	Input voltage		$-0.5 \sim V_{DD}$	V
V_R	Clamping diode reverse voltage		80	V
I_F	Clamping diode forward current		1.5	A
P_d	Power dissipation	$T_a = 25^\circ C$, when mounted on board	1.47(P)/1.00(FP)	W
T_{opr}	Operating temperature		$-40 \sim +85$	$^\circ C$
T_{stg}	Storage temperature		$-55 \sim +125$	$^\circ C$

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RECOMMENDED OPERATING CONDITIONS (Unless otherwise noted, Ta = -40 ~ +85°C)

Symbol	Parameter	Conditions	Limits			Unit
			min	typ	max	
VDD	Supply voltage		4.5	5.0	5.5	V
VDS	Drain-source voltage		0	—	80	V
IDS	Drain current (Current per 1 circuit when 4 circuits are coming on simultaneously)	VDD = 5V, Duty Cycle P : no more than 4% FP : no more than 2%	0	—	1.25	A
		VDD = 5V, Duty Cycle P : no more than 36% FP : no more than 15%	0	—	0.7	
VIH	"H" input voltage		VCC-1.0	—	VCC	V
VIL	"L" input voltage		0	—	VCC-3.0	V

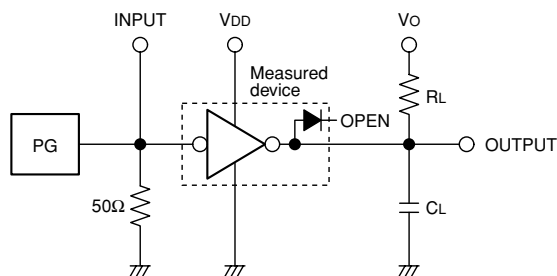
ELECTRICAL CHARACTERISTICS (Unless otherwise noted, Ta = 25°C)

Symbol	Parameter	Test conditions	Limits			Unit
			min	typ	max	
IDD(ON)	On supply current	VDD = 5.5V, VI = 0V, 1 circuit only	—	130	300	μA
IDD(OFF)	Off supply current	VDD = 5.5V, VI = 5.5V	—	—	10	μA
IO(LEAK)	Output leak current	VDD = 5.5V, VI = 5.5V, VDS = 80V	—	—	10	μA
VON	Output on voltage	VI = 4.5V, IDS = 0.7A	—	0.45	0.72	V
		VI = 4.5V, IDS = 1.25A	—	0.9	1.44	
RON	Output on resistance	VI = 4.5V, IDS = 1.25A	—	0.72	1.15	Ω
IIH	"H" input current	VDD = 5.5V, VI = 5.5V	—	—	10	μA
IIL	"L" input current	VDD = 5.5V, VI = 0V	—	-130	-300	μA
IR	Clamping diode reverse current	VR = 80V	—	—	10	μA
VF	Clamping diode forward voltage	IF = 1.25A	—	1.3	2.0	V

SWITCHING CHARACTERISTICS (Unless otherwise noted, Ta = 25°C)

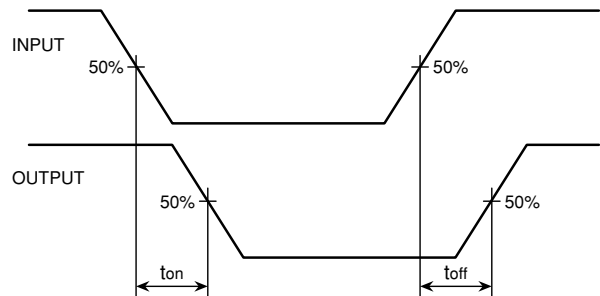
Symbol	Parameter	Test conditions	Limits			Unit
			min	typ	max	
ton	Turn-on time	CL = 15pF (Note 1)	—	45	—	ns
toff	Turn-off time		—	125	—	ns

Note 1 : TEST CIRCUIT



- (1) Pulse generator (PG) characteristics : PRR = 1kHz, tw = 10μs, tr = 6ns, tf = 6ns, Zo = 50Ω, VIH = 5V
- (2) Input-output conditions : RL = 8.3Ω, Vo = 10V, VDD = 4.5V
- (3) Electrostatic capacity CL includes floating capacitance at connections and input capacitance at probes.

TIMING DIAGRAM

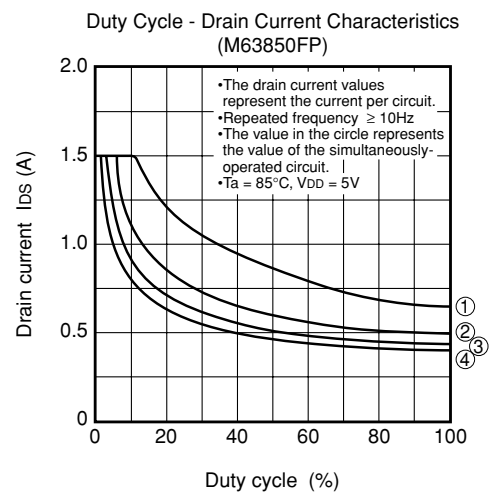
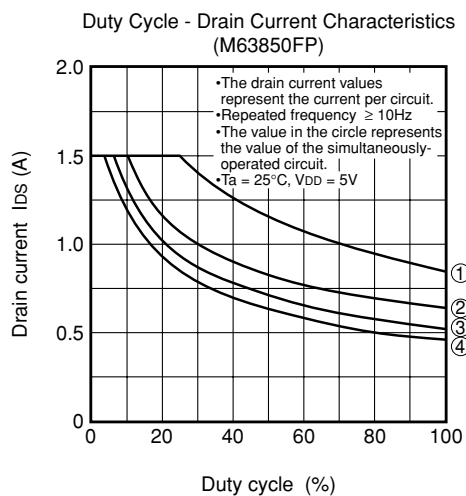
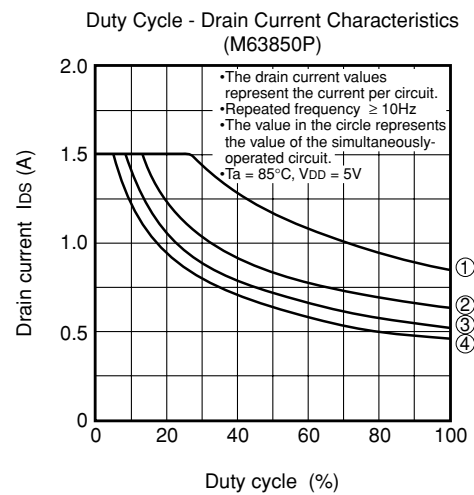
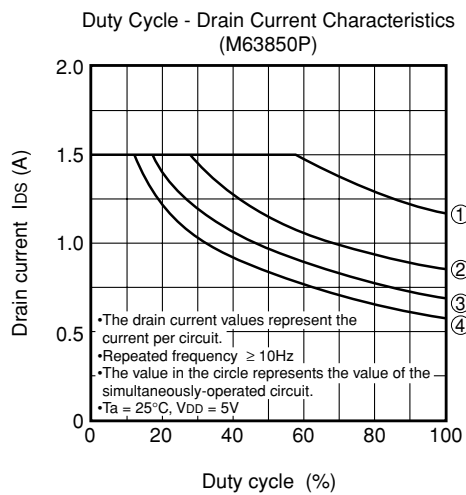
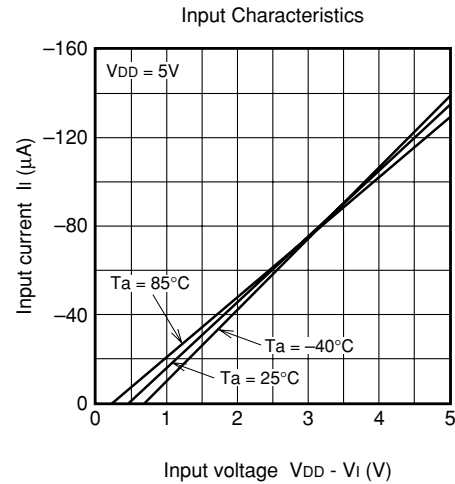
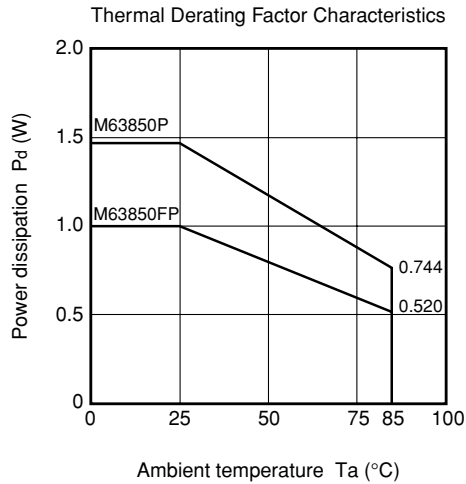


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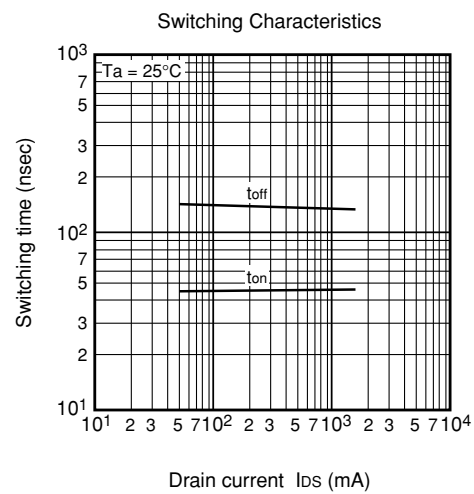
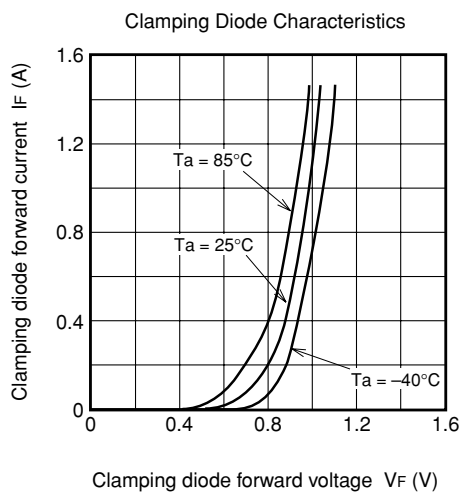
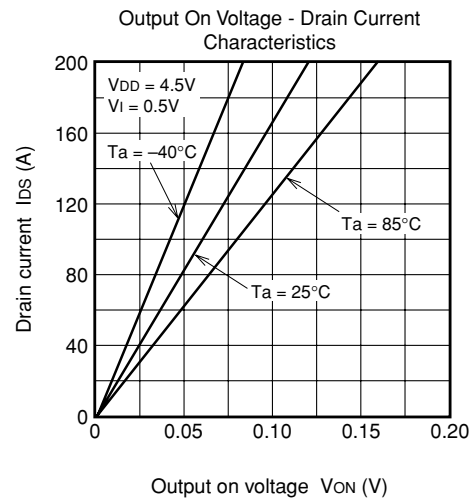
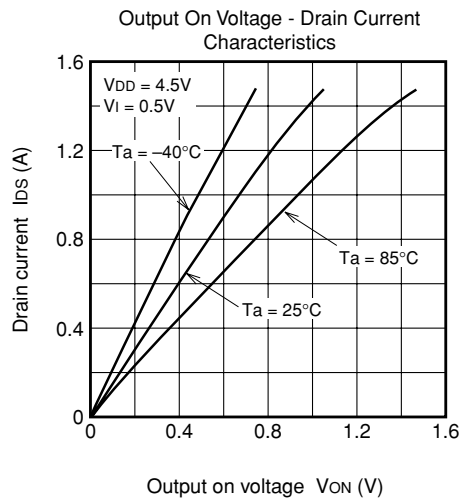
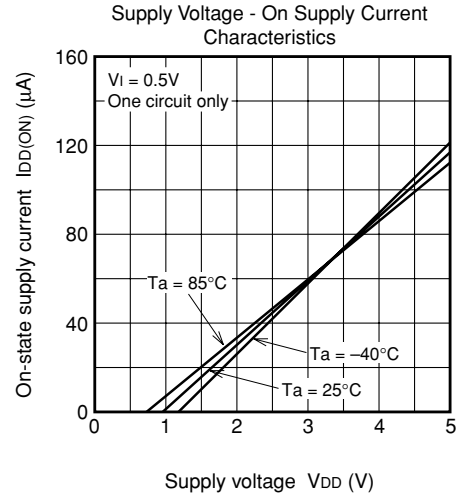
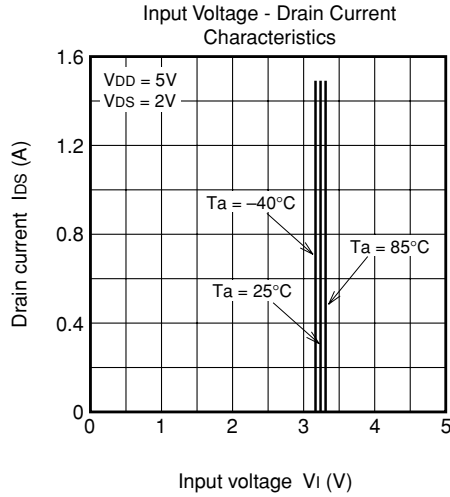
TYPICAL CHARACTERISTICS



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