

## CDx4HCT573 Octal Transparent D-Type Latches With 3-State Outputs

## 1 Features

- 4.5-V to 5.5-V  $V_{CC}$  operation
- Wide operating temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- Balanced propagation delays and transition times
- Standard outputs drive up to 10 LS-TTL loads
- Significant power reduction compared to LS-TTL Logic ICs
- Inputs are TTL-voltage compatible

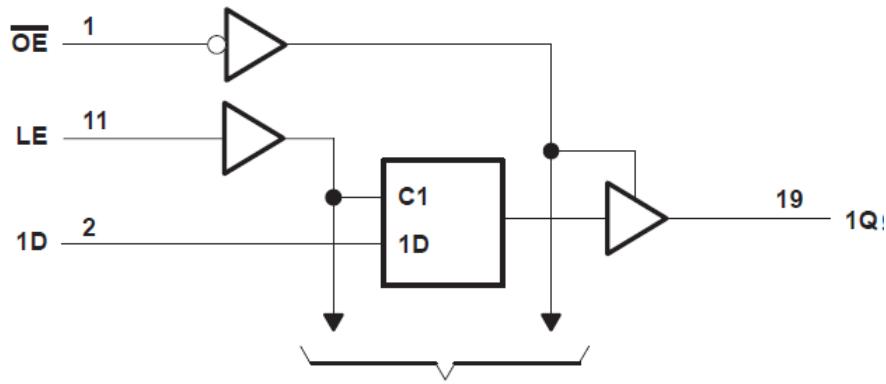
## 2 Description

The 'HCT573 devices are octal transparent D-type latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

## Device Information

| PART NUMBER   | PACKAGE <sup>(1)</sup> | BODY SIZE (NOM)           |
|---------------|------------------------|---------------------------|
| CD74HCT573M   | SOIC (20)              | 12.80 mm $\times$ 7.50 mm |
| CD74HCT573DBR | SSOP (20)              | 7.20 mm $\times$ 5.30 mm  |
| CD74HCT573E   | PDIP (20)              | 25.40 mm $\times$ 6.35 mm |
| CD54HCT573F   | CDIP (20)              | 26.92 mm $\times$ 6.92 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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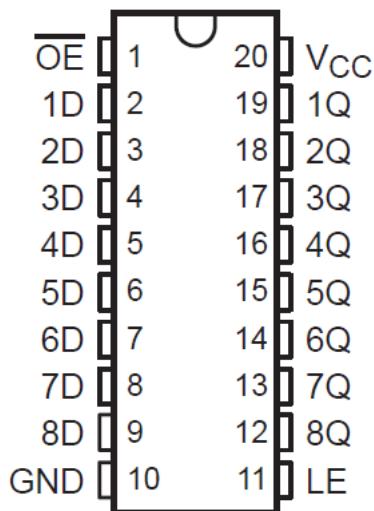
## 3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| <b>Changes from Revision D (January 2022) to Revision E (June 2022)</b>  | <b>Page</b> |
|--|-------------|
| • Junction-to-ambient thermal resistance values increased. DW was 58 is now 109.1, DB was 70 is now 122.7, N was 69 is now 84.6..... | <b>4</b>    |

| <b>Changes from Revision C (May 2004) to Revision D (January 2022)</b>   | <b>Page</b> |
|--|-------------|
| • Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards..... | <b>1</b>    |

## 4 Pin Configuration and Functions



**J, DB, N, or DW Package**  
**20-Pin CDIP, SSOP, PDIP, SOIC**  
**Top View**

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |   |  | MIN  | MAX | UNIT |
|------------------|---|--|------|-----|------|
| V <sub>CC</sub>  | Supply voltage range                                |  | -0.5 | 7   | V    |
| I <sub>IK</sub>  | Input clamp current <sup>(2)</sup>                  | V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub> |      | ±20 | mA   |
| I <sub>OK</sub>  | Output clamp current <sup>(2)</sup>                 | V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> |      | ±20 | mA   |
| I <sub>O</sub>   | Continuous output drain current per output          | V <sub>O</sub> = 0 to V <sub>CC</sub>                  |      | ±35 | mA   |
| I <sub>O</sub>   | Continuous output source or sink current per output | V <sub>O</sub> = 0 to V <sub>CC</sub>                  |      | ±25 | mA   |
|                  | Continuous current through V <sub>CC</sub> or GND   |  |      | ±50 | mA   |
| T <sub>J</sub>   | Junction temperature                                |  |      | 150 | °C   |
| T <sub>stg</sub> | Storage temperature range                           |  | -65  | 150 | °C   |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 Recommended Operating Conditions<sup>(1)</sup>

|                 |                                    | T <sub>A</sub> = 25°C |                 | T <sub>A</sub> = -55°C to 125°C |                 | T <sub>A</sub> = -40°C to 85°C |                 | UNIT |
|-----------------|------------------------------------|-----------------------|-----------------|---------------------------------|-----------------|--------------------------------|-----------------|------|
|                 |                                    | MIN                   | MAX             | MIN                             | MAX             | MIN                            | MAX             |      |
| V <sub>CC</sub> | Supply voltage                     | 4.5                   | 5.5             | 4.5                             | 5.5             | 4.5                            | 5.5             | V    |
| V <sub>IH</sub> | High-level input voltage           | 2                     |                 | 2                               |                 | 2                              |                 | V    |
| V <sub>IL</sub> | Low-level input voltage            |                       | 0.8             |                                 | 0.8             |                                | 0.8             | V    |
| V <sub>I</sub>  | Input voltage                      |                       | V <sub>CC</sub> |                                 | V <sub>CC</sub> |                                | V <sub>CC</sub> | V    |
| V <sub>O</sub>  | Output voltage                     |                       | V <sub>CC</sub> |                                 | V <sub>CC</sub> |                                | V <sub>CC</sub> | V    |
| Δt/Δv           | Input transition rise or fall rate |                       | 500             |                                 | 500             |                                | 500             | ns   |

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

### 5.3 Thermal Information

| THERMAL METRIC        |   | DW (SOIC) | DB (SSOP) | N (PDIP) | UNIT |
|-----------------------|---|-----------|-----------|----------|------|
|                       |   | 20 PINS   | 20 PINS   | 20 PINS  |      |
| R <sub>θJA</sub>      | Junction-to-ambient thermal resistance <sup>(1)</sup> | 109.1     | 122.7     | 84.6     | °C/W |
| R <sub>θJC(top)</sub> | Junction-to-case (top) thermal resistance             | 76        | 81.6      | 72.5     | °C/W |
| R <sub>θJB</sub>      | Junction-to-board thermal resistance                  | 77.6      | 77.5      | 65.3     | °C/W |
| Ψ <sub>JT</sub>       | Junction-to-top characterization parameter            | 51.5      | 46.1      | 55.3     | °C/W |
| Ψ <sub>JB</sub>       | Junction-to-board characterization parameter          | 77.1      | 77.1      | 65.2     | °C/W |
| R <sub>θJC(bot)</sub> | Junction-to-case (bottom) thermal resistance          | N/A       | N/A       | N/A      | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

## 5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                       | TEST CONDITIONS   |                          | V <sub>CC</sub> | T <sub>A</sub> = 25°C |     | T <sub>A</sub> = -55°C to 125°C |     | T <sub>A</sub> = -40°C to 85°C |     | UNIT |
|---------------------------------|---|--------------------------|-----------------|-----------------------|-----|---------------------------------|-----|--------------------------------|-----|------|
|                                 |   |                          |                 | MIN                   | MAX | MIN                             | MAX | MIN                            | MAX |      |
| V <sub>OH</sub>                 | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>       | I <sub>OH</sub> = -20 µA | 4.5 V           | 4.4                   |     | 4.4                             |     | 4.4                            |     | V    |
|                                 |   | I <sub>OH</sub> = -6 mA  |                 | 3.98                  |     | 3.7                             |     | 3.84                           |     |      |
| V <sub>OL</sub>                 | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>       | I <sub>OL</sub> = 20 µA  | 4.5 V           | 0.1                   |     | 0.1                             |     | 0.1                            |     | V    |
|                                 |   | I <sub>OL</sub> = 6 mA   |                 | 0.26                  |     | 0.4                             |     | 0.33                           |     |      |
| I <sub>I</sub>                  | V <sub>I</sub> = V <sub>CC</sub> or 0                     |                          | 5.5 V           | ±0.1                  |     | ±1                              |     | ±1                             |     | µA   |
| I <sub>oz</sub>                 | V <sub>O</sub> = V <sub>CC</sub> or 0                     |                          | 5.5 V           | ±0.5                  |     | ±10                             |     | ±5                             |     | µA   |
| I <sub>cc</sub>                 | V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0 |                          | 5.5 V           | 8                     |     | 160                             |     | 80                             |     | µA   |
| ΔI <sub>CC</sub> <sup>(1)</sup> | OE input held at V <sub>CC</sub> - 2.1 V                  |                          | 4.5 V to 5.5 V  | 450                   |     | 612.5                           |     | 562.5                          |     | µA   |
|                                 | Any D input held at V <sub>CC</sub> - 2.1 V               |                          | 4.5 V to 5.5 V  | 108                   |     | 147                             |     | 135                            |     | µA   |
|                                 | LE input held at V <sub>CC</sub> - 2.1 V                  |                          | 4.5 V to 5.5 V  | 234                   |     | 318.5                           |     | 292.5                          |     | µA   |
| C <sub>i</sub>                  |   |                          |                 | 10                    |     | 10                              |     | 10                             |     | pF   |
| C <sub>o</sub>                  |   |                          |                 | 20                    |     | 20                              |     | 20                             |     | pF   |

(1) Additional quiescent supply current per input pin, TTL inputs high, 1 unit load. For dual-supply systems, theoretical worst-case (V<sub>I</sub> = 2.4 V, V<sub>CC</sub> = 5.5 V) specification is 1.8 mA.

## 5.5 Timing Requirements

over recommended operating free-air temperature range, V<sub>CC</sub> = 4.5 V (unless otherwise noted) (see [Figure 6-1](#))

|                 |                              | T <sub>A</sub> = 25°C | T <sub>A</sub> = -55°C to 125°C |     | T <sub>A</sub> = -40°C to 85°C |     | UNIT |
|-----------------|------------------------------|-----------------------|---------------------------------|-----|--------------------------------|-----|------|
|                 |                              |                       | MIN                             | MAX | MIN                            | MAX |      |
| t <sub>w</sub>  | Pulse duration, LE high      | 16                    |                                 | 24  |                                | 20  | ns   |
| t <sub>su</sub> | Setup time, data before LE ↓ | 13                    |                                 | 20  |                                | 16  | ns   |
| t <sub>h</sub>  | Hold time, data after LE ↓   | 10                    |                                 | 15  |                                | 13  | ns   |

## 5.6 Switching Characteristics

over recommended operating free-air temperature range, V<sub>CC</sub> = 4.5 V (unless otherwise noted) (see [Figure 6-1](#))

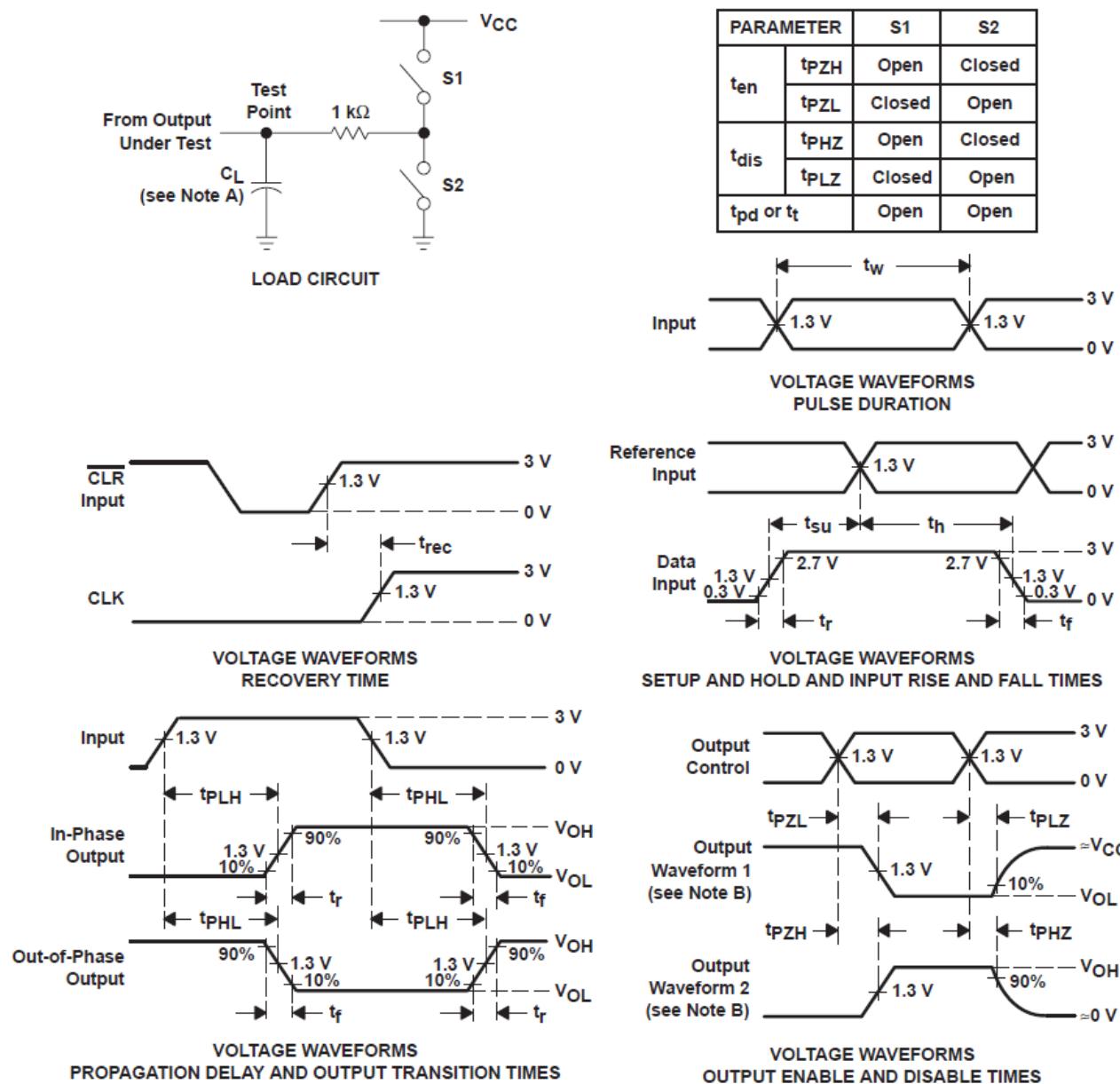
| PARAMETER        | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE       | T <sub>A</sub> = 25°C |     | T <sub>A</sub> = -55°C to 125°C |     | T <sub>A</sub> = -40°C to 85°C |     | UNIT |
|------------------|--------------|-------------|------------------------|-----------------------|-----|---------------------------------|-----|--------------------------------|-----|------|
|                  |              |             |                        | MIN                   | MAX | MIN                             | MAX | MIN                            | MAX |      |
| t <sub>pd</sub>  | D            | Q           | C <sub>L</sub> = 50 pF | 35                    |     | 53                              |     | 44                             |     | ns   |
|                  | LE           |             |                        | 35                    |     | 53                              |     | 44                             |     |      |
| t <sub>en</sub>  | OE           | Q           | C <sub>L</sub> = 50 pF | 35                    |     | 53                              |     | 44                             |     | ns   |
| t <sub>dis</sub> | OE           | Q           | C <sub>L</sub> = 50 pF | 35                    |     | 53                              |     | 44                             |     | ns   |
| t <sub>t</sub>   |              | Q           | C <sub>L</sub> = 50 pF | 12                    |     | 18                              |     | 15                             |     | ns   |

## 5.7 Operating Characteristics

V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

| PARAMETER       |                               | TYP | UNIT |
|-----------------|-------------------------------|-----|------|
| C <sub>pd</sub> | Power dissipation capacitance | 53  | pF   |

## 6 Parameter Measurement Information



- C<sub>L</sub> includes probe and test-fixture capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> = 6 ns, t<sub>f</sub> = 6 ns.
- For clock inputs, f<sub>msx</sub> is measured with the input duty cycle at 50%.
- The outputs are measured one at a time, with one input transition per measurement.
- t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
- t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
- t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>.

Figure 6-1. Load Circuit and Voltage Waveforms

## 7 Detailed Description

### 7.1 Overview

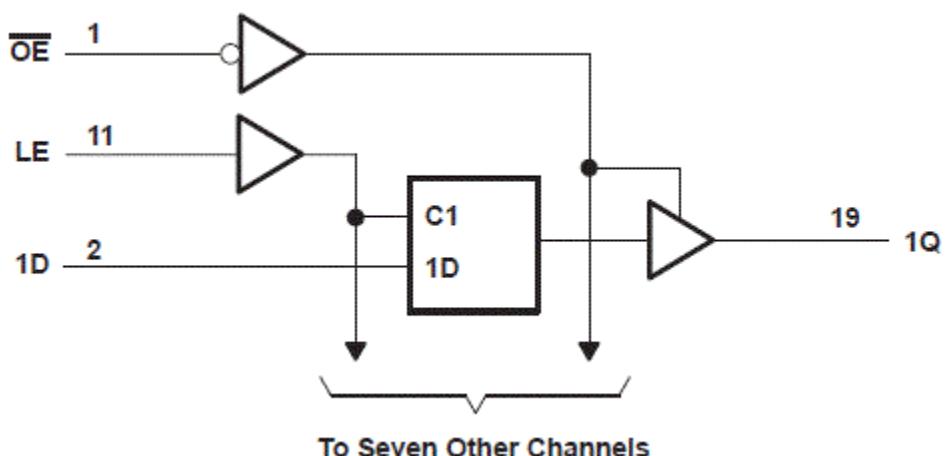
The 'HCT573 devices are octal transparent D-type latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to VCC through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### 7.2 Functional Block Diagram



### 7.3 Device Functional Modes

**Table 7-1. Function Table  
(each latch)**

| INPUTS          |    |   | OUTPUT Q |
|-----------------|----|---|----------|
| $\overline{OE}$ | LE | D |          |
| L               | H  | H | H        |
| L               | H  | L | L        |
| L               | L  | X | $Q_0$    |
| H               | X  | X | Z        |

## 8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 9 Layout

### 9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable part number | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)             |
|-----------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------------------|
| 5962-8685601RA        | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8685601RA<br>CD54HCT573F3A |
| CD54HCT573F           | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD54HCT573F                     |
| CD54HCT573F.A         | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD54HCT573F                     |
| CD54HCT573F3A         | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8685601RA<br>CD54HCT573F3A |
| CD54HCT573F3A.A       | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8685601RA<br>CD54HCT573F3A |
| CD74HCT573DBR         | Active        | Production           | SSOP (DB)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HK573                           |
| CD74HCT573DBR.A       | Active        | Production           | SSOP (DB)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HK573                           |
| CD74HCT573E           | Active        | Production           | PDIP (N)   20  | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HCT573E                     |
| CD74HCT573E.A         | Active        | Production           | PDIP (N)   20  | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HCT573E                     |
| CD74HCT573M           | Obsolete      | Production           | SOIC (DW)   20 | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | HCT573M                         |
| CD74HCT573M96         | Active        | Production           | SOIC (DW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HCT573M                         |
| CD74HCT573M96.A       | Active        | Production           | SOIC (DW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HCT573M                         |
| CD74HCT573M96G4       | Active        | Production           | SOIC (DW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HCT573M                         |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

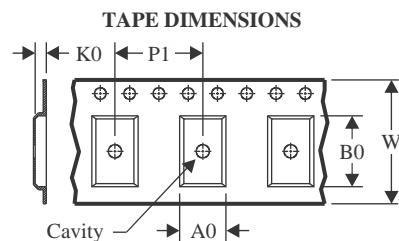
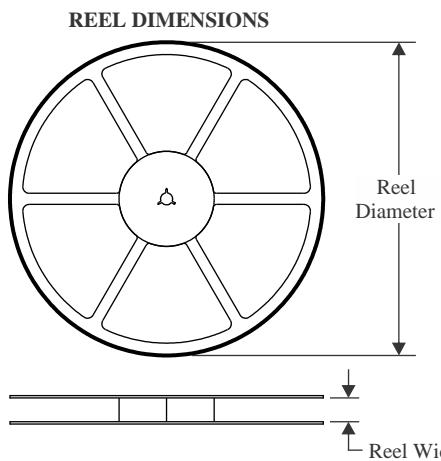
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD54HCT573, CD74HCT573 :**

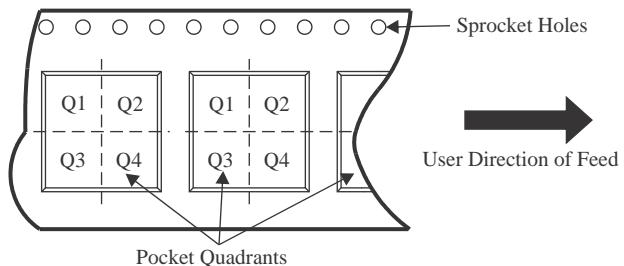
- Catalog : [CD74HCT573](#)
- Military : [CD54HCT573](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

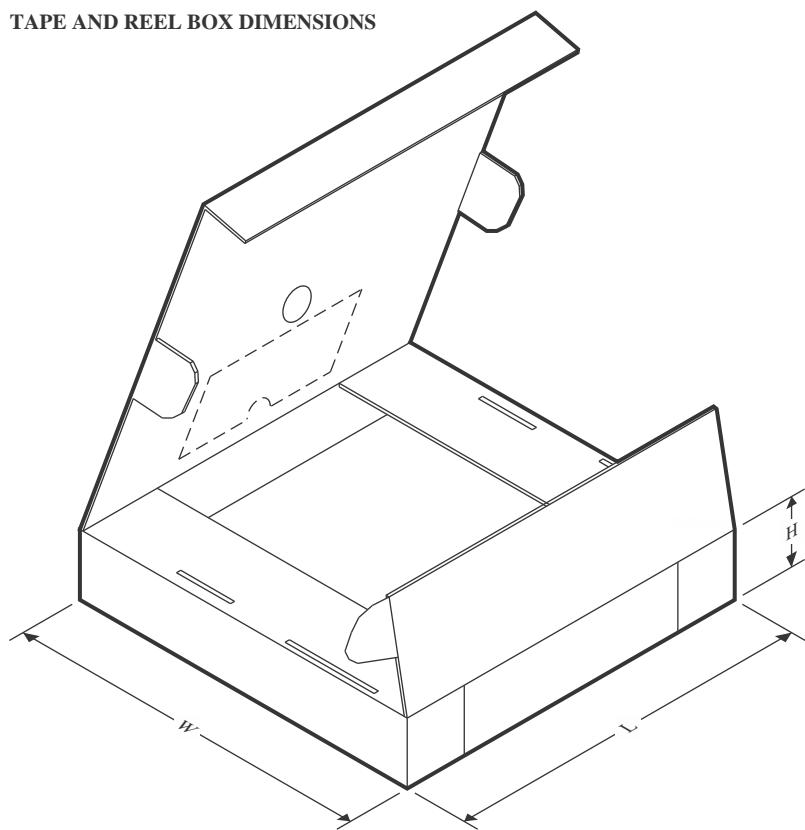
**TAPE AND REEL INFORMATION**


|    |   |
|----|---|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


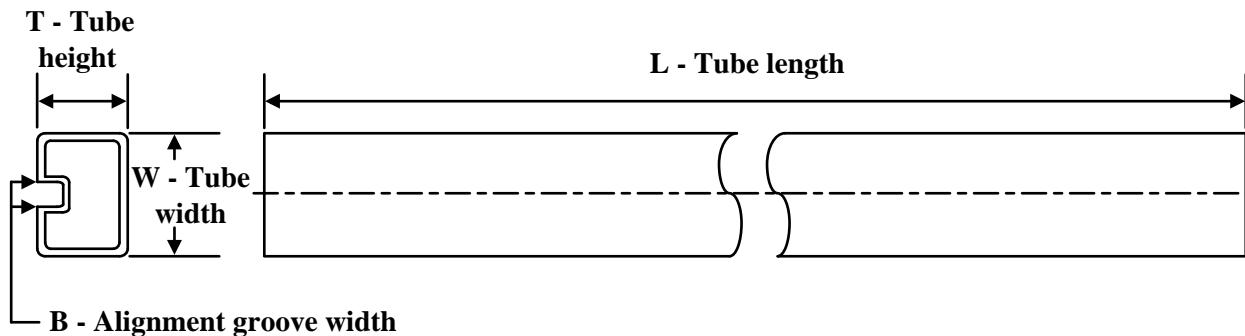
\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74HCT573DBR | SSOP         | DB              | 20   | 2000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |
| CD74HCT573M96 | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| CD74HCT573M96 | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.9    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74HCT573DBR | SSOP         | DB              | 20   | 2000 | 353.0       | 353.0      | 32.0        |
| CD74HCT573M96 | SOIC         | DW              | 20   | 2000 | 356.0       | 356.0      | 45.0        |
| CD74HCT573M96 | SOIC         | DW              | 20   | 2000 | 356.0       | 356.0      | 45.0        |

**TUBE**


\*All dimensions are nominal

| Device        | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T ( $\mu$ m) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------------|--------|
| CD74HCT573E   | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230        | 4.32   |
| CD74HCT573E.A | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230        | 4.32   |

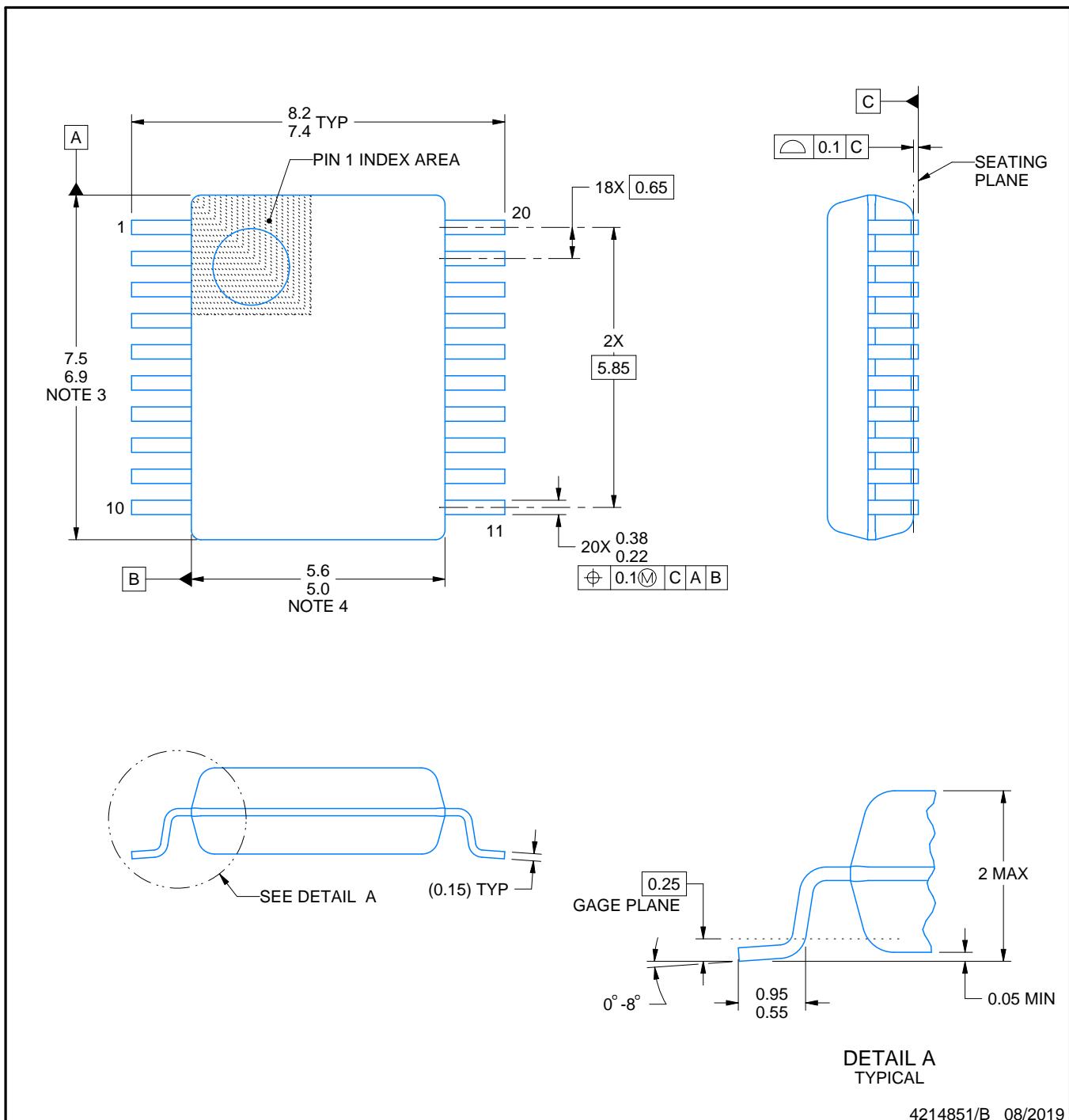
# PACKAGE OUTLINE

DB0020A



SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



## NOTES:

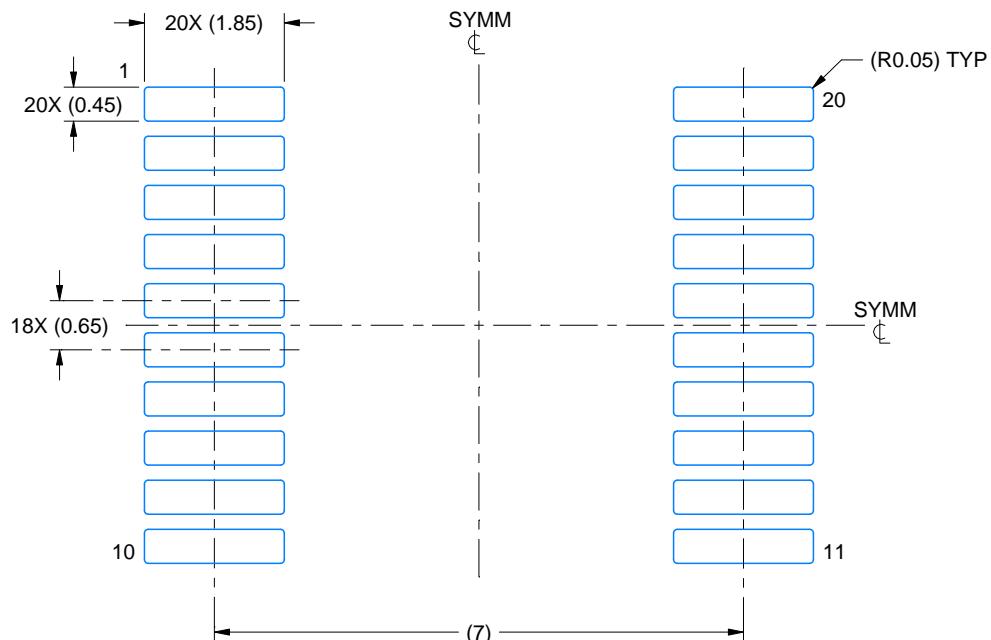
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

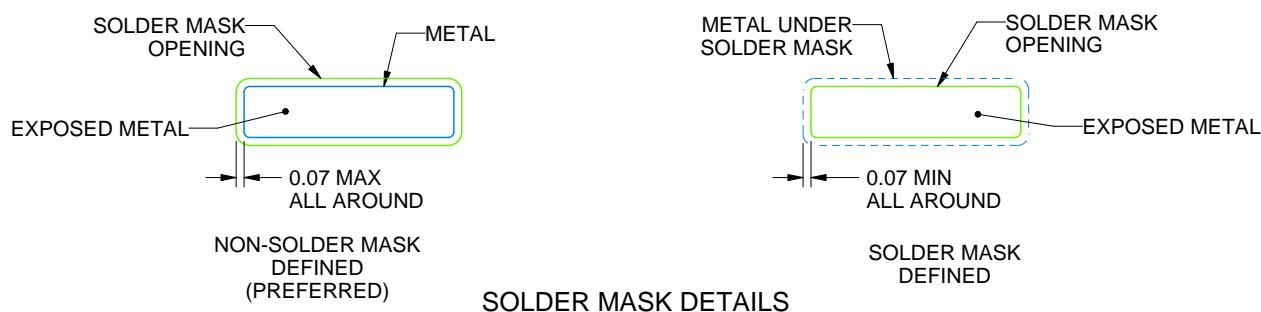
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

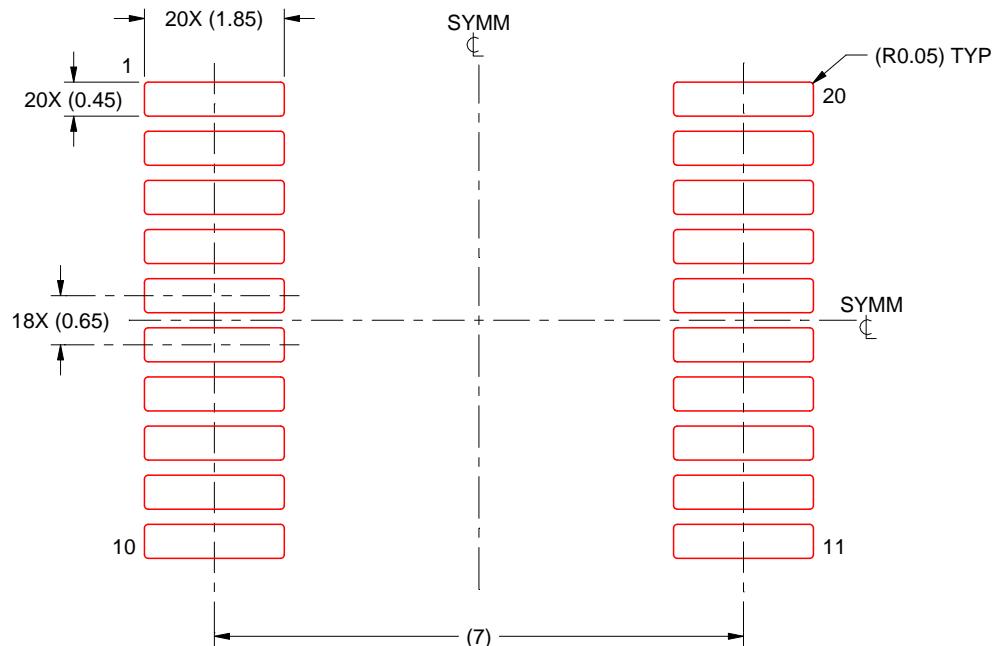
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

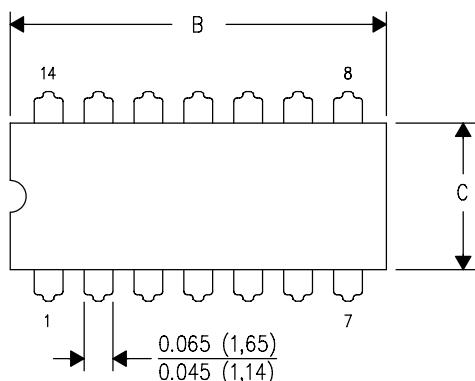
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

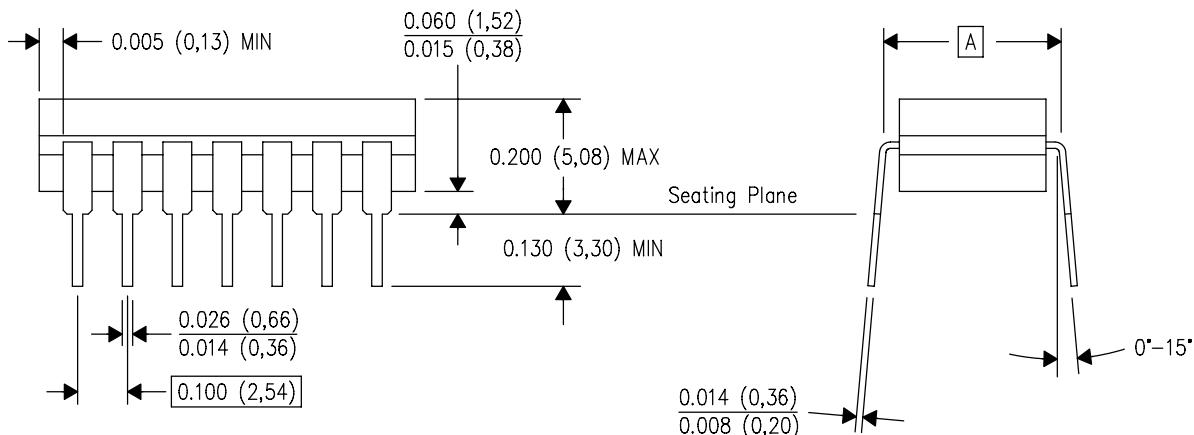
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



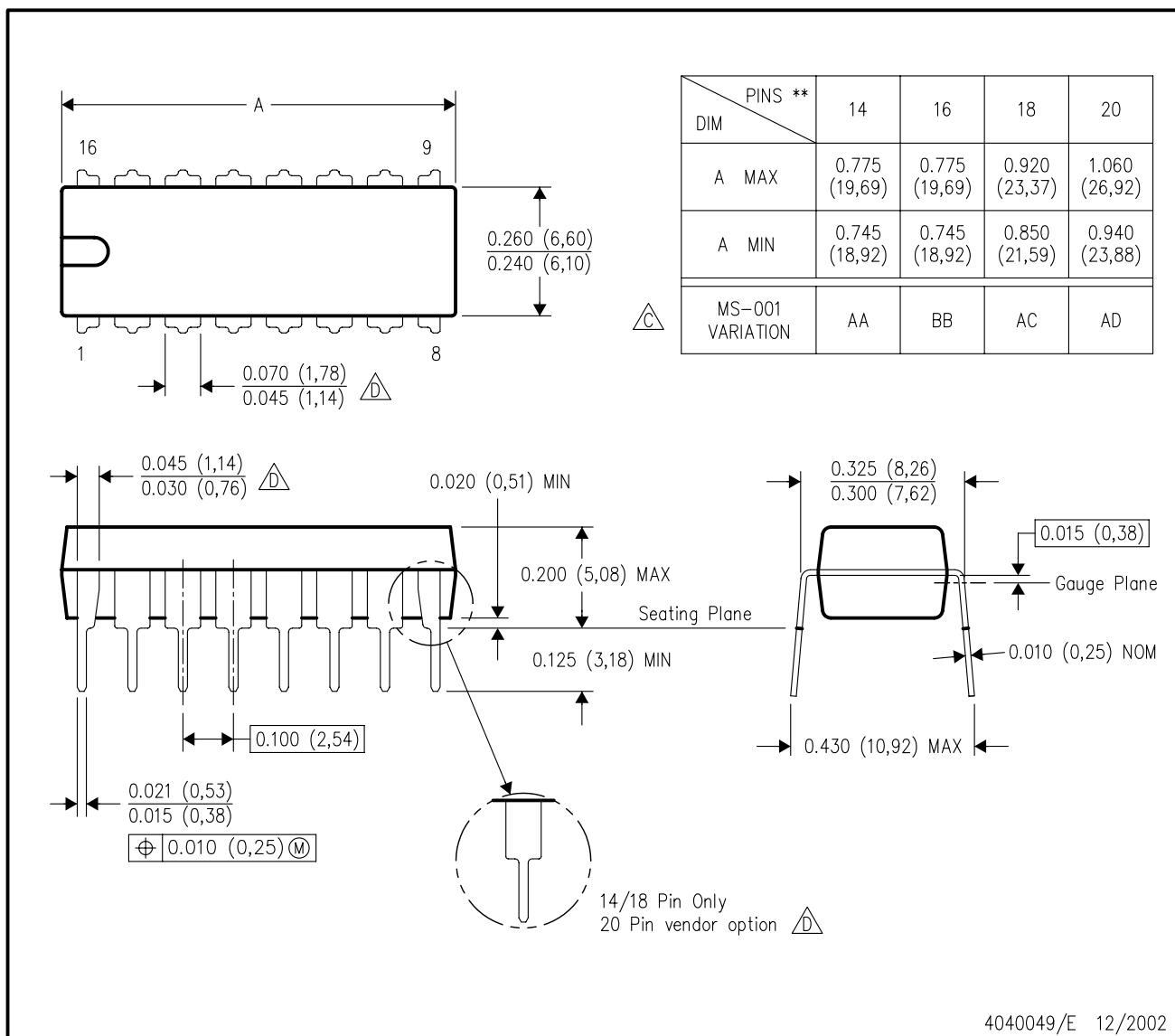
4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

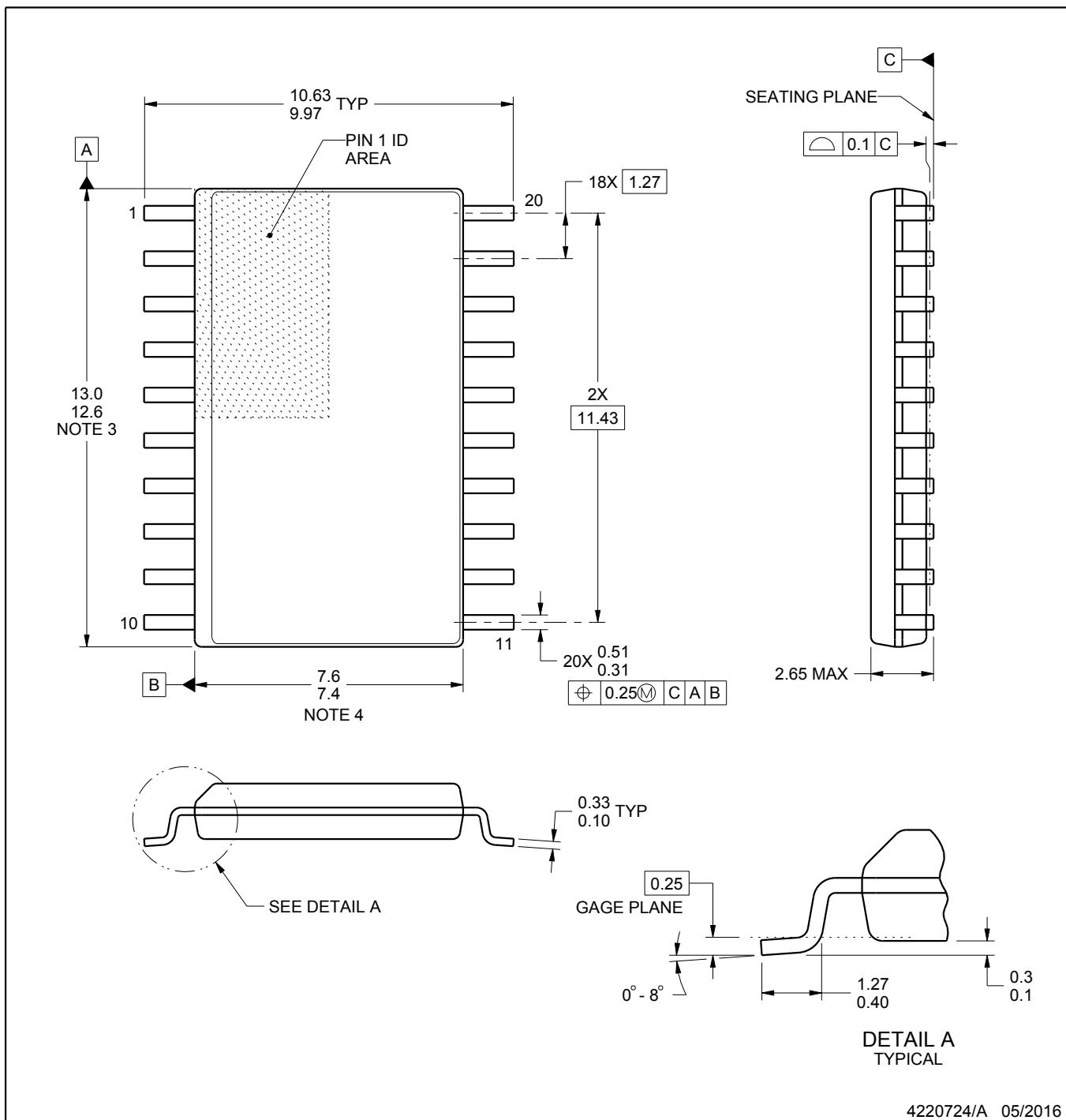
# PACKAGE OUTLINE

DW0020A



SOIC - 2.65 mm max height

SOIC



NOTES:

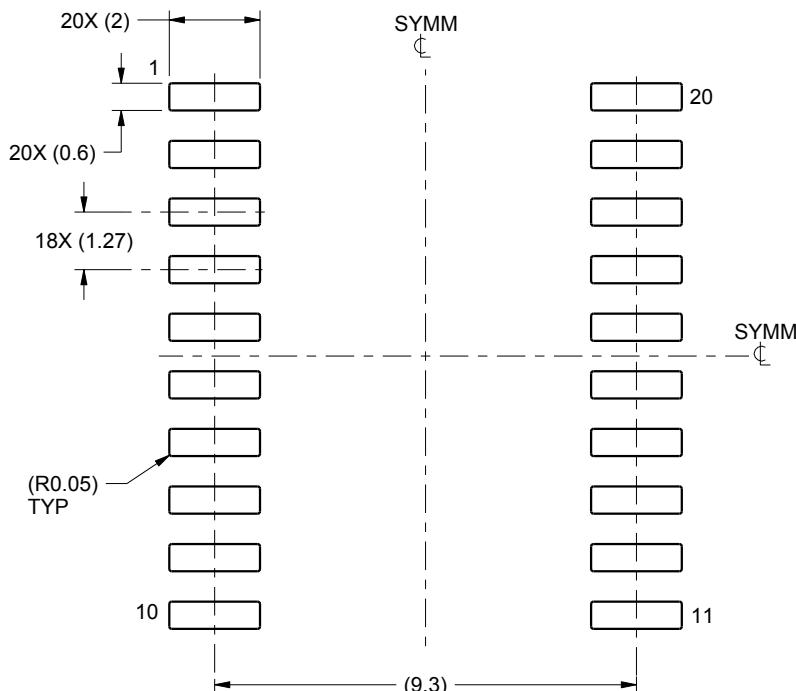
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

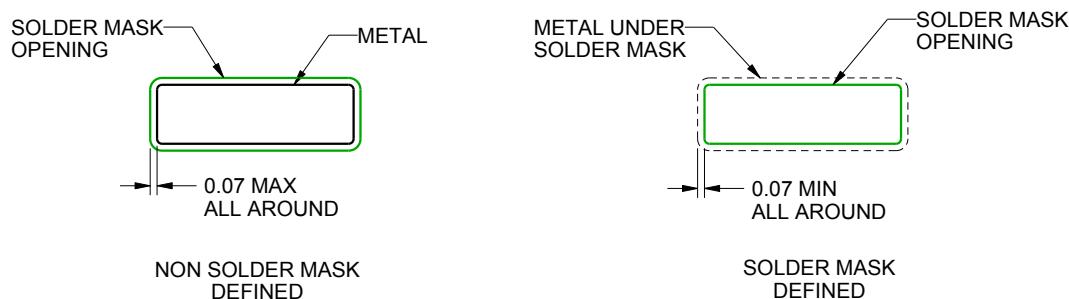
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

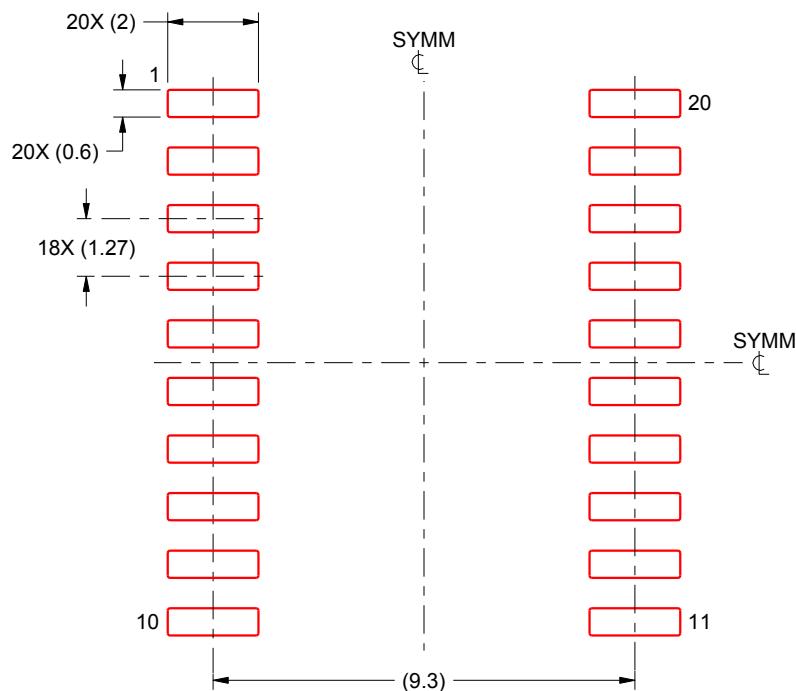
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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