FAIRCHILD SEMICONDUCTOR™

December 2000

QFET™

# FQD13N10L / FQU13N10L

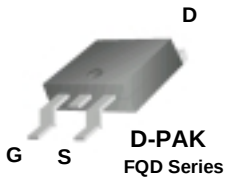
## 100V LOGIC N-Channel MOSFET

### General Description

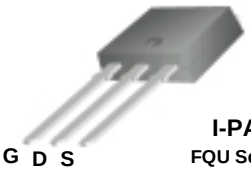
These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.
This advanced technology is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation modes. These devices are well suited for low voltage applications such as high efficiency switching DC/DC converters, and DC motor control.

### Features

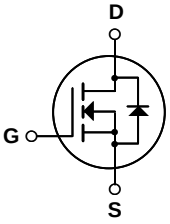
- 10A, 100V, $R_{DS(on)}$ = 0.18Ω @$V_{GS}$ = 10 V
- Low gate charge ( typical 8.7 nC)
- Low Crss ( typical 20 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability




D-PAK
FQD Series




I-PAK
FQU Series




## Absolute Maximum Ratings

$T_C$ = 25°C unless otherwise noted

| Symbol | Parameter | | FQD13N10L / FQU13N10L | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 100 | V |
| $I_D$ | Drain Current - Continuous ($T_C$ = 25°C) | | 10 | A |
| | - Continuous ($T_C$ = 100°C) | | 6.3 | A |
| $I_{DM}$ | Drain Current - Pulsed | (Note 1) | 40 | A |
| $V_{GSS}$ | Gate-Source Voltage | | ± 20 | V |
| $E_{AS}$ | Single Pulsed Avalanche Energy | (Note 2) | 95 | mJ |
| $I_{AR}$ | Avalanche Current | (Note 1) | 10 | A |
| $E_{AR}$ | Repetitive Avalanche Energy | (Note 1) | 4.0 | mJ |
| dv/dt | Peak Diode Recovery dv/dt | (Note 3) | 6.0 | V/ns |
| $P_D$ | Power Dissipation ($T_A$ = 25°C) * | | 2.5 | W |
| | Power Dissipation ($T_C$ = 25°C) | | 40 | W |
| | - Derate above 25°C | | 0.32 | W/°C |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature Range | | -55 to +150 | °C |
| $T_L$ | Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds | | 300 | °C |

## Thermal Characteristics

| Symbol | Parameter | Typ | Max | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | -- | 3.13 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient * | -- | 50 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | -- | 110 | °C/W |

* When mounted on the minimum pad size recommended (PCB Mount)

## Electrical Characteristics

$T_C$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 μA | 100 | -- | -- | V |
| $\Delta BV_{DSS}$ / $\Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, Referenced to 25°C | -- | 0.09 | -- | V/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 100 V, $V_{GS}$ = 0 V | -- | -- | 1 | μA |
| | | $V_{DS}$ = 80 V, $T_C$ = 125°C | -- | -- | 10 | μA |
| $I_{GSSF}$ | Gate-Body Leakage Current, Forward | $V_{GS}$ = 20 V, $V_{DS}$ = 0 V | -- | -- | 100 | nA |
| $I_{GSSR}$ | Gate-Body Leakage Current, Reverse | $V_{GS}$ = -20 V, $V_{DS}$ = 0 V | -- | -- | -100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | 1.0 | -- | 2.0 | V |
| $R_{DS(on)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = 10 V, $I_D$ = 5.0 A<br>$V_{GS}$ = 5 V, $I_D$ = 5.0 A | -- | 0.142<br>0.158 | 0.18<br>0.2 | Ω |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 30 V, $I_D$ = 5.0 A (Note 4) | -- | 8.7 | -- | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 25 V, $V_{GS}$ = 0 V, f = 1.0 MHz | -- | 400 | 520 | pF |
| $C_{oss}$ | Output Capacitance | | -- | 95 | 125 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | -- | 20 | 25 | pF |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 50 V, $I_D$ = 12.8 A, $R_G$ = 25 Ω (Note 4, 5) | -- | 7.5 | 25 | ns |
| $t_r$ | Turn-On Rise Time | | -- | 220 | 450 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | -- | 22 | 55 | ns |
| $t_f$ | Turn-Off Fall Time | | -- | 72 | 150 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 80 V, $I_D$ = 12.8 A, $V_{GS}$ = 5 V (Note 4, 5) | -- | 8.7 | 12 | nC |
| $Q_{gs}$ | Gate-Source Charge | | -- | 2.0 | -- | nC |
| $Q_{gd}$ | Gate-Drain Charge | | -- | 5.3 | -- | nC |
| **Drain-Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $I_S$ | Maximum Continuous Drain-Source Diode Forward Current | | -- | -- | 10 | A |
| $I_{SM}$ | Maximum Pulsed Drain-Source Diode Forward Current | | -- | -- | 40 | A |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 10 A | -- | -- | 1.5 | V |
| $t_{rr}$ | Reverse Recovery Time | $V_{GS}$ = 0 V, $I_S$ = 12.8 A, $dI_F$ / dt = 100 A/μs (Note 4) | -- | 75 | -- | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | -- | 0.17 | -- | μC |

**Notes:**
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 1.43mH, $I_{AS}$ = 10A, $V_{DD}$ = 25V, $R_G$ = 25 Ω, Starting $T_J$ = 25°C
3. $I_{SD}$ ≤ 12.8A, di/dt ≤ 300A/μs, $V_{DD}$ ≤ $BV_{DSS}$, Starting $T_J$ = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

## Typical Characteristics

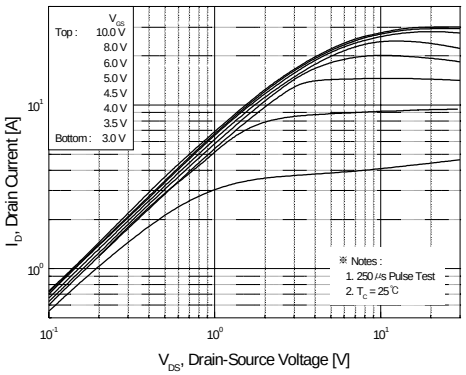



**Figure 1. On-Region Characteristics**

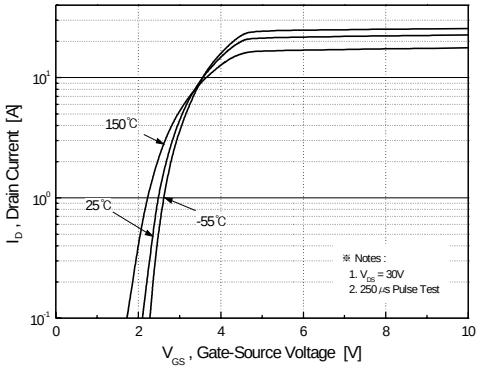



**Figure 2. Transfer Characteristics**

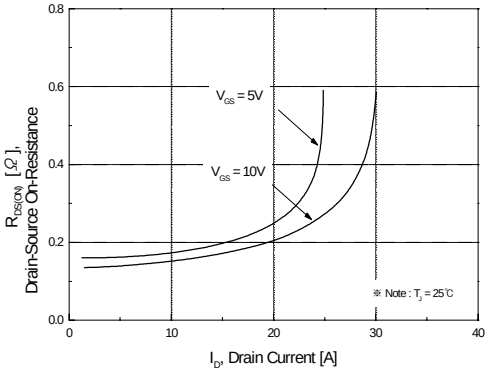



**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**

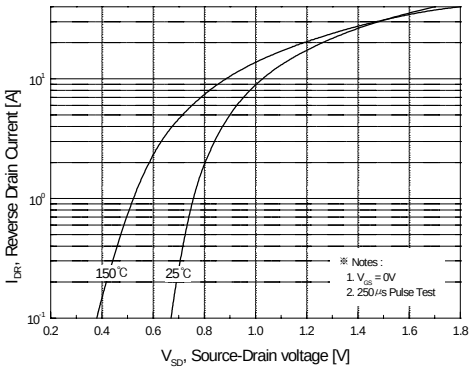



**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**

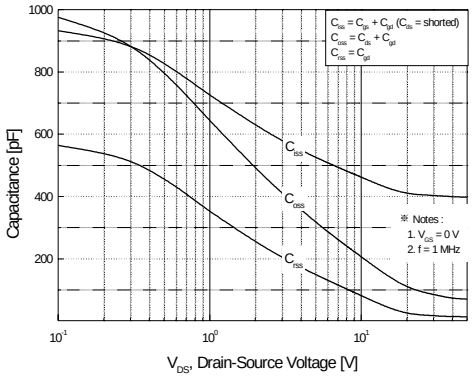



**Figure 5. Capacitance Characteristics**

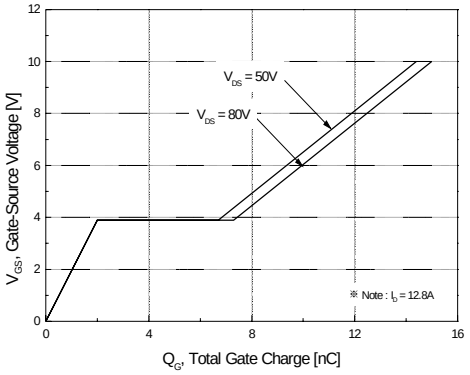



**Figure 6. Gate Charge Characteristics**

## Typical Characteristics (Continued)

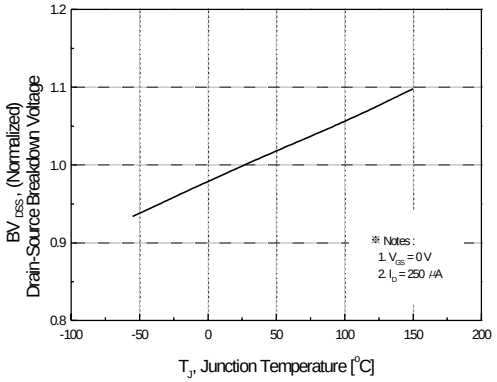



**Figure 7. Breakdown Voltage Variation vs. Temperature**

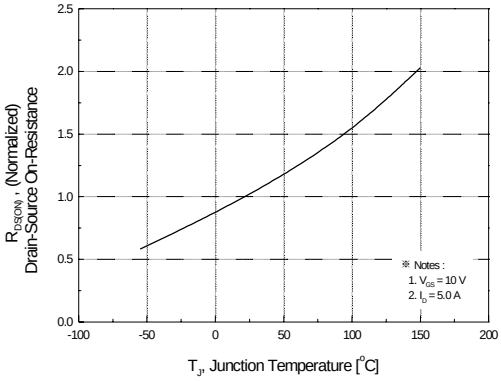



**Figure 8. On-Resistance Variation vs. Temperature**

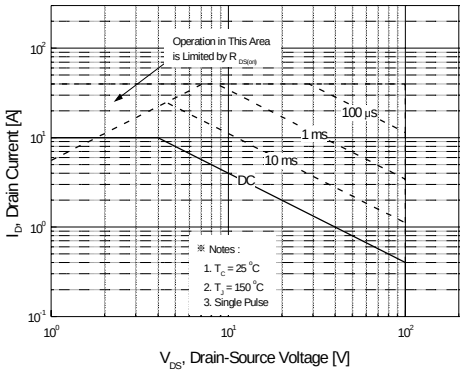



**Figure 9. Maximum Safe Operating Area**

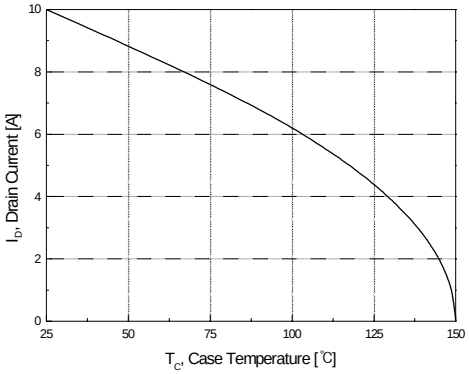



**Figure 10. Maximum Drain Current vs. Case Temperature**

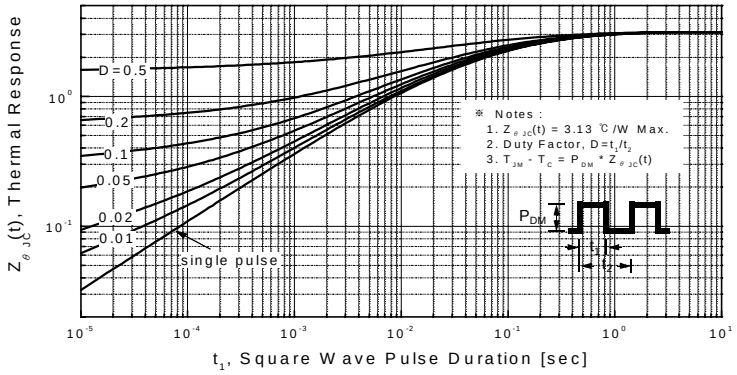
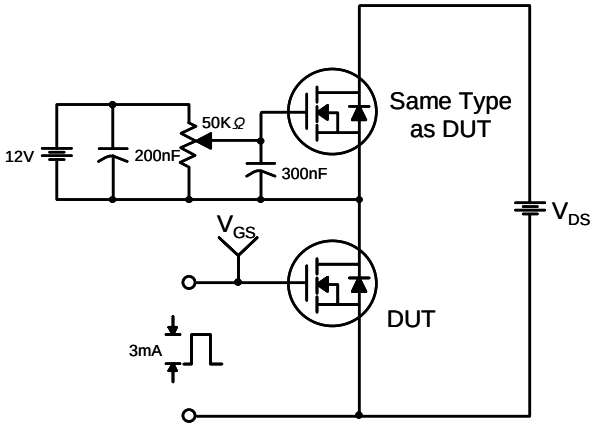
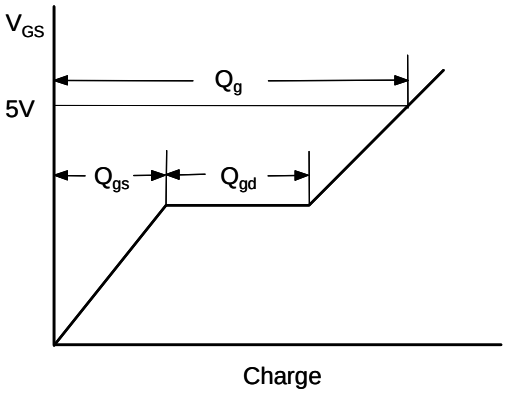


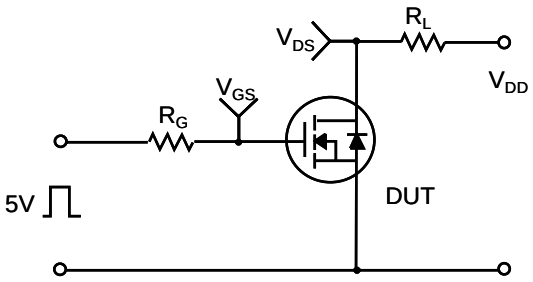

**Figure 11. Transient Thermal Response Curve**

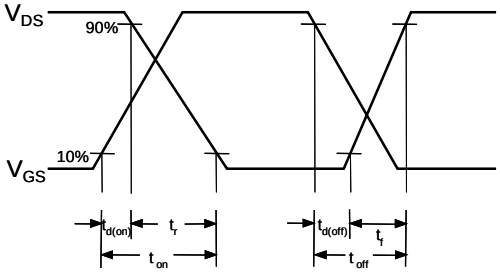
### Gate Charge Test Circuit & Waveform



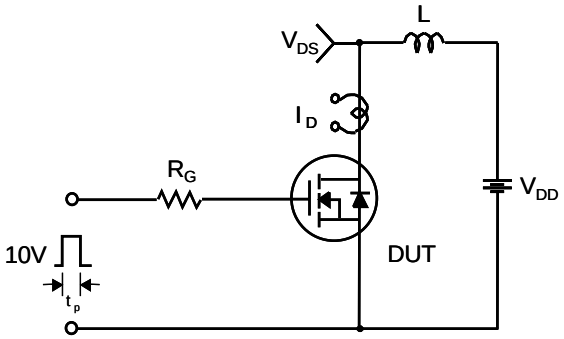




### Resistive Switching Test Circuit & Waveforms

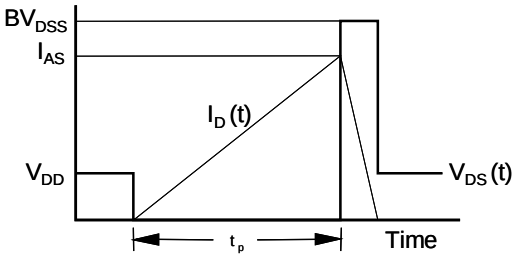


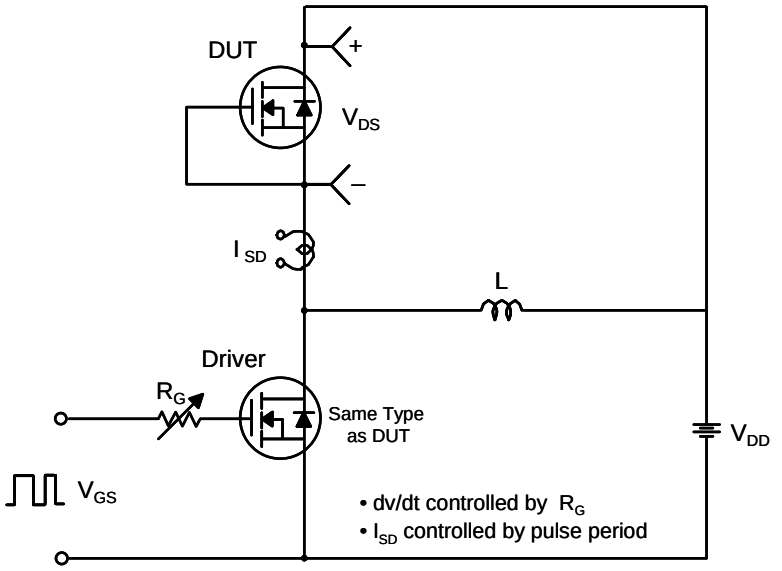

### Unclamped Inductive Switching Test Circuit & Waveforms

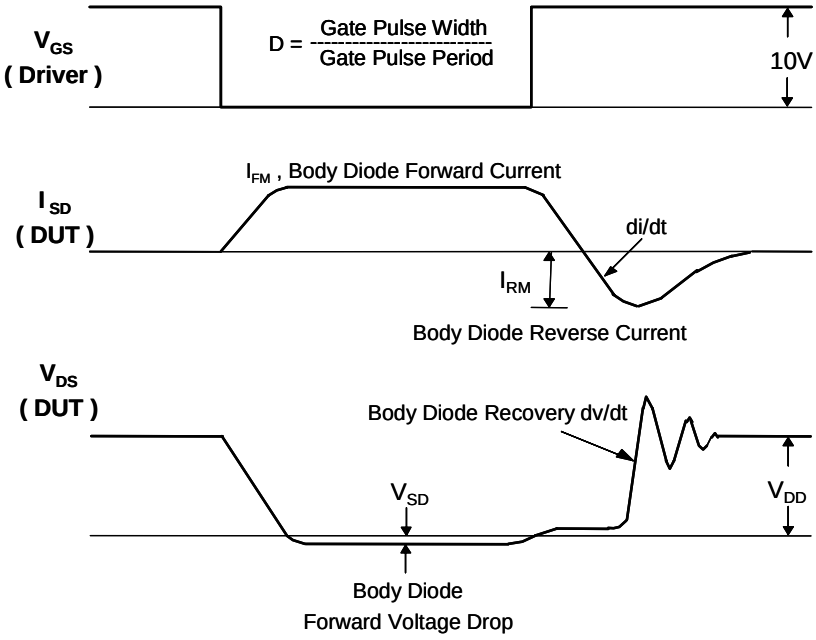



$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



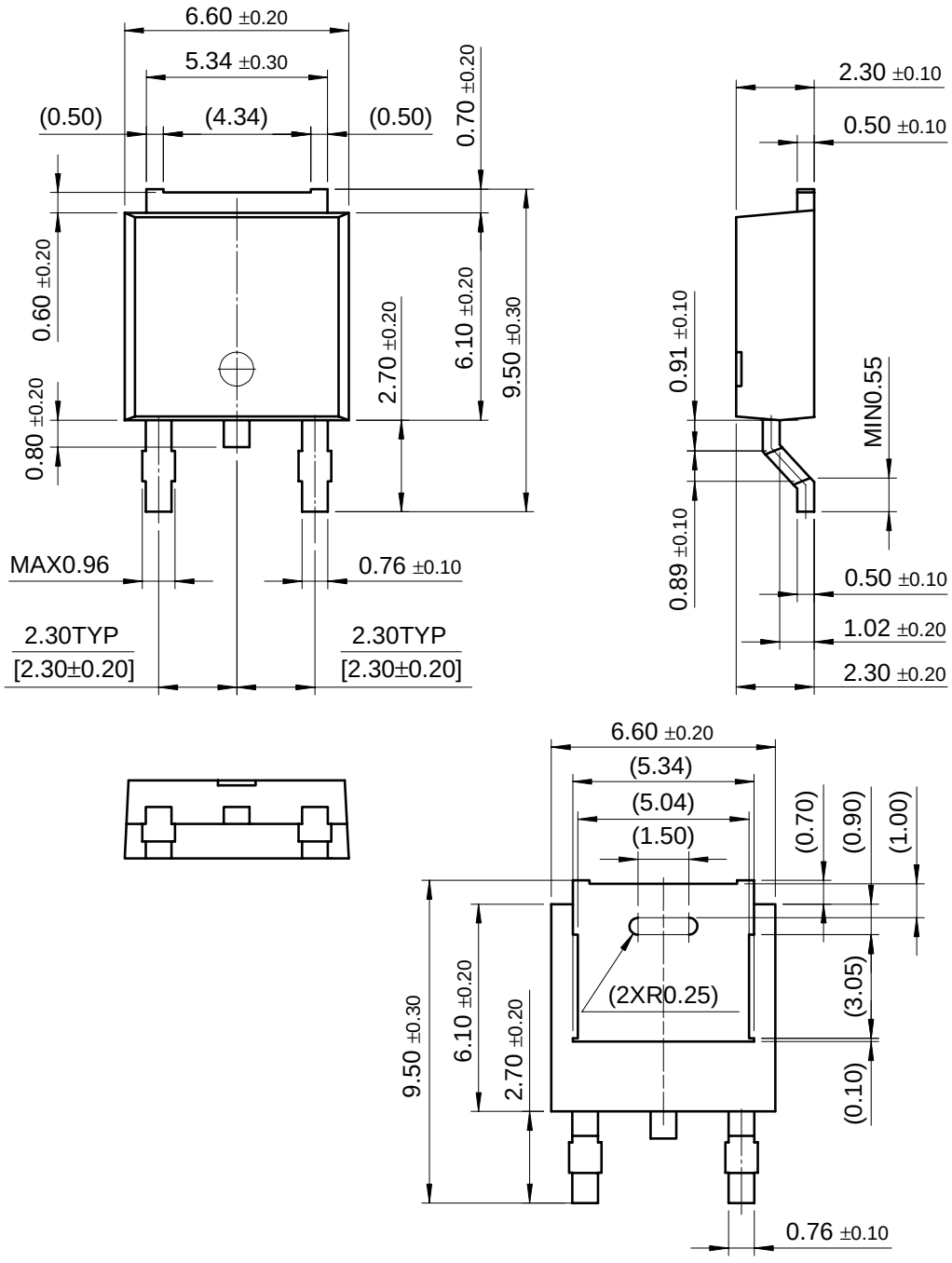
**Peak Diode Recovery dv/dt Test Circuit & Waveforms**



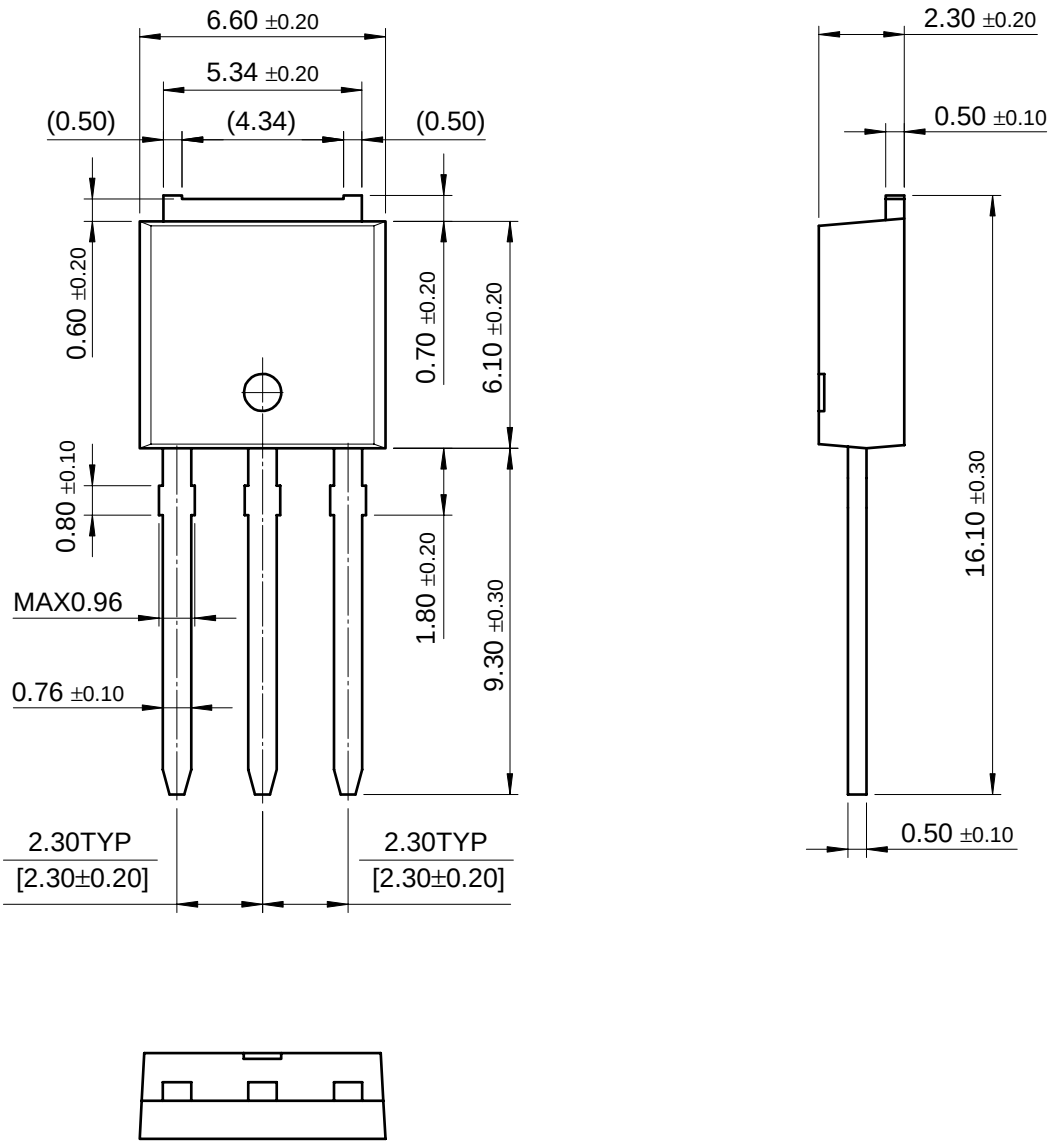
**Package Dimensions**

# DPAK



**Package Dimensions** (Continued)

# IPAK



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