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N04C1633E3BM(2)-MAS

32x4 Combination Memory Multi-Chip Package (MCP)

32Mb (2Mbx16) Boot Sector Flash Memory plus 4Mb (256Kbx16) Low Power SRAM

OVERVIEW & FEATURES

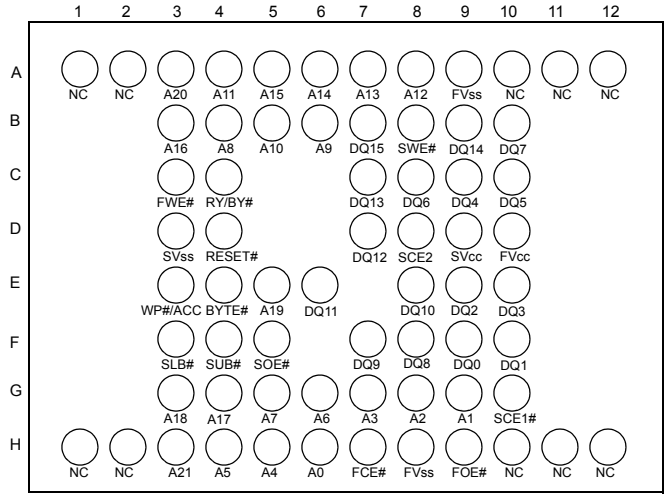
- **Single 3.0 to 3.6V Power Supply Operation**
- **Wide operating temperature range of 0°C to +70°C**

Flash Characteristics

- **Flexible Sector Architecture**
  - Eight 8-Kbyte sectors; sixty-three 64-Kbyte sectors
- **Sector Protection Features**
  - A hardware method of locking a sector to prevent any program or erase operations within that sector
  - Sectors can be locked in-system or via programming equipment
  - Temporary Sector Unprotect feature allows code changes in previously locked sectors
- **Unlock Bypass Program Command**
  - Reduces overall programming time when issuing multiple program command sequences
- **Secured Silicon Sector**
  - 128-word sector for permanent, secure identification through an 8-word random Electronic Serial Number
  - May be programmed and locked at the factory or by the customer
  - Accessible through a command sequence
- **Top or Bottom Boot Block Configurations Available**
- **Compatibility with JEDEC standards**
  - Pinout and software compatible with single-power supply Flash
  - Superior inadvertent write protection
- **Fast access times of 90ns**
- **Ultra Low Power Consumption (typical values at 5 MHz)**
  - 200 nA Automatic Sleep mode current
  - 200 nA standby mode current
  - 9 mA read current
  - 20 mA program/erase current
- **Cycling Endurance: 1,000,000 cycles per sector typical**
- **Data Retention: 20 years typical**
- **CFI (Common Flash Interface) Compliant**
  - Provides device-specific information to the system, allowing host software to easily reconfigure for different Flash devices
- **Erase Suspend/Erase Resume**
  - Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Data# Polling and Toggle Bits**
  - Provides a software method of detecting program or erase operation completion
  - Unlock Bypass Program Command
    Reduces overall programming time when issuing multiple program command sequences
- **Ready/Busy# Pin (RY/BY#)**
  - Provides a hardware method of detecting program or erase cycle completion
- **Hardware Reset Pin (RESET#)**
  - Hardware method to reset the device to reading array data
- **WP#/ACC input pin**
  - Write protect (WP#) function allows protection of two outermost boot sectors, regardless of sector protect status
  - Acceleration (ACC) function provides accelerated program times

SRAM Characteristics

- **Fast access times of 70ns**
- **256Kb x 16 bit architecture**
  - x8 operation via Byte Select control
- **Ultra Low Power Consumption (typical values at 5 MHz)**
  - 4 uA standby mode current
  - 8 mA read/write current



A21 position reserved for 64Mb flash density

General Description

The N04C1633E3B is a 32 Mbit, 3.3 Volt Flash memory combined with a 4Mb low power SRAM integrated into a single 66-ball multi-chip BGA package (MCP). Both standard (lead) and GREEN (lead-free) BGA packages are available.The Flash is organized as 2,097,152 words or 4,194,304 bytes. The word-wide data (x16) appears on DQ15–DQ0; the byte-wide (x8) data appears on DQ7–DQ0. The SRAM is organized as 1,048,576 words (DQ15–DQ0) and Byte Selects (SUB# and SLB#) can be used to operate in a byte mode. The Flash device is designed to be programmed in-system with the standard system 3.3 volt V_{CC} supply and can also be programmed in standard EPROM programmers.

The Flash device offers access times of 90ns and the SRAM offers access times of 70ns allowing high speed microprocessors to operate without wait states. To eliminate bus contention both devices have separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

The MCP requires only **3.3 volt power supplies** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations of the Flash.

The **Secured Silicon Sector** is an extra sector capable of being permanently locked by customers. The **Secured Silicon Indicator Bit** (DQ7) is permanently set to a 1 if the part is **factory locked**, and set to a 0 if customer lockable. **Note that the 32Mb Flash has a Secured Silicon Sector size of 128 words (256 bytes)**.

The Flash device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The **Unlock Bypass** mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend/Erase Resume** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

The Flash and SRAM devices offer two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both these modes.

The details of the Flash device built in this MCP are included in sections 8 through 13 with the AC/DC characteristics for both Flash and SRAM devices included in sections 14-20 of this datasheet.

The Flash technology used combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

1. Key Parameters

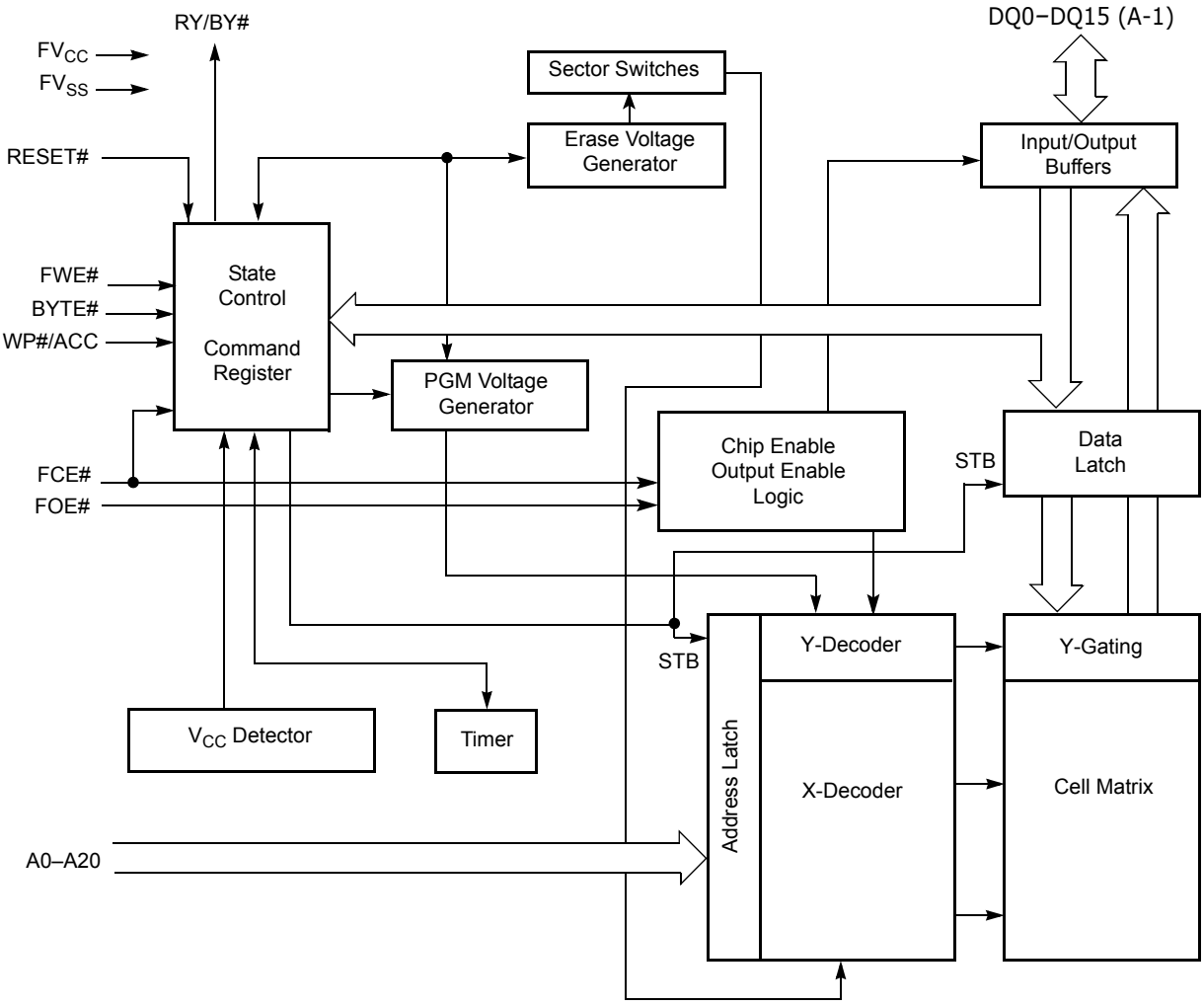
Performance	Voltage Range: V_{CC} = 3.0–3.6 V	Flash	SRAM
Max access time, ns (t_{ACC})		90	70
Max CE# access time, ns (t_{CE})		90	70
Max OE# access time, ns (t_{OE})		35	30

Note
See Flash AC Characteristics and SRAM AC Characteristics on for full specifications.

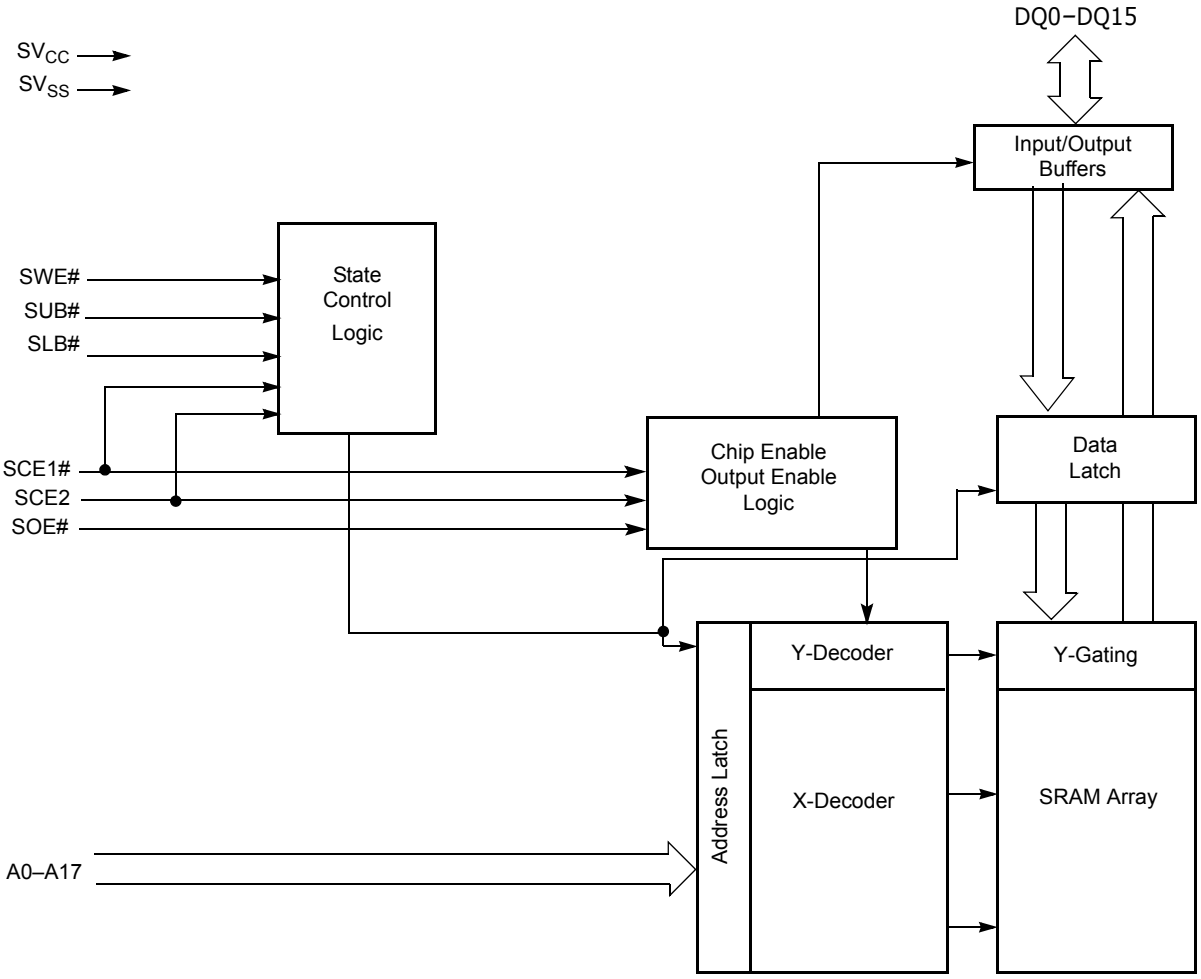
1.1 Ordering Part Number Information

AMI Part Number	Boot Sector	Package
N04C1633E3BM-MAS	Bottom	Standard BGA
N04C1633E3BM2-MAS	Bottom	Green BGA

2. Flash Block Diagram



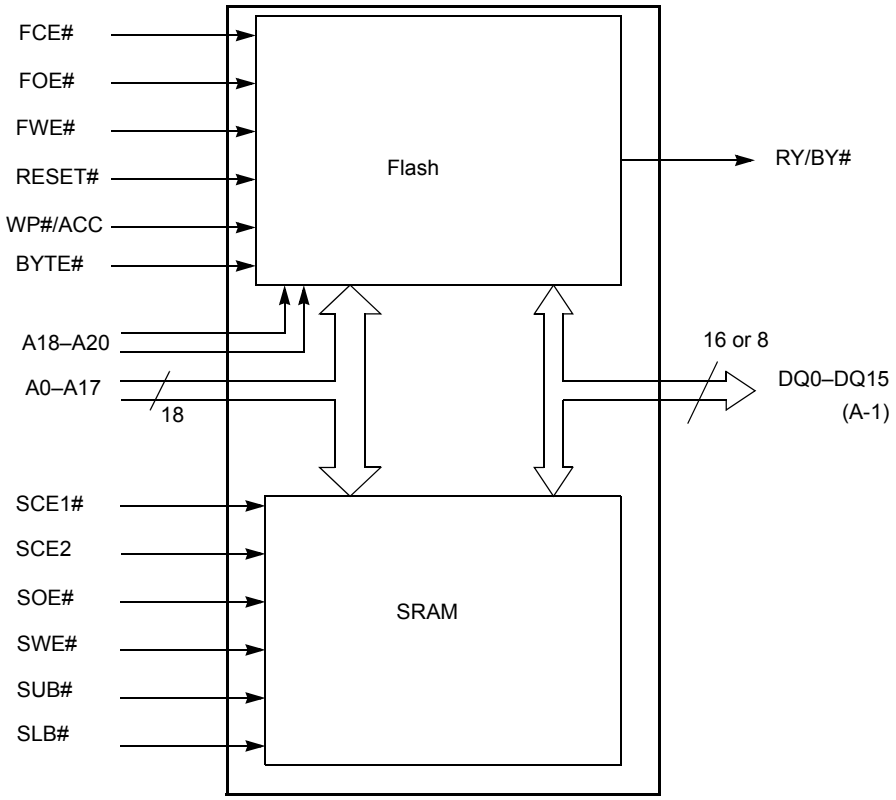
3. SRAM Block Diagram



4. Pin Configuration

A0–A20	21 addresses, A0-A20 used by the Flash and A0-A17 used by the SRAM
DQ0–DQ14	15 data inputs/outputs, used by both the SRAM and Flash
DQ15/A-1	DQ15 (data input/output, Flash word mode and SRAM), A-1 (LSB address input, Flash byte mode)
BYTE#	Selects 8-bit or 16-bit mode for Flash
FCE#	Flash chip enable
FOE#	Flash output enable
FWE#	Flash write enable
RESET#	Flash hardware reset pin
WP#/ACC	Flash Hardware Write Protect input/Programming Acceleration input.
RY/BY#	Flash ready/busy output
SCE1#	SRAM chip enable 1
SCE2	SRAM chip enable 2
SOE#	SRAM output enable
SWE#	SRAM write enable
SUB#	SRAM upper byte select for controlling DQ8-15
SLB#	SRAM lower byte select for controlling DQ0-7
FV_{CC}	3.3 volt-only single power supply for Flash
FV_{SS}	Flash ground
SV_{CC}	3.3 volt-only single power supply for SRAM
FV_{SS}	SRAM ground
NC	Pin not connected internally

5. MCP Block Diagram



6. Absolute Maximum Ratings

Storage Temperature Plastic Packages	–65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Voltage with Respect to Ground	
V_{CC} (Note 1)	–0.3 V to +4.0 V
FOE# and RESET# (Note 2)	–0.3 V to +12.5 V
All other pins (Note 1)	–0.3 V to V_{CC}+0.3 V
Output Short Circuit Current (Note 3)	200 mA

Notes

1. *Minimum DC voltage on input or I/O pins is –0.3 V. During voltage transitions, input or I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 14.1 on page 35. Maximum DC voltage on input or I/O pins is V_{CC} +0.3 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 14.2 on page 35.*
2. *Minimum DC input voltage on pins FOE#, and RESET# is -0.5 V. During voltage transitions, FOE#, and RESET# may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 14.1 on page 35. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
3. *Stresses above those listed under* Absolute Maximum Ratings *may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

6.1 Special Handling Instructions

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

7. Device Bus Operations (Functional Truth Table)

This section describes the requirements and use of the device bus operations. The input registers are composed of latches that store the commands, along with the address and data information needed to execute the command. The following table lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 7.1 Device Bus Operations

Flash Operation	FCE#	FOE#	FWE#	RESET#	WP#/ACC	Addresses (Note 1)	DQ0–DQ7	DQ8–DQ15	
								BYTE# = V_{IH}	BYTE# = V_{IL}
Read	L	L	H	H	L/H	A_{IN}	D_{OUT}	D_{OUT}	DQ8–DQ14 = High-Z, DQ15 = A-1
Write	L	H	L	H	(Note 3)	A_{IN}	(Note 4)	(Note 4)	
Accelerated Program	L	H	L	H	V_{HH}	A_{IN}	(Note 4)	(Note 4)	
Standby	$V_{CC} \pm 0.3$ V	X	X	$V_{CC} \pm 0.3$ V	H	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	L/H	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	L/H	X	High-Z	High-Z	High-Z
Sector Protect (Note 2)	L	H	L	V_{ID}	L/H	Sector Address, A6 = L, A1 = H, A0 = L	(Note 4)	X	X
Sector Unprotect (Note 2)	L	H	L	V_{ID}	(Note 3)	Sector Address, A6 = H, A1 = H, A0 = L	(Note 4)	X	X
Temporary Sector Unprotect	X	X	X	V_{ID}	(Note 3)	A_{IN}	(Note 4)	(Note 4)	High-Z

SRAM Operation	SCE1#	SCE2	SOE#	SWE#	SUB#	SLB#	Addresses	DQ0–DQ7	DQ8–DQ15
Read	L	H	L	H	L	L	A_{IN}	D_{OUT}	D_{OUT}
Read Upper Byte Only	L	H	L	H	L	H	A_{IN}	High-Z	D_{OUT}
Read Lower Byte Only	L	H	L	H	H	L	A_{IN}	D_{OUT}	High-Z
Write	L	H	H	L	L	L	A_{IN}	D_{IN}	D_{IN}
Write Upper Byte Only	L	H	H	L	L	H	A_{IN}	High-Z	D_{IN}
Write Lower Byte Only	L	H	H	L	H	L	A_{IN}	D_{IN}	High-Z
Standby	H	X	X	X	X	X	X	High-Z	High-Z
Standby	X	L	X	X	X	X	X	High-Z	High-Z
Standby	X	X	X	X	H	H	X	High-Z	High-Z
Output Disable (active power)	L	H	H	H	L	L	X	High-Z	High-Z

Legend

L = Logic Low = V_{IL}, H = Logic High = V_{IH}

V_{ID} = 12.0 ± 0.5 V

X = Don't Care

A_{IN} = Address In

D_{IN} = Data In, D_{OUT} = Data Out

Notes

1. *Addresses are A20:A0 in word mode (BYTE# = V_{IH}), A20:A-1 in byte mode (BYTE# = V_{IL}).*
2. *The sector protect and sector unprotect functions may also be implemented via programming equipment*
3. *If WP#/ACC = V_{IL}, the two outermost boot sectors remain protected. If WP#/ACC = V_{IH}, the two outermost boot sector protection depends on whether they were last protected or unprotected. If WP#/ACC = V_{HH}, all sectors are unprotected*
4. *D_{IN} or D_{OUT} as required by command sequence, data polling, or sector protection algorithm*

8. Flash Operation Descriptions

8.1 Requirements for Reading Array Data

To read array data from the outputs, the system must drive the FCE# and FOE# pins to V_{IL}. FCE# is the power control and selects the device. FOE# is the output control and gates array data to the output pins. FWE# should remain at V_{IH}. The BYTE# pin determines whether the device outputs array data in words or bytes.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See *Reading Array Data* on page 23 for more information. Refer to the AC *Read Operations* on page 40 for timing specifications and to Figure 18.1 on page 40 for the timing diagram. I_{CC1} in *DC Characteristics* on page 36 represents the active current specification for reading array data.

8.2 Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive FWE# and FCE# to V_{IL}, and FOE# to V_{IH}.

For program operations, the BYTE# pin determines whether the device accepts program data in bytes or words. See below for more information.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word or byte, instead of four. *Word/Byte Program Command Sequence* on page 24 has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 8.1 on page 12 and Table 8.1 on page 13 indicate the address space that each sector occupies. A “sector address” consists of the address bits required to uniquely select a sector. The *Flash Command Definitions* on page 23 has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to *Autoselect Command Sequence* on page 23 for more information.

I_{CC2} in *DC Characteristics* on page 36 represents the active current specification for the write mode. *Flash AC Characteristics* on page 40 contains timing specification tables and timing diagrams for write operations.

8.3 Flash Word/Byte Configuration

The BYTE# pin controls whether the Flash device data I/O pins DQ15–DQ0 operate in the byte or word configuration. If the BYTE# pin is set at logic *1*, the Flash device is in word configuration, DQ15–DQ0 are active and controlled by CE# and OE#.

If the BYTE# pin is set at logic *0*, the Flash device is in byte configuration, and only data I/O pins DQ0–DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8–DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

8.4 Program and Erase Operation Status

During an erase or program operation, the system may check the status of the operation by reading the status bits on DQ7–DQ0. Standard read cycle timings and I_{CC} read specifications apply. Refer to *Flash Write Operation Status* on page 30 for more information, and to *Flash AC Characteristics* on page 40 for timing diagrams.

8.5 Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This is one of two functions provided by the WP#/ACC pin. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts V_{HH} on this pin, the device automatically enters the previously mentioned Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the WP#/ACC pin returns the device to normal operation. Note that the WP#/ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result. In addition, the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.

8.6 Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the FOE# input.

The device enters the CMOS standby mode when the FCE# and RESET# pins are both held at $V_{CC} \pm 0.3$ V. (Note that this is a more restricted voltage range than V_{IH}.) If FCE# and RESET# are held at V_{IH}, but not within $V_{CC} \pm 0.3$ V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} and I_{CC4} represents the standby current specification shown in the table in *DC Characteristics* on page 36.

8.7 Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ASM}. The automatic sleep mode is independent of the FCE#, FWE#, and FOE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{CC4} in the *DC Characteristics* on page 36 represents the automatic sleep mode current specification. Maximum $t_{ASM} = t_{ACC}$ +30ns.

8.8 RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the system drives the RESET# pin to V_{IL} for at least a period of t_{RP}, the device **immediately terminates** any operation in progress, tristates all data output pins, and ignores all read/write attempts for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at $V_{SS} \pm 0.3$ V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within $V_{SS} \pm 0.3$ V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a *0* (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is *1*), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH}.

Refer to the tables in *Flash AC Characteristics* on page 40 for RESET# parameters and to Figure 18.2 on page 41 for the timing diagram.

8.9 Output Disable Mode

When the FOE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

8.10 Sector Address Tables

Table 8.1 Top Boot Sector Addresses (Sheet 1 of 2)

Sector	Sector Address A20–A12	Sector Size (Kbytes/ Kwords)	(x8) Address Range	(x16) Address Range
SA0	000000xxx	64/32	000000h–00FFFFh	000000h–07FFFh
SA1	000001xxx	64/32	010000h–01FFFFh	008000h–0FFFFh
SA2	000010xxx	64/32	020000h–02FFFFh	010000h–17FFFh
SA3	000011xxx	64/32	030000h–03FFFFh	018000h–01FFFFh
SA4	000100xxx	64/32	040000h–04FFFFh	020000h–027FFFh
SA5	000101xxx	64/32	050000h–05FFFFh	028000h–02FFFFh
SA6	000110xxx	64/32	060000h–06FFFFh	030000h–037FFFh
SA7	000111xxx	64/32	070000h–07FFFFh	038000h–03FFFFh
SA8	001000xxx	64/32	080000h–08FFFFh	040000h–047FFFh
SA9	001001xxx	64/32	090000h–09FFFFh	048000h–04FFFFh
SA10	001010xxx	64/32	0A0000h–0AFFFFh	050000h–057FFFh
SA11	001011xxx	64/32	0B0000h–0BFFFFh	058000h–05FFFFh
SA12	001100xxx	64/32	0C0000h–0CFFFFh	060000h–067FFFh
SA13	001101xxx	64/32	0D0000h–0DFFFFh	068000h–06FFFFh
SA14	001110xxx	64/32	0E0000h–0EFFFFh	070000h–077FFFh
SA15	001111xxx	64/32	0F0000h–0FFFFFh	078000h–07FFFFh
SA16	010000xxx	64/32	100000h–10FFFFh	080000h–087FFFh
SA17	010001xxx	64/32	110000h–11FFFFh	088000h–08FFFFh
SA18	010010xxx	64/32	120000h–12FFFFh	090000h–097FFFh
SA19	010011xxx	64/32	130000h–13FFFFh	098000h–09FFFFh
SA20	010100xxx	64/32	140000h–14FFFFh	0A0000h–0A7FFFh
SA21	010101xxx	64/32	150000h–15FFFFh	0A8000h–0AFFFFh
SA22	010110xxx	64/32	160000h–16FFFFh	0B0000h–0B7FFFh
SA23	010111xxx	64/32	170000h–17FFFFh	0B8000h–0BFFFFh
SA24	011000xxx	64/32	180000h–18FFFFh	0C0000h–0C7FFFh
SA25	011001xxx	64/32	190000h–19FFFFh	0C8000h–0CFFFFh
SA26	011010xxx	64/32	1A0000h–1AFFFFh	0D0000h–0D7FFFh
SA27	011011xxx	64/32	1B0000h–1BFFFFh	0D8000h–0DFFFFh
SA28	011100xxx	64/32	1C0000h–1CFFFFh	0E0000h–0E7FFFh
SA29	011101xxx	64/32	1D0000h–1DFFFFh	0E8000h–0EFFFFh
SA30	011110xxx	64/32	1E0000h–1EFFFFh	0F0000h–0F7FFFh
SA31	011111xxx	64/32	1F0000h–1FFFFFh	0F8000h–0FFFFFh
SA32	100000xxx	64/32	200000h–20FFFFh	100000h–107FFFh
SA33	100001xxx	64/32	210000h–21FFFFh	108000h–10FFFFh
SA34	100010xxx	64/32	220000h–22FFFFh	110000h–117FFFh
SA35	100011xxx	64/32	230000h–23FFFFh	118000h–11FFFFh
SA36	100100xxx	64/32	240000h–24FFFFh	120000h–127FFFh
SA37	100101xxx	64/32	250000h–25FFFFh	128000h–12FFFFh
SA38	100110xxx	64/32	260000h–26FFFFh	130000h–137FFFh
SA39	100111xxx	64/32	270000h–27FFFFh	138000h–13FFFFh
SA40	101000xxx	64/32	280000h–28FFFFh	140000h–147FFFh
SA41	101001xxx	64/32	290000h–29FFFFh	148000h–14FFFFh
SA42	101010xxx	64/32	2A0000h–2AFFFFh	150000h–157FFFh

Table 8.1 Top Boot Sector Addresses (Sheet 2 of 2)

Sector	Sector Address A20–A12	Sector Size (Kbytes/ Kwords)	(x8) Address Range	(x16) Address Range
SA43	101011xxx	64/32	2B0000h–2BFFFFh	158000h–15FFFFh
SA44	101100xxx	64/32	2C0000h–2CFFFFh	160000h–167FFFh
SA45	101101xxx	64/32	2D0000h–2DFFFFh	168000h–16FFFFh
SA46	101110xxx	64/32	2E0000h–2EFFFFh	170000h–177FFFh
SA47	101111xxx	64/32	2F0000h–2FFFFFh	178000h–17FFFFh
SA48	110000xxx	64/32	300000h–30FFFFh	180000h–187FFFh
SA49	110001xxx	64/32	310000h–31FFFFh	188000h–18FFFFh
SA50	110010xxx	64/32	320000h–32FFFFh	190000h–197FFFh
SA51	110011xxx	64/32	330000h–33FFFFh	198000h–19FFFFh
SA52	110100xxx	64/32	340000h–34FFFFh	1A0000h–1A7FFFh
SA53	110101xxx	64/32	350000h–35FFFFh	1A8000h–1AFFFFh
SA54	110110xxx	64/32	360000h–36FFFFh	1B0000h–1B7FFFh
SA55	110111xxx	64/32	370000h–37FFFFh	1B8000h–1BFFFFh
SA56	111000xxx	64/32	380000h–38FFFFh	1C0000h–1C7FFFh
SA57	111001xxx	64/32	390000h–39FFFFh	1C8000h–1CFFFFh
SA58	111010xxx	64/32	3A0000h–3AFFFFh	1D0000h–1D7FFFh
SA59	111011xxx	64/32	3B0000h–3BFFFFh	1D8000h–1DFFFFh
SA60	111100xxx	64/32	3C0000h–3CFFFFh	1E0000h–1E7FFFh
SA61	111101xxx	64/32	3D0000h–3DFFFFh	1E8000h–1EFFFFh
SA62	111110xxx	64/32	3E0000h–3EFFFFh	1F0000h–1F7FFFh
SA63	111111000	8/4	3F0000h–3F1FFFh	1F8000h–1F8FFFh
SA64	111111001	8/4	3F2000h–3F3FFFh	1F9000h–1F9FFFh
SA65	111111010	8/4	3F4000h–3F5FFFh	1FA000h–1FAFFFh
SA66	111111011	8/4	3F6000h–3F7FFFh	1FB000h–1FBFFFh
SA67	111111100	8/4	3F8000h–3F9FFFh	1FC000h–1FCFFFh
SA68	111111101	8/4	3FA000h–3FBFFFh	1FD000h–1FDFFFh
SA69	111111110	8/4	3FC000h–3FDFFFh	1FE000h–1FEFFFh
SA70	111111111	8/4	3FE000h–3FFFFFh	1FF000h–1FFFFFh

Note
The address range is A20:A-1 in byte mode (BYTE#=V_{IL}) or A20:A0 in word mode (BYTE#=V_{IH}).

Table 8.2 Top Boot Secured Silicon Sector Addresses

Sector Address A20–A12	Sector Size (bytes/words)	(x8) Address Range	(x16) Address Range
111111111	256/128	3FFF00h–3FFFFFh	1FFF80h–1FFFFFh

Table 8.3 Bottom Boot Sector Addresses (Sheet 1 of 2)

Sector	Sector Address A20–A12	Sector Size (Kbytes/ Kwords)	(x8) Address Range	(x16) Address Range
SA0	000000000	8/4	000000h-001FFFh	000000h–000FFFh
SA1	000000001	8/4	002000h-003FFFh	001000h–001FFFh
SA2	000000010	8/4	004000h-005FFFh	002000h–002FFFh
SA3	000000011	8/4	006000h-007FFFh	003000h–003FFFh
SA4	000000100	8/4	008000h-009FFFh	004000h–004FFFh
SA5	000000101	8/4	00A000h-00BFFFh	005000h–005FFFh
SA6	000000110	8/4	00C000h-00DFFFh	006000h–006FFFh
SA7	000000111	8/4	00E000h-00FFFFh	007000h–007FFFh
SA8	000001xxx	64/32	010000h-01FFFFh	008000h–00FFFFh
SA9	000010xxx	64/32	020000h-02FFFFh	010000h–017FFFh
SA10	000011xxx	64/32	030000h-03FFFFh	018000h–01FFFFh
SA11	000100xxx	64/32	040000h-04FFFFh	020000h–027FFFh
SA12	000101xxx	64/32	050000h-05FFFFh	028000h–02FFFFh
SA13	000110xxx	64/32	060000h-06FFFFh	030000h–037FFFh
SA14	000111xxx	64/32	070000h-07FFFFh	038000h–03FFFFh
SA15	001000xxx	64/32	080000h-08FFFFh	040000h–047FFFh
SA16	001001xxx	64/32	090000h-09FFFFh	048000h–04FFFFh
SA17	001010xxx	64/32	0A0000h-0AFFFFh	050000h–057FFFh
SA18	001011xxx	64/32	0B0000h-0BFFFFh	058000h–05FFFFh
SA19	001100xxx	64/32	0C0000h-0CFFFFh	060000h–067FFFh
SA20	001101xxx	64/32	0D0000h-0DFFFFh	068000h–06FFFFh
SA21	001110xxx	64/32	0E0000h-0EFFFFh	070000h–077FFFh
SA22	001111xxx	64/32	0F0000h-0FFFFFh	078000h–07FFFFh
SA23	010000xxx	64/32	100000h-10FFFFh	080000h–087FFFh
SA24	010001xxx	64/32	110000h-11FFFFh	088000h–08FFFFh
SA25	010010xxx	64/32	120000h-12FFFFh	090000h–097FFFh
SA26	010011xxx	64/32	130000h-13FFFFh	098000h–09FFFFh
SA27	010100xxx	64/32	140000h-14FFFFh	0A0000h–0A7FFFh
SA28	010101xxx	64/32	150000h-15FFFFh	0A8000h–0AFFFFh
SA29	010110xxx	64/32	160000h-16FFFFh	0B0000h–0B7FFFh
SA30	010111xxx	64/32	170000h-17FFFFh	0B8000h–0BFFFFh
SA31	011000xxx	64/32	180000h-18FFFFh	0C0000h–0C7FFFh
SA32	011001xxx	64/32	190000h-19FFFFh	0C8000h–0CFFFFh
SA33	011010xxx	64/32	1A0000h-1AFFFFh	0D0000h–0D7FFFh
SA34	011011xxx	64/32	1B0000h-1BFFFFh	0D8000h–0DFFFFh
SA35	011100xxx	64/32	1C0000h-1CFFFFh	0E0000h–0E7FFFh
SA36	011101xxx	64/32	1D0000h-1DFFFFh	0E8000h–0EFFFFh
SA37	011110xxx	64/32	1E0000h-1EFFFFh	0F0000h–0F7FFFh
SA38	011111xxx	64/32	1F0000h-1FFFFFh	0F8000h–0FFFFFh
SA39	100000xxx	64/32	200000h-20FFFFh	100000h–107FFFh
SA40	100001xxx	64/32	210000h-21FFFFh	108000h–10FFFFh
SA41	100010xxx	64/32	220000h-22FFFFh	110000h–117FFFh
SA42	100011xxx	64/32	230000h-23FFFFh	118000h–11FFFFh
SA43	100100xxx	64/32	240000h-24FFFFh	120000h–127FFFh

Table 8.3 Bottom Boot Sector Addresses (Sheet 2 of 2)

Sector	Sector Address A20–A12	Sector Size (Kbytes/ Kwords)	(x8) Address Range	(x16) Address Range
SA44	100101xxx	64/32	250000h-25FFFFh	128000h–12FFFFh
SA45	100110xxx	64/32	260000h-26FFFFh	130000h–137FFFh
SA46	100111xxx	64/32	270000h-27FFFFh	138000h–13FFFFh
SA47	101000xxx	64/32	280000h-28FFFFh	140000h–147FFFh
SA48	101001xxx	64/32	290000h-29FFFFh	148000h–14FFFFh
SA49	101010xxx	64/32	2A0000h-2AFFFFh	150000h–157FFFh
SA50	101011xxx	64/32	2B0000h-2BFFFFh	158000h–15FFFFh
SA51	101100xxx	64/32	2C0000h-2CFFFFh	160000h–167FFFh
SA52	101101xxx	64/32	2D0000h-2DFFFFh	168000h–16FFFFh
SA53	101110xxx	64/32	2E0000h-2EFFFFh	170000h–177FFFh
SA54	101111xxx	64/32	2F0000h-2FFFFFh	178000h–17FFFFh
SA55	111000xxx	64/32	300000h-30FFFFh	180000h–187FFFh
SA56	110001xxx	64/32	310000h-31FFFFh	188000h–18FFFFh
SA57	110010xxx	64/32	320000h-32FFFFh	190000h–197FFFh
SA58	110011xxx	64/32	330000h-33FFFFh	198000h–19FFFFh
SA59	110100xxx	64/32	340000h-34FFFFh	1A0000h–1A7FFFh
SA60	110101xxx	64/32	350000h-35FFFFh	1A8000h–1AFFFFh
SA61	110110xxx	64/32	360000h-36FFFFh	1B0000h–1B7FFFh
SA62	110111xxx	64/32	370000h-37FFFFh	1B8000h–1BFFFFh
SA63	111000xxx	64/32	380000h-38FFFFh	1C0000h–1C7FFFh
SA64	111001xxx	64/32	390000h-39FFFFh	1C8000h–1CFFFFh
SA65	111010xxx	64/32	3A0000h-3AFFFFh	1D0000h–1D7FFFh
SA66	111011xxx	64/32	3B0000h-3BFFFFh	1D8000h–1DFFFFh
SA67	111100xxx	64/32	3C0000h-3CFFFFh	1E0000h–1E7FFFh
SA68	111101xxx	64/32	3D0000h-3DFFFFh	1E8000h–1EFFFFh
SA69	111110xxx	64/32	3E0000h-3EFFFFh	1F0000h–1F7FFFh
SA70	111111xxx	64/32	3F0000h-3FFFFFh	1F8000h–1FFFFFh

1. Note: The address range is A20:A-1 in byte mode (BYTE#=V_{IL}) or A20:A0 in word mode (BYTE#=V_{IH}).

Table 8.4 Bottom Boot Secured Silicon Sector Addresses

Sector Address A20–A12	Sector Size (bytes/words)	(x8) Address Range	(x16) Address Range
000000000	256/128	000000h-0000FFh	00000h-0007Fh

8.11 Sector Protection/Unprotection

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors.

The device is shipped with all sectors unprotected. Spansion offers the option of programming and protecting sectors at its factory prior to shipping the device through Spansion's ExpressFlash™ Service. Contact a Spansion representative for details.

Sector protection/unprotection requires V_{ID} on the RESET# pin, and can be implemented either in-system or via programming equipment. Figure 8.2 on page 18 shows the algorithms and Figure 18.13 on page 48 shows the timing diagram. This method uses standard microprocessor bus cycle timing. For sector unprotect, all unprotected sectors must first be protected prior to the first sector unprotect write cycle.

Table 8.5 Sector Block Addresses for Protection/Unprotection — Top Boot

Sector / Sector Block	A20–A12	Sector/Sector Block Size
SA0-SA3	000000XXX, 000001XXX, 000010XXX, 000011XXX	256 (4x64) Kbytes
SA4-SA7	0001XXXXX	256 (4x64) Kbytes
SA8-SA11	0010XXXXX	256 (4x64) Kbytes
SA12-SA15	0011XXXXX	256 (4x64) Kbytes
SA16-SA19	0100XXXXX	256 (4x64) Kbytes
SA20-SA23	0101XXXXX	256 (4x64) Kbytes
SA24-SA27	0110XXXXX	256 (4x64) Kbytes
SA28-SA31	0111XXXXX	256 (4x64) Kbytes
SA32-SA35	1000XXXXX	256 (4x64) Kbytes
SA36-SA39	1001XXXXX	256 (4x64) Kbytes
SA40-SA43	1010XXXXX	256 (4x64) Kbytes
SA44-SA47	1011XXXXX	256 (4x64) Kbytes
SA48-SA51	1100XXXXX	256 (4x64) Kbytes
SA52-SA55	1101XXXXX	256 (4x64) Kbytes
SA56-SA59	1110XXXXX	256 (4x64) Kbytes
SA60-SA62	111100XXX, 111101XXX, 111110XXX	192 (3x64) Kbytes
SA63	111111000	8 Kbytes
SA64	111111001	8 Kbytes
SA65	111111010	8 Kbytes
SA66	111111011	8 Kbytes
SA67	111111100	8 Kbytes
SA68	111111101	8 Kbytes
SA69	111111110	8 Kbytes
SA70	111111111	8 Kbytes

Table 8.6 Sector Block Addresses for Protection/Unprotection — Bottom Boot

Sector / Sector Block	A20–A12	Sector/Sector Block Size
SA70-SA67	111111XXX, 111110XXX, 111101XXX, 111100XXX	256 (4x64) Kbytes
SA66-SA63	1110XXXXX	256 (4x64) Kbytes
SA62-SA59	1101XXXXX	256 (4x64) Kbytes
SA58-SA55	1100XXXXX	256 (4x64) Kbytes
SA54-SA51	1011XXXXX	256 (4x64) Kbytes
SA50-SA47	1010XXXXX	256 (4x64) Kbytes
SA46-SA43	1001XXXXX	256 (4x64) Kbytes
SA42-SA39	1000XXXXX	256 (4x64) Kbytes
SA38-SA35	0111XXXXX	256 (4x64) Kbytes
SA34-SA31	0110XXXXX	256 (4x64) Kbytes
SA30-SA27	0101XXXXX	256 (4x64) Kbytes
SA26-SA23	0100XXXXX	256 (4x64) Kbytes
SA22–SA19	0011XXXXX	256 (4x64) Kbytes
SA18-SA15	0010XXXXX	256 (4x64) Kbytes
SA14-SA11	0001XXXXX	256 (4x64) Kbytes
SA10-SA8	000011XXX, 000010XXX, 000001XXX	192 (3x64) Kbytes
SA7	000000111	8 Kbytes
SA6	000000110	8 Kbytes
SA5	000000101	8 Kbytes
SA4	000000100	8 Kbytes
SA3	000000011	8 Kbytes
SA2	000000010	8 Kbytes
SA1	000000001	8 Kbytes
SA0	000000000	8 Kbytes

8.12 Write Protect (WP#)

The Write Protect function provides a hardware method of protecting certain boot sectors without using V_{ID}. This function is one of two provided by the WP#/ACC pin.

If the system asserts V_{IL} on the WP#/ACC pin, the device disables program and erase functions in the two *outermost* 8-Kbyte boot sectors independently of whether those sectors were protected or unprotected using the method described in Sector Protection/Unprotection. The two outermost 8-Kbyte boot sectors are the two sectors containing the lowest addresses in a bottom-boot-configured device, or the two sectors containing the highest addresses in a top-boot-configured device.

If the system asserts V_{IH} on the WP#/ACC pin, the device reverts to whether the two outermost 8-KByte boot sectors were last set to be protected or unprotected. That is, sector protection or unprotection for these two sectors depends on whether they were last protected or unprotected using the method described in Sector Protection/Unprotection

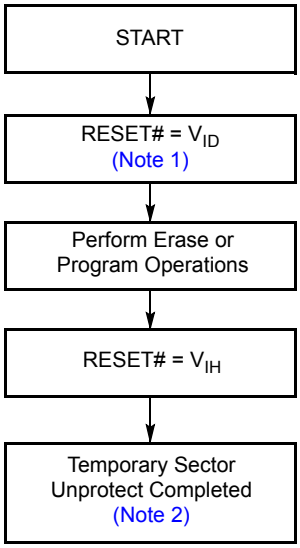
Note that the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.

8.13 Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the RESET# pin to V_{ID}. During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the

RESET# pin, all the previously protected sectors are protected again. Figure 8.1 shows the algorithm, and Figure 18.11 on page 47 shows the timing diagrams, for this feature.

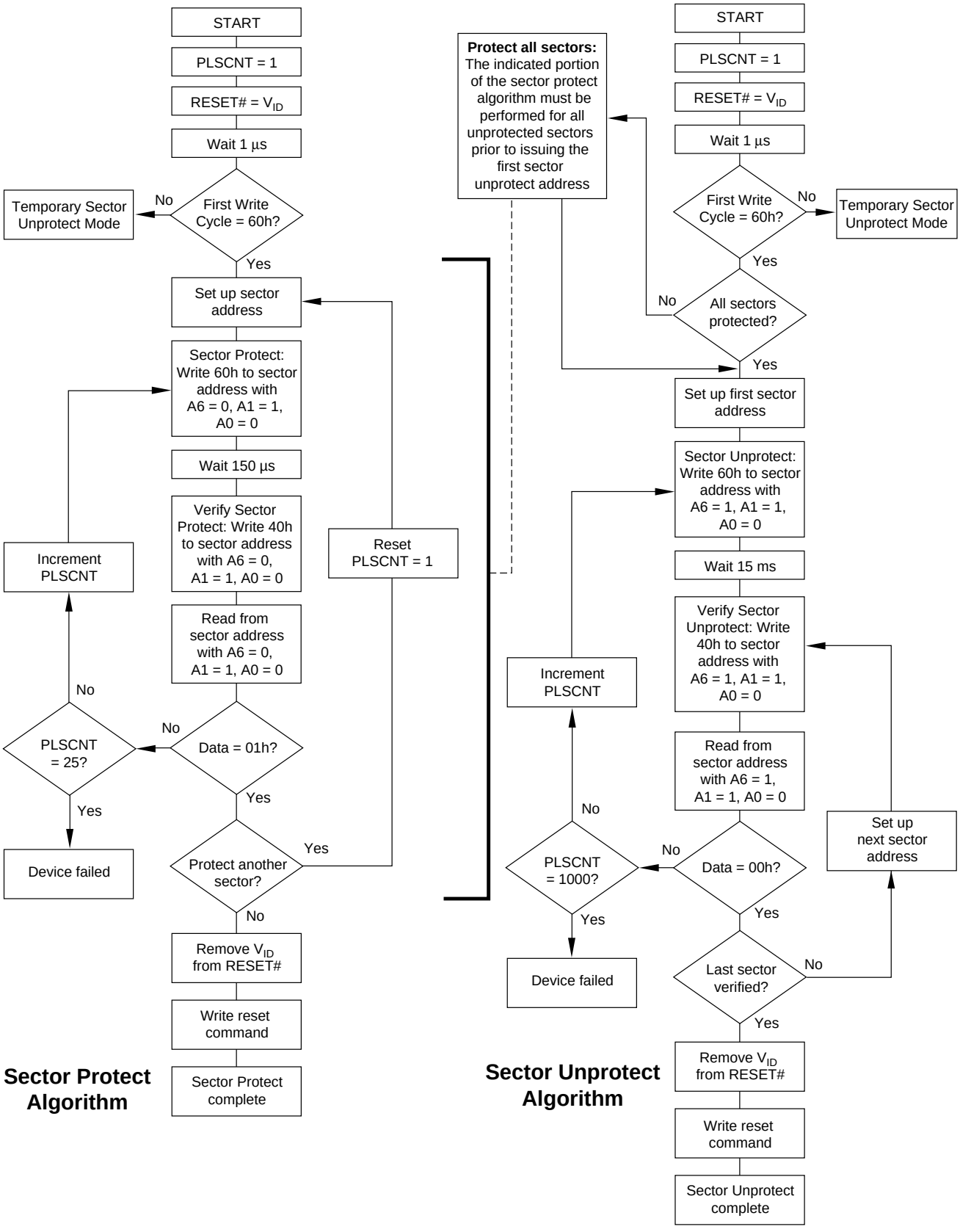
Figure 8.1 Temporary Sector Unprotect Operation



Notes

1. *All protected sectors unprotected.*
2. *All previously protected sectors are protected once again.*

Figure 8.2 In-System Sector Protect/Unprotect Algorithms



9. Secured Silicon Sector Flash Memory Region

The Secured Silicon Sector feature provides a 256-byte Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN).

This Secured Silicon Sector is customer-lockable and customers can utilize the sector in any manner they choose. The Secured Silicon Sector Indicator Bit is permanently set to a *0.*

The system accesses the Secured Silicon Sector through a command sequence (see Enter Secured Silicon Sector/Exit Secured Silicon Sector Command Sequence on page 24). After the system writes the Enter Secured Silicon Sector command sequence, it may read the Secured Silicon Sector by using the addresses normally occupied by the boot sectors. This mode of operation continues until the system issues the Exit Secured Silicon Sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to the boot sectors.

The Secured Silicon Sector can be programmed once, and then permanently locked after it ships. Note that the accelerated programming (ACC) and unlock bypass functions are not available when programming the Secured Silicon Sector.

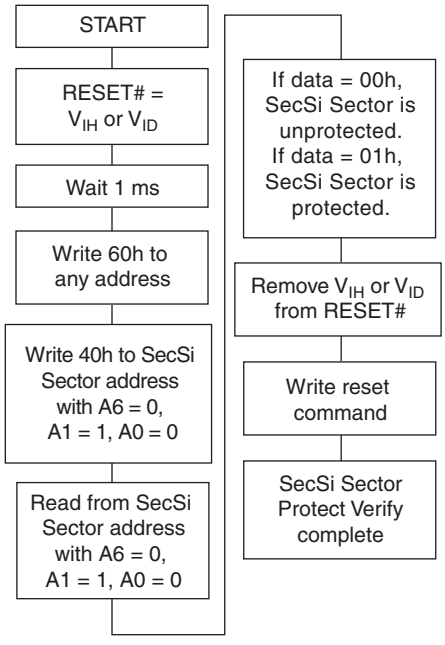
The Secured Silicon Sector area can be protected using the following procedures:

- Write the three-cycle Enter Secured Silicon Region command sequence, and then follow the in-system sector protect algorithm as shown in Figure 8.2 on page 18, except that *RESET# may be at either V_{IH} or V_{ID}*. This allows in-system protection of the Secured Silicon Sector without raising any device pin to a high voltage. Note that this method is only applicable to the Secured Silicon Sector.
- To verify the protect/unprotect status of the Secured Silicon Sector, follow the algorithm shown in Figure 9.1 on page 19.

Once the Secured Silicon Sector is locked and verified, the system must write the Exit Secured Silicon Sector Region command sequence to return to reading and writing the remainder of the array.

The Secured Silicon Sector protection must be used with caution since, once protected, there is no procedure available for unprotecting the Secured Silicon Sector area, and none of the bits in the Secured Silicon Sector memory space can be modified in any way.

Figure 9.1 Secured Silicon Sector Protect Verify



10. Common Flash Memory Interface (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h in word mode (or address AAh in byte mode), any time the device is ready to read array data. The system can read CFI information at the addresses given in Table 10.1 to Table 10.4 on page 21. In word mode, the upper address bits (A7–MSB) must be all zeros. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Table 10.1 to Table 10.4 on page 21. The system must write the reset command to return the device to the autoselect mode.

Table 10.1 CFI Query Identification String

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
10h 11h 12h	20h 22h 24h	0051h 0052h 0059h	Query Unique ASCII string “QRY”
13h 14h	26h 28h	0002h 0000h	Primary OEM Command Set
15h 16h	2Ah 2Ch	0040h 0000h	Address for Primary Extended Table
17h 18h	2Eh 30h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	32h 34h	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 10.2 System Interface String

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
1Bh	36h	0027h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	38h	0036h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	3Ah	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	3Ch	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	3Eh	0004h	Typical timeout per single byte/word write 2^N µs
20h	40h	0000h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	42h	000Ah	Typical timeout per individual block erase 2^N ms
22h	44h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	46h	0005h	Max. timeout for byte/word write 2^N times typical
24h	48h	0000h	Max. timeout for buffer write 2^N times typical
25h	4Ah	0004h	Max. timeout per individual block erase 2^N times typical
26h	4Ch	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 10.3 Device Geometry Definition

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
27h	4Eh	0016h	Device Size = 2^N byte
28h 29h	50h 52h	0002h 0000h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	54h 56h	0000h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	58h	0002h	Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	5Ah 5Ch 5Eh 60h	0007h 0000h 0020h 0000h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
31h 32h 33h 34h	62h 64h 66h 68h	003Eh 0000h 0000h 0001h	Erase Block Region 2 Information
35h 36h 37h 38h	6Ah 6Ch 6Eh 70h	0000h 0000h 0000h 0000h	Erase Block Region 3 Information
39h 3Ah 3Bh 3Ch	72h 74h 76h 78h	0000h 0000h 0000h 0000h	Erase Block Region 4 Information

Table 10.4 Primary Vendor-Specific Extended Query

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
40h 41h 42h	80h 82h 84h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	86h	0031h	Major version number, ASCII
44h	88h	0031h	Minor version number, ASCII
45h	8Ah	0000h	Address Sensitive Unlock
46h	8Ch	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	8Eh	0001h	Sector Protect 0 = Not Supported, X = Number of sectors per group
48h	90h	0001h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	92h	0004h	Sector Protect/Unprotect scheme 01 = 29F040 mode, 02 = 29F016 mode, 03 = 29F400 mode, 04 = 29LV800A mode
4Ah	94h	0000h	Simultaneous Operation 00 = Not Supported, 01 = Supported
4Bh	96h	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	98h	0000h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	9Ah	00B5h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	9Ch	00C5h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	9Eh	000xh	Top/Bottom Boot Sector Flag (3 = Top Boot, 2 = Bottom Boot)

10.1 Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Table 12.1 on page 31 for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

10.1.1 Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

10.1.2 Write Pulse *Glitch* Protection

Noise pulses of less than 5 ns (typical) on FOE#, FCE# or FWE# do not initiate a write cycle.

10.1.3 Logical Inhibit

Write cycles are inhibited by holding any one of FOE# = V_{IL}, FCE# = V_{IH} or FWE# = V_{IH}. To initiate a write cycle, FCE# and FWE# must be a logical zero while FOE# is a logical one.

10.1.4 Power-Up Write Inhibit

If FWE# = FCE# = V_{IL} and FOE# = V_{IH} during power up, the device does not accept commands on the rising edge of FWE#. The internal state machine is automatically reset to reading array data on power-up.

11. Flash Command Definitions

Writing specific address and data commands or sequences into the command register initiates device operations. Table 12.1 on page 31 defines the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** resets the device to reading array data.

All addresses are latched on the falling edge of FWE# or FCE#, whichever happens later. All data is latched on the rising edge of FWE# or FCE#, whichever happens first. Refer to the appropriate timing diagrams in *Flash AC Characteristics* on page 40.

11.1 Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See *Erase Suspend/ Erase Resume Commands* on page 26 for more information on this mode.

The system *must* issue the reset command to re-enable the device for reading array data if DQ5 goes high, or while in the autoselect mode. See *Reset Command* on page 23.

See also *Requirements for Reading Array Data* on page 8 for more information. The *Read Operations* on page 40 provides the read parameters, and Figure 18.1 on page 40 shows the timing diagram.

11.2 Reset Command

Writing the reset command to the device resets the device to reading array data. Address bits are don't care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command *must* be written to return to reading array data (also applies to autoselect during Erase Suspend).

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

11.3 Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a sector is protected. Table 12.1 on page 31 shows the address and data requirements.

The autoselect command sequence is initiated by writing two unlock cycles, followed by the autoselect command. The device then enters the autoselect mode, and the system may read at any address any number of times, without initiating another command sequence.

A read cycle at address XX00h retrieves the manufacturer code. A read cycle at address XX01h returns the device code. A read cycle containing a sector address (SA) and the address 02h in word mode (or 04h in byte mode) returns 01h if that sector is protected, or 00h if it is unprotected. Refer to Table 8.1 on page 12 and Table 8.1 on page 13 for valid sector addresses.

The system must write the reset command to exit the autoselect mode and return to reading array data.

11.4 Enter Secured Silicon Sector/Exit Secured Silicon Sector Command Sequence

The Secured Silicon Sector region provides a secured data area containing a random, sixteen-byte electronic serial number (ESN). The system can access the Secured Silicon Sector region by issuing the three-cycle Enter Secured Silicon Sector command sequence. The device continues to access the Secured Silicon Sector region until the system issues the four-cycle Exit Secured Silicon Sector command sequence. The Exit Secured Silicon Sector command sequence returns the device to normal operation. Table 11.1 on page 37 and Table 11.2 on page 38 show the addresses and data requirements for both command sequences. Note that the ACC function and unlock bypass modes are not available when the device enters the Secured Silicon Sector. See also Secured Silicon Sector Flash Memory Region on page 19 for further information.

11.5 Word/Byte Program Command Sequence

The system may program the device by word or byte, depending on the state of the BYTE# pin. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically generates the program pulses and verifies the programmed cell margin. Table 12.1 on page 31 shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. See *Flash Write Operation Status* on page 30 for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the programming operation. The Byte Program command sequence should be reinitiated once the device has reset to reading array data, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from a *0* back to a *1*.** Attempting to do so may halt the operation and set DQ5 to *1*, or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still *0*. Only erase operations can convert a *0* to a *1*.

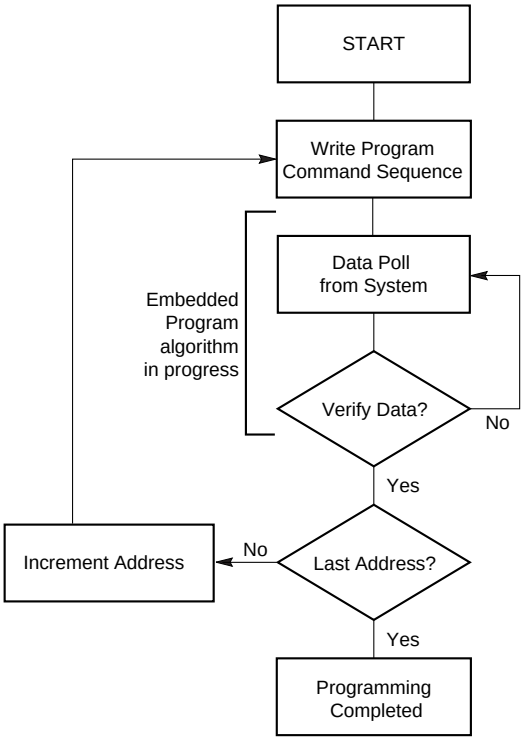
11.6 Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program bytes or words to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 12.1 on page 31 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the data 90h; the second cycle the data 00h. Addresses are don't care for both cycles. The device then returns to reading array data.

Figure 11.1 on page 25 illustrates the algorithm for the program operation. See *Erase/Program Operations* on page 43 for parameters, and to Figure 18.5 on page 44 for timing diagrams.

Figure 11.1 Program Operation



Note
See Table 12.1 on page 31 for program command sequence.

11.7 Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 12.1 on page 31 shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Embedded Erase algorithm are ignored. Note that a **hardware reset** during the chip erase operation immediately terminates the operation. The Chip Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. See *Flash Write Operation Status* on page 30 for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Figure 11.2 on page 27 illustrates the algorithm for the erase operation. See *Erase/Program Operations* on page 43 for parameters, and Figure 18.6 on page 44 for timing diagrams.

11.8 Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. Table 12.1 on page 31 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram the memory prior to erase. The Embedded Erase algorithm automatically programs and verifies the sector for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 µs begins. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise the last address and command might not be accepted, and erasure may begin. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. If the time between additional sector erase commands can be assumed to be less than 50 µs, the system need not monitor DQ3. **Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to reading array data.** The system must rewrite the command sequence and any additional sector addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out. (See *DQ3: Sector Erase Timer* on page 34.) The time-out begins from the rising edge of the final FWE# pulse in the command sequence.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. Note that a **hardware reset** during the sector erase operation immediately terminates the operation. The Sector Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. (Refer to *Flash Write Operation Status* on page 30 for information on these status bits.)

Figure 11.2 on page 27 illustrates the algorithm for the erase operation. Refer to *Erase/Program Operations* on page 43 for parameters, and to Figure 18.6 on page 44 for timing diagrams.

11.9 Erase Suspend/Erase Resume Commands

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Writing the Erase Suspend command during the Sector Erase time-out immediately terminates the time-out period and suspends the erase operation. Addresses are *don't-cares* when writing the Erase Suspend command.

When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 20 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

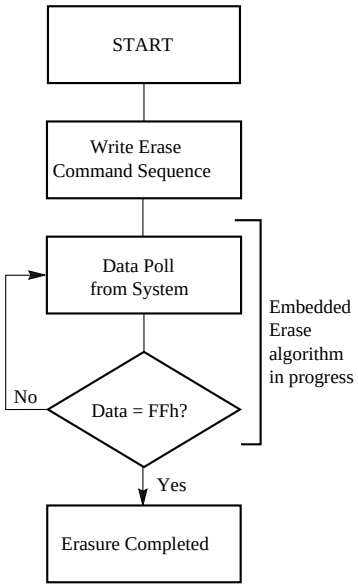
After the erase operation has been suspended, the system can read array data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) Normal read and write timings and command definitions apply. Reading at any address within erase-suspended sectors produces status data on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. See *Flash Write Operation Status* on page 30 for information on these status bits.

After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See *Flash Write Operation Status* on page 30 for more information.

The system may also write the autoselect command sequence when the device is in the Erase Suspend mode. The device allows reading autoselect codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. See *Autoselect Command Sequence* on page 23 for more information.

The system must write the Erase Resume command (address bits are *don't care*) to exit the erase suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device has resumed erasing.

Figure 11.2 Erase Operation



Notes

1. *See Table 12.1 on page 31 for erase command sequence.*
2. *See DQ3: Sector Erase Timer on page 34 for more information.*

12. Flash Command Definitions

Table 12.1 Flash Command Definitions, x8 Mode

Command Sequence (Note 1)		Cycles	Bus Cycles (Notes 2–5)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 6)		1	RA	RD										
Reset (Note 7)		1	XXX	F0										
Autoselect (Note 8)	Manufacturer ID	4	AAA	AA	555	55	AAA	90	X00	01				
	Device ID, Top Boot	4	AAA	AA	555	55	AAA	90	X02	22F6				
	Device ID, Bottom Boot	4	AAA	AA	555	55	AAA	90	X02	F9				
	Secured Silicon Sector Factory Protect, Top Boot (Note 9)	4	AAA	AA	555	55	AAA	90	X06	8D/1D				
	Secured Silicon Sector Factory Protect, Bottom Boot (Note 9)	4	AAA	AA	555	55	AAA	90	X06	9D/0D				
	Sector Protect Verify (Note 10)	4	AAA	AA	555	55	AAA	90	(SA)X04	(Note 10)				
Enter Secured Silicon Sector Region		3	AAA	AA	555	55	AAA	88						
Exit Secured Silicon Sector Region		4	AAA	AA	555	55	AAA	90	XXX	00				
CFI Query (Note 11)		1	AA	98										
Program		4	AAA	AA	555	55	AAA	A0	PA	PD				
Unlock Bypass		3	AAA	AA	555	55	AAA	20						
Unlock Bypass Program (Note 12)		2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 13)		2	XXX	90	XXX	00								
Chip Erase		6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10
Sector Erase		6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	SA	30
Erase Suspend (Note 14)		1	XXX	B0										
Erase Resume (Note 15)		1	XXX	30										

Table 12.2 Flash Command Definitions, x16 Mode

Command Sequence (Note 1)		Cycles	Bus Cycles (Notes 2–5)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 6)		1	RA	RD										
Reset (Note 7)		1	XXX	F0										
Autoselect (Note 8)	Manufacturer ID	4	555	AA	2AA	55	555	90	X00	01				
	Device ID, Top Boot	4	555	AA	2AA	55	555	90	X01	22F6				
	Device ID, Bottom Boot	4	555	AA	2AA	55	555	90	X01	22F9				
	Secured Silicon Sector Factory Protect, Top Boot (Note 9)	4	555	AA	2AA	55	555	90	X03	8D/0D				
	Secured Silicon Sector Factory Protect, Bottom Boot (Note 9)	4	555	AA	2AA	55	555	90	X03	9D/1D				
	Sector Protect Verify (Note 10)	4	555	AA	2AA	55	555	90	(SA)X02	(Note 10)				
Enter Secured Silicon Sector Region		3	555	AA	2AA	55	555	88						
Exit Secured Silicon Sector Region		4	555	AA	2AA	55	555	90	XXX	00				
CFI Query (Note 11)		1	55	98										
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Unlock Bypass		3	555	AA	2AA	55	555	20						
Unlock Bypass Program (Note 12)		2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 13)		2	XXX	90	XXX	00								

Table 12.2 Flash Command Definitions, x16 Mode

Command Sequence (Note 1)	Cycles	Bus Cycles (Notes 2–5)											
		First		Second		Third		Fourth		Fifth		Sixth	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Chip Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Erase Suspend (Note 14)	1	XXX	B0										
Erase Resume (Note 15)	1	XXX	30										

Legend

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the FWE# or FCE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of FWE# or FCE# pulse, whichever happens first.

SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A19–A12 uniquely select any sector.

Notes

1. *See Table 7.1 on page 9 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except for the read cycle and the fourth cycle of the autoselect command sequence, all bus cycles are write cycles.*
4. *Data bits DQ15–DQ8 are don't cares for unlock and command cycles.*
5. *Address bits A19–A11 are don't cares for unlock and command cycles, unless SA or PA required.*
6. *No unlock or command cycles required when reading array data.*
7. *The Reset command is required to return to reading array data when device is in the autoselect mode, or if DQ5 goes high (while the device is providing status data).*
8. *The fourth cycle of the autoselect command sequence is a read cycle.*
9. *For Top Boot device, the data is 0Dh. For Bottom Boot device, the data is 1Dh.*
10. *The data is 00h for an unprotected sector and 01h for a protected sector. See "Autoselect Command Sequence" for more information.*
11. *Command is valid when device is ready to read array data or when device is in autoselect mode.*
12. *The Unlock Bypass command is required prior to the Unlock Bypass Program command.*
13. *The Unlock Bypass Reset command is required to return to reading array data when the device is in the unlock bypass mode. F0 is also acceptable.*
14. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*
15. *The Erase Resume command is valid only during the Erase Suspend mode.*

13. Flash Write Operation Status

The device provides several bits to determine the status of a write operation: DQ2, DQ3, DQ5, DQ6, DQ7, and RY/BY#. Table 13.1 on page 34 and the following subsections describe the functions of these bits. DQ7, RY/BY#, and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

13.1 DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final FWE# pulse in the program or erase command sequence.

During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then the device returns to reading array data.

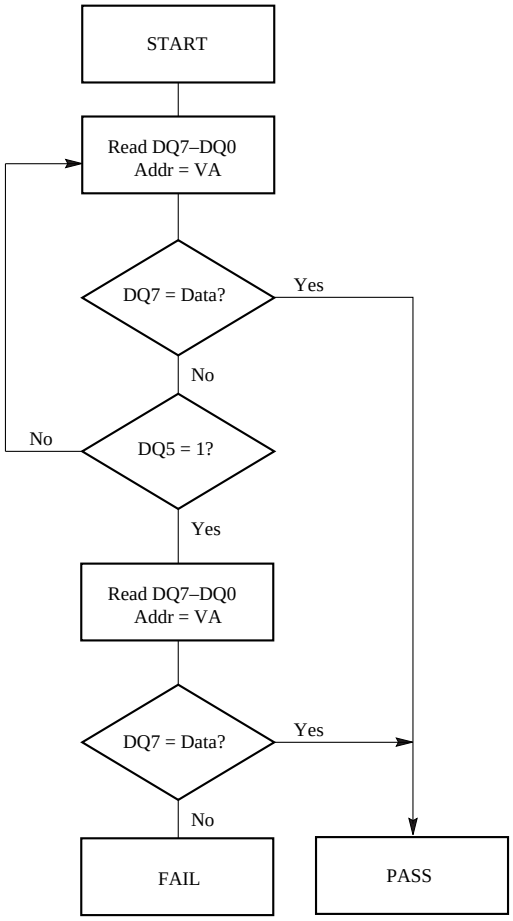
During the Embedded Erase algorithm, Data# Polling produces a *0* on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a *1* on DQ7. This is analogous to the complement/true datum output described for the Embedded Program algorithm: the erase function changes all the bits in a sector to *1*; prior to this, the device outputs the *complement*, or *0*. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the device returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

When the system detects DQ7 has changed from the complement to true data, it can read valid data at DQ7–DQ0 on the *following* read cycles. This is because DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (FOE#) is asserted low. Figure 18.8 on page 45, illustrates this.

Table 13.1 on page 34 shows the outputs for Data# Polling on DQ7. Figure 13.2 on page 33 shows the Data# Polling algorithm.

Figure 13.1 Data# Polling Algorithm



Notes

1. *VA = Valid address for programming. During a sector erase operation, a valid address is an address within any sector selected for erasure. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = 1 because DQ7 may change simultaneously with DQ5.*

13.2 RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin that indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final FWE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is ready to read array data (including during the Erase Suspend mode), or is in the standby mode.

Table 13.1 on page 34 shows the outputs for RY/BY#. Figures Figure 18.1 on page 40, Figure 18.2 on page 41, Figure 18.5 on page 44 and Figure 18.6 on page 44 shows RY/BY# for read, reset, program, and erase operations, respectively.

13.3 DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final FWE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. (The system may use either FOE# or FCE# to control the read cycles.) When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see *DQ7: Data# Polling* on page 30).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 13.1 on page 34 shows the outputs for Toggle Bit I on DQ6. Figure 13.2 on page 33 shows the toggle bit algorithm in flowchart form, and *Reading Toggle Bits DQ6/DQ2* on page 33 explains the algorithm. Figure 18.9 on page 46 shows the toggle bit timing diagrams. Figure 18.10 on page 46 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on *DQ2: Toggle Bit II* on page 32.

13.4 DQ2: Toggle Bit II

The “Toggle Bit II” on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final FWE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either FOE# or FCE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 13.1 on page 34 to compare outputs for DQ2 and DQ6.

Figure 13.2 on page 33 shows the toggle bit algorithm in flowchart form, and the section *Reading Toggle Bits DQ6/DQ2* on page 33 explains the algorithm. See also the *DQ6: Toggle Bit I* on page 32 subsection. Figure 18.9 on page 46 shows the toggle bit timing diagram. Figure 18.10 on page 46 shows the differences between DQ2 and DQ6 in graphical form.

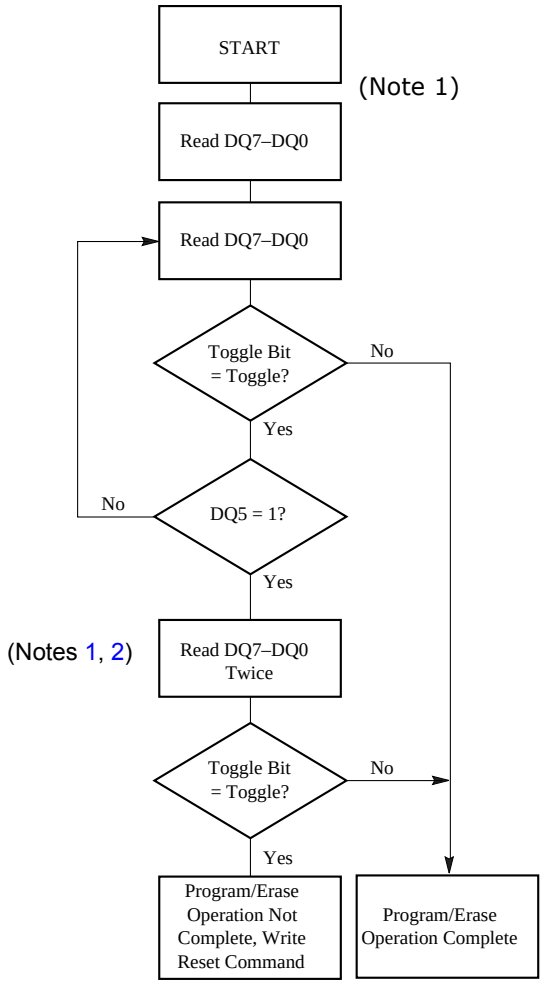
13.5 Reading Toggle Bits DQ6/DQ2

Refer to Figure 13.2 on page 33 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 13.2 on page 33).

Figure 13.2 Toggle Bit Algorithm



Notes

1. *Read toggle bit twice to determine whether or not it is toggling. See text.*
2. *Recheck toggle bit because it may stop toggling as DQ5 changes to* 1. *See text.*

13.6 DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a *1*. This is a failure condition that indicates the program or erase cycle was not successfully completed.

The DQ5 failure condition may appear if the system tries to program a *1* to a location that is previously programmed to *0*. **Only an erase operation can change a *0* back to a *1*.** Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, DQ5 produces a *1*.

Under both these conditions, the system must issue the reset command to return the device to reading array data.

13.7 DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out is complete, DQ3 switches from *0* to *1*. The system may ignore DQ3 if the system can guarantee that the time between additional sector erase commands will always be less than 50 μs. See also *Sector Erase Command Sequence* on page 26.

After the sector erase command sequence is written, the system should read the status on DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure the device has accepted the command sequence, and then read DQ3. If DQ3 is *1*, the internally controlled erase cycle has begun; all further commands (other than Erase Suspend) are ignored until the erase operation is complete. If DQ3 is *0*, the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted. Table 13.1 shows the outputs for DQ3.

Table 13.1 Write Operation Status

Operation		DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	RY/BY#
Standard Mode	Embedded Program Algorithm	DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm	0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Reading within Erase Suspended Sector	1	No toggle	0	N/A	Toggle	1
	Reading within Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend-Program	DQ7#	Toggle	0	N/A	N/A	0

Notes

1. *DQ5 switches to* 1 *when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. See DQ5: Exceeded Timing Limits on page 34 for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*

14. Flash and SRAM Operating Ranges

Temperature range

Ambient Temperature (T_A) 0°C to +70°C

V_{CC} Supply Voltages

V_{CC} for standard voltage range 3.0 V to 3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Figure 14.1 Maximum Negative Overshoot Waveform

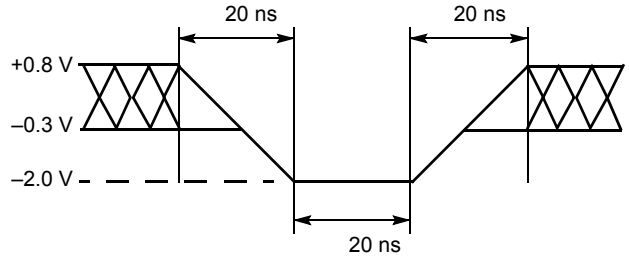
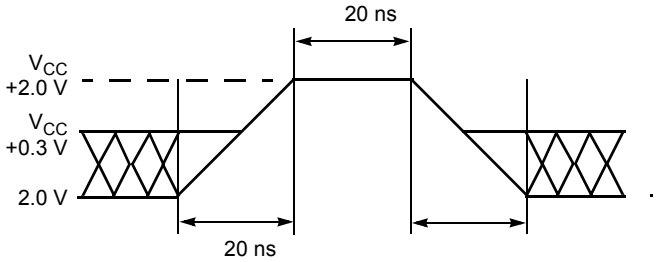


Figure 14.2 Maximum Positive Overshoot Waveform



15. DC Characteristics

15.1 Flash CMOS Compatible

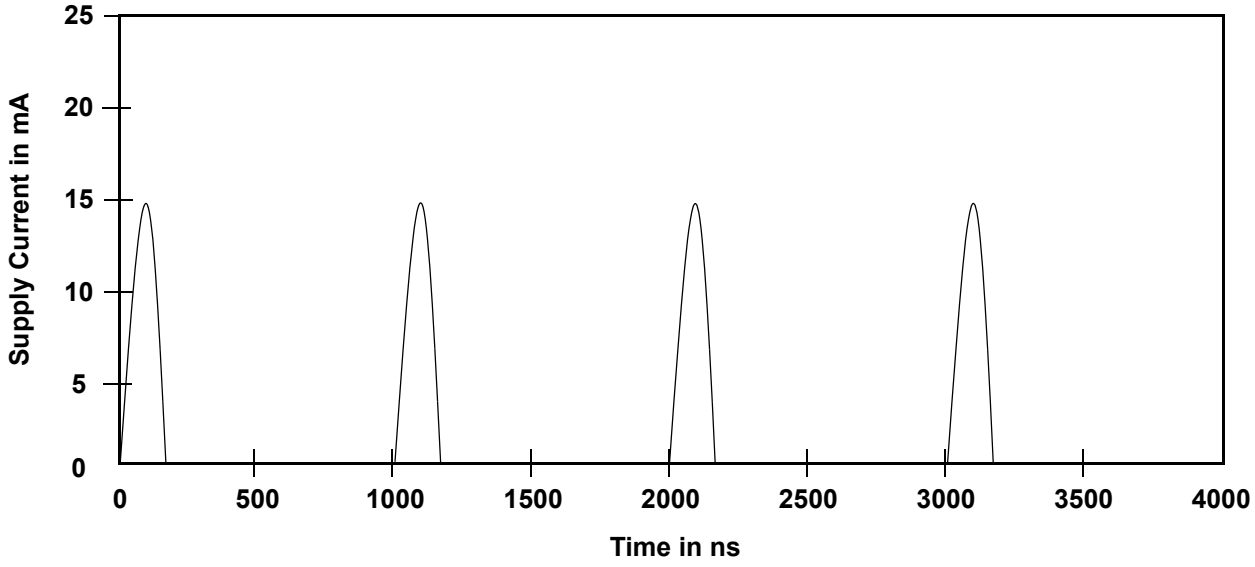
Parameter	Description	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current (Note 1)	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	
I_{CC1}	V_{CC} Active Read Current (Notes 2, 3)	FCE# = V_{IL}, FOE# = V_{IH}, Byte Mode	10 MHz		15	30	mA
			5 MHz		9	16	
			1 MHz		2	4	
		FCE# = V_{IL}, FOE# = V_{IH}, Word Mode	10 MHz		18	35	
			5 MHz		9	16	
			1 MHz		2	4	
I_{CC2}	V_{CC} Active Write Current (Notes 3, 4, 5)	FCE# = V_{IL}, FOE# = V_{IH}			20	35	mA
I_{CC3}	V_{CC} Standby Current (Note 3)	FCE#, RESET# = V_{CC}±0.3 V			0.2	5	µA
I_{CC4}	V_{CC} Standby Current During Reset (Notes 3)	RESET# = V_{SS} ± 0.3 V			0.2	5	µA
I_{CC5}	Automatic Sleep Mode (Notes 3, 6)	$V_{IH} = V_{CC}$ ± 0.3 V; $V_{IL} = V_{SS}$ ± 0.3 V			0.2	5	µA
I_{ACC}	ACC Accelerated Program Current, Word or Byte	FCE# = V_{IL}, FOE# = V_{IH}	ACC pin		5	10	mA
			V_{CC} pin		15	30	mA
V_{IL}	Input Low Voltage			–0.5		0.8	V
V_{IH}	Input High Voltage			0.7 x V_{CC}		V_{CC} + 0.3	V
V_{HH}	Voltage for WP#/ACC Sector Protect/ Unprotect and Program Acceleration	V_{CC} = 3.0 V ± 10%		11.5		12.5	V
V_{ID}	Voltage for Temporary Sector Unprotect	V_{CC} = 3.3 V		11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA, $V_{CC} = V_{CC\ min}$				0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -2.0 mA, $V_{CC} = V_{CC\ min}$		2.4			V
V_{OH2}		I_{OH} = -100 µA, $V_{CC} = V_{CC\ min}$		V_{CC}–0.4			V
V_{LKO}	Low V_{CC} Lock-Out Voltage (Note 3)			2.3		2.5	V

Notes

1. *On the ACC pin only, the maximum input load current when ACC = V_{IL} is ±5.0 µA.*
2. *The I_{CC} current listed is typically less than 2 mA/MHz, with FOE# at V_{IH}. Typical V_{CC} is 3.0 V.*
3. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CC}$max.*
4. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
5. *Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns. Typical sleep mode current is 200 nA.*
6. *Not 100% tested.*

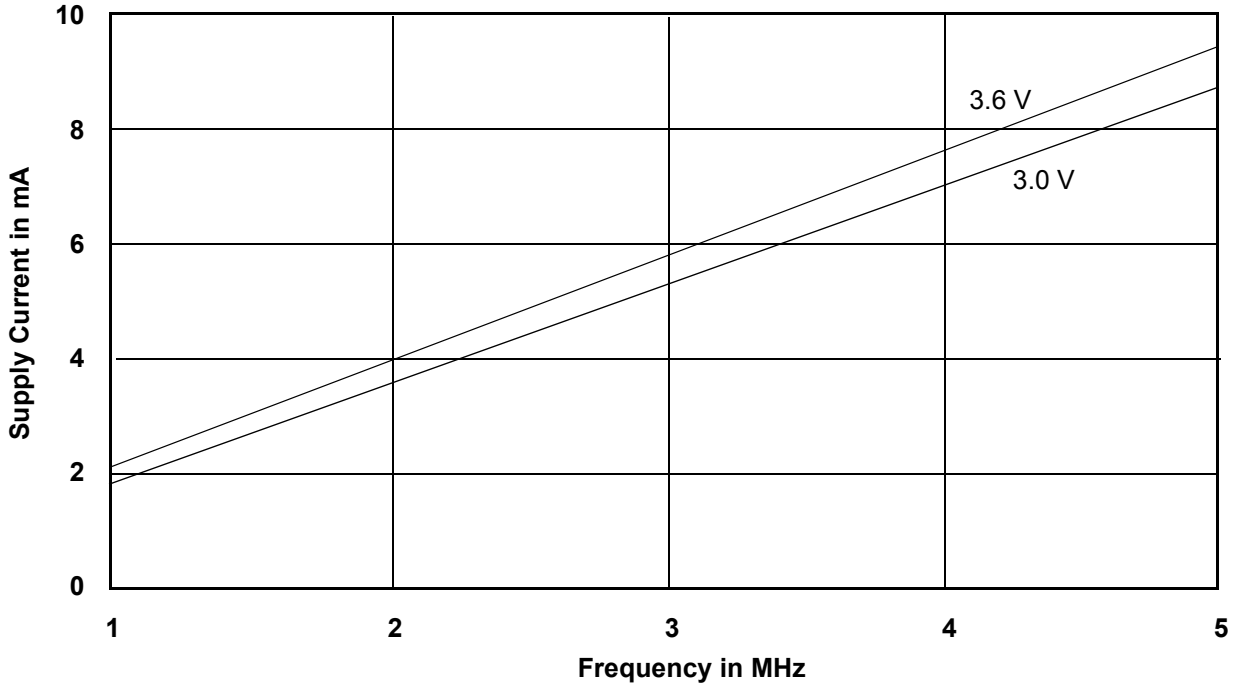
15.2 Zero Power Flash

Figure 15.1 I_{CC1} Current vs. Time (Showing Active and Automatic Sleep Currents)



Note
Addresses are switching at 1 MHz

Figure 15.2 Typical I_{CC1} vs. Frequency



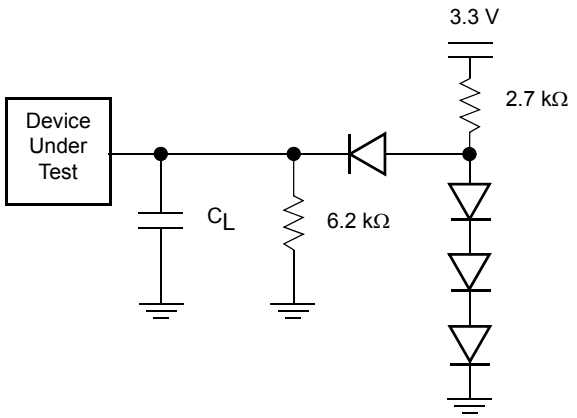
Note
T = 25 °C

15.3 SRAM CMOS Compatible

Parameter	Description	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±0.5	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, SOE# = V_{IH},Or chip disabled				±0.5	µA
I_{CC}	V_{CC} Active Read and Write Current (Notes 1, 3)	SCE1# = $V_{IL,\ F}$SCE2 = V_{IH}	70ns		10	16	mA
I_{SB}	V_{CC} Standby Current (Note 3)	SCE1# = V_{CC}±0.3 V, SCE2 = V_{SS} ± 0.3 V or SUB# = SLB# = V_{CC}±0.3 V			4	20	µA
I_{DR}	Data Retention Current	SCE1# = V_{CC}±0.3 V, SCE2 = V_{SS} ± 0.3 V or SUB# = SLB# = V_{CC}±0.3 V	Vcc = 1.8V		2	10	V
V_{IL}	Input Low Voltage			–0.3		0.6	V
V_{IH}	Input High Voltage			0.7 x V_{CC}		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 0.2 mA, $V_{CC} = V_{CC\ min}$				0.2	V
V_{OH}	Output High Voltage	I_{OH} = -0.2 mA, $V_{CC} = V_{CC\ min}$		V_{CC}–0.2			V

16. Test Conditions

Figure 16.1 Test Setup



Note
Diodes are IN3064 or equivalent.

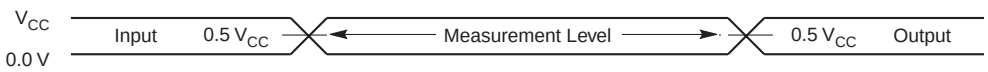
Table 16.1 Test Specifications

Test Condition		Unit
Output Load	1 TTL gate	
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	5	ns
Input Pulse Levels	0.0 or V_{CC}	V
Input timing measurement reference levels	0.5 V_{CC}	
Output timing measurement reference levels	0.5 V_{CC}	

17. Key to Switching Waveforms

Waveform	Inputs	Outputs
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

Figure 17.1 Input Waveforms and Measurement Levels



18. Flash AC Characteristics

For the Timing Diagrams, within the Flash AC Characteristics section, all control signal names refer to the Flash control signals. (i.e. CE# = FCE#, OE# = FOE# and WE# = FWE#)

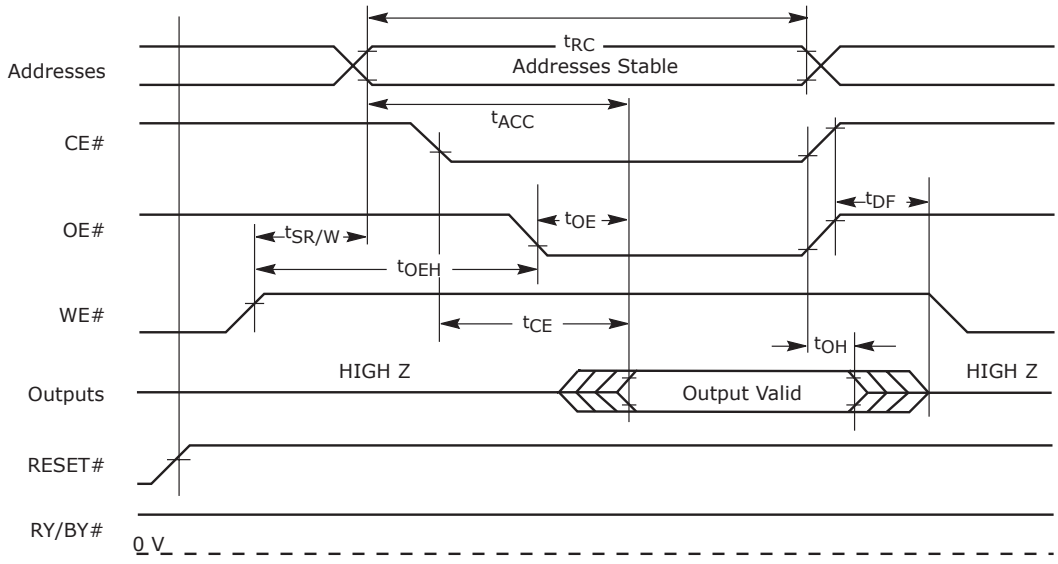
18.1 Read Operations

Parameter		Description		Test Setup		Value	Unit
JEDEC	Std						
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	90	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		FCE# = V_{IL} FOE# = V_{IL}	Max	90	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		FOE# = V_{IL}	Max	90	
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	35	
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1)			Max	16	
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 1)			Max	16	
	$t_{SR/W}$	Latency Between Read and Write Operations			Min	20	
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0	
			Toggle and Data# Polling		Min	10	
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, FCE# or FOE#, Whichever Occurs First (Note 1)			Min	0	

Notes

1. *Not 100% tested.*
2. *See Figure 16.1 on page 39 and Table 16.1 on page 39 for test specifications.*

Figure 18.1 Read Operations Timings

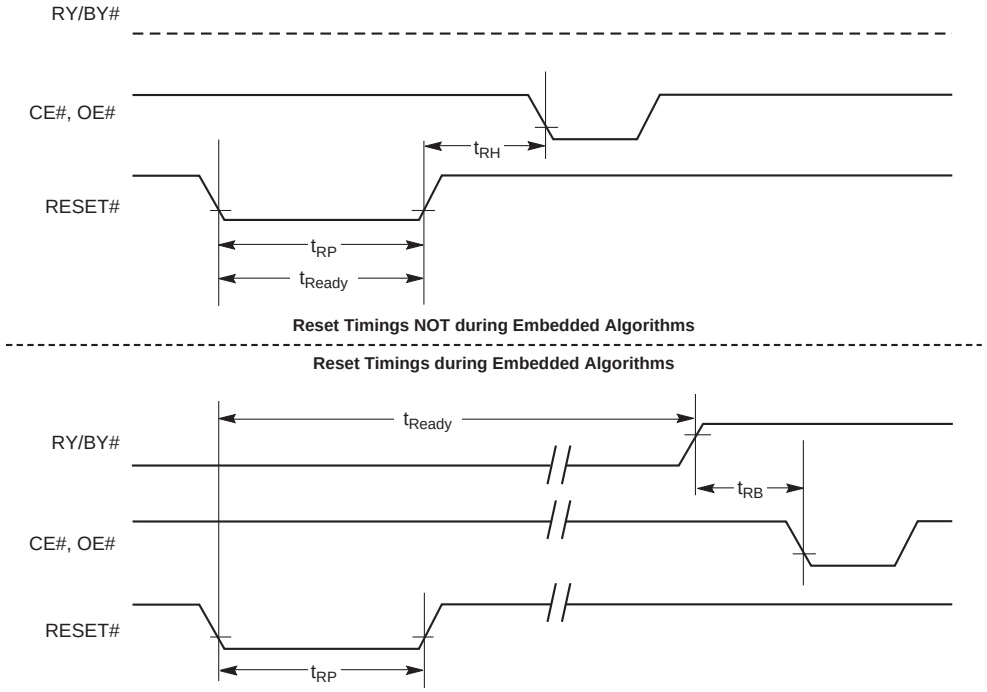


18.2 Hardware Reset (RESET#)

Parameter		Description	Test Setup	Value	Unit
JEDEC	Std				
	t_{READY}	RESET# Pin Low (During Embedded Algorithms) to Read or Write (See Note)	Max	20	µs
	t_{READY}	RESET# Pin Low (NOT During Embedded Algorithms) to Read or Write (See Note)	Max	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	RESET# High Time Before Read (See Note)		50	ns
	t_{RPD}	RESET# Low to Standby Mode		20	µs
	t_{RB}	RY/BY# Recovery Time		0	ns

Note
Not 100% tested.

Figure 18.2 RESET# Timings



18.3 Word/Byte Configuration (BYTE#)

Parameter		Description		Value	Unit
JEDEC	Std				
	t_{ELFL}/t_{ELFH}	FCE# to BYTE# Switching Low or High	Max	5	ns
	t_{FLQZ}	BYTE# Switching Low to Output HIGH Z	Max	16	
	t_{FHQV}	BYTE# Switching High to Output Active	Min	90	

Figure 18.3 BYTE# Timings for Read Operations

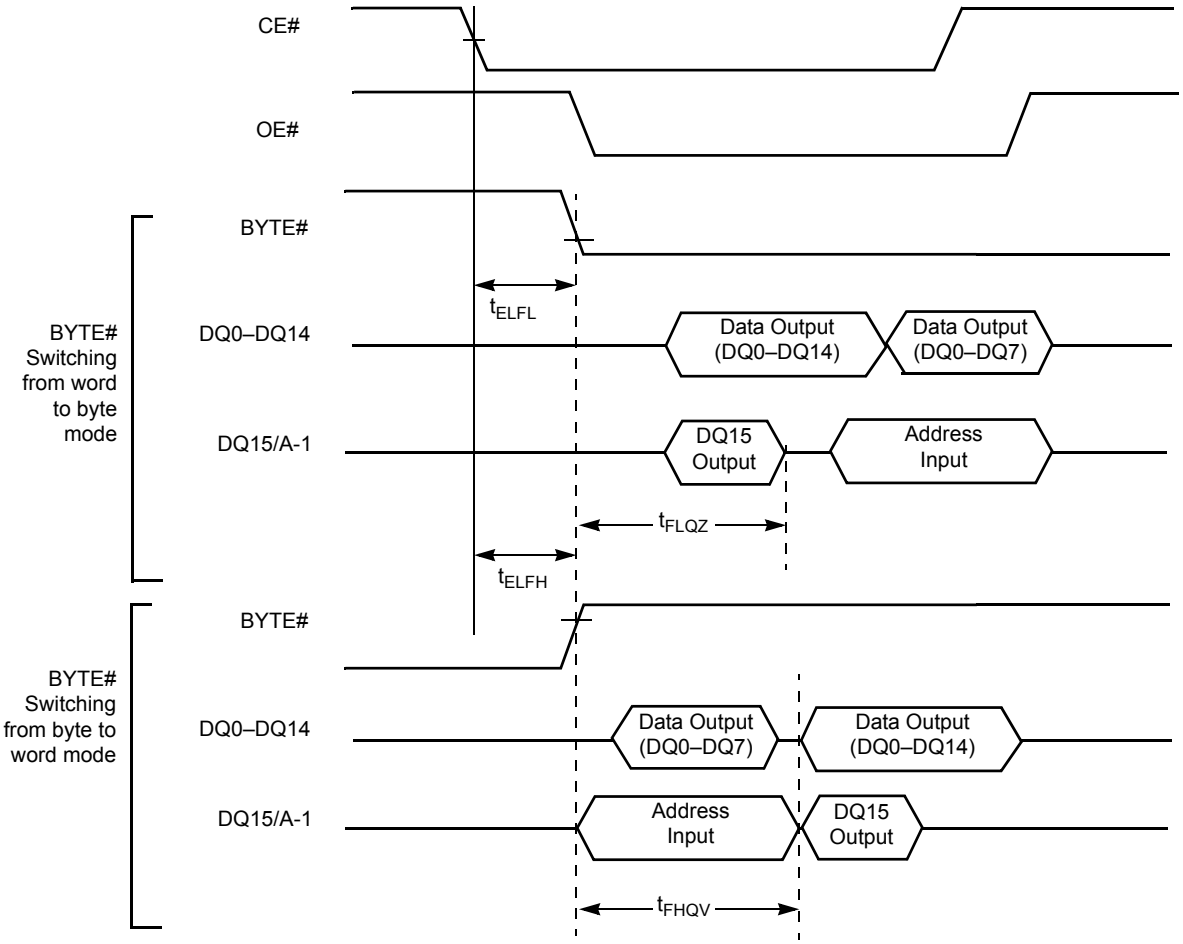
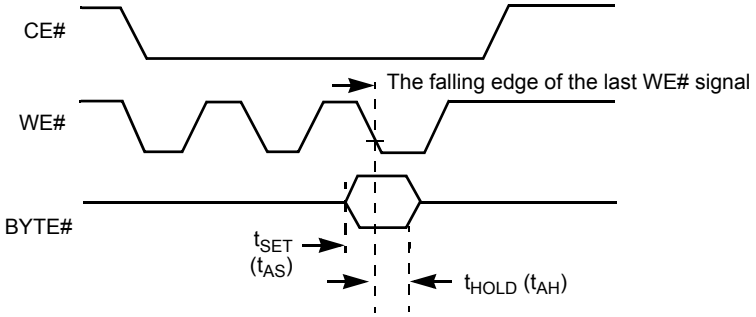


Figure 18.4 BYTE# Timings for Write Operations



Note
Refer to the Erase/Program Operations table for t_{AS} and t_{AH} specifications.

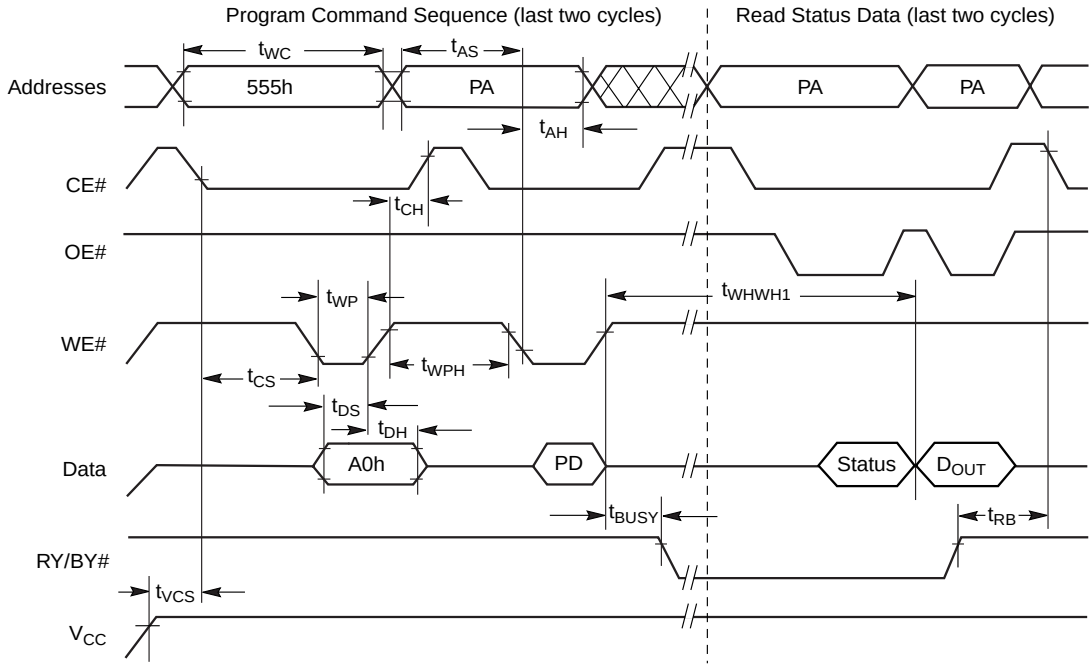
18.4 Erase/Program Operations

Parameter		Description			Value	Unit
JEDEC	Std					
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	90	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0	
t_{WLAX}	t_{AH}	Address Hold Time		Min	45	
t_{DVWH}	t_{DS}	Data Setup Time		Min	45	
t_{WHDX}	t_{DH}	Data Hold Time		Min	0	
	t_{OES}	Output Enable Setup Time		Min	0	
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (FOE# High to FWE# Low)		Min	0	
t_{ELWL}	t_{CS}	FCE# Setup Time		Min	0	
t_{WHEH}	t_{CH}	FCE# Hold Time		Min	0	
t_{WLWH}	t_{WP}	Write Pulse Width		Min	35	
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min	30	
	$t_{SR/W}$	Latency Between Read and Write Operations		Min	20	
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Byte	Typ	9	µs
			Word	Typ	11	
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation, Word or Byte (Note 2)		Typ	7	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)			0.7	sec
	t_{VCS}	V_{CC} Setup Time (Note 1)		Min	50	µs
	t_{RB}	Recovery Time from RY/BY#			0	ns
	t_{BUSY}	Program/Erase Valid to RY/BY# Delay		Max	90	

Notes

1. *Not 100% tested.*
2. *See Erase and Programming Performance on page 50 for more information.*

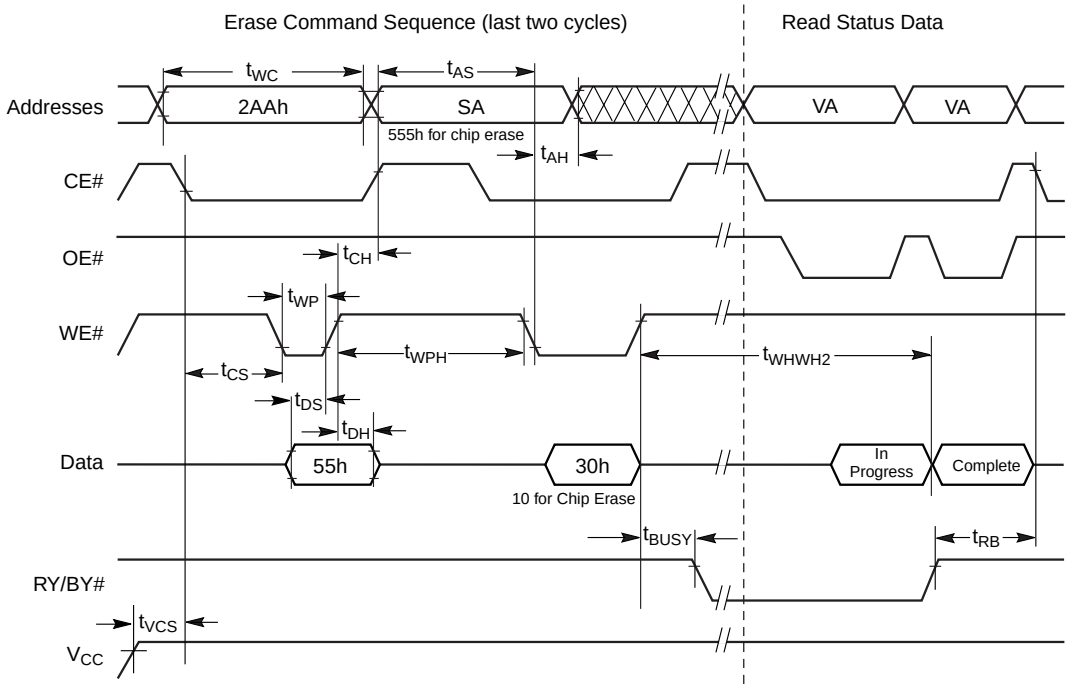
Figure 18.5 Program Operation Timings



Notes

1. *PA = program address, PD = program data, D_{OUT} is the true data at the program address.*
2. *Illustration shows device in word mode.*

Figure 18.6 Chip/Sector Erase Operation Timings



Notes

1. *SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see Flash Write Operation Status on page 30).*
2. *Illustration shows device in word mode.*

Figure 18.7 Back to Back Read/Write Cycle Timing

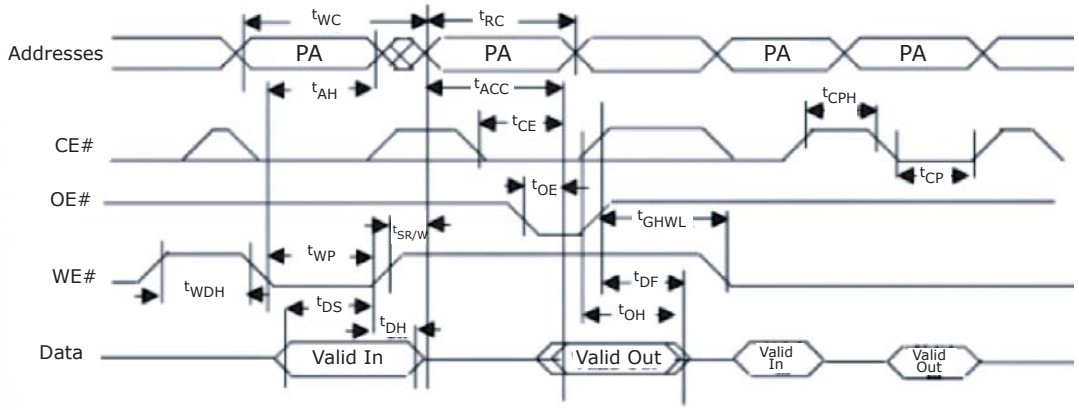
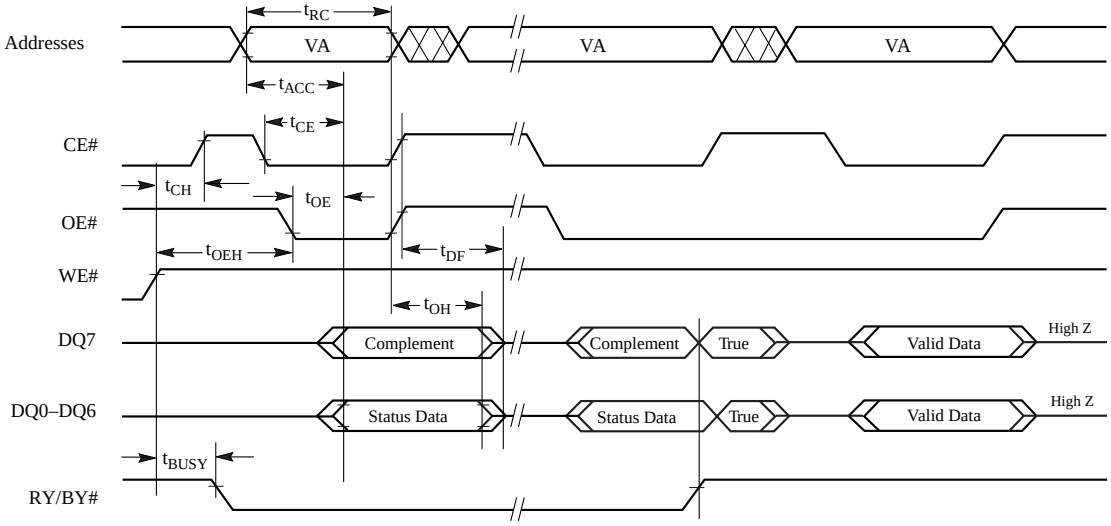


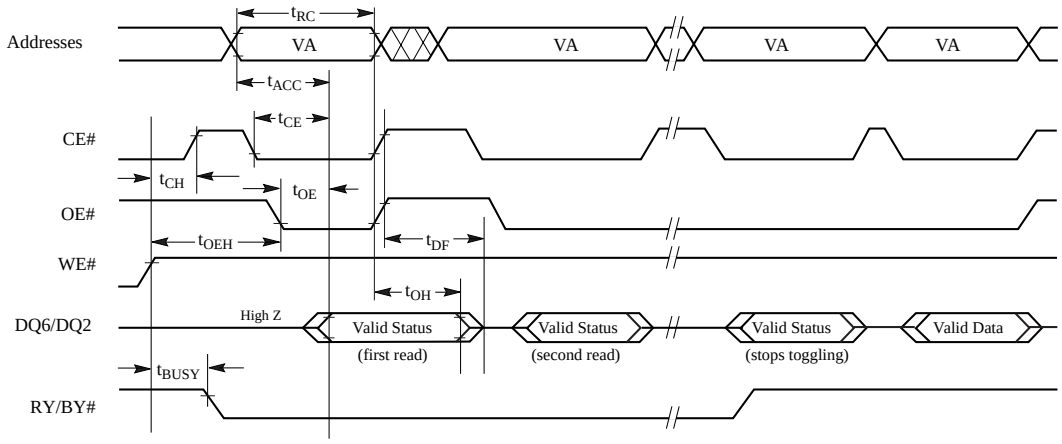
Figure 18.8 Data# Polling Timings (During Embedded Algorithms)



Note

VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.

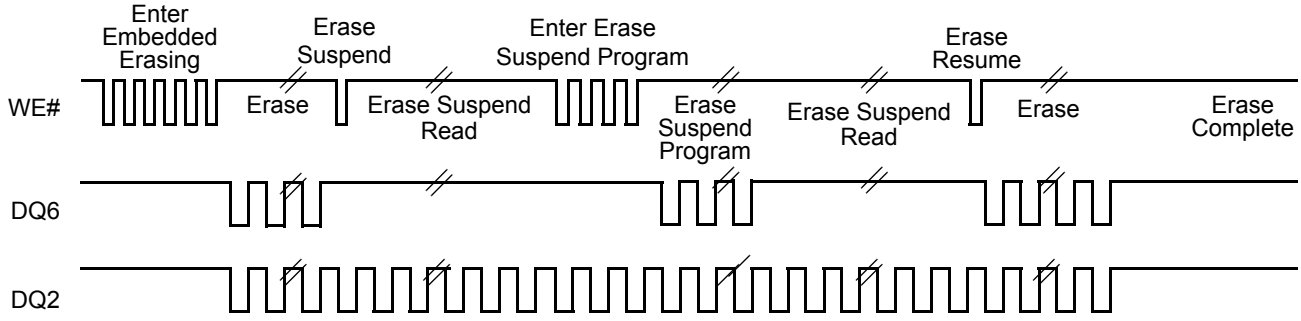
Figure 18.9 Toggle Bit Timings (During Embedded Algorithms)



Note

VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

Figure 18.10 DQ2 vs. DQ6 for Erase and Erase Suspend Operations



Note

The system may use CE# or OE# to toggle DQ2 and DQ6. DQ2 toggles only when read at an address within an erase-suspended sector.

18.5 Temporary Sector Unprotect

Parameter		Description		Value	Unit
JEDEC	Std				
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs

Note
Not 100% tested.

Figure 18.11 Temporary Sector Unprotect Timing Diagram

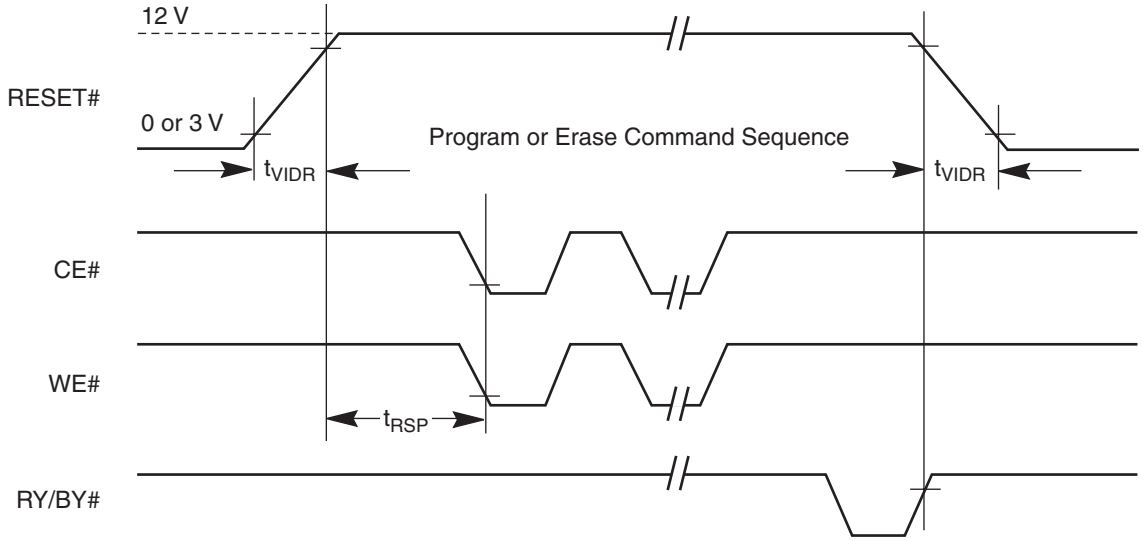


Figure 18.12 Accelerated Program Timing Diagram

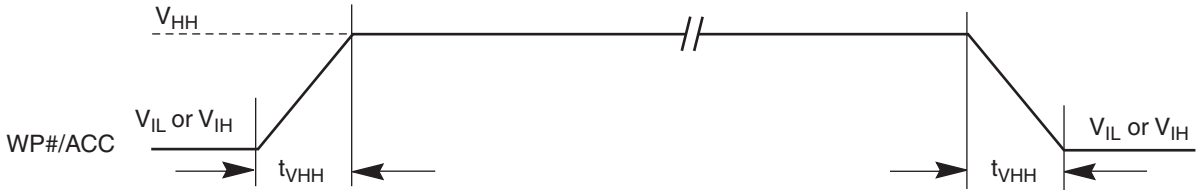
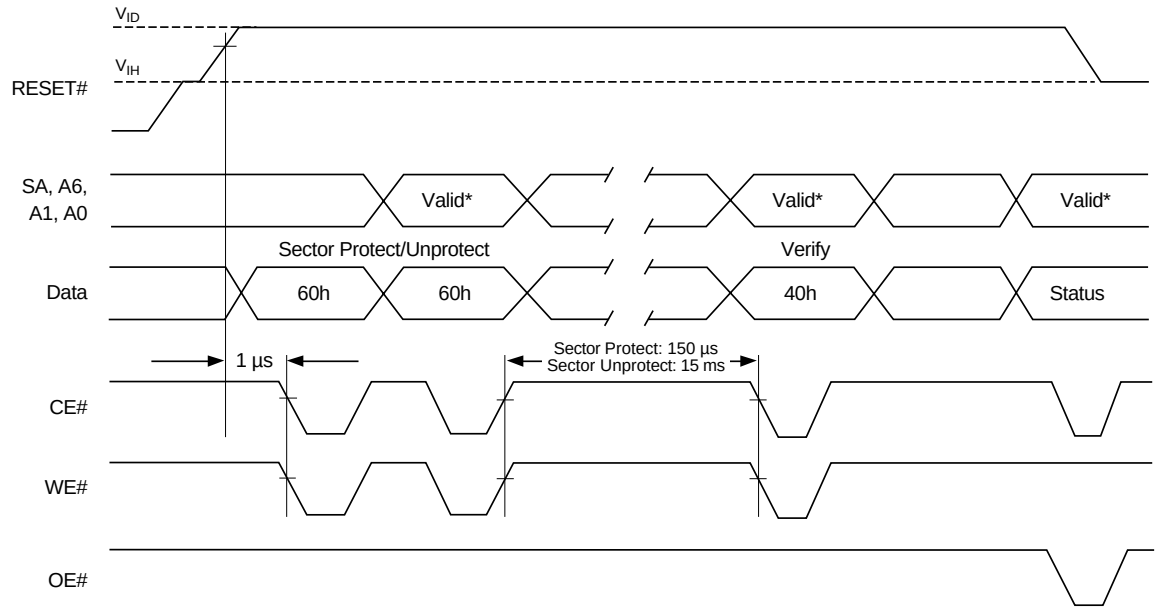


Figure 18.13 Sector Protect/Unprotect Timing Diagram



Note
For sector protect, A6 = 0, A1 = 1, A0 = 0. For sector unprotect, A6 = 1, A1 = 1, A0 = 0.

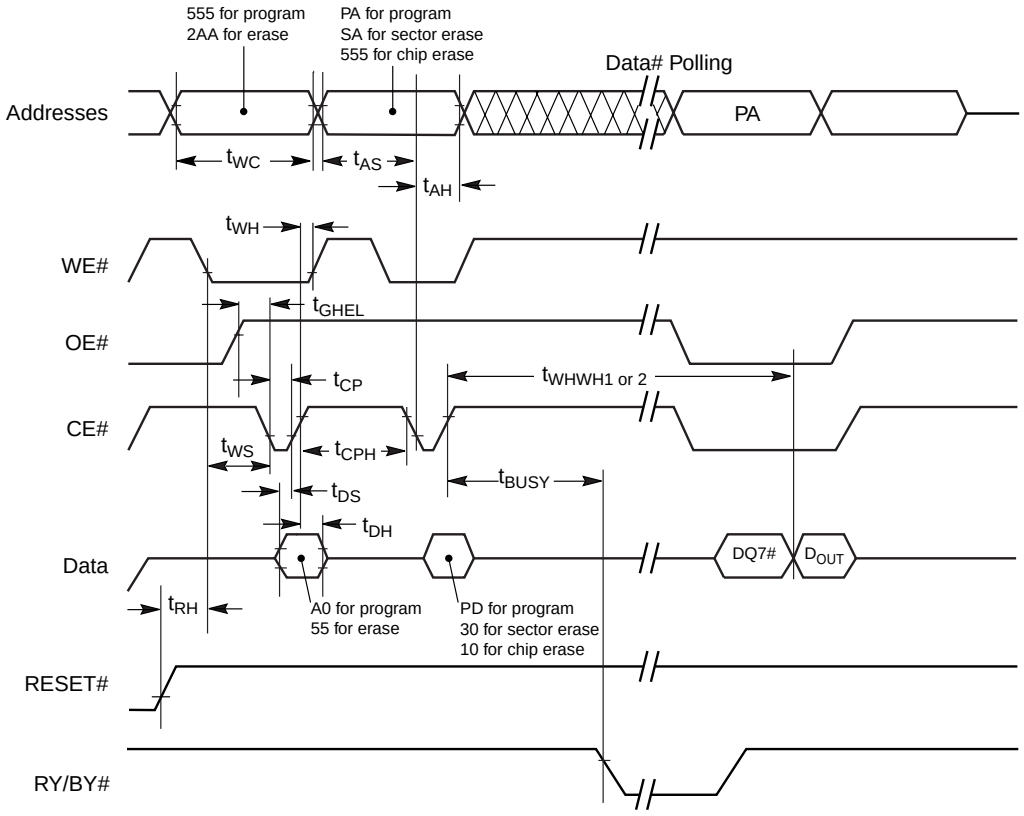
18.6 Alternate FCE# Controlled Erase/Program Operations

Parameter						
JEDEC	Std	Description			Value	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	90	ns
t_{AVEL}	t_{AS}	Address Setup Time		Min	0	ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	45	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	45	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0	ns
	t_{OES}	Output Enable Setup Time		Min	0	ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (FOE# High to FWE# Low)		Min	0	ns
t_{WLEL}	t_{WS}	FWE# Setup Time		Min	0	ns
t_{EHWH}	t_{WH}	FWE# Hold Time		Min	0	ns
t_{ELEH}	t_{CP}	FCE# Pulse Width		Min	35	ns
t_{EHEL}	t_{CPH}	FCE# Pulse Width High		Min	30	ns
	$t_{SR/W}$	Latency Between Read and Write Operations		Min	20	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Byte	Typ	9	µs
			Word	Typ	11	
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation, Word or Byte (Note 2)		Typ	7	
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	0.7	sec

Notes

1. *Not 100% tested.*
2. *See Erase and Programming Performance on page 50 for more information.*

Figure 18.14 Alternate CE# Controlled Write Operation Timings



Notes

1. *PA = program address, PD = program data, DQ7# = complement of the data written to the device, D_{OUT} = data written to the device.*
2. *Figure indicates the last two bus cycles of the command sequence.*
3. *Word mode address used as an example.*

19. Erase and Programming Performance

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time		0.7	10	s	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time		45		s	
Byte Programming Time		9	300	µs	Excludes system level overhead (Note 5)
Word Programming Time		11	360	µs	
Accelerated Byte/Word Programming Time		7	210	µs	
Chip Programming Time (Note 3)	Byte Mode	36	108	s	
	Word Mode	24	72	s	

Notes

1. *Typical program and erase times assume the following conditions: 25°C, V_{CC} = 3.0 V, 100,000 cycles, checkerboard data pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 3.0 V, 1,000,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 12.1 on page 31 for further information on command definitions.*
6. *The device has a minimum erase and program cycle endurance of 100,000 cycles per sector.*

20. SRAM AC Characteristics

20.1 Read Operations

Parameter	Symbol	Min	Max	Units
Read Cycle Time	t_{RC}	70		ns
Address Access Time	t_{AA}		70	
Chip Enable to Valid Output	t_{CE}		70	
Output Enable to Valid Output	t_{OE}		25	
Byte Select to Valid Output	t_{LB}, t_{UB}		70	
Chip Enable to Low-Z Output	t_{LZ}	10		
Output Enable to Low-Z Output	t_{OLZ}	5		
Byte Select to Low-Z Output	t_{BZ}	10		
Chip Enable to Output High Z Output (Note 1)	t_{HZ}	0	20	
Output Enable to Output High Z Output (Note 1)	t_{OHZ}	0	20	
Byte Select to Output High Z Output (Note 1)	t_{BHZ}	0	20	
Output Hold from Address Change	t_{OEH}	10		

Notes
1. Not 100% tested.

Figure 20.1 Read Operation Timings (Address Control)

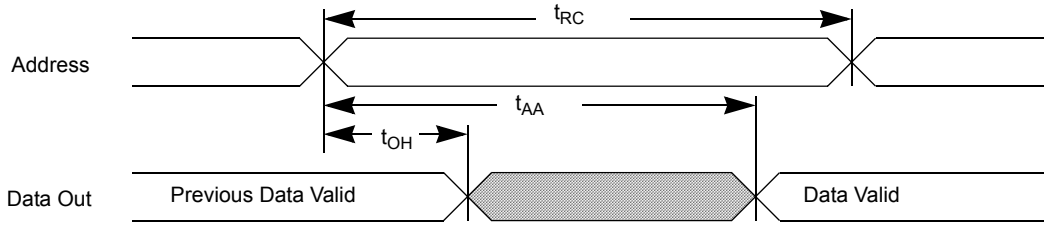
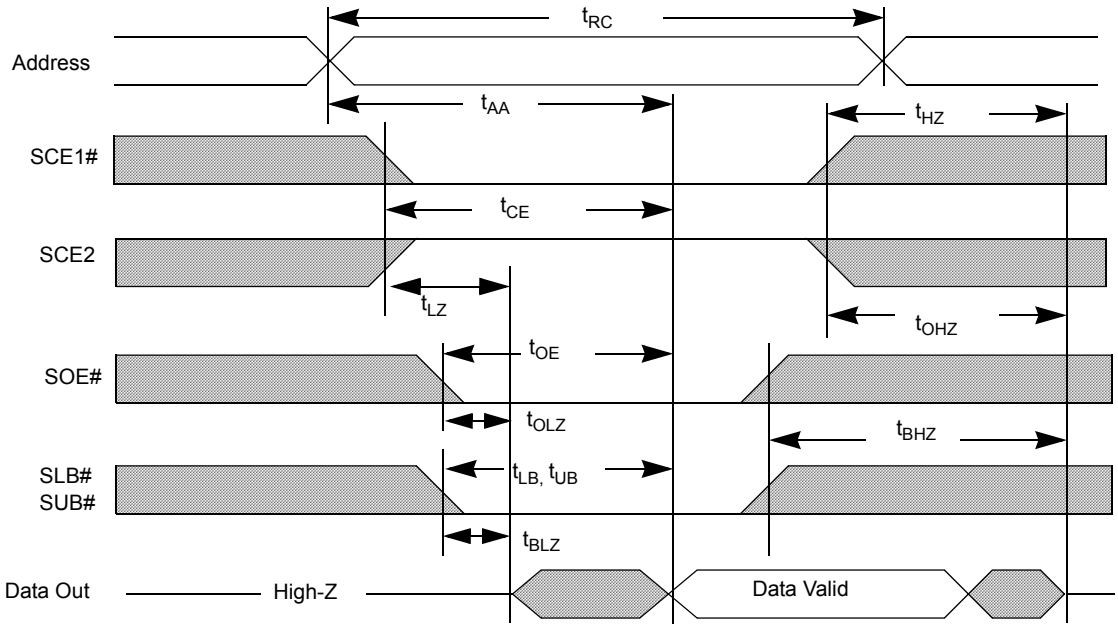


Figure 20.2 Read Operation Timings



20.2 Write Operations

Parameter	Symbol	Min	Max	Units
Write Cycle Time	t_{WC}	70		ns
Chip Enable to End of Write	t_{CW}	50		
Address Valid to End of Write	t_{AW}	50		
Byte Select to End of Write	t_{BW}	50		
Write Pulse Width	t_{WP}	40		
Address Setup Time	t_{AS}	0		
Write Recovery Time	t_{WR}	0		
Write to High-Z Output	t_{WHZ}		20	
Data to Write Time Overlap	t_{DW}	40		
Data Hold from Write Time	t_{DH}	0		
End Write to Low-Z Output	t_{OW}	5		

Figure 20.3 Write Operation Timings (WE# Control)

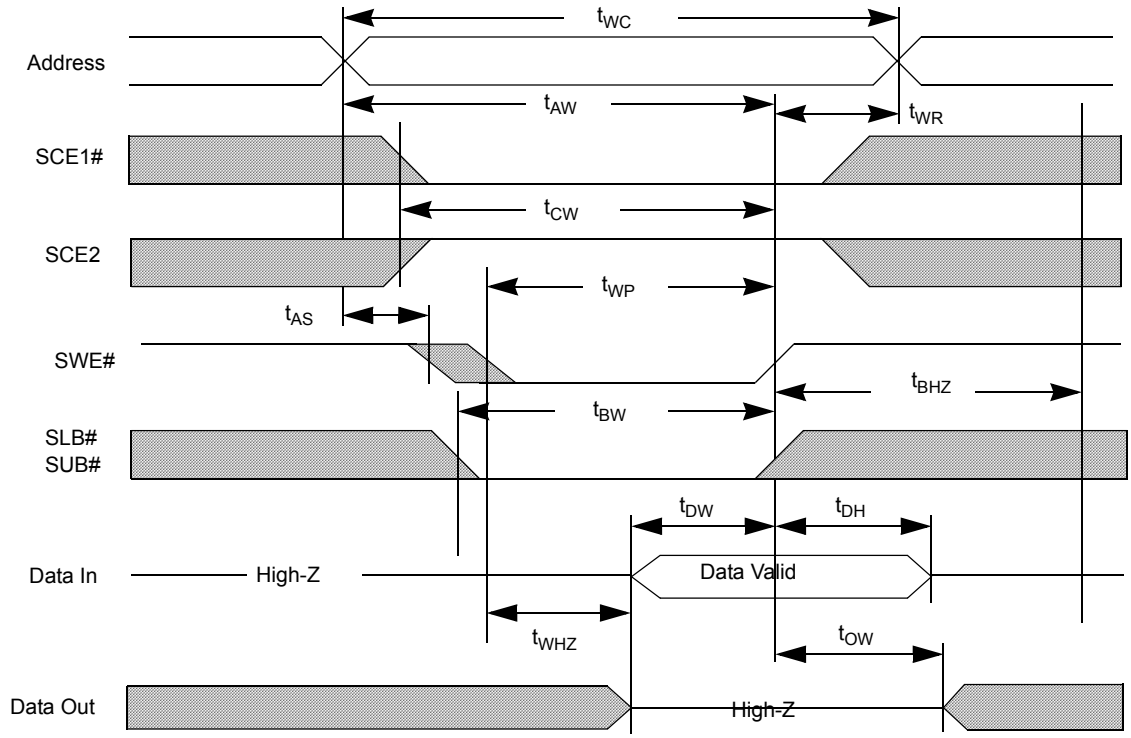
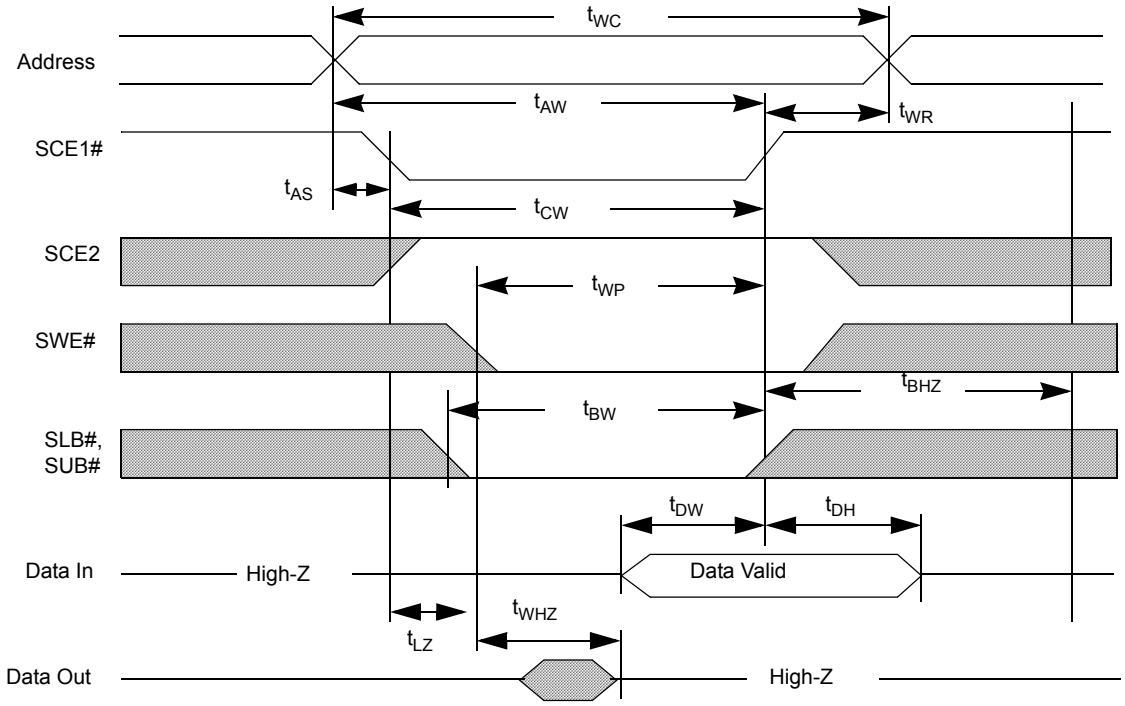


Figure 20.4 Write Operation Timings (CE1# Control)



21. BGA Pin Capacitance

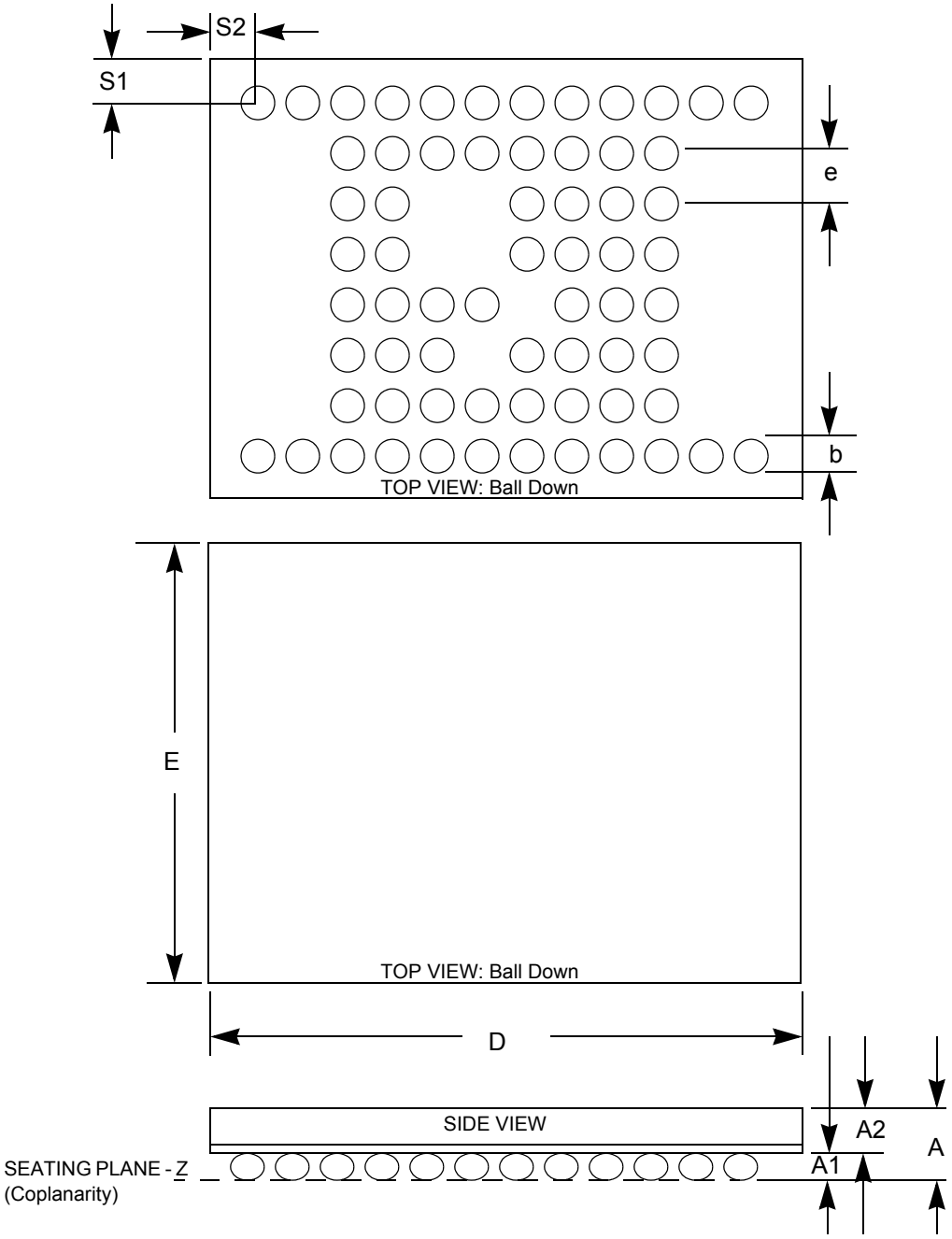
Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	8	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	12	16	pF

Notes

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

22. Physical Dimensions

Figure 22.1 66-Ball Fine-Pitch Ball Grid Array (FBGA) 12 mm x 8 mm



		Min	Nom	Max			Min	Nom	Max
Package height	A	1.20	1.30	1.40	Body width	E	7.90	8.00	8.10
Solder ball height	A1	0.30	0.35	0.40	Ball pitch	e		0.80	
Package body thickness	A2	0.92	0.97	1.02	Seating plane coplanarity	Z			0.10
Ball lead diameter	b	0.325	0.40	0.475	Corner to first bump distance	S1	1.10	1.20	1.30
Body length	D	11.90	12.00	12.10	Corner to first bump distance	S2	1.50	1.60	1.70

23. Revision Summary

23.1 Revision A (June 11, 2007)

Initial Release

23.2 Revision B (June 13, 2007)

Flash speed = 90ns

23.3 Revision C (June 19, 2007)

Added A21 for 64Mb flash expansion and fixed A19 ball definition

23.4 Revision D (July 24, 2007)

Added Green package option

23.5 Revision E (August 10, 2007)

Corrected part number and removed top boot option from order table

23.6 Revision F (January 7, 2007)

Changed part number for unique device

23.7 Revision G (June 10, 2008)

Modified Figure 22.1 to specify package view as TOP view.