

# CD4018B Types

## CMOS Presettable Divide-By-'N' Counter

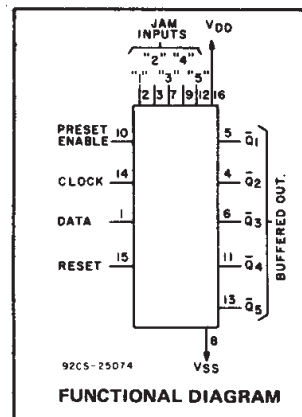
### High-Voltage Types (20-Volt Rating)

■ CD4018B types consist of 5 Johnson-Counter stages, buffered Q outputs from each stage, and counter preset control gating. CLOCK, RESET, DATA, PRESET ENABLE, and 5 individual JAM inputs are provided. Divide by 10, 8, 6, 4, or 2 counter configurations can be implemented by feeding the  $\bar{Q}_5$ ,  $\bar{Q}_4$ ,  $\bar{Q}_3$ ,  $\bar{Q}_2$ ,  $\bar{Q}_1$  signals, respectively, back to the DATA input. Divide-by-9, 7, 5; or 3 counter configurations can be implemented by the use of a CD4011B to gate the feedback connection to the DATA input. Divide-by functions greater than 10 can be achieved by use of multiple CD4018B units. The counter is advanced one count at the positive clock-signal transition. Schmitt Trigger action on the clock line permits unlimited clock rise and fall times. A high RESET signal clears the counter to an all-zero condition. A high PRESET-ENABLE signal allows information on the JAM inputs to preset the counter. Anti-lock gating is provided to assure the proper counting sequence.

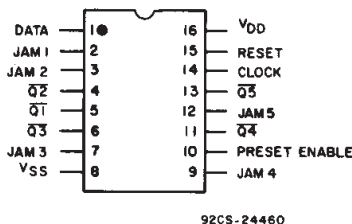
The CD4018B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

### Features:

- Medium speed operation . . . . . 10 MHz (typ.) at  $V_{DD} - V_{SS} = 10\text{ V}$
- Fully static operation
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of  $1\text{ }\mu\text{A}$  at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =  $1\text{ V}$  at  $V_{DD} = 5\text{ V}$   
 $2\text{ V}$  at  $V_{DD} = 10\text{ V}$   
 $2.5\text{ V}$  at  $V_{DD} = 15\text{ V}$
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"



**TERMINAL DIAGRAM  
Top View**



### Applications:

- Fixed and programmable divide-by-10, 9, 8, 7, 6, 5, 4, 3, 2 counters
- Fixed and programmable counters greater than 10
- Programmable decade counters
- Divide-by-"N" counters/frequency synthesizers
- Frequency division
- Counter control/timers

### MAXIMUM RATINGS, Absolute-Maximum Values:

#### DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )

Voltages referenced to  $V_{SS}$  Terminal) . . . . . -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5V to  $V_{DD} + 0.5\text{ V}$

DC INPUT CURRENT, ANY ONE INPUT . . . . .  $\pm 10\text{ mA}$

#### POWER DISSIPATION PER PACKAGE ( $P_D$ ):

For  $T_A = -55^\circ\text{C}$  to  $+100^\circ\text{C}$  . . . . . 500mW

For  $T_A = +100^\circ\text{C}$  to  $+125^\circ\text{C}$  . . . . . Derate Linearly at 12mW/°C to 200mW

#### DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR  $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$  . . . . . 100mW

OPERATING-TEMPERATURE RANGE ( $T_A$ ) . . . . .  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$

STORAGE TEMPERATURE RANGE ( $T_{stg}$ ) . . . . .  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$

#### LEAD TEMPERATURE (DURING SOLDERING):

At distance  $1/16 \pm 1/32$  inch ( $1.59 \pm 0.79\text{ mm}$ ) from case for 10s max . . . . .  $+265^\circ\text{C}$

## CD4018B Types

**RECOMMENDED OPERATING CONDITIONS** at  $T_A = 25^\circ\text{C}$ , Unless Otherwise Specified  
 For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

| CHARACTERISTIC                                                           | $V_{DD}$      | Min.            | Max.          | UNITS         |
|--------------------------------------------------------------------------|---------------|-----------------|---------------|---------------|
| Supply Voltage Range (at $T_A = \text{Full Package-Temperature Range}$ ) |               | 3               | 18            | V             |
| Clock Input Frequency, $f_{CL}$                                          | 5<br>10<br>15 | —<br>—<br>—     | 3<br>7<br>8.5 | MHz           |
| Clock Pulse Width, $t_W$                                                 | 5<br>10<br>15 | 160<br>70<br>50 | —<br>—<br>—   | ns            |
| Clock Rise & Fall Time, $t_{rCL}, t_{fCL}$                               | 5<br>10<br>15 | Unlimited       |               | $\mu\text{s}$ |
| Data Input Set-Up Time, $t_S$                                            | 5<br>10<br>15 | 40<br>12<br>16  | —<br>—<br>—   | ns            |
| Data Input Hold Time, $t_H$                                              | 5<br>10<br>15 | 140<br>80<br>60 | —<br>—<br>—   | ns            |
| Preset or Reset Pulse Width, $t_W$                                       | 5<br>10<br>15 | 160<br>70<br>50 | —<br>—<br>—   | ns            |
| Preset or Reset Removal Time                                             | 5<br>10<br>15 | 160<br>60<br>40 | —<br>—<br>—   | ns            |

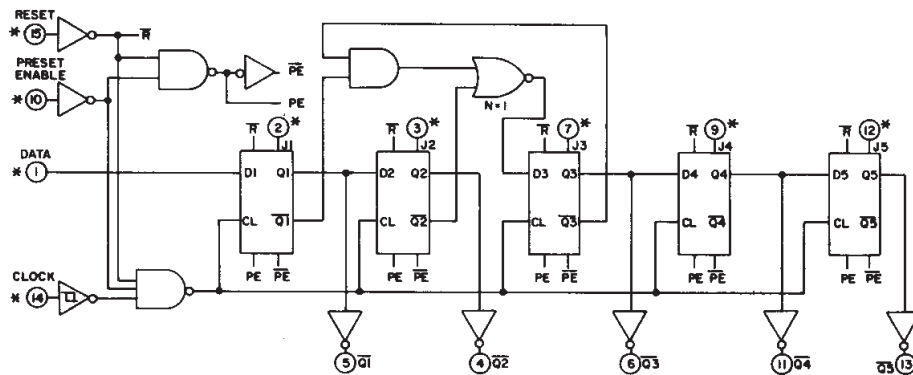


Fig. 1 — Logic diagram.

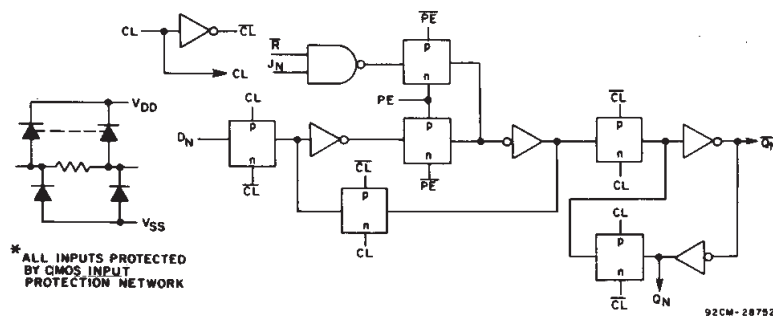


Fig. 2 — Detail of a typical stage.

# CD4018B Types

## STATIC ELECTRICAL CHARACTERISTICS

| CHARAC-<br>TERISTIC                                         | CONDITIONS            |                        |                        | LIMITS AT INDICATED TEMPERATURES (°C) |       |       |       |       |                   |      | UNITS |
|-------------------------------------------------------------|-----------------------|------------------------|------------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
|                                                             | V <sub>O</sub><br>(V) | V <sub>IN</sub><br>(V) | V <sub>DD</sub><br>(V) | -55                                   | -40   | +85   | +125  | +25   |                   |      |       |
|                                                             |                       |                        |                        |                                       |       |       |       | Min.  | Typ.              | Max. |       |
| Quiescent<br>Device<br>Current,<br>I <sub>DD</sub> Max.     | —                     | 0,5                    | 5                      | 5                                     | 5     | 150   | 150   | —     | 0.04              | 5    | μA    |
|                                                             | —                     | 0,10                   | 10                     | 10                                    | 10    | 300   | 300   | —     | 0.04              | 10   |       |
|                                                             | —                     | 0,15                   | 15                     | 20                                    | 20    | 600   | 600   | —     | 0.04              | 20   |       |
|                                                             | —                     | 0,20                   | 20                     | 100                                   | 100   | 3000  | 3000  | —     | 0.08              | 100  |       |
| Output Low<br>(Sink) Current<br>I <sub>OL</sub> Min.        | 0.4                   | 0,5                    | 5                      | 0.64                                  | 0.61  | 0.42  | 0.36  | 0.51  | 1                 | —    | mA    |
|                                                             | 0.5                   | 0,10                   | 10                     | 1.6                                   | 1.5   | 1.1   | 0.9   | 1.3   | 2.6               | —    |       |
|                                                             | 1.5                   | 0,15                   | 15                     | 4.2                                   | 4     | 2.8   | 2.4   | 3.4   | 6.8               | —    |       |
| Output High<br>(Source)<br>Current,<br>I <sub>OH</sub> Min. | 4.6                   | 0,5                    | 5                      | -0.64                                 | -0.61 | -0.42 | -0.36 | -0.51 | -1                | —    | mA    |
|                                                             | 2.5                   | 0,5                    | 5                      | -2                                    | -1.8  | -1.3  | -1.15 | -1.6  | -3.2              | —    |       |
|                                                             | 9.5                   | 0,10                   | 10                     | -1.6                                  | -1.5  | -1.1  | -0.9  | -1.3  | -2.6              | —    |       |
|                                                             | 13.5                  | 0,15                   | 15                     | -4.2                                  | -4    | -2.8  | -2.4  | -3.4  | -6.8              | —    |       |
| Output Voltage:<br>Low-Level,<br>V <sub>OL</sub> Max.       | —                     | 0,5                    | 5                      | 0.05                                  |       |       |       | —     | 0                 | 0.05 | V     |
|                                                             | —                     | 0,10                   | 10                     | 0.05                                  |       |       |       | —     | 0                 | 0.05 |       |
|                                                             | —                     | 0,15                   | 15                     | 0.05                                  |       |       |       | —     | 0                 | 0.05 |       |
| Output<br>Voltage:<br>High-Level,<br>V <sub>OH</sub> Min.   | —                     | 0,5                    | 5                      | 4.95                                  |       |       |       | 4.95  | 5                 | —    | V     |
|                                                             | —                     | 0,10                   | 10                     | 9.95                                  |       |       |       | 9.95  | 10                | —    |       |
|                                                             | —                     | 0,15                   | 15                     | 14.95                                 |       |       |       | 14.95 | 15                | —    |       |
| Input Low<br>Voltage<br>V <sub>IL</sub> Max.                | 0.5,4.5               | —                      | 5                      | 1.5                                   |       |       |       | —     | —                 | 1.5  | V     |
|                                                             | 1,9                   | —                      | 10                     | 3                                     |       |       |       | —     | —                 | 3    |       |
|                                                             | 1.5,13.5              | —                      | 15                     | 4                                     |       |       |       | —     | —                 | 4    |       |
| Input High<br>Voltage,<br>V <sub>IH</sub> Min.              | 0.5,4.5               | —                      | 5                      | 3.5                                   |       |       |       | 3.5   | —                 | —    | V     |
|                                                             | 1,9                   | —                      | 10                     | 7                                     |       |       |       | 7     | —                 | —    |       |
|                                                             | 1.5,13.5              | —                      | 15                     | 11                                    |       |       |       | 11    | —                 | —    |       |
| Input Current<br>I <sub>IN</sub> Max.                       | —                     | 0,18                   | 18                     | ±0.1                                  | ±0.1  | ±1    | ±1    | —     | ±10 <sup>-5</sup> | ±0.1 | μA    |

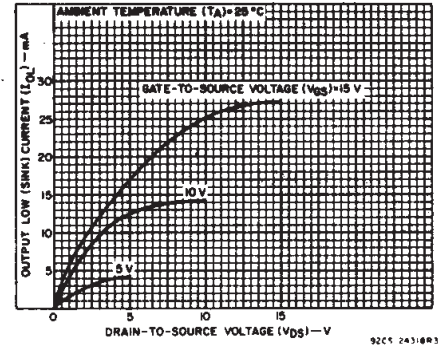


Fig. 3 - Typical output low (sink) current characteristics.

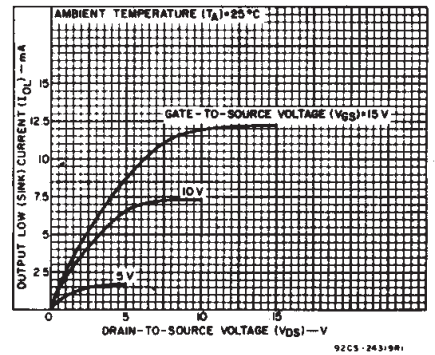


Fig. 4 - Minimum output low (sink) current characteristics.

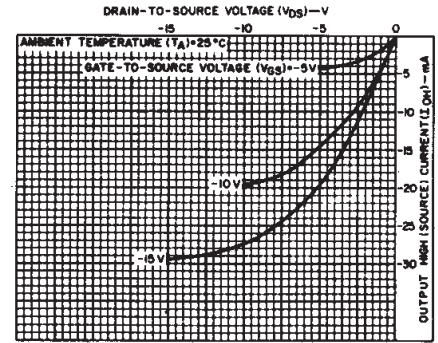


Fig. 5 - Typical output high (source) current characteristics.

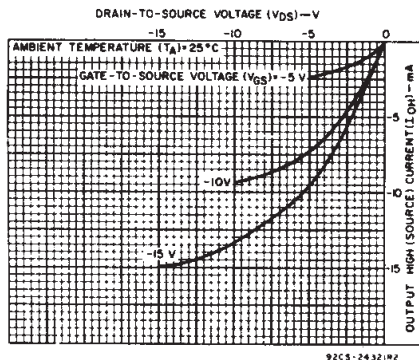


Fig. 6 - Minimum output high (source) current characteristics.

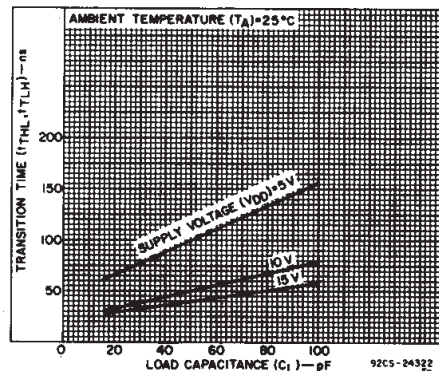


Fig. 7 - Typical transition time as a function of load capacitance.

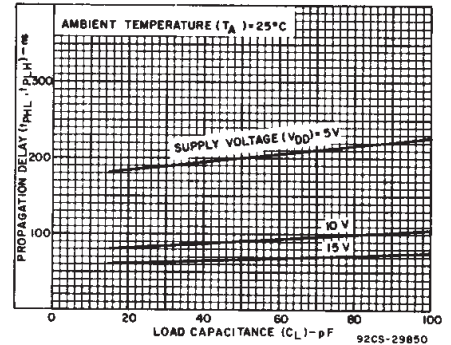


Fig. 8 - Typical propagation delay time as a function of load capacitance (CLOCK to Q).

# CD4018B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ , Input  $t_r, t_f = 20\text{ ns}$ ,  
 $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}\Omega$

| CHARACTERISTIC                                                                          | TEST CONDITIONS | LIMITS              |           |      |      | UNITS |
|-----------------------------------------------------------------------------------------|-----------------|---------------------|-----------|------|------|-------|
|                                                                                         |                 | V <sub>DD</sub> (V) | Min.      | Typ. | Max. |       |
| CLOCKED OPERATION                                                                       |                 |                     |           |      |      |       |
| Propagation Delay Time;<br>t <sub>PLH</sub> , t <sub>PHL</sub>                          |                 | 5                   | —         | 200  | 400  | ns    |
|                                                                                         |                 | 10                  | —         | 90   | 180  |       |
|                                                                                         |                 | 15                  | —         | 65   | 130  |       |
| Transition Time;<br>t <sub>THL</sub> , t <sub>TLH</sub>                                 |                 | 5                   | —         | 100  | 200  | ns    |
|                                                                                         |                 | 10                  | —         | 50   | 100  |       |
|                                                                                         |                 | 15                  | —         | 40   | 80   |       |
| Maximum Clock Input<br>Frequency, f <sub>CL</sub>                                       |                 | 5                   | 3         | 6    | —    | MHz   |
|                                                                                         |                 | 10                  | 7         | 14   | —    |       |
|                                                                                         |                 | 15                  | 8.5       | 17   | —    |       |
| Minimum Clock Pulse Width,<br>t <sub>W</sub>                                            |                 | 5                   | —         | 80   | 160  | ns    |
|                                                                                         |                 | 10                  | —         | 35   | 70   |       |
|                                                                                         |                 | 15                  | —         | 25   | 50   |       |
| Clock Rise & Fall Time;<br>t <sub>rCL</sub> , t <sub>fCL</sub>                          |                 | 5                   | Unlimited |      |      | μs    |
|                                                                                         |                 | 10                  |           |      |      |       |
|                                                                                         |                 | 15                  |           |      |      |       |
| Minimum Data Input Set-Up<br>Time, t <sub>S</sub>                                       |                 | 5                   | —         | 20   | 40   | ns    |
|                                                                                         |                 | 10                  | —         | 6    | 12   |       |
|                                                                                         |                 | 15                  | —         | 3    | 6    |       |
| Minimum Data Input Hold<br>Time, t <sub>H</sub>                                         |                 | 5                   | —         | 70   | 140  | ns    |
|                                                                                         |                 | 10                  | —         | 40   | 80   |       |
|                                                                                         |                 | 15                  | —         | 30   | 60   |       |
| Average Input Capacitance, C <sub>I</sub>                                               | Any Input       | —                   | 5         | 7.5  | pF   |       |
| PRESET* OR RESET OPERATION                                                              |                 |                     |           |      |      |       |
| Propagation Delay Time;<br>Preset or Reset to Q̄<br>t <sub>PLH</sub> , t <sub>PHL</sub> |                 | 5                   | —         | 275  | 550  | ns    |
|                                                                                         |                 | 10                  | —         | 125  | 250  |       |
|                                                                                         |                 | 15                  | —         | 90   | 180  |       |
| Minimum Preset or Reset<br>Pulse Width,<br>t <sub>W</sub>                               |                 | 5                   | —         | 80   | 160  | ns    |
|                                                                                         |                 | 10                  | —         | 35   | 70   |       |
|                                                                                         |                 | 15                  | —         | 25   | 50   |       |
| Minimum Preset or Reset<br>Removal Time                                                 |                 | 5                   | —         | 80   | 160  | ns    |
|                                                                                         |                 | 10                  | —         | 30   | 60   |       |
|                                                                                         |                 | 15                  | —         | 20   | 40   |       |

\* At PRESET ENABLE or JAM Inputs.

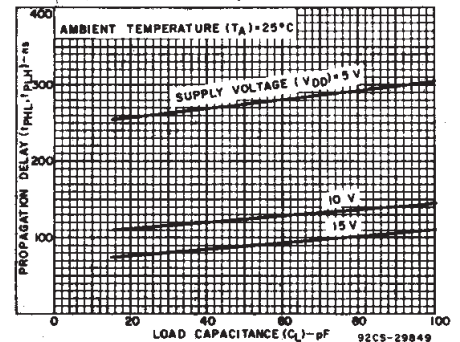


Fig. 9 — Typical propagation delay time as a function of load capacitance (RESET to Q).

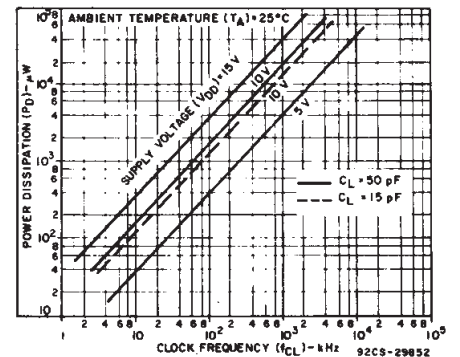


Fig. 10 — Typical dynamic power dissipation as a function of clock input frequency.

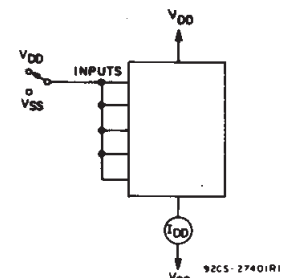


Fig. 11 — Quiescent device current test circuit.

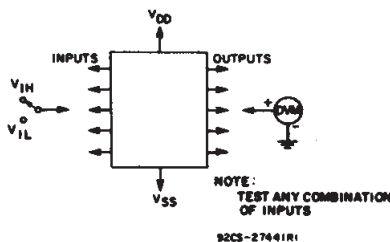


Fig. 12 — Input voltage test circuit.

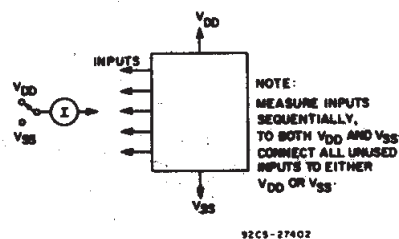


Fig. 13 — Input current test circuit.

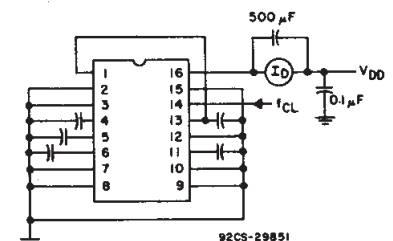


Fig. 14 — Dynamic power dissipation test circuit.

# CD4018B Types

("DATA" INPUT TIED TO  $\bar{Q}_5$  FOR DECADE COUNTER CONFIGURATION)

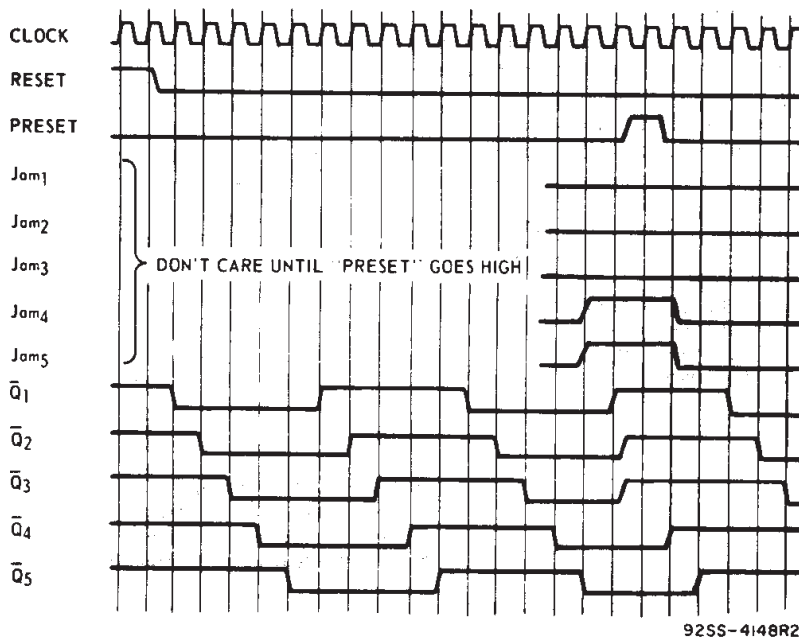


Fig. 15 — Timing diagram.

EXTERNAL CONNECTIONS FOR DIVIDE BY 10, 9, 8, 7, 6, 5, 4, 3 OPERATION

|              |             |                                                          |
|--------------|-------------|----------------------------------------------------------|
| DIVIDE BY 10 | $\bar{Q}_5$ | CONNECTED BACK TO "DATA" NO EXTERNAL COMPONENTS REQUIRED |
| DIVIDE BY 8  | $\bar{Q}_4$ |                                                          |
| DIVIDE BY 6  | $\bar{Q}_3$ |                                                          |
| DIVIDE BY 4  | $\bar{Q}_2$ |                                                          |
| DIVIDE BY 2  | $\bar{Q}_1$ |                                                          |

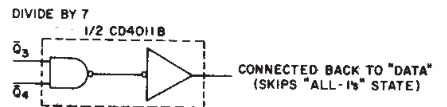
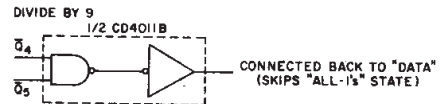
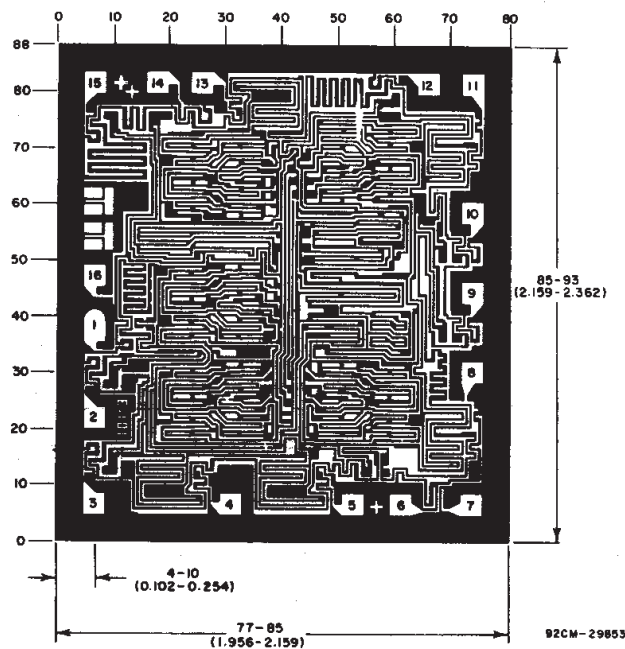


Fig. 16 — External connections for divide by 10, 9, 8, 7, 5, 4, 3, 2 operation.



Chip dimensions and pad layout for CD4018B

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

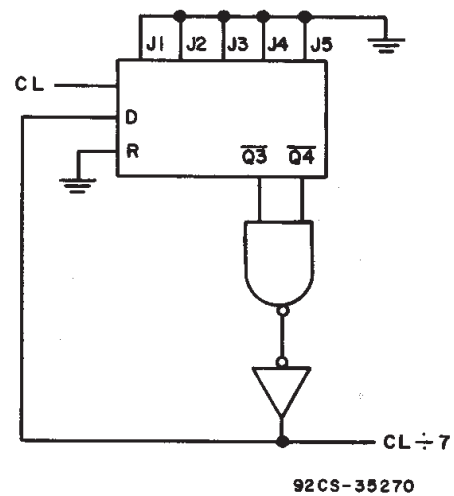


Fig. 17 — Example of divide by 7.

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup>    | Lead/<br>Ball Finish | MSL Peak Temp <sup>(3)</sup> | Samples<br>(Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| CD4018BE         | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)             | CU NIPDAU            | N / A for Pkg Type           |                             |
| CD4018BEE4       | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)             | CU NIPDAU            | N / A for Pkg Type           |                             |
| CD4018BF         | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                        | A42                  | N / A for Pkg Type           |                             |
| CD4018BF3A       | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                        | A42                  | N / A for Pkg Type           |                             |
| CD4018BM         | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD4018BM96       | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD4018BM96E4     | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD4018BM96G4     | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD4018BME4       | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD4018BMG4       | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD4018BMT        | ACTIVE                | SOIC         | D               | 16   | 250         | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD4018BMTE4      | ACTIVE                | SOIC         | D               | 16   | 250         | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD4018BMTG4      | ACTIVE                | SOIC         | D               | 16   | 250         | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD4018BNSR       | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD4018BNSRE4     | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD4018BNSRG4     | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD4018BPW        | ACTIVE                | TSSOP        | PW              | 16   | 90          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD4018BPWE4      | ACTIVE                | TSSOP        | PW              | 16   | 90          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/<br>Ball Finish | MSL Peak Temp <sup>(3)</sup> | Samples<br>(Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|----------------------|------------------------------|-----------------------------|
| CD4018BPWG4      | ACTIVE                | TSSOP        | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| JM38510/05652BEA | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                     | A42                  | N / A for Pkg Type           |                             |
| M38510/05652BEA  | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                     | A42                  | N / A for Pkg Type           |                             |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### OTHER QUALIFIED VERSIONS OF CD4018B, CD4018B-MIL :

• Catalog: [CD4018B](#)

• Military: [CD4018B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


|    |                                                           |
|----|-----------------------------------------------------------|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD4018BM96 | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| CD4018BNSR | SO           | NS              | 16   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD4018BM96 | SOIC         | D               | 16   | 2500 | 333.2       | 345.9      | 28.6        |
| CD4018BNSR | SO           | NS              | 16   | 2000 | 367.0       | 367.0      | 38.0        |

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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|                               |                                                                                          |
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