File Number **2325**

**IRFD310, IRFD311, IRFD312, IRFD313**

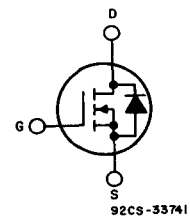
# Power MOS Field-Effect Transistors

## N-Channel Enhancement-Mode Power Field-Effect Transistors

0.3 A and 0.4 A, 350 V - 400 V
$r_{DS(on)}$ = 3.6 Ω and 5.0 Ω

**Features:**
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

**N-CHANNEL ENHANCEMENT MODE**

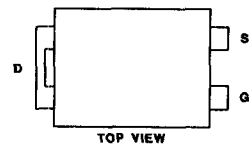



**TERMINAL DIAGRAM**

The IRFD310, IRFD311, IRFD312, and IRFD313 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD-types are supplied in the 4-Pin dual-in-line plastic package.

**TERMINAL DESIGNATION**




**4-PIN DIP**

**Absolute Maximum Ratings**

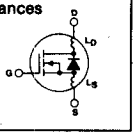
| Parameter | | IRFD310 | IRFD311 | IRFD312 | IRFD313 | Units |
|---|---|---|---|---|---|---|
| $V_{DS}$ | Drain - Source Voltage ① | 400 | 350 | 400 | 350 | V |
| $V_{DGR}$ | Drain - Gate Voltage ($R_{GS}$ = 20 KΩ) ① | 400 | 350 | 400 | 350 | V |
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current | 0.4 | 0.4 | 0.3 | 0.3 | A |
| $I_{DM}$ | Pulsed Drain Current ③ | 1.6 | 1.6 | 1.2 | 1.2 | A |
| $V_{GS}$ | Gate - Source Voltage | ±20 | | | | V |
| $P_D$ @ $T_C$ = 25°C | Max. Power Dissipation | 1 (See Fig. 14) | | | | W |
| | Linear Derating Factor | 0.008 (See Fig. 14) | | | | W/°C |
| $I_{LM}$ | Inductive Current, Clamped ④ | 1.6 | 1.6 | 1.2 | 1.2 | A |
| $T_J$<br>$T_{stg}$ | Operating Junction and<br>Storage Temperature Range | -55 to 150 | | | | °C |
| | Lead Temperature | 300 (0.063 in. (1.6mm) from case for 10s) | | | | °C |

# IRFD310, IRFD311, IRFD312, IRFD313

## Electrical Characteristics @ $T_C$ = 25°C (Unless Otherwise Specified)

| | Parameter | Type | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain - Source Breakdown Voltage | IRFD310 IRFD312 | 400 | — | — | V | $V_{GS}$ = 0V |
| | | IRFD311 IRFD313 | 350 | — | — | V | $I_D$ = 250μA |
| $V_{GS(th)}$ | Gate Threshold Voltage | ALL | 2.0 | — | 4.0 | V | $V_{DS} = V_{GS}$, $I_D$ = 250μ A |
| $I_{GSS}$ | Gate-Source Leakage Forward | ALL | — | — | 500 | nA | $V_{GS}$ = 20V |
| $I_{GSS}$ | Gate-Source Leakage Reverse | ALL | — | — | -500 | nA | $V_{GS}$ = -20V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | ALL | — | — | 250 | μA | $V_{DS}$ = Max. Rating, $V_{GS}$ = 0V |
| | | | — | — | 1000 | μA | $V_{DS}$ = Max. Rating x 0.8, $V_{GS}$ = 0V, $T_C$ = 125°C |
| $I_{D(on)}$ | On-State Drain Current ② | IRFD310 IRFD311 | 0.4 | — | — | A | $V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, $V_{GS}$ = 10V |
| | | IRFD312 IRFD313 | 0.3 | — | — | A | |
| $R_{DS(on)}$ | Static Drain-Source On-State Resistance ② | IRFD310 IRFD311 | — | 3.3 | 3.6 | Ω | $V_{GS}$ = 10V, $I_D$ = 0.2A |
| | | IRFD312 IRFD313 | — | 3.6 | 5.0 | Ω | |
| $g_{fs}$ | Forward Transconductance ② | ALL | 0.5 | 1.2 | — | S(℧) | $V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, $I_D$ = 0.2A |
| $C_{iss}$ | Input Capacitance | ALL | — | 135 | — | pF | $V_{GS}$ = 0V, $V_{DS}$ = 25V, f = 1.0 MHz See Fig. 10 |
| $C_{oss}$ | Output Capacitance | ALL | — | 35 | — | pF | |
| $C_{rss}$ | Reverse Transfer Capacitance | ALL | — | 8.0 | — | pF | |
| $t_{d(on)}$ | Turn-On Delay Time | ALL | — | 3.0 | 10 | ns | $V_{DD} \simeq 0.5BV_{DSS}$, $I_D$ = 0.2A, $Z_o$ = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.) |
| $t_r$ | Rise Time | ALL | — | 10 | 20 | ns | |
| $t_{d(off)}$ | Turn-Off Delay Time | ALL | — | 5.0 | 10 | ns | |
| $t_f$ | Fall Time | ALL | — | 8.0 | 15 | ns | |
| $Q_g$ | Total Gate Charge (Gate-Source Plus Gate-Drain) | ALL | — | 6.0 | 7.5 | nC | $V_{GS}$ = 10V, $I_D$ = 0.4A, $V_{DS}$ = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.) |
| $Q_{gs}$ | Gate-Source Charge | ALL | — | 3.0 | 4.5 | nC | |
| $Q_{gd}$ | Gate-Drain ("Miller") Charge | ALL | — | 3.0 | 4.5 | nC | |
| $L_D$ | Internal Drain Inductance | ALL | — | 4.0 | — | nH | Measured from the drain lead, 2.0 mm (0.08 in.) from package to center of die. |
| $L_S$ | Internal Source Inductance | ALL | — | 6.0 | — | nH | Measured from the source lead, 2.0 mm (0.08 in.) from package to source bonding pad. |

Modified MOSFET symbol showing the internal device inductances

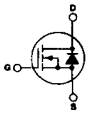



## Thermal Resistance

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| $R_{thJA}$ | Junction-to-Ambient | ALL | — | — | 120 | °C/W | Free Air Operation |

## Source-Drain Diode Ratings and Characteristics

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | IRFD310 IRFD311 | — | — | 0.4 | A | Modified MOSFET symbol showing the integral reverse P-N junction rectifier. |
| | | IRFD312 IRFD313 | — | — | 0.3 | A | |
| $I_{SM}$ | Pulse Source Current (Body Diode) ③ | IRFD310 IRFD311 | — | — | 1.6 | A | |
| | | IRFD312 IRFD313 | — | — | 1.2 | A | |
| $V_{SD}$ | Diode Forward Voltage ② | IRFD310 IRFD311 | — | — | 1.6 | V | $T_C$ = 25°C, $I_S$ = 1.6A, $V_{GS}$ = 0V |
| | | IRFD312 IRFD313 | — | — | 1.5 | V | $T_C$ = 25°C, $I_S$ = 1.2A, $V_{GS}$ = 0V |
| $t_{rr}$ | Reverse Recovery Time | ALL | — | 380 | — | ns | $T_J$ = 150°C, $I_F$ = 1.6A, $dI_F/dt$ = 100A/μs |
| $Q_{RR}$ | Reverse Recovered Charge | ALL | — | 2.7 | — | μC | $T_J$ = 150°C, $I_F$ = 1.6A, $dI_F/dt$ = 100A/μs |
| $t_{on}$ | Forward Turn-on Time | ALL | Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$. | | | | |




① $T_J$ = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ See figs. 14, 15. L = 100 μH.

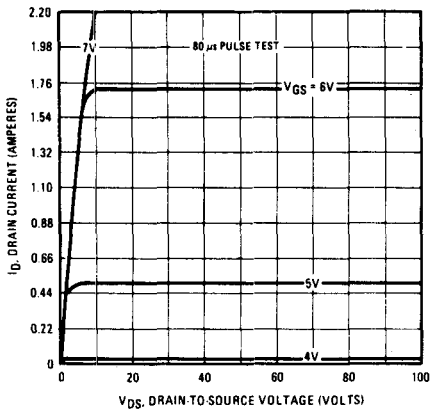



Fig. 1 — Typical Output Characteristics

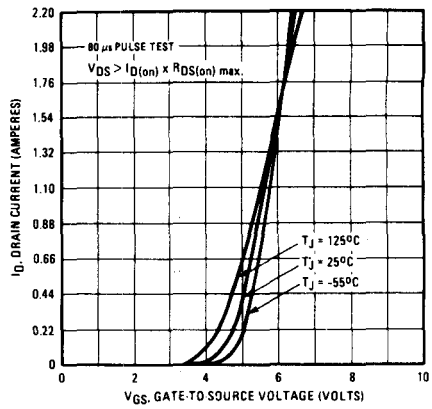



Fig. 2 — Typical Transfer Characteristics

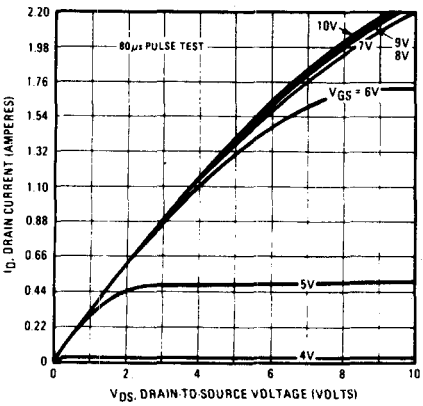



Fig. 3 — Typical Saturation Characteristics

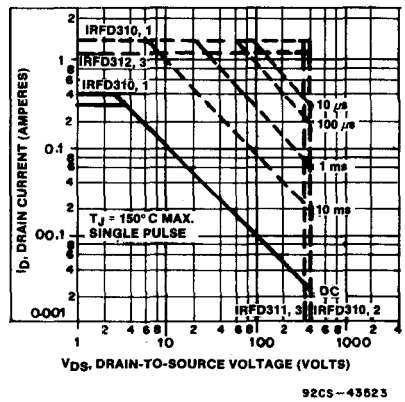



Fig. 4 — Maximum Safe Operating Area

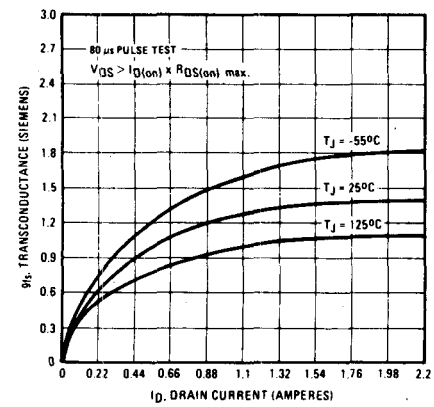



Fig. 5 — Typical Transconductance Vs. Drain Current

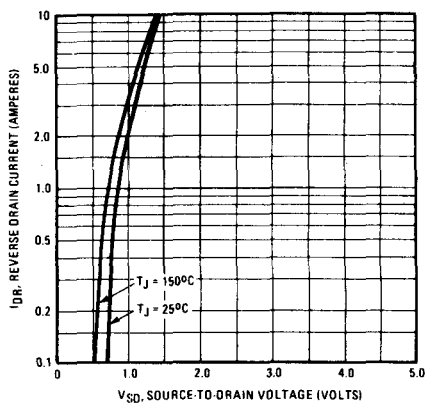



Fig. 6 — Typical Source-Drain Diode Forward Voltage

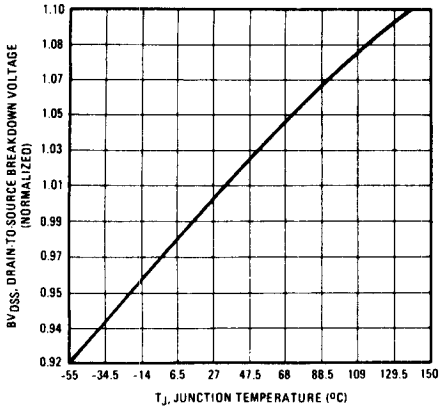



Fig. 7 — Breakdown Voltage Vs. Temperature

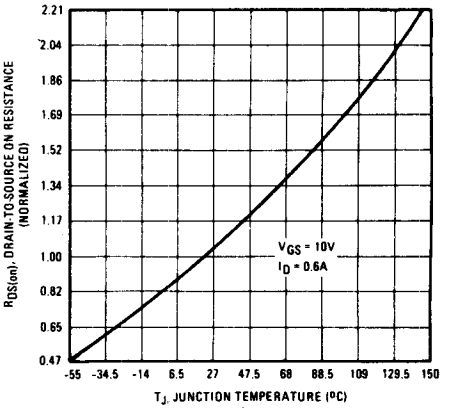



Fig. 8 — Normalized On-Resistance Vs. Temperature

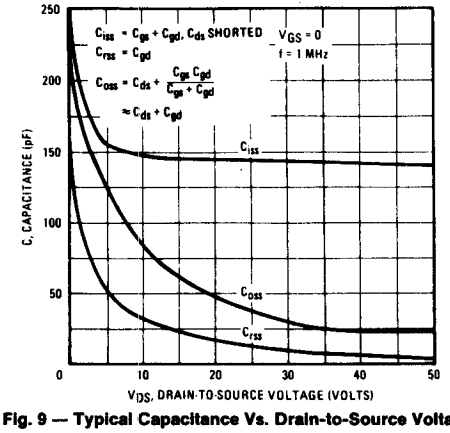



Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

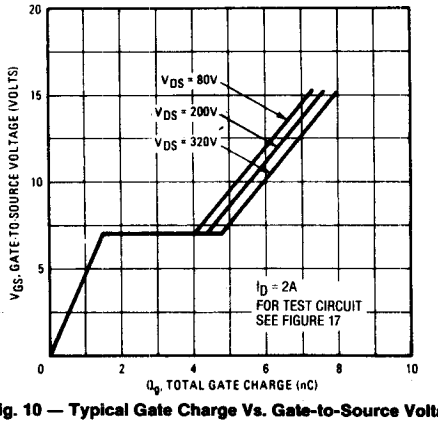



Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

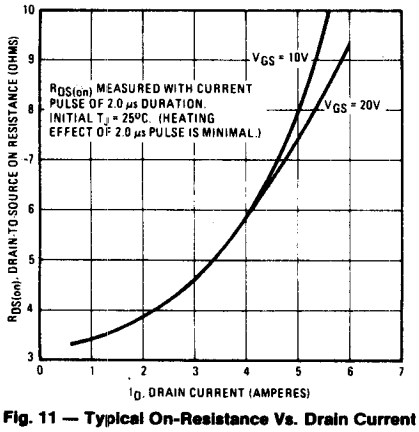



Fig. 11 — Typical On-Resistance Vs. Drain Current

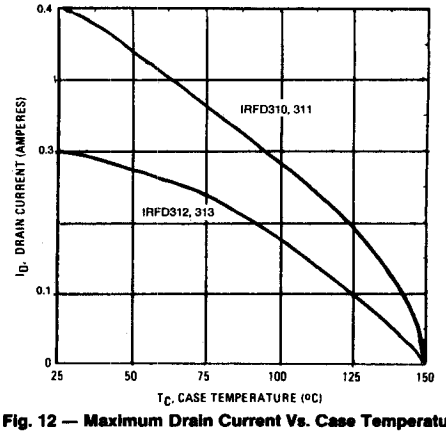



Fig. 12 — Maximum Drain Current Vs. Case Temperature

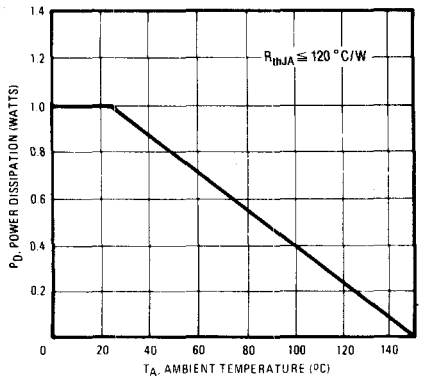



Fig. 13 — Power Vs. Temperature Derating Curve

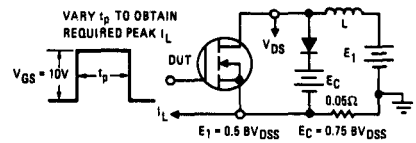



Fig. 14 — Clamped inductive test circuit.

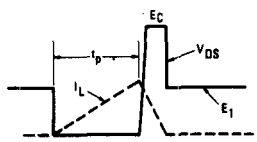



Fig. 15 — Clamped inductive waveforms.

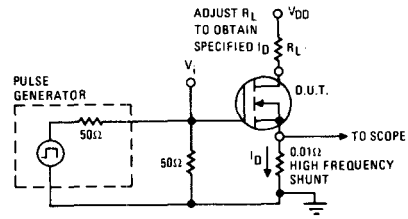



Fig. 16 — Switching Time Test Circuit

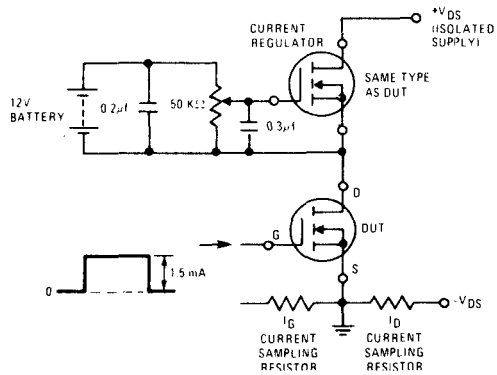



Fig. 17 — Gate Charge Test Circuit