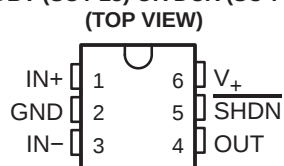


TLV341, TLV342, TLV344 LOW-VOLTAGE RAIL-TO-RAIL OUTPUT CMOS OPERATIONAL AMPLIFIERS WITH SHUTDOWN

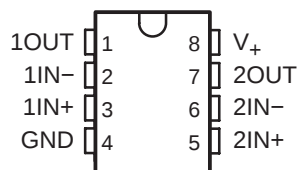
SLVS568B – JANUARY 2005 – REVISED DECEMBER 2005

- 1.8-V and 5-V Performance
- Low Offset (A Grade)
 - 1.25 mV Max (25°C)
 - 1.7 mV Max (–40°C to 125°C)
- Rail-to-Rail Output Swing
- Wide Common-Mode Input Voltage Range . . . –0.2 V to ($V_+ - 0.5$ V)
- Input Bias Current . . . 1 pA (Typ)
- Input Offset Voltage . . . 0.3 mV (Typ)
- Low Supply Current . . . 70 μ A/Channel
- Low Shutdown Current . . . 10 pA (Typ)
- Gain Bandwidth . . . 2.3 MHz (Typ)
- Slew Rate . . . 0.9 V/ μ s (Typ)
- Turn-On Time From Shutdown . . . 5 μ s (Typ)
- Input Referred Voltage Noise (at 10 kHz) . . . 20 nV/ $\sqrt{\text{Hz}}$
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
- Applications
 - Cordless/Cellular Phones
 - Consumer Electronics (Laptops, PDAs)
 - Audio Pre-Amp for Voice
 - Portable/Battery-Powered Electronic Equipment
 - Supply Current Monitoring
 - Battery Monitoring
 - Buffers
 - Filters
 - Drivers

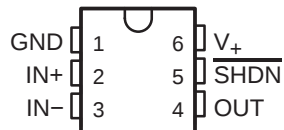
TLV341 . . . DBV (SOT-23) OR DCK (SC-70) PACKAGE



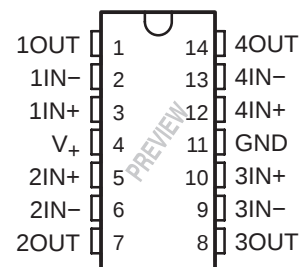
TLV342 . . . D (SOIC) OR DGK (MSOP) PACKAGE
(TOP VIEW)



TLV341 . . . DRL (SOT-563) PACKAGE
(TOP VIEW)



TLV344 . . . D (SOIC) OR PW (TSSOP) PACKAGE
(TOP VIEW)



description/ordering information

The TLV341, TLV342, and TLV344 are single, dual, and quad CMOS operational amplifiers, respectively, with low-voltage, low-power, and rail-to-rail output swing capabilities. The PMOS input stage offers an ultra-low input bias current of 1 pA (typ) and an offset voltage of 0.3 mV (typ). For applications requiring excellent dc precision, the A grade (TLV34xA) has a low offset voltage of 1.25 mV (max) at 25°C.

These single-supply amplifiers are designed specifically for ultra-low-voltage (1.5-V to 5-V) operation, with a common-mode input voltage range that typically extends from –0.2 V to 0.5 V from the positive supply rail. Additional features include 20-nV/ $\sqrt{\text{Hz}}$ voltage noise at 10 kHz, 2.3-MHz unity-gain bandwidth, and 0.9-V/ μ s slew rate.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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TLV341, TLV342, TLV344

LOW-VOLTAGE RAIL-TO-RAIL OUTPUT CMOS OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLVS568B – JANUARY 2005 – REVISED DECEMBER 2005

description/ordering information (continued)

The TLV341 (single) also offers a shutdown ($\overline{\text{SHDN}}$) pin that can be used to disable the device. In shutdown mode, the supply current is reduced to 45 pA (typ). Offered in both the SOT-23 and smaller SC-70 packages, the TLV341 is suitable for the most space-constrained applications. The dual TLV342 is offered in the standard SOIC and MSOP packages.

An extended industrial temperature range from -40°C to 125°C makes the TLV34x suitable in a wide variety of commercial and industrial applications.

ORDERING INFORMATION

T_A	MAX V_{IO} (25°C)	PACKAGE [†]			ORDERABLE PART NUMBER	TOP-SIDE MARKING [‡]
-40°C to 125°C	Standard grade: 4 mV	Single	SOT-23 – DBV	Reel of 3000	TLV341IDBVR	YC9_
				Reel of 250	TLV341IDBVT	
			SC-70 – DCK	Reel of 3000	TLV341IDCKR	Y4_
				Reel of 250	TLV341IDCKT	
			SOT-563 – DRL		TLV341IDRLR	Y4_
		Dual	SOIC – D	Tube of 75	TLV342ID	TY342
				Reel of 2500	TLV342IDR	
			MSOP/VSSOP – DGK	Reel of 2500	TLV342IDGKR	PREVIEW
				Reel of 250	TLV342IDGKT	
		Quad	SOIC – D	Tube of 50	TLV344ID	PREVIEW
				Reel of 2500	TLV344IDR	
			TSSOP – PW	Tube of 90	TLV344IPWR	PREVIEW
				Reel of 2000	TLV344IPWR	
	A grade: 1.25 mV	Single	SOT-23 – DBV	Reel of 3000	TLV341AIDBVR	YCG_
				Reel of 250	TLV341AIDBVT	
			SC-70 – DCK	Reel of 3000	TLV341AIDCKR	Y5_
				Reel of 250	TLV341AIDCKT	
		Dual	SOIC – D	Tube of 75	TLV342AID	TY342A
				Reel of 2500	TLV342AIDR	
			MSOP/VSSOP – DGK	Reel of 2500	TLV342AIDGKR	PREVIEW
				Reel of 250	TLV342AIDGKT	
		Quad	SOIC – D	Tube of 50	TLV344AID	PREVIEW
				Reel of 2500	TLV344AIDR	
			TSSOP – PW	Tube of 90	TLV344AIPWR	PREVIEW
				Reel of 2000	TLV344AIPWR	

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

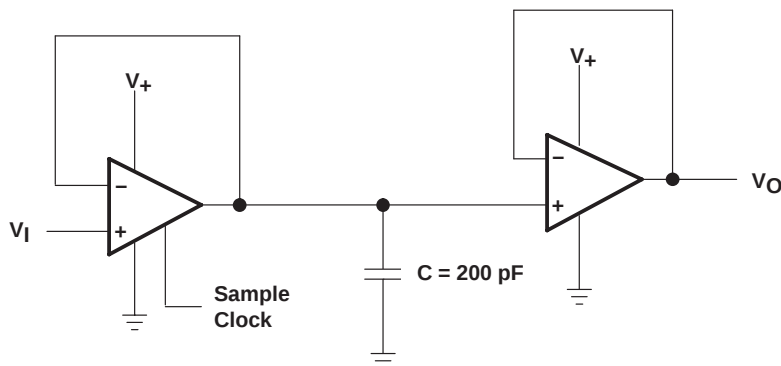
[‡] DBV/DCK/DRL: The actual top-side marking has one additional character that designates the assembly/test site.

TLV341, TLV342, TLV344

LOW-VOLTAGE RAIL-TO-RAIL OUTPUT CMOS OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLVS568B – JANUARY 2005 – REVISED DECEMBER 2005

symbol (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_+ (see Note 1)	5.5 V
Differential input voltage, V_{ID} (see Note 2)	± 5.5 V
Input voltage range, V_I (either input)	0 to 5.5 V
Package thermal impedance, θ_{JA} (see Notes 3 and 4):	
D package (8 pin)	97°C/W
D package (14 pin)	86°C/W
DBV package	165°C/W
DCK package	259°C/W
DGK package	172°C/W
DRL package	142°C/W
PW package	113°C/W
Operating virtual junction temperature	150°C
Storage temperature range, T_{stg}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values (except differential voltages and V_+ specified for the measurement of I_{OS}) are with respect to the network GND.
 2. Differential voltages are at $IN+$ with respect to $IN-$.
 3. Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Selecting the maximum of 150°C can affect reliability.
 4. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

	MIN	MAX	UNIT
V_+ Supply voltage (single-supply operation)	1.5	5.5	V
T_A Operating free-air temperature	-40	125	°C

ESD protection

TEST CONDITIONS	TYP	UNIT
Human-Body Model	2000	V
Machine Model	200	V



TLV341, TLV342, TLV344

LOW-VOLTAGE RAIL-TO-RAIL OUTPUT CMOS OPERATIONAL AMPLIFIERS

WITH SHUTDOWN

SLVS568B – JANUARY 2005 – REVISED DECEMBER 2005

electrical characteristics, $V_+ = 1.8\text{ V}$, $\text{GND} = 0$, $V_{\text{IC}} = V_{\text{O}} = V_+/2$, $R_{\text{L}} > 1\text{ M}\Omega$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_{A}	MIN	TYP [†]	MAX	UNIT
V_{IO} Input offset voltage	Standard grade	25°C	0.3	4		mV
		Full range		4.5		
	A grade	25°C	0.3	1.25		
		0°C to 125°C	0.3	1.5		
		–40°C to 125°C	0.3	1.7		
$\alpha_{V_{\text{IO}}}$ Average temperature coefficient of input offset voltage		Full range	1.9			$\mu\text{V}/^\circ\text{C}$
I_{IB} Input bias current		25°C	1	100		pA
		–40°C to 85°C		375		
		–40°C to 125°C		3000		
I_{IO} Input offset current		25°C	6.6			fA
CMRR Common-mode rejection ratio	$0 \leq V_{\text{ICR}} \leq 1.2\text{ V}$	25°C	60	85		dB
		Full range	50			
k_{SVR} Supply-voltage rejection ratio	$1.8\text{ V} \leq V_+ \leq 5\text{ V}$	25°C	75	95		dB
		Full range	65			
V_{ICR} Common-mode input voltage range	CMRR $\geq 60\text{ dB}$	25°C	0		1.2	V
A_{V} Large-signal voltage gain (see Note 5)	$R_{\text{L}} = 10\text{ k}\Omega$ to 1.35 V	25°C	70	110		dB
		Full range	60			
	$R_{\text{L}} = 2\text{ k}\Omega$ to 1.35 V	25°C	65	100		
		Full range	55			
V_{O} Output swing (delta from supply rails)	$R_{\text{L}} = 2\text{ k}\Omega$ to 0.9 V	Low level	25°C	22	50	mV
			Full range		75	
		High level	25°C	25	50	
			Full range		75	
	$R_{\text{L}} = 10\text{ k}\Omega$ to 0.9 V	Low level	25°C	14	20	
			Full range		25	
		High level	25°C	7	20	
			Full range		25	
I_{CC} Supply current (per channel)		25°C	70	150		μA
		Full range		200		
I_{OS} Output short-circuit current	Sourcing	25°C	6	12		mA
	Sinking		10	20		
SR Slew rate	$R_{\text{L}} = 10\text{ k}\Omega$, Note 6	25°C	0.9			$\text{V}/\mu\text{s}$
GBW Unity-gain bandwidth	$R_{\text{L}} = 100\text{ k}\Omega$, $C_{\text{L}} = 200\text{ pF}$	25°C	2.2			MHz
Φ_{m} Phase margin	$R_{\text{L}} = 100\text{ k}\Omega$, $C_{\text{L}} = 20\text{ pF}$	25°C	55			°
G_{m} Gain margin	$R_{\text{L}} = 100\text{ k}\Omega$, $C_{\text{L}} = 20\text{ pF}$	25°C	15			dB
V_{n} Equivalent input noise voltage	$f = 1\text{ kHz}$	25°C	33			$\text{nV}/\sqrt{\text{Hz}}$
I_{n} Equivalent input noise current	$f = 1\text{ kHz}$	25°C	0.001			$\text{pA}/\sqrt{\text{Hz}}$
THD Total harmonic distortion	$f = 1\text{ kHz}$, $A_{\text{V}} = 1$, $R_{\text{L}} = 600\text{ }\Omega$, $V_{\text{I}} = 1\text{ V}_{\text{PP}}$	25°C	0.015			%

[†] Typical values represent the most likely parametric norm.

NOTES: 5. $\text{GND} + 0.2\text{ V} \leq V_{\text{O}} \leq V_{\text{CC}} + -0.2\text{ V}$

6. Connected as voltage follower with 2-V_{PP} step input. Number specified is the slower of the positive and negative slew rates.



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TLV341, TLV342, TLV344

**LOW-VOLTAGE RAIL-TO-RAIL OUTPUT CMOS OPERATIONAL AMPLIFIERS
WITH SHUTDOWN**

SLVS568B – JANUARY 2005 – REVISED DECEMBER 2005

shutdown characteristics, $V_+ = 1.8\text{ V}$, $\text{GND} = 0$, $V_{\text{IC}} = V_{\text{O}} = V_+/2$, $R_{\text{L}} > 1\text{ M}\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_{A}	MIN	TYP	MAX	UNIT
$I_{\text{CC}}(\text{SHDN})$	Supply current in shutdown mode	$V_{\text{SD}} = 0\text{ V}$	25°C		0.01	1	μA
			Full range			1.5	μA
$t_{\text{(on)}}$	Amplifier turn-on time		25°C		5		μs
V_{SD}	Shutdown pin voltage range	ON mode	25°C		1.5 to 1.8		V
		Shutdown mode			0 to 0.5		



TLV341, TLV342, TLV344

LOW-VOLTAGE RAIL-TO-RAIL OUTPUT CMOS OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLVS568B – JANUARY 2005 – REVISED DECEMBER 2005

electrical characteristics, $V_+ = 5\text{ V}$, $\text{GND} = 0$, $V_{\text{IC}} = V_{\text{O}} = V_+/2$, $R_{\text{L}} > 1\text{ M}\Omega$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_{A}	MIN	TYP [†]	MAX	UNIT
V_{IO} Input offset voltage	Standard grade	25°C		0.3	4	mV
		Full range			4.5	
	A grade	25°C		0.3	1.25	
		0°C to 125°C		0.3	1.5	
		–40°C to 125°C		0.3	1.7	
$\alpha_{V_{\text{IO}}}$ Average temperature coefficient of input offset voltage		Full range		1.9		$\mu\text{V}/^\circ\text{C}$
I_{IB} Input bias current		25°C		1	200	pA
		–40°C to 85°C			375	
		–40°C to 125°C			3000	
I_{IO} Input offset current		25°C		6.6		fA
CMRR Common-mode rejection ratio	$0 \leq V_{\text{ICR}} \leq 4.4\text{ V}$	25°C	75	90		dB
		Full range	70			
k_{SVR} Supply-voltage rejection ratio	$1.8\text{ V} \leq V_+ \leq 5\text{ V}$	25°C	75	95		dB
		Full range	65			
V_{ICR} Common-mode input voltage range	CMRR $\geq 70\text{ dB}$	25°C	0	–0.2 to 4.5	4.4	V
A_{V} Large-signal voltage gain (see Note 5)	$R_{\text{L}} = 10\text{ k}\Omega$ to 2.5 V	25°C	80	110		dB
		Full range	70			
	$R_{\text{L}} = 2\text{ k}\Omega$ to 2.5 V	25°C	75	105		
		Full range	60			
V_{O} Output swing (delta from supply voltage)	$R_{\text{L}} = 2\text{ k}\Omega$ to 2.5 V	Low level	25°C	40	60	mV
			Full range		85	
		High level	25°C	25	60	
			Full range		85	
	$R_{\text{L}} = 10\text{ k}\Omega$ to 2.5 V	Low level	25°C	18	30	
			Full range		40	
		High level	25°C	7	15	
			Full range		20	
I_{CC} Supply current (per channel)		25°C		75	150	μA
		Full range			200	
I_{OS} Output short-circuit current	Sourcing	25°C	60	113		mA
	Sinking		80	115		
SR Slew rate	$R_{\text{L}} = 10\text{ k}\Omega$, Note 6	25°C		1		$\text{V}/\mu\text{s}$
GBW Unity-gain bandwidth	$R_{\text{L}} = 10\text{ k}\Omega$, $C_{\text{L}} = 200\text{ pF}$	25°C		2.3		MHz
Φ_{m} Phase margin	$R_{\text{L}} = 100\text{ k}\Omega$, $C_{\text{L}} = 20\text{ pF}$	25°C		55		°
G_{m} Gain margin	$R_{\text{L}} = 100\text{ k}\Omega$, $C_{\text{L}} = 20\text{ pF}$	25°C		15		dB
V_{n} Equivalent input noise voltage	$f = 1\text{ kHz}$	25°C		33		$\text{nV}/\sqrt{\text{Hz}}$
I_{n} Equivalent input noise current	$f = 1\text{ kHz}$	25°C		0.001		$\text{pA}/\sqrt{\text{Hz}}$
THD Total harmonic distortion	$f = 1\text{ kHz}$, $A_{\text{V}} = 1$, $R_{\text{L}} = 600\text{ }\Omega$, $V_{\text{I}} = 1\text{ V}_{\text{pp}}$	25°C		0.012		%

[†] Typical values represent the most likely parametric norm.

NOTES: 5. $\text{GND} + 0.2\text{ V} \leq V_{\text{O}} \leq V_{\text{CC}+} - 0.2\text{ V}$

6. Connected as voltage follower with 2-V_{pp} step input. Number specified is the slower of the positive and negative slew rates.



TLV341, TLV342, TLV344

**LOW-VOLTAGE RAIL-TO-RAIL OUTPUT CMOS OPERATIONAL AMPLIFIERS
WITH SHUTDOWN**

SLVS568B – JANUARY 2005 – REVISED DECEMBER 2005

shutdown characteristics, $V_+ = 5\text{ V}$, $\text{GND} = 0$, $V_{\text{IC}} = V_{\text{O}} = V_+/2$, $R_{\text{L}} > 1\text{ M}\Omega$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_{A}	MIN	TYP	MAX	UNIT
$I_{\text{CC}}(\text{SHDN})$ Supply current in shutdown mode	$V_{\text{SD}} = 0\text{ V}$	25°C		0.01	1	μA
		Full range			1.5	
$t_{\text{(on)}}$ Amplifier turn-on time		25°C		5		μs
V_{SD} Shutdown pin voltage range	ON mode	25°C	3.1 to 5	4.5 to 5		V
	Shutdown mode		0 to 1	0 to 0.8		



TLV341, TLV342, TLV344

LOW-VOLTAGE RAIL-TO-RAIL OUTPUT CMOS OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLVS568B – JANUARY 2005 – REVISED DECEMBER 2005

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

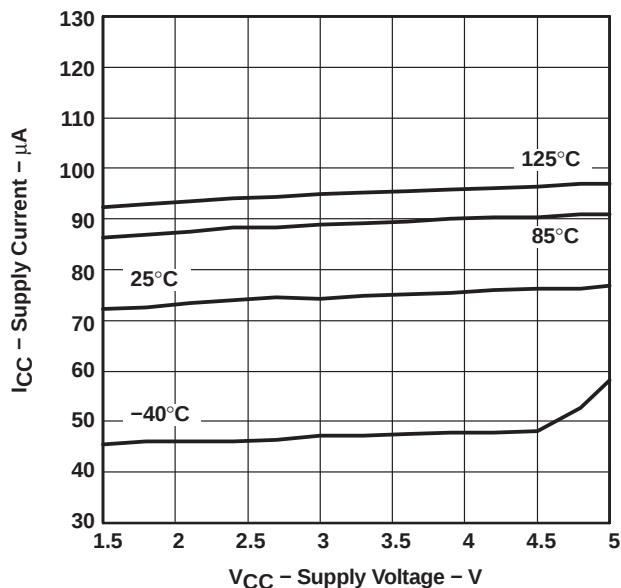


Figure 1

INPUT BIAS CURRENT
vs
TEMPERATURE

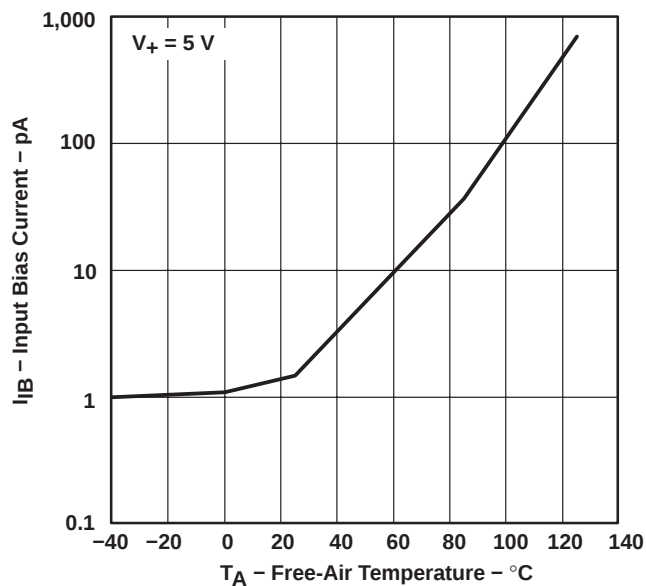


Figure 2

OUTPUT VOLTAGE SWING
vs
SUPPLY VOLTAGE

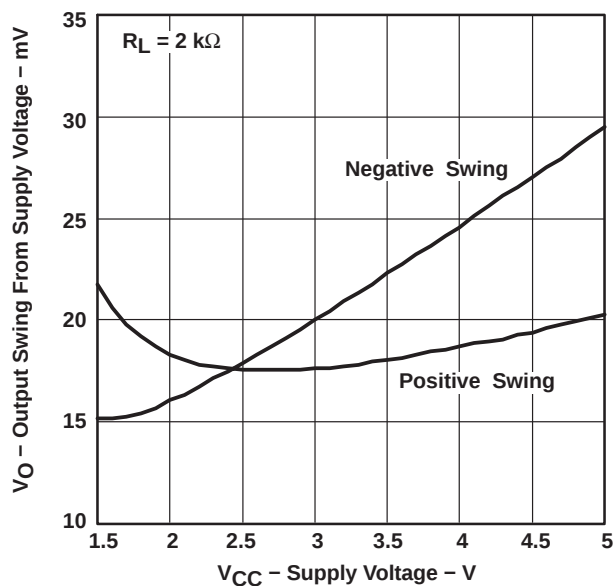


Figure 3

OUTPUT VOLTAGE SWING
vs
SUPPLY VOLTAGE

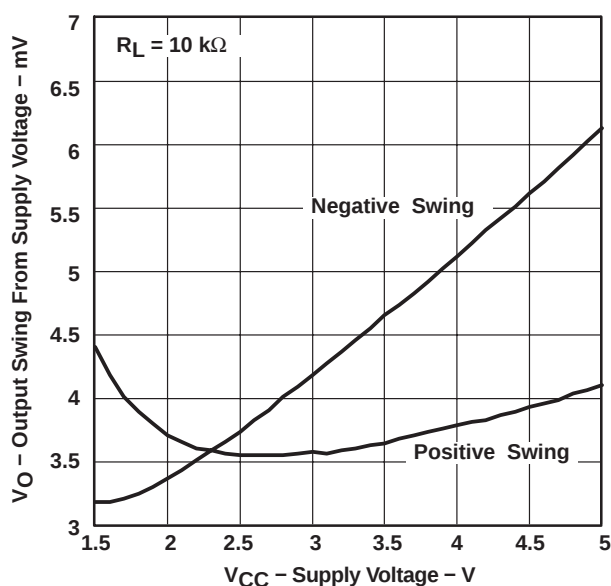


Figure 4

TLV341, TLV342, TLV344

LOW-VOLTAGE RAIL-TO-RAIL OUTPUT CMOS OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLVS568B – JANUARY 2005 – REVISED DECEMBER 2005

TYPICAL CHARACTERISTICS

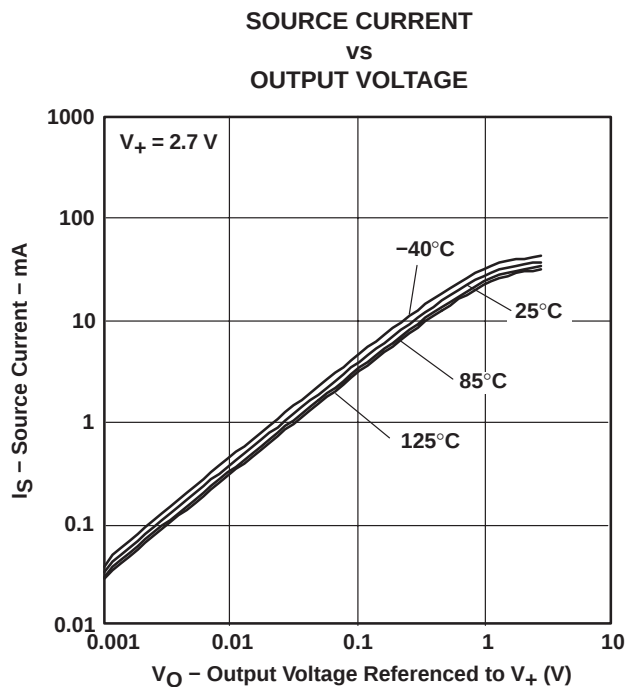


Figure 5

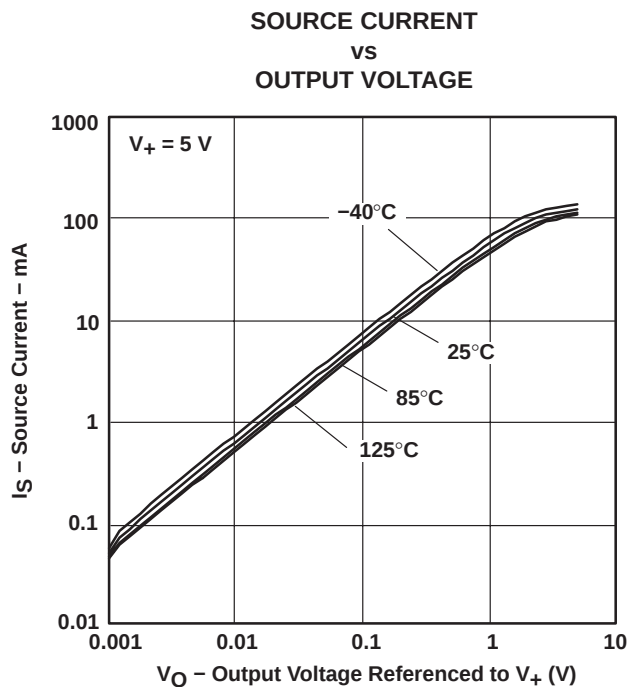


Figure 6

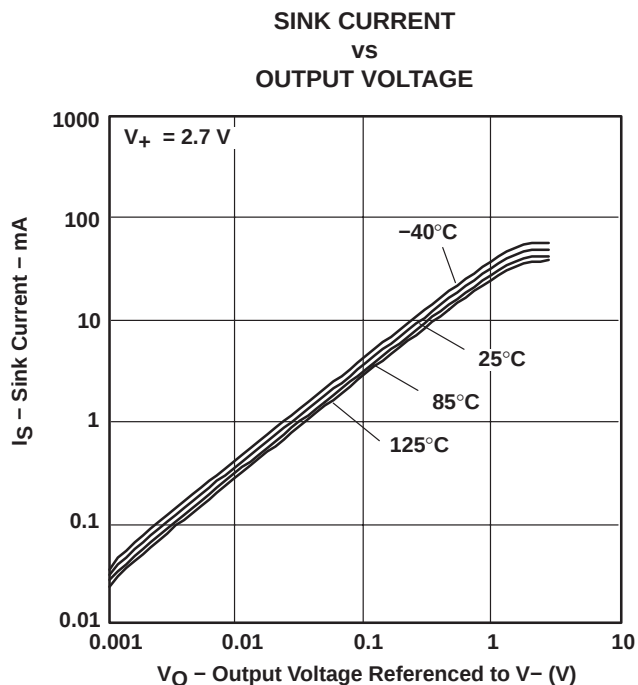


Figure 7

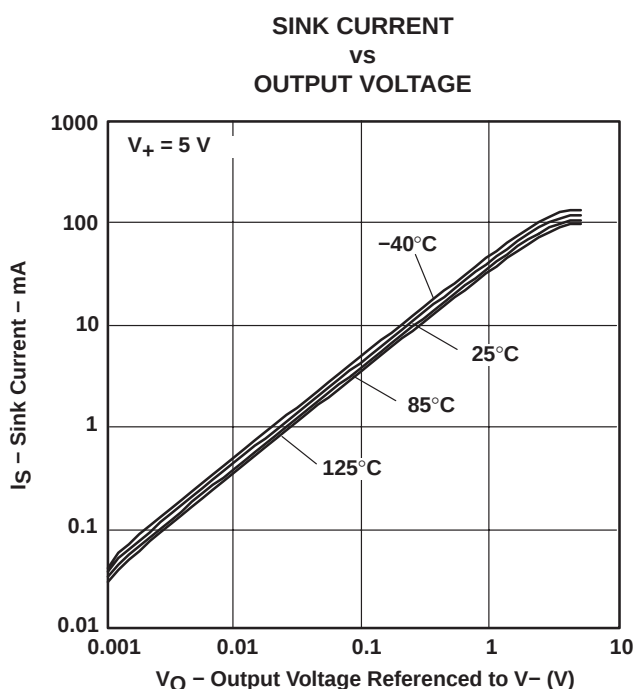


Figure 8

TLV341, TLV342, TLV344

LOW-VOLTAGE RAIL-TO-RAIL OUTPUT CMOS OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLVS568B – JANUARY 2005 – REVISED DECEMBER 2005

TYPICAL CHARACTERISTICS

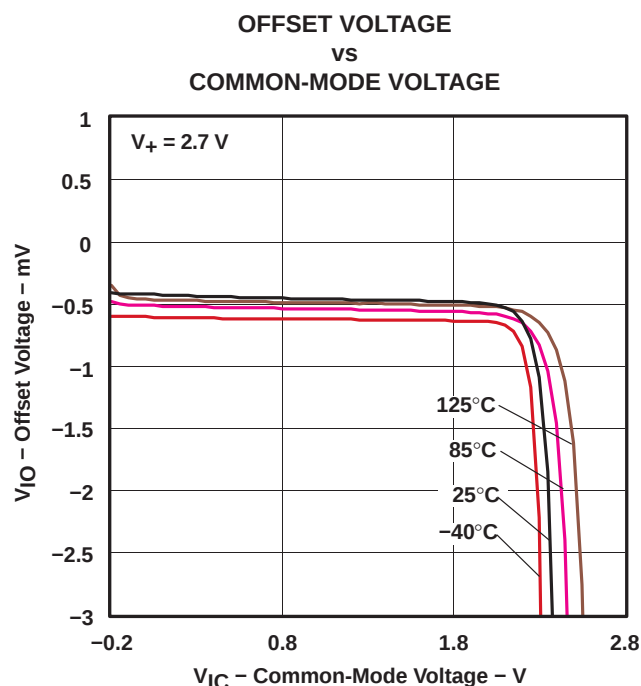


Figure 9

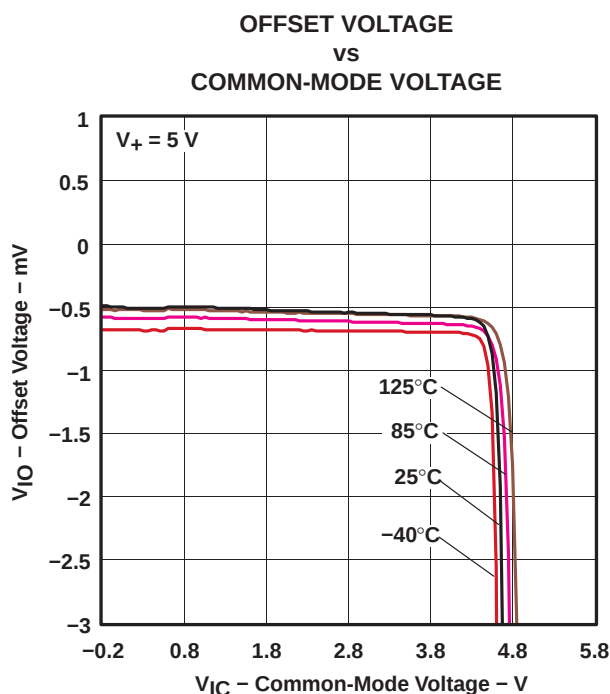


Figure 10

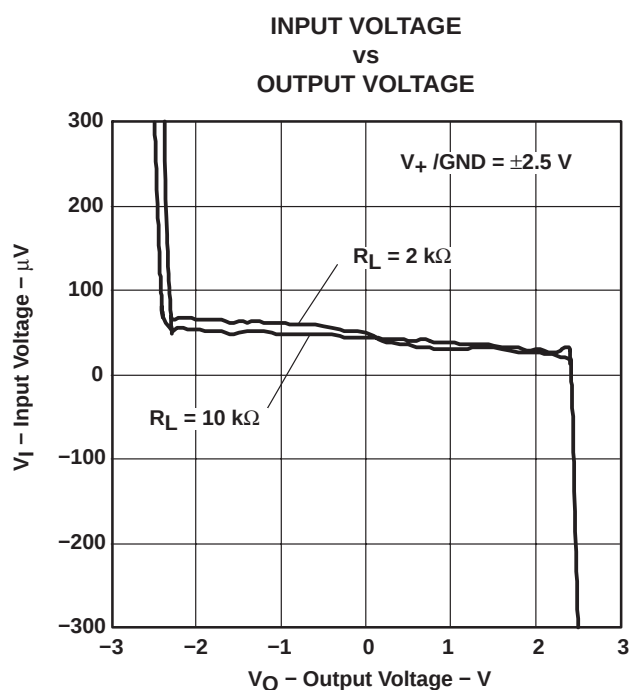


Figure 11

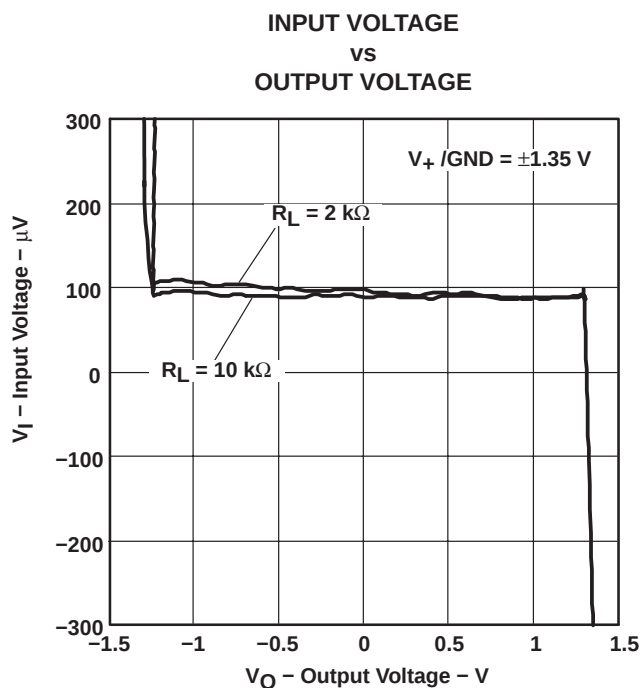


Figure 12

TLV341, TLV342, TLV344

LOW-VOLTAGE RAIL-TO-RAIL OUTPUT CMOS OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLVS568B – JANUARY 2005 – REVISED DECEMBER 2005

TYPICAL CHARACTERISTICS

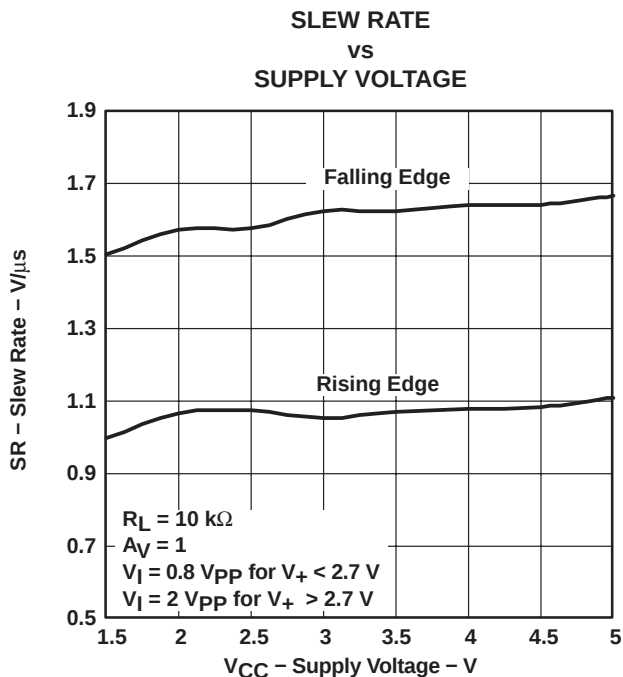


Figure 13

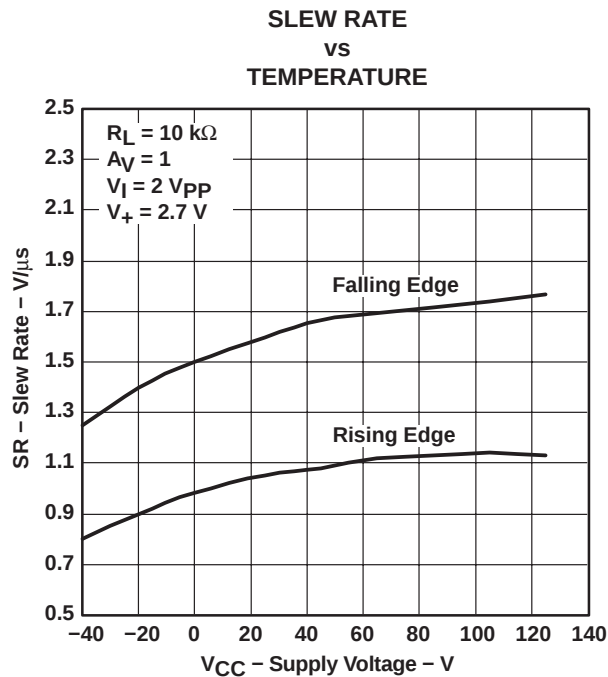


Figure 14

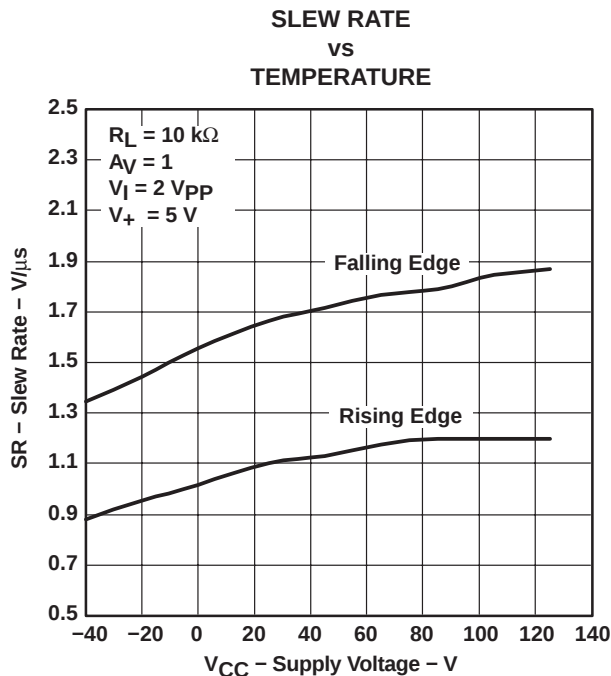


Figure 15

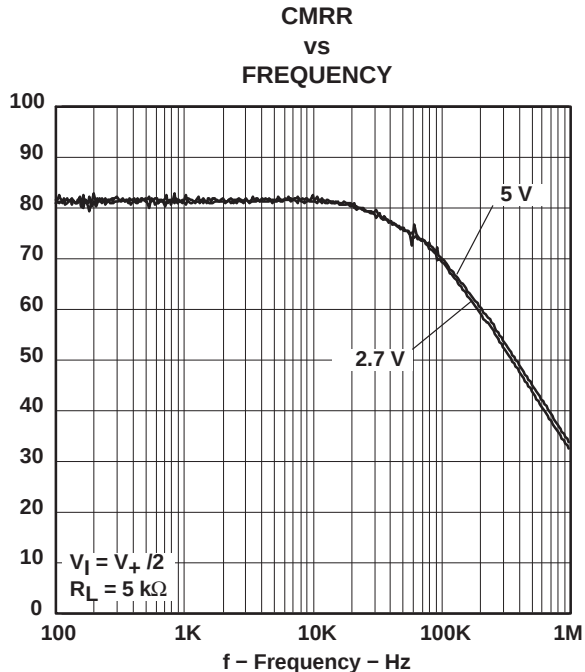


Figure 16

TLV341, TLV342, TLV344

LOW-VOLTAGE RAIL-TO-RAIL OUTPUT CMOS OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLVS568B – JANUARY 2005 – REVISED DECEMBER 2005

TYPICAL CHARACTERISTICS

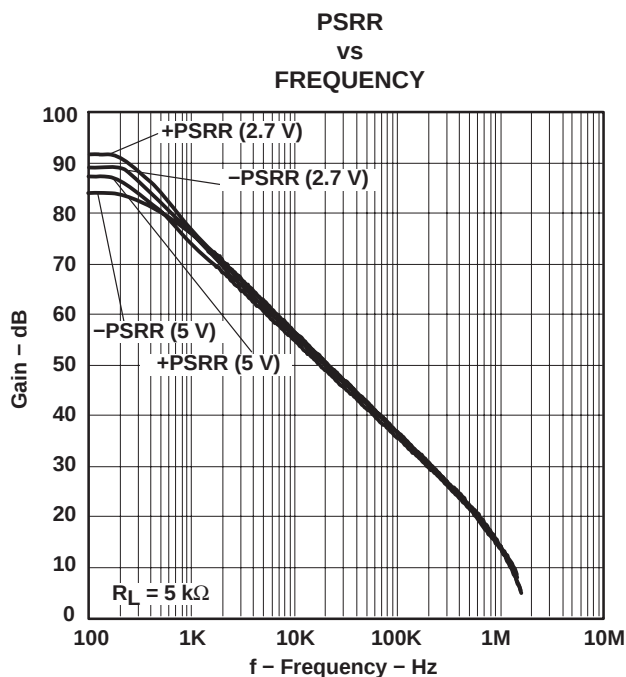


Figure 17

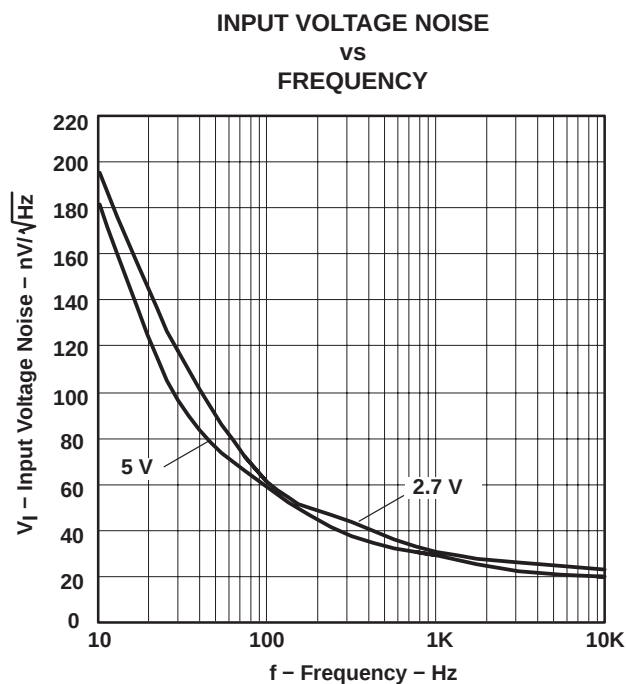


Figure 18

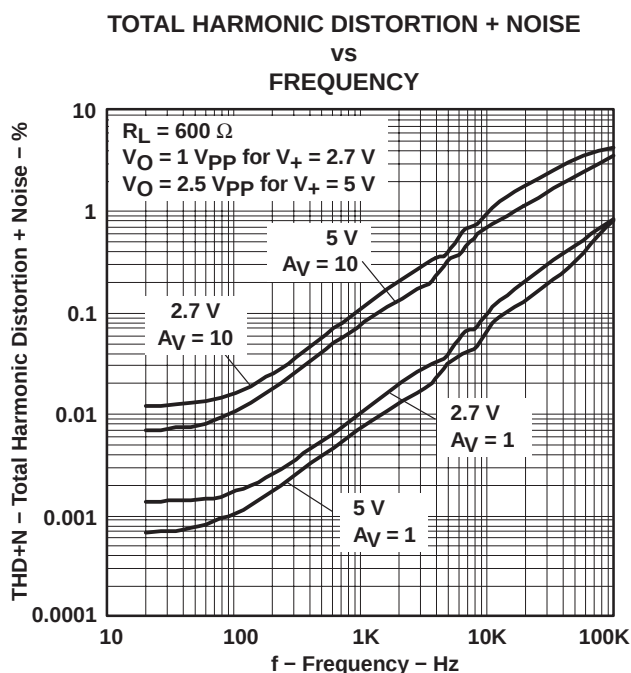


Figure 19

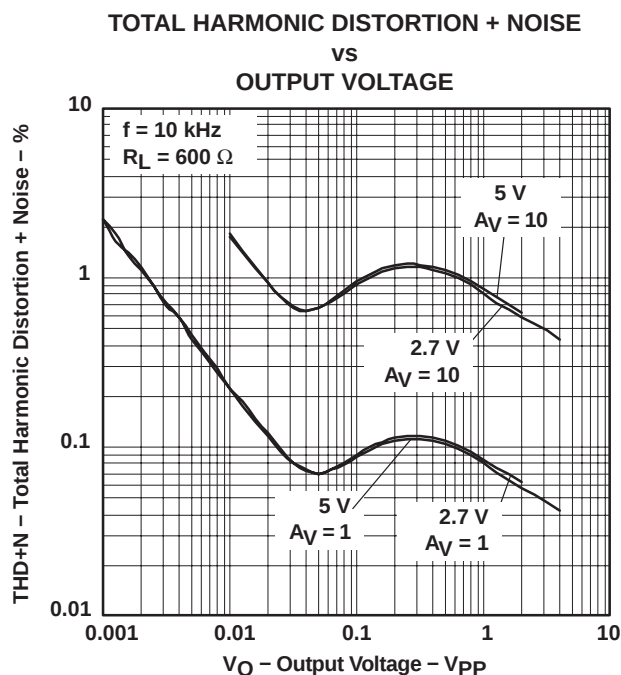


Figure 20

TLV341, TLV342, TLV344

LOW-VOLTAGE RAIL-TO-RAIL OUTPUT CMOS OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLVS568B – JANUARY 2005 – REVISED DECEMBER 2005

TYPICAL CHARACTERISTICS

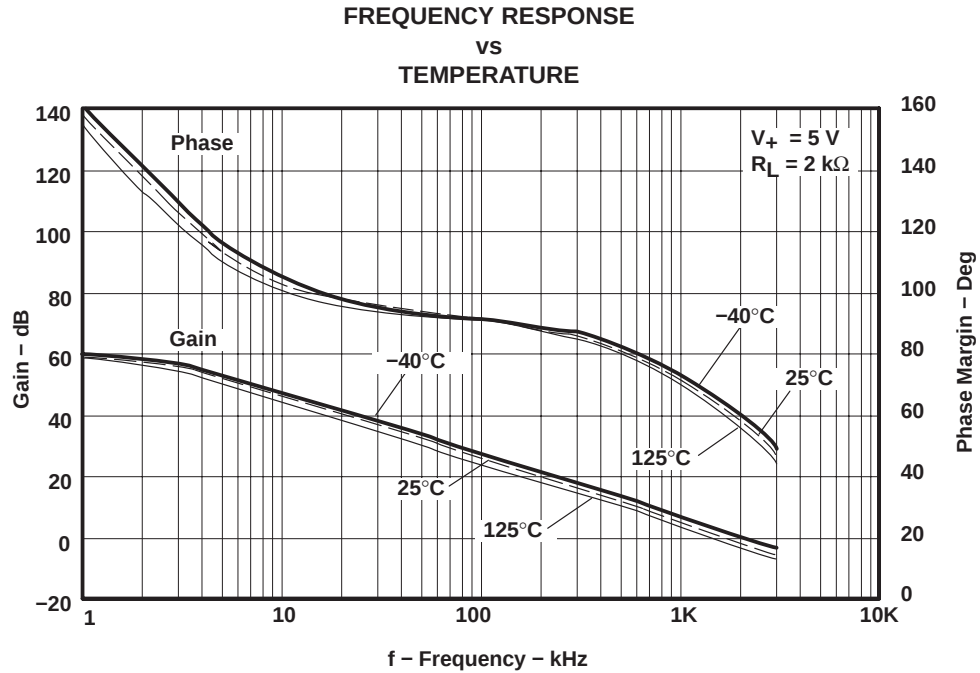


Figure 21

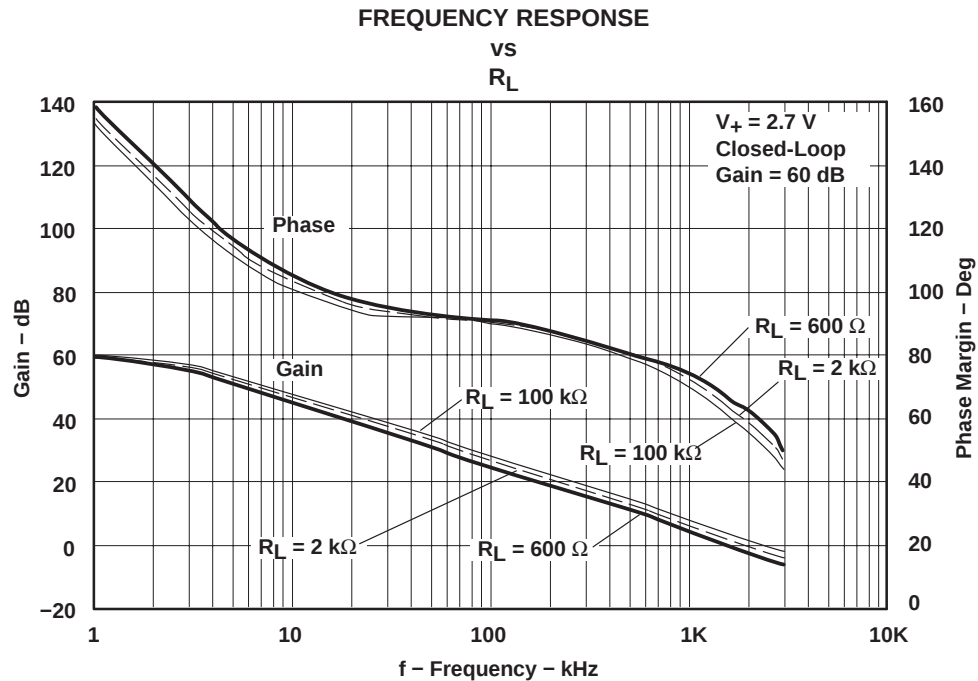


Figure 22

TLV341, TLV342, TLV344

LOW-VOLTAGE RAIL-TO-RAIL OUTPUT CMOS OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLVS568B – JANUARY 2005 – REVISED DECEMBER 2005

TYPICAL CHARACTERISTICS

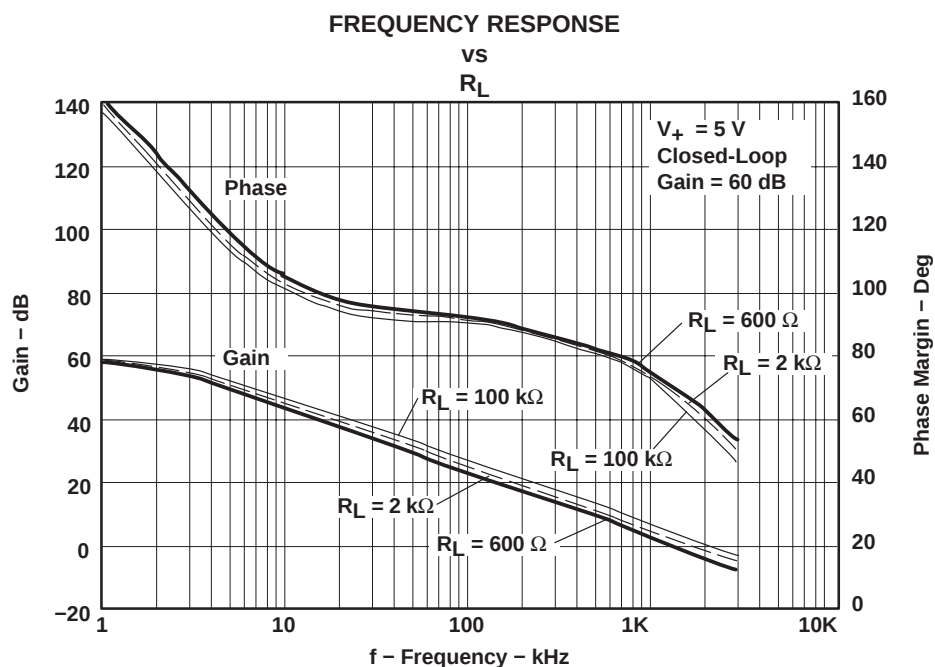


Figure 23

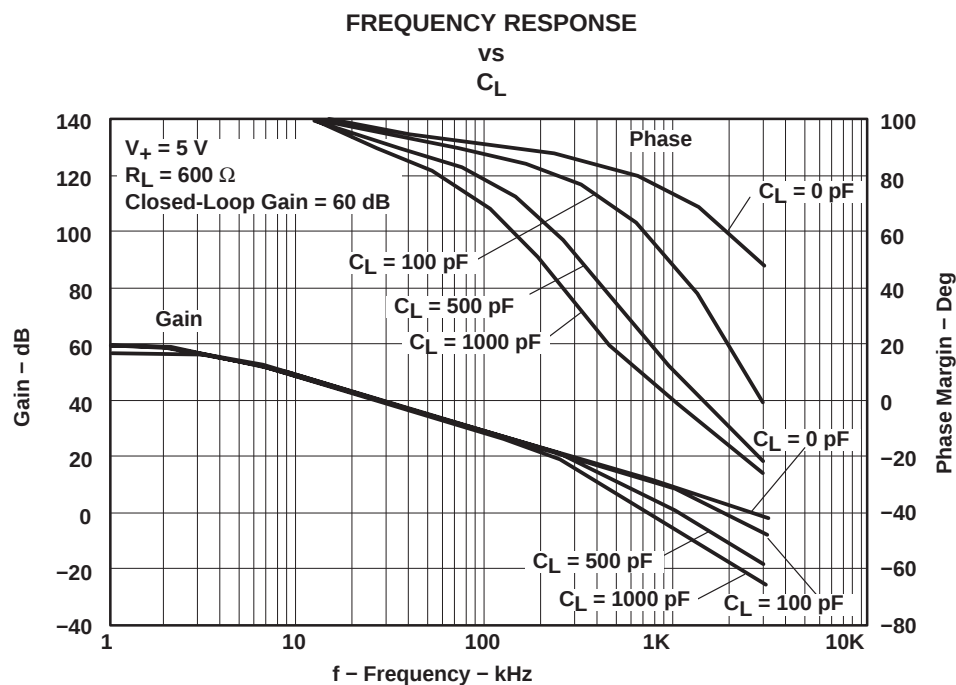


Figure 24

TLV341, TLV342, TLV344

LOW-VOLTAGE RAIL-TO-RAIL OUTPUT CMOS OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLVS568B – JANUARY 2005 – REVISED DECEMBER 2005

TYPICAL CHARACTERISTICS

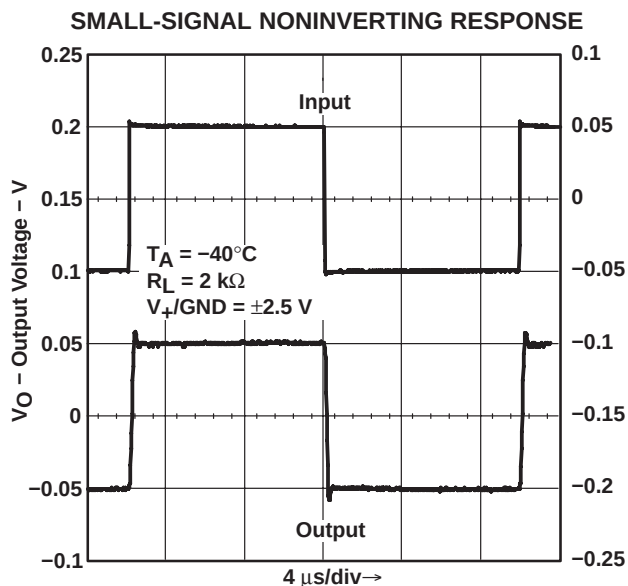


Figure 25

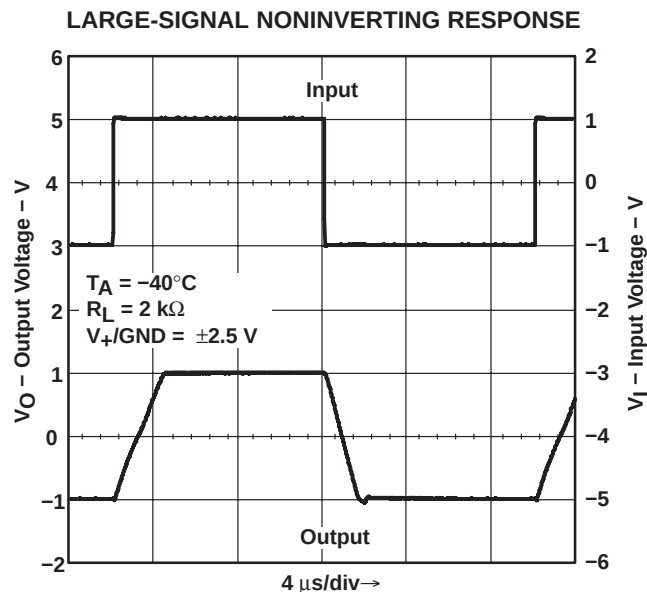


Figure 26

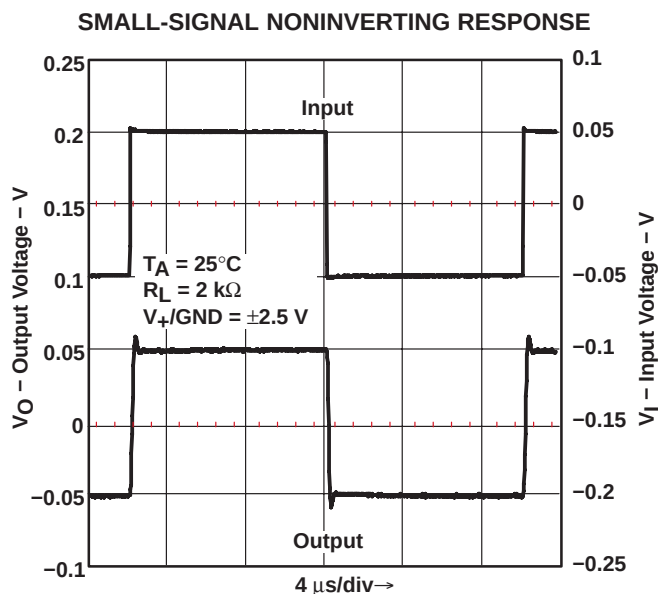


Figure 27

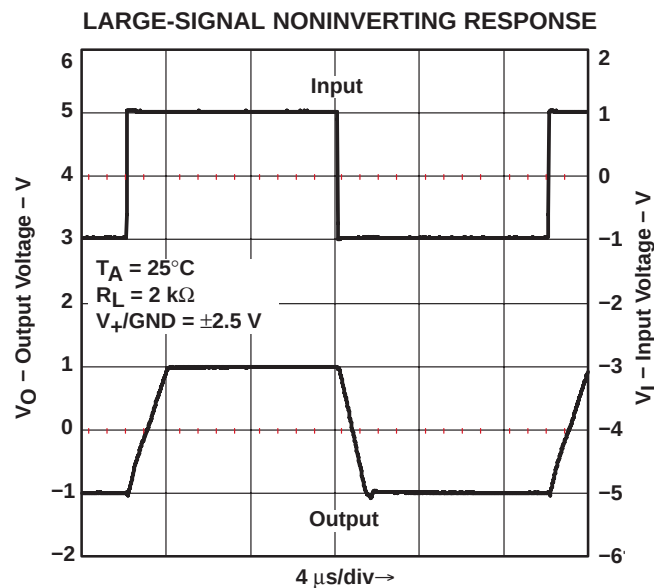


Figure 28

TLV341, TLV342, TLV344

LOW-VOLTAGE RAIL-TO-RAIL OUTPUT CMOS OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLVS568B – JANUARY 2005 – REVISED DECEMBER 2005

TYPICAL CHARACTERISTICS

SMALL-SIGNAL NONINVERTING RESPONSE

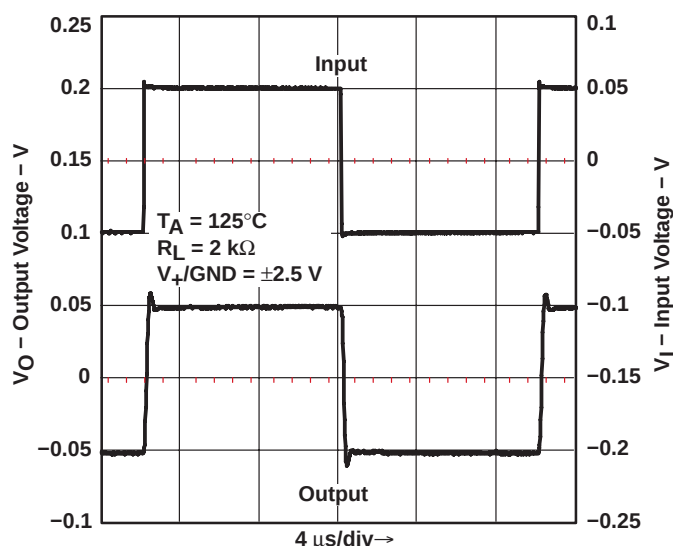


Figure 29

LARGE-SIGNAL NONINVERTING RESPONSE

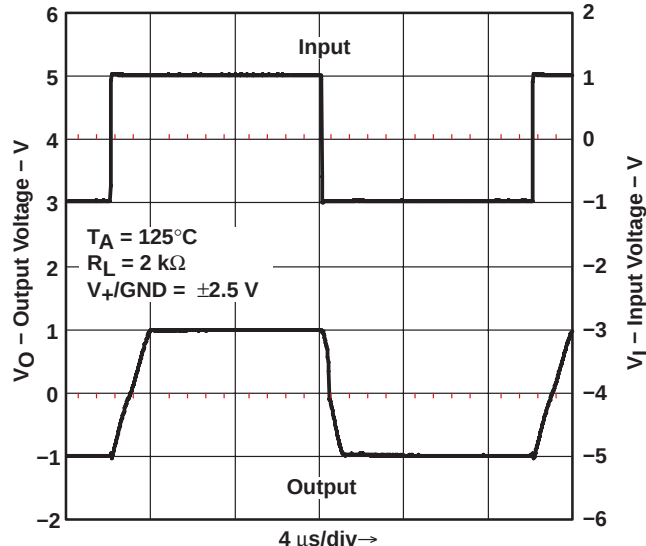


Figure 30

SMALL-SIGNAL INVERTING RESPONSE

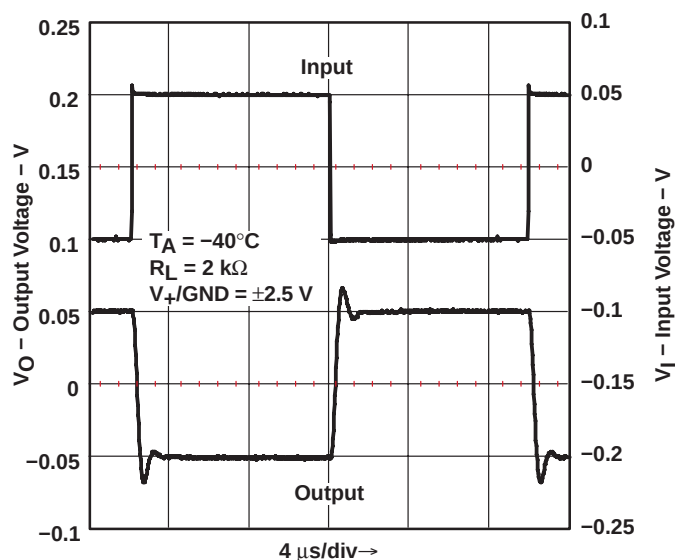


Figure 31

LARGE-SIGNAL INVERTING RESPONSE

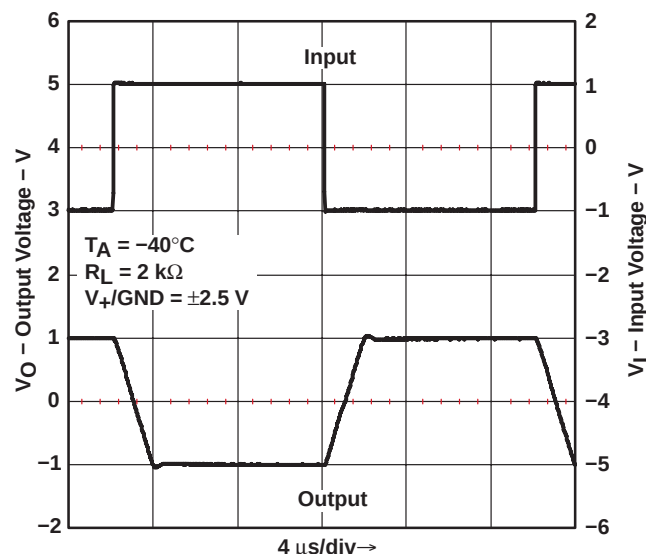


Figure 32

TLV341, TLV342, TLV344

LOW-VOLTAGE RAIL-TO-RAIL OUTPUT CMOS OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLVS568B – JANUARY 2005 – REVISED DECEMBER 2005

TYPICAL CHARACTERISTICS

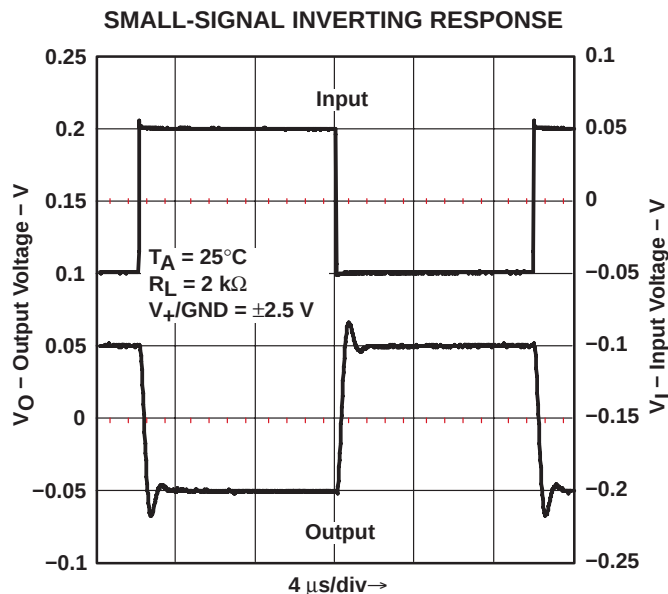


Figure 33

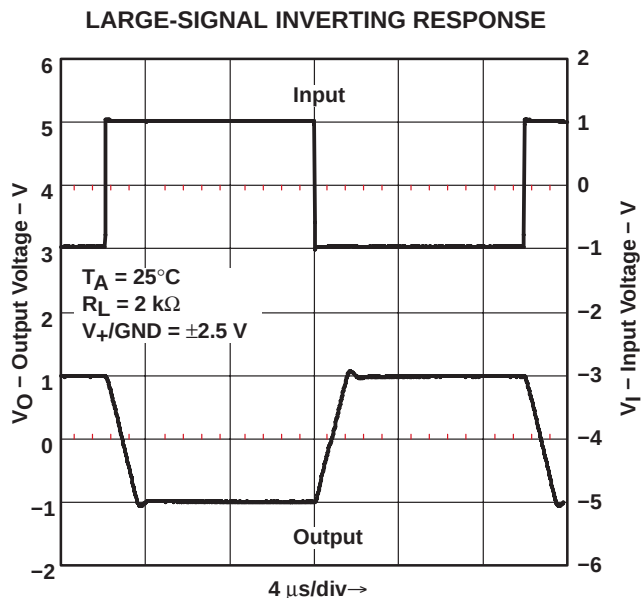


Figure 34

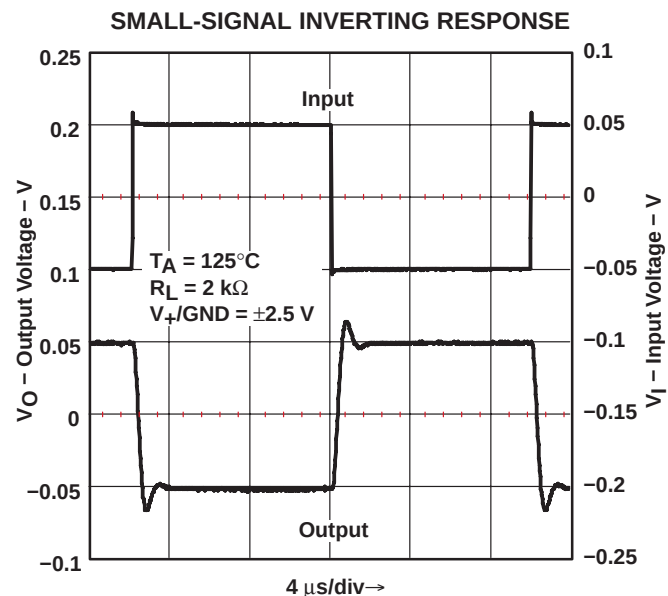


Figure 35

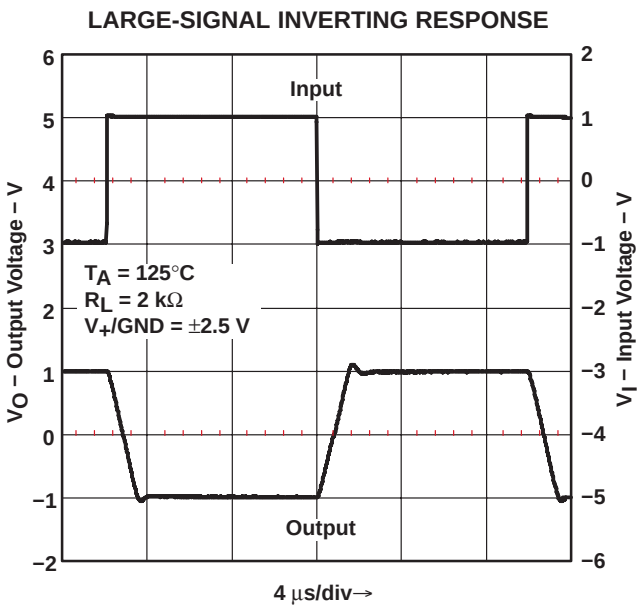


Figure 36

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TLV341AIDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV341AIDBVRE4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV341AIDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV341AIDBVTE4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV341AIDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV341AIDCKRE4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV341AIDCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV341AIDCKTE4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV341IDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV341IDBVRE4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV341IDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV341IDBVTE4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV341IDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV341IDCKRE4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV341IDCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV341IDCKTE4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV341IDRLR	ACTIVE	SOP	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV341IDRLRG4	ACTIVE	SOP	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV342AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV342AIDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV342AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV342AIDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV342ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV342IDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV342IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TLV342IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

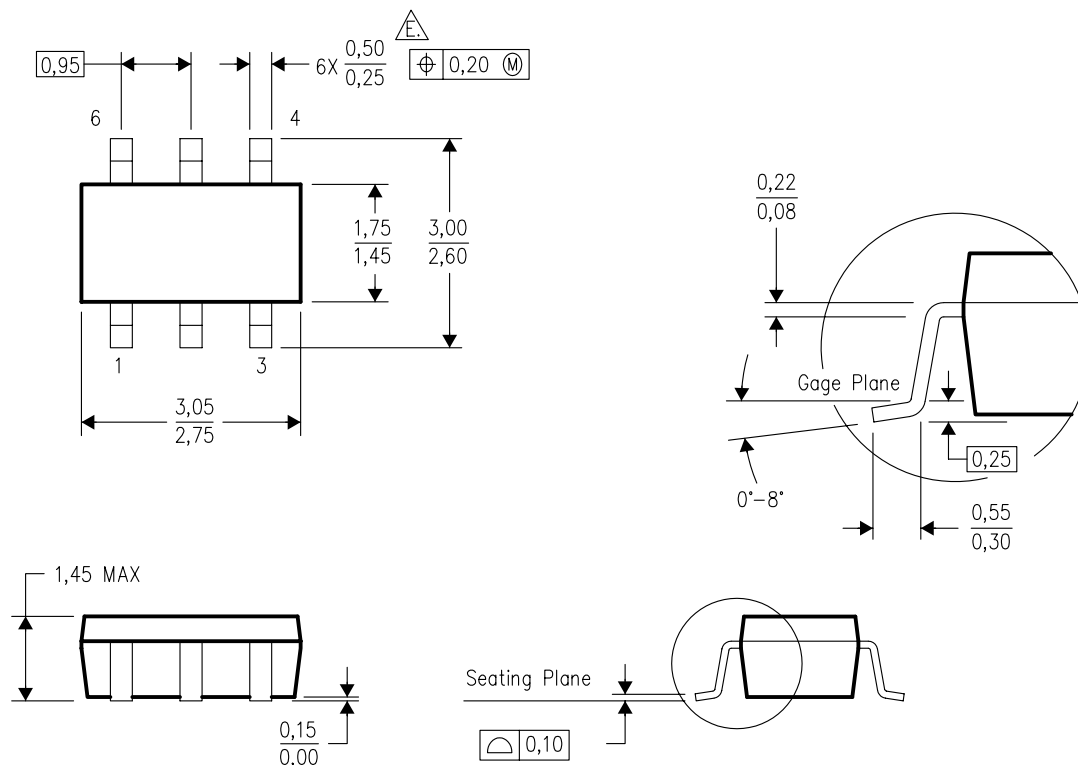
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE

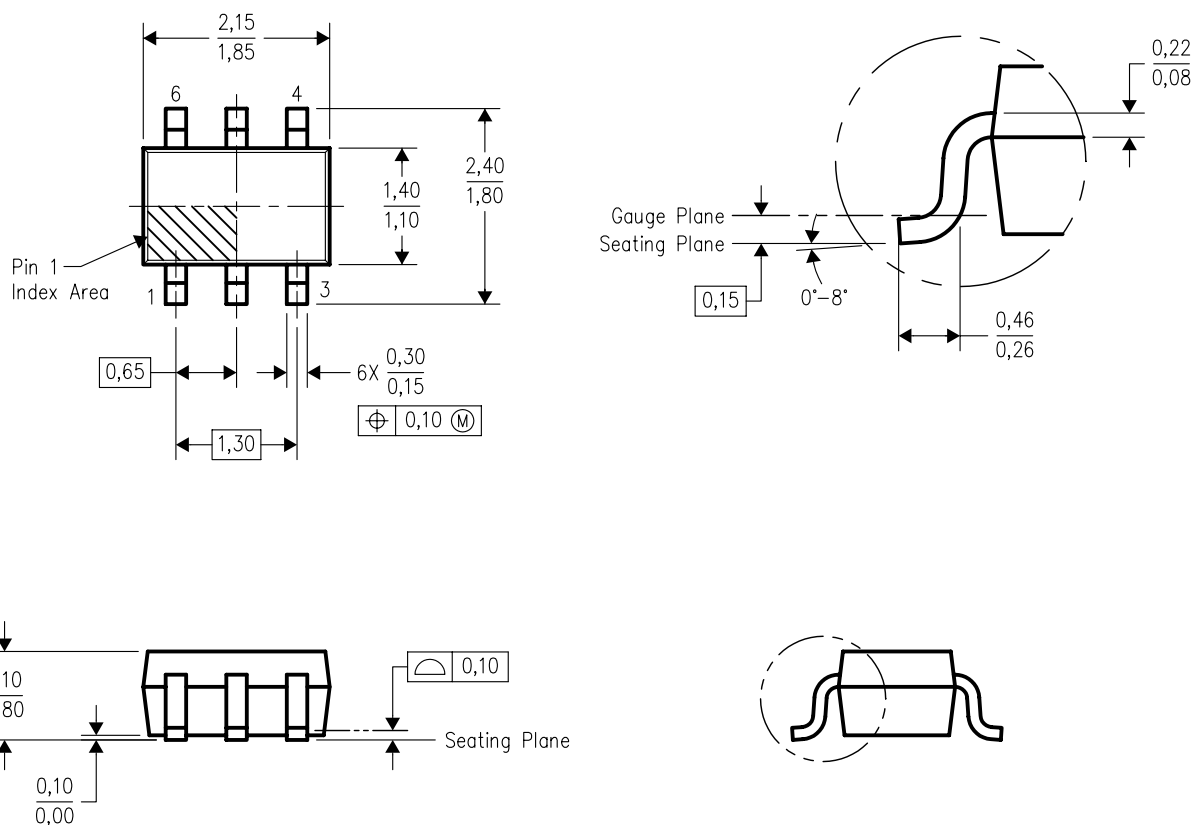


4073253-5/J 10/2005

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
-  Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE

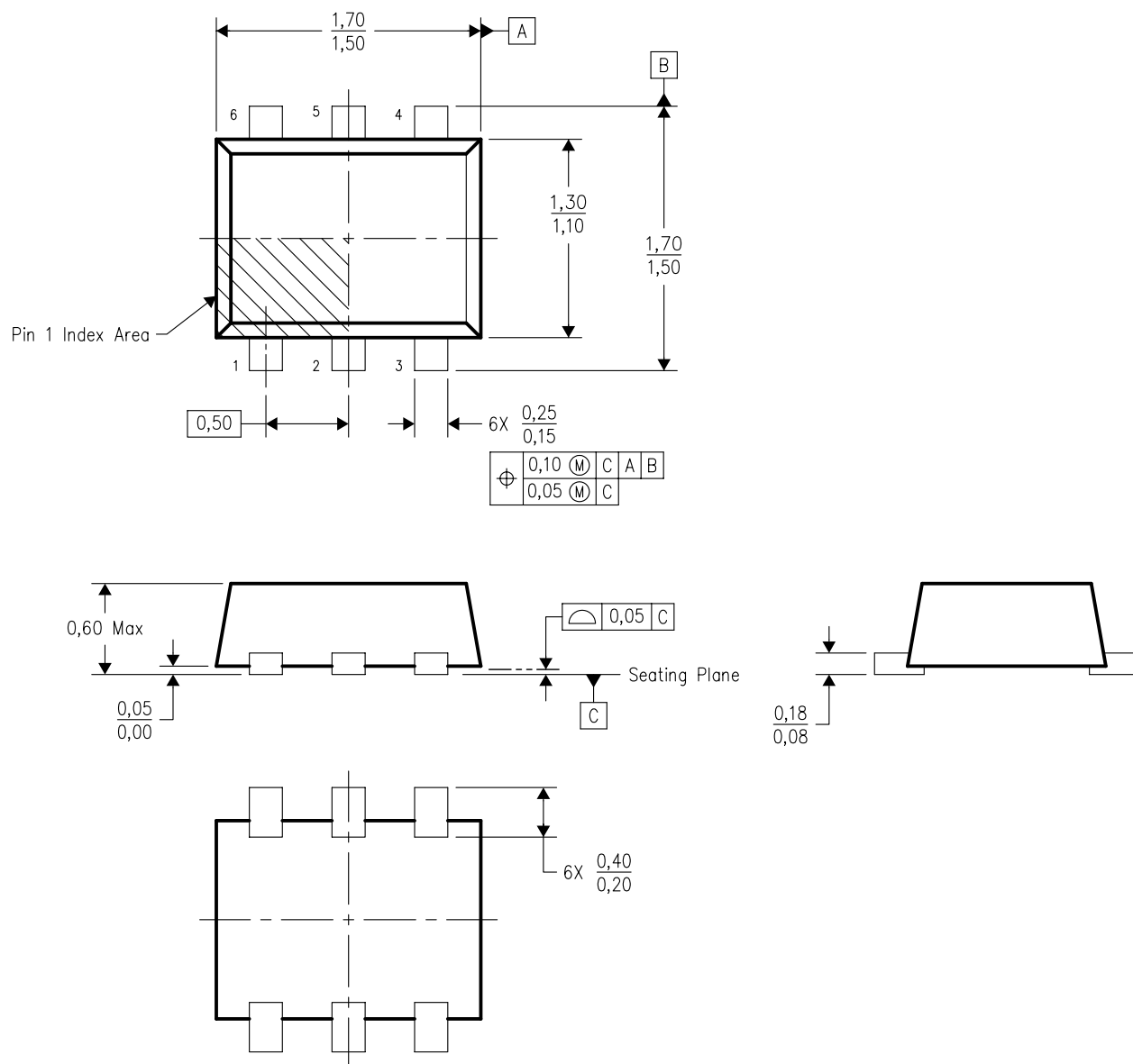


4093553-3/E 10/2005

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-203 variation AB.

DRL (R-PDSO-N6)

PLASTIC SMALL OUTLINE

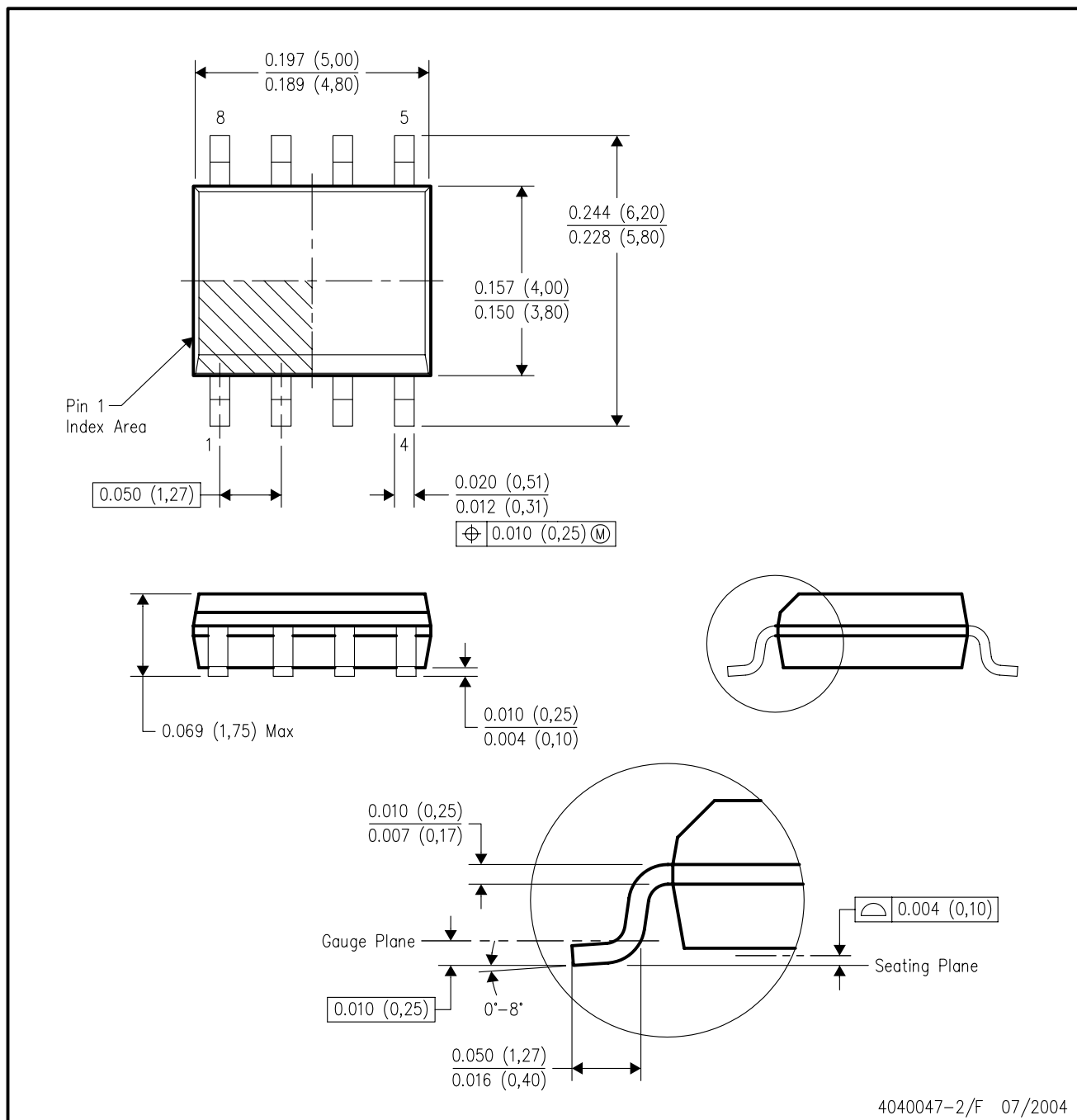


4205622-3/B 07/2004

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. JEDEC package registration is pending.

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AA.

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