MPF970 (SILICON)
MPF971

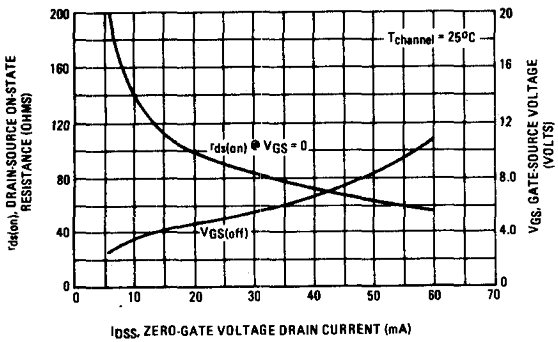
SILICON P-CHANNEL JUNCTION FIELD–EFFECT TRANSISTORS

Depletion Mode (Type A) Junction Field-Effect Transistors designed for chopper and high-speed switching applications.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	30	Vdc
Reverse Gate-Source Voltage	V_{GSR}	30	Vdc
Forward Gate Current	I_{GF}	10	mAdc
Total Device Dissipation @ $T_A = 25^oC$ Derate above 25^oC	P_D	350 2.8	mW mW/^oC
Storage Temperature Range	T_{stg}	-65 to +150	^oC
Operating Temperature Range	$T_{channel}$	-65 to +150	^oC

FIGURE 1 – EFFECT OF I_{DSS} ON DRAIN-SOURCE RESISTANCE AND GATE-SOURCE VOLTAGE



The Zero-Gate-Voltage Drain Current (I_{DSS}), is the principle determinant of other J-FET characteristics. Figure 1 shows the relationship of Gate-Source *Off Voltage ($V_{GS(off)}$) and Drain-Source On Resistance ($r_{ds(on)}$) to I_{DSS}.* Most of the devices will be within ±10% of the values shown in Figure 1. This data will be useful in predicting the characteristic variations for a given part number.

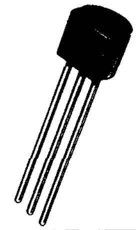
For example:

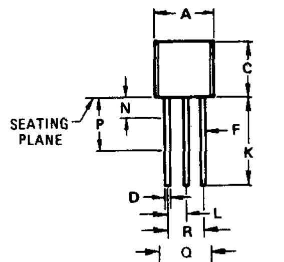
Unknown

$r_{ds(on)}$ and V_{GS} range for an MPF970

The electrical characteristics table indicates that an MPF970 has an I_{DSS} range of 15 to 60 mA. Figure 1 shows $r_{ds(on)}$ = 110 Ohms for I_{DSS} = 15 mA and 56 Ohms for I_{DSS} = 60 mA. The corresponding V_{GS} values are 4.1 volts and 10.8 volts.

P-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS





STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage (I_G = 1.0 μAdc, V_{DS} = 0)		$V_{(BR)GSS}$	30	–	–	Vdc
Gate-Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 10 nAdc)	MPF970	$V_{GS(off)}$	5.0	–	12	Vdc
	MPF971		1.0	–	7.0	
Gate Reverse Current (V_{GS} = 15 Vdc, V_{DS} = 0)		I_{GSS}	–	–	1.0	nAdc
(V_{GS} = 15 Vdc, V_{DS} = 0, T_A = 150°C)			–	–	1.0	μAdc
Drain-Cutoff Current (V_{DS} = 15 Vdc, V_{GS} = 12 Vdc)	MPF970	$I_{D(off)}$	–	–	10	nAdc
(V_{DS} = 15 Vdc, V_{GS} = 12 Vdc, T_A = 150°C)	MPF970		–	–	10	μAdc
(V_{DS} = 15 Vdc, V_{GS} = 7.0 Vdc)	MPF971		–	–	10	nAdc
(V_{DS} = 15 Vdc, V_{GS} = 7.0 Vdc, T_A = 150°C)	MPF971		–	–	10	μAdc
ON CHARACTERISTICS						
Zero-Gate Voltage Drain Current (1) (V_{DS} = 20 Vdc, V_{GS} = 0)	MPF970	I_{DSS}	15	–	60	mAdc
	MPF971		2.0	–	30	
Drain-Source "ON" Voltage (I_D = 10 mAdc, V_{GS} = 0)		$V_{DS(on)}$	–	–	1.5	Vdc
(I_D = 1.5 mAdc, V_{GS} = 0)			–	–	1.5	
Static Drain-Source "ON" Resistance (I_D = 1.0 mAdc, V_{GS} = 0)	MPF970	$r_{DS(on)}$	–	–	100	Ohms
	MPF971		–	–	250	
SMALL-SIGNAL CHARACTERISTICS						
Drain-Source "ON" Resistance (V_{GS} = 0, I_D = 0, f = 1.0 kHz)	MPF970	$r_{ds(on)}$	–	–	100	Ohms
	MPF971		–	–	250	
Input Capacitance (V_{GS} = 12 Vdc, V_{DS} = 0, f = 1.0 MHz)	MPF970	C_{iss}	–	–	12	pF
(V_{GS} = 7.0 Vdc, V_{DS} = 0, f = 1.0 MHz)	MPF971		–	–	12	
Reverse Transfer Capacitance (V_{GS} = 12 Vdc, V_{DS} = 0, f = 1.0 MHz)	MPF970	C_{rss}	–	–	5.0	pF
(V_{GS} = 7.0 Vdc, V_{DS} = 0, f = 1.0 MHz)	MPF971		–	–	5.0	
SWITCHING CHARACTERISTICS (See Figure 6, R_K = 0) (1)						
Turn-On Time ($I_{D(on)}$ = 10 mAdc, $V_{GS(off)}$ = 12 Vdc)	MPF970	t_{on}	–	3.5	8.0	ns
($I_{D(on)}$ = 1.5 mAdc, $V_{GS(off)}$ = 7.0 Vdc)	MPF971		–	5.0	10	
Rise Time ($I_{D(on)}$ = 10 mAdc, $V_{GS(off)}$ = 12 Vdc)	MPF970	t_r	–	2.0	5.0	ns
($I_{D(on)}$ = 1.5 mAdc, $V_{GS(off)}$ = 7.0 Vdc)	MPF971		–	3.0	5.0	
Turn-Off Time ($I_{D(on)}$ = 10 mAdc, $V_{GS(off)}$ = 12 Vdc)	MPF970	t_{off}	–	13	25	ns
($I_{D(on)}$ = 1.5 mAdc, $V_{GS(off)}$ = 7.0 Vdc)	MPF971		–	88	120	
Fall Time ($I_{D(on)}$ = 10 mAdc, $V_{GS(off)}$ = 12 Vdc)	MPF970	t_f	–	9.0	15	ns
($I_{D(on)}$ = 1.5 mAdc, $V_{GS(off)}$ = 7.0 Vdc)	MPF971		–	68	80	

(1) Pulse Test: Pulse Width ≤ 100 μs, Duty Cycle ≤ 1.0%.

FIGURE 2 – TURN-ON DELAY TIME

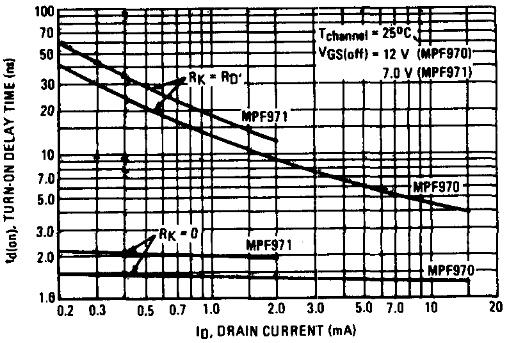


FIGURE 3 – RISE TIME

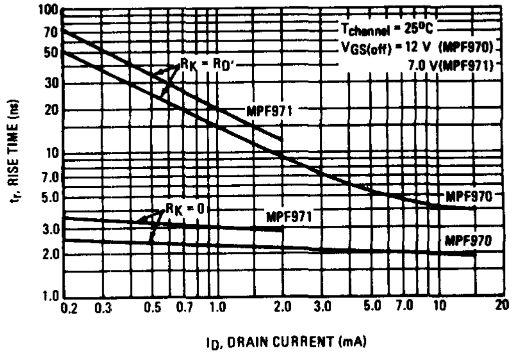


FIGURE 4 – TURN-OFF DELAY TIME

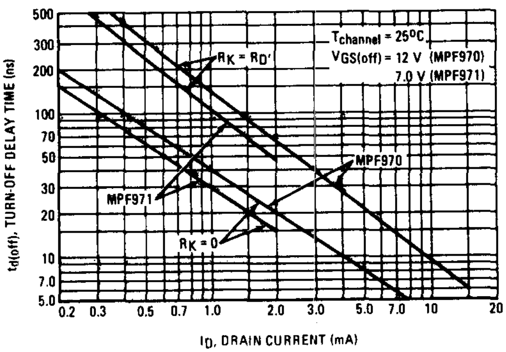


FIGURE 5 – FALL TIME

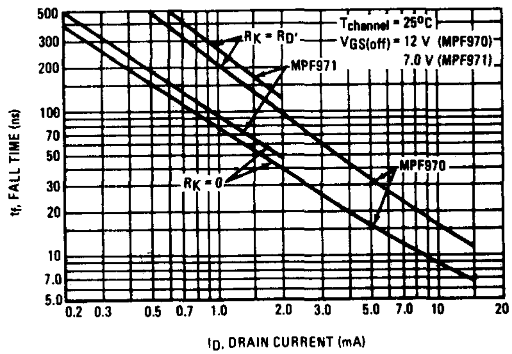
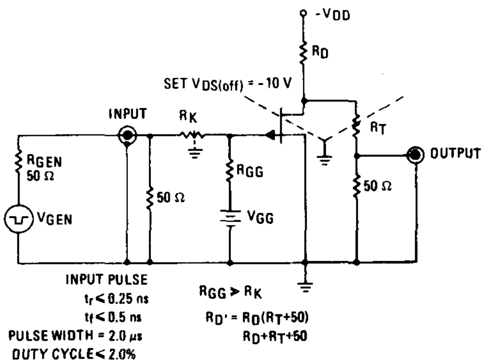


FIGURE 6 – SWITCHING TIME TEST CIRCUIT



NOTE 1

The switching characteristics shown above were measured using a test circuit similar to Figure 6. At the beginning of the switching interval, the gate voltage is at Gate Supply Voltage ($+V_{GG}$). The Drain-Source Voltage (V_{DS}) is slightly lower than Drain Supply Voltage (V_{DD}) due to the voltage divider. Thus Reverse Transfer Capacitance (C_{rss}) or Gate-Drain Capacitance (C_{gd}) is charged to $V_{GG} + V_{DS}$.

During the turn-on interval, Gate-Source Capacitance (C_{gs}) discharges through the series combination of R_{Gen} and R_K. C_{gd} must discharge to $V_{DS(on)}$ through R_G and R_K in series with the parallel combination of effective load impedance (R'_D) and Drain-Source Resistance (r_{ds}). During the turn-off, this charge flow is reversed.

Predicting turn-on time is somewhat difficult as the channel resistance r_{ds} is a function of the gate-source voltage. While C_{gs} discharges, V_{GS} approaches zero and r_{ds} decreases. Since C_{gd} discharges through r_{ds}, turn-on time is non-linear. During turn-off, the situation is reversed with r_{ds} increasing as C_{gd} charges.

The above switching curves show two impedance conditions; 1) R_K is equal to R_D, which simulates the switching behavior of *cascaded stages where the driving source impedance* is normally the load impedance of the previous stage, and 2) $R_K = 0$ (low impedance) the driving source impedance is that of the generator.

FIGURE 7 – TYPICAL FORWARD TRANSFER ADMITTANCE

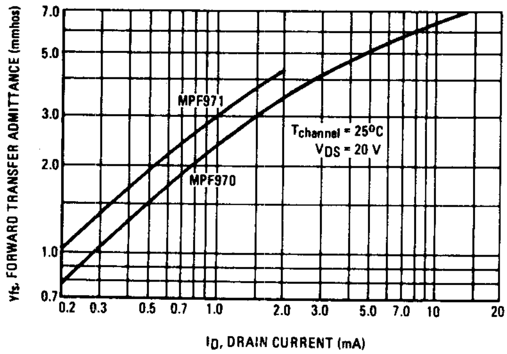


FIGURE 8 – TYPICAL CAPACITANCE

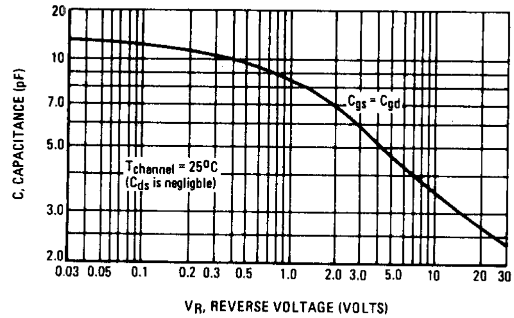


FIGURE 9 – EFFECT OF GATE-SOURCE VOLTAGE ON DRAIN-SOURCE RESISTANCE

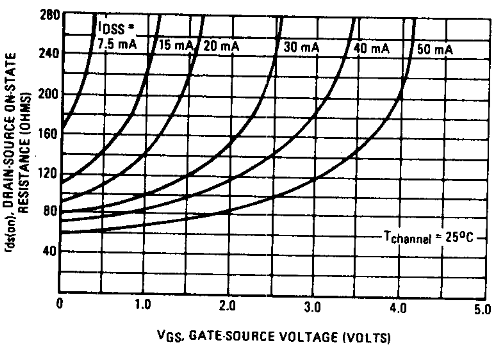


FIGURE 10 – EFFECT OF TEMPERATURE ON DRAIN-SOURCE ON-STATE RESISTANCE

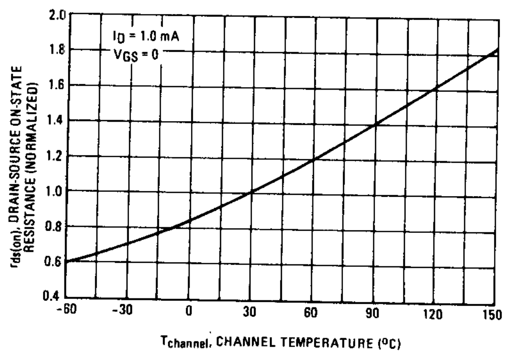
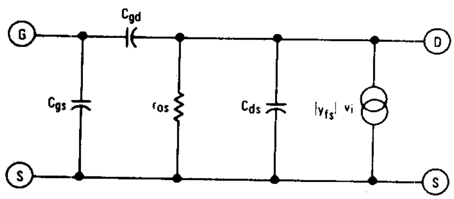


FIGURE 11 – LOW FREQUENCY CIRCUIT MODEL



$y_{is} = j\omega C_{iss}$
$y_{os} = 1/r_{oss} + j\omega C_{oss}$
$y_{fs} = |y_{fs}|$
$y_{rs} = -j\omega C_{rss}$

$C_{iss} = C_{gd} + C_{gs}$
$C_{rss} = C_{gd}$
$C_{oss} = C_{gd} + C_{ds},\ C_{ds} \approx 0$