36 V, 19 MHz, Low Noise, Low Bias Current, JFET Operational Amplifier

ADA4627-1

FEATURES

Low offset voltage: 200 µV maximum
Offset drift: 1 µV/°C typical
Very low input bias current: 5 pA maximum
Extended temperature range: −40°C to +125°C
±5 V to ±15 V dual supply
Guaranteed GBW: 16 MHz
Voltage noise: 6.1 nV/√Hz at 1 kHz
High slew rate: 60 V/µs
High gain: 120 dB typical
High CMRR: 116 dB typical
High PSRR: 112 dB typical
Low supply current: 7.5 mA maximum

APPLICATIONS

High impedance sensors
Photodiode amplifier
Precision instrumentation
Phase-locked loop filters
High end, professional audio
DAC output amplifier
ATE
Medical

PIN CONFIGURATIONS

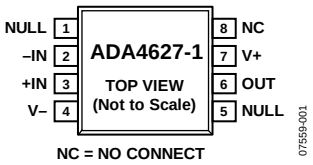

Figure 1. 8-Lead SOIC_N (R-8)

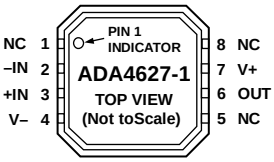

Figure 2. 8-Lead LFCSP_VD (CP-8-2)

GENERAL DESCRIPTION

The ADA4627-1 is a wide bandwidth precision amplifier featuring low noise, very low offset, drift, and bias current. Operation is specified from ±5 V to ±15 V dual supply.

The ADA4627-1 provides benefits previously found in few amplifiers. This amplifier combines the best specifications of precision dc and high speed ac op amps.

With a typical offset voltage of only 70 µV, drift of less than 1 µV/°C, and noise of only 0.86 µV p-p (0.1 Hz to 10 Hz), the ADA4627-1 is suited for applications in which error sources cannot be tolerated.

The ADA4627-1 is specified for both the industrial temperature range of −25°C to +85°C and the extended industrial temperature range of −40°C to +125°C. It is available in tiny 8-lead LFCSP and 8-lead SOIC packages.

The ADA4627-1 is a member of a growing series of high speed, precision op amps offered by Analog Devices, Inc. (see Table 1).

Table 1. High Speed Precision Op Amps

Supply	5 V Low Cost	5 V	26 V Low Power	30 V Low Cost	30 V
Single	AD8615	AD8651	AD8610	AD8510	ADA4627-1
Dual	AD8616	AD8652	AD8620	AD8512	
Quad	AD8618			AD8513	

Rev. B

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9/09—Rev. 0 to Rev. A

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7/09—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—30 V OPERATION

V_{SY} = ±15 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 2.

			B Grade			A Grade			
Parameter	**Symbol**	**Test Conditions/Comments**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
INPUT CHARACTERISTICS									
Offset Voltage[1]	V_{OS}			70	200		120	300	µV
		−40°C ≤ T_A ≤ +85°C			350			410	µV
		−40°C ≤ T_A ≤ +125°C			400			660	µV
Offset Voltage Drift, Average	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		1	2		1	3	µV/°C
Power Supply Rejection Ratio	PSRR	V_{SY} = ±4.5 V to ±18 V	106	112		103	108		dB
		−40°C ≤ T_A ≤ +125°C	101			99			dB
Input Bias Current[2]	I_B			1	5		1	5	pA
		−40°C ≤ T_A ≤ +85°C			0.5			0.5	nA
		−40°C ≤ T_A ≤ +125°C			2			2	nA
Input Offset Current	I_{OS}			0.5	5		0.5	5	pA
		−40°C ≤ T_A ≤ +85°C			0.5			0.5	nA
		−40°C ≤ T_A ≤ +125°C			2			2	nA
NOISE PERFORMANCE									
Voltage Noise Density	e_n	f = 10 Hz		16.5	40		16.5	40	nV/√Hz
		f = 100 Hz		7.9	20		7.9	20	nV/√Hz
		f = 1 kHz		6.1	8		6.1	8	nV/√Hz
		f = 10 kHz		4.8	6		4.8	6	nV/√Hz
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.69	1.6		0.69	1.6	µV p-p
Current Noise Density	i_n	f = 100 Hz		1.6			2.5		fA/√Hz
Current Noise	i_n p-p	0.1 Hz to 10 Hz		30			48		fA p-p
Input Resistance	R_{IN}			10			10		TΩ
Input Capacitance, Differential Mode	C_{INDM}			8			8		pF
Input Capacitance, Common Mode	C_{INCM}			7			7		pF
Input Voltage Range			−11		+11	−11		+11	V
		−40°C ≤ T_A ≤ +125°C	−10.5		+10.5	−10.5		+10.5	V
Common-Mode Rejection Ratio	CMRR	−40°C ≤ T_A ≤ +125°C, V_{CM} = −11 V to +11 V	106	116		100	110		dB
		V_{CM} = −10.5 V to +10.5 V	98			97			dB
Large Signal Voltage Gain	A_{VO}	R_L = 1 kΩ, V_O = −10 V to +10 V	112	120		106	120		dB
		−40 ≤ T_A ≤ +85°C	110			104			dB
		−40 ≤ T_A ≤ +125°C	102			100			dB
DYNAMIC PERFORMANCE									
Slew Rate	SR	10 V step, R_L = 1 kΩ, C_L = 100 pF, A_V = +1	40	56/78[3]		40	56/78[3]		V/µs
	SR	10 V step, R_L = 1 kΩ, C_L = 100 pF, R_s = R_f = 1 kΩ, A_V = −1	40	82/84[3]		40	82/84[3]		V/µs
Settling Time to 0.01%	t_S	V_{IN} = 10 V step, C_L = 35 pF, R_L = 1 kΩ, A_V = −1		550			550		ns
Settling Time to 0.1%	t_S	V_{IN} = 10 V step, C_L = 35 pF, R_L = 1 kΩ, A_V = −1		450			450		ns
Gain Bandwidth Product	GBP	R_L = 1 kΩ, C_L = 20 pF, A_V = 1	16[4]	19		16[4]	19		MHz
Phase Margin	Φ_M	R_L = 1 kΩ, C_L = 20 pF, A_V = 1		72			72		Degrees
Total Harmonic Distortion + Noise	THD + N	f = 1 kHz, A_V = 1		0.000045			0.000045		%

Parameter	Symbol	Test Conditions/Comments	B Grade			A Grade			Unit
			Min	Typ	Max	Min	Typ	Max	
POWER SUPPLY									
Supply Current per Amplifier	I_{SY}	I_O = 0 mA		±7.0	±7.5		±7.0	±7.5	mA
		−40°C ≤ T_A ≤ +125°C			±7.8			±7.8	mA
OUTPUT CHARACTERISTICS									
Output Voltage High	V_{OH}	R_L = 1 kΩ to V_{CM}	12.0	12.3		12.0	12.3		V
		−40°C ≤ T_A ≤ +85°C	11.8			11.8			V
		−40°C ≤ T_A ≤ +125°C	11.7			11.7			V
Output Voltage Low	V_{OL}	R_L = 1 kΩ to V_{CM}		−12.7	−12.3	−12.7	−12.3		V
		−40°C ≤ T_A ≤ +85°C			−12.1		−12.1		V
		−40°C ≤ T_A ≤ +125°C			−12.0		−12.0		V
Output Current	I_{OUT}	V_O = ±10 V		±45			±45		mA
Short-Circuit Current	I_{SC}	T_A = 25°C		+70/−55			+70/−55		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = −100		41			41		Ω

[1] V_{OS} is measured fully warmed-up.
[2] Tested/extrapolated from 125°C.
[3] Rising/falling.
[4] Not tested. Guaranteed by simulation and characterization.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	36 V
Input Voltage Range[1]	(V–) – 0.3 V to (V+) + 0.3 V
Input Current[1]	±10 mA
Differential Input Voltage[2]	$\pm V_{SY}$
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C
ESD Human Body Model	2.5 kV

[1] Input pin has clamp diodes to the power supply pins. Input current should be limited to 10 mA or less whenever input signals exceed the power supply rail by 0.3 V.
[2] Differential input voltage is limited to ±30 V or the supply voltage, whichever is less.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. This was measured using a standard two-layer board. For the LFCSP package, the exposed pad should be soldered to a copper plane.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC_N (R-8)	155	45	°C/W
8-Lead LFCSP (CP-8-2)	77	14	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

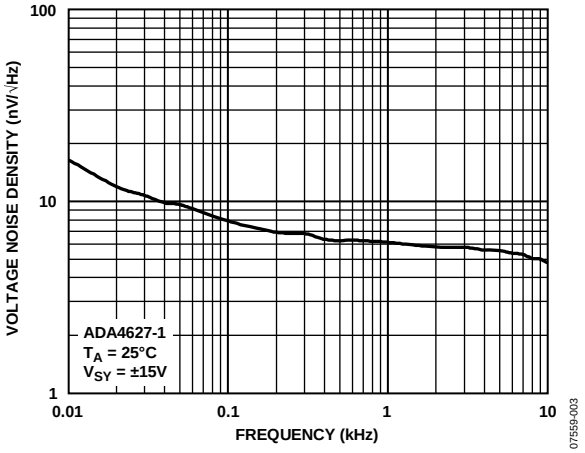

Figure 3. Voltage Noise Density

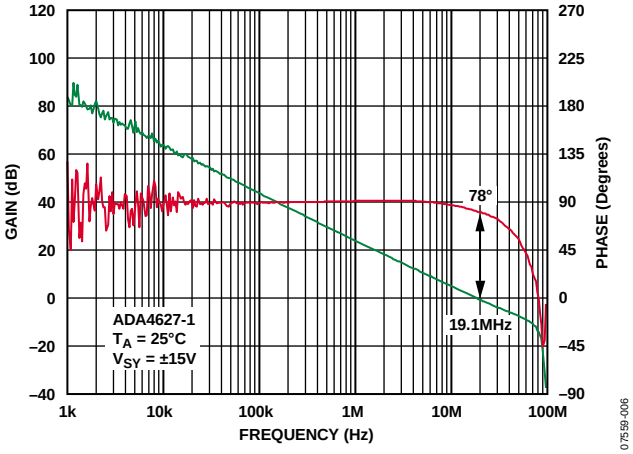

Figure 6. Open-Loop Gain and Phase vs. Frequency

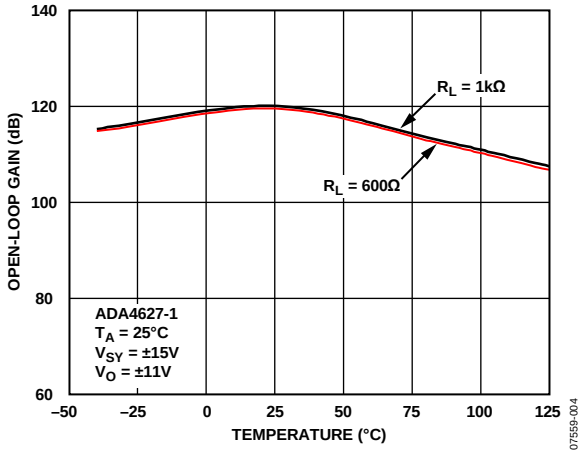

Figure 4. Open-Loop Gain vs. Temperature

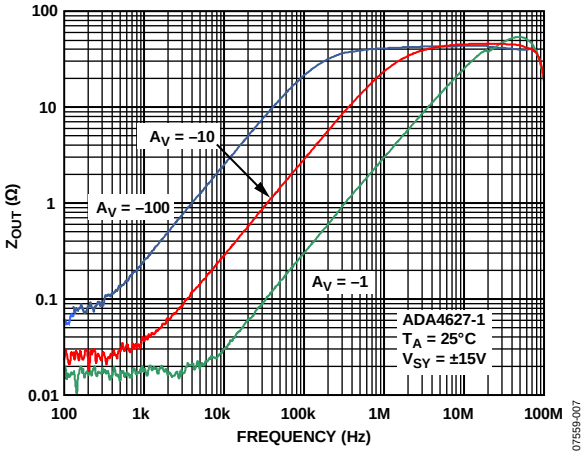

Figure 7. Closed-Loop Z_{OUT} vs. Frequency

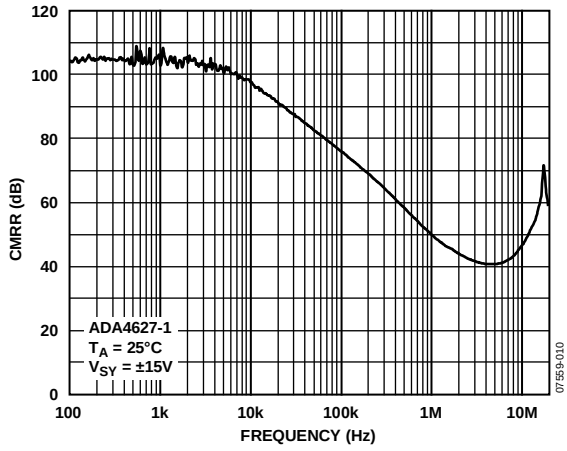

Figure 5. CMRR vs. Frequency

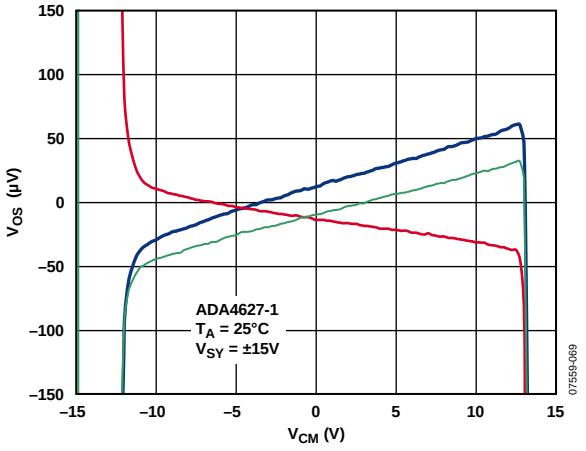

Figure 8. V_{OS} vs. Common-Mode Voltage

T_A = 25°C, unless otherwise noted.

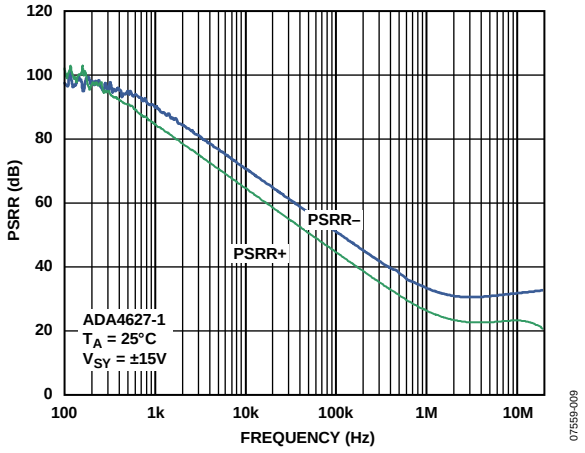

Figure 9. PSRR vs. Frequency

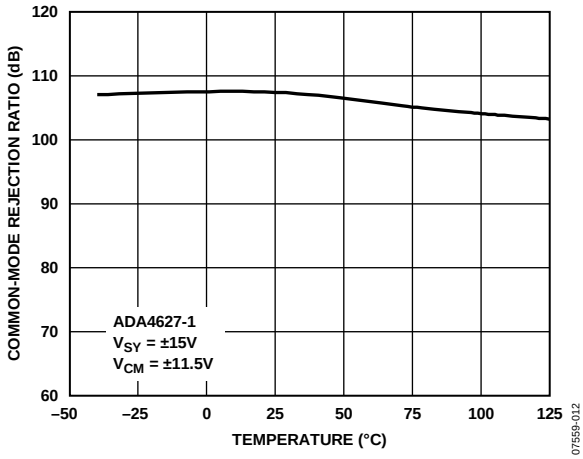

Figure 12. CMRR vs. Temperature

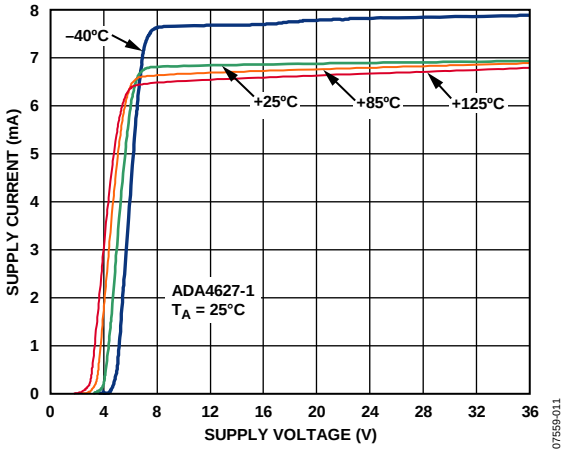

Figure 10. Supply Current vs. Supply Voltage and Temperature

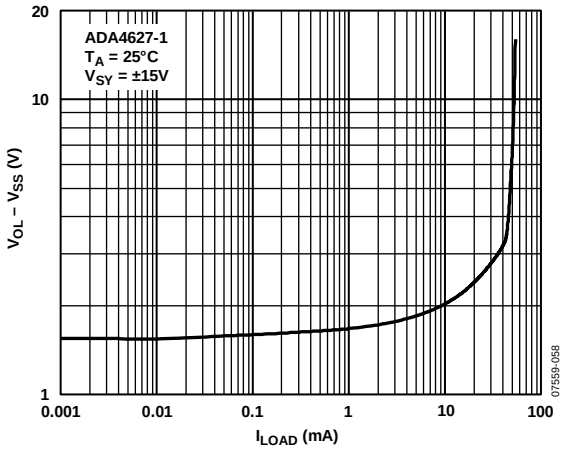

Figure 13. V_{OUT} Sinking vs. I_{LOAD} Current

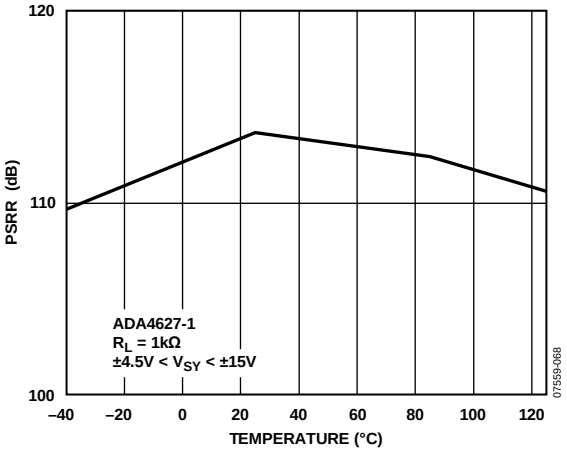

Figure 11. PSRR vs. Temperature

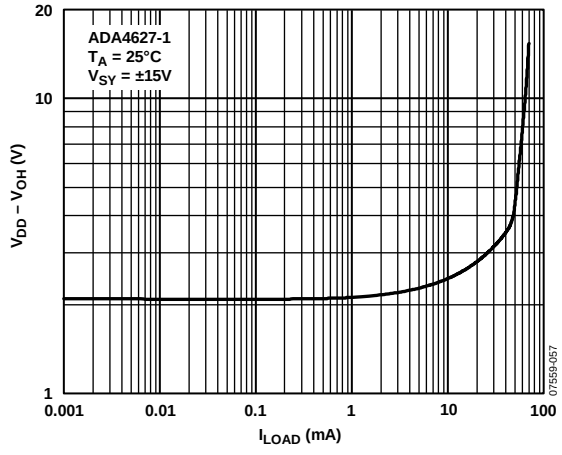

Figure 14. V_{OUT} Sourcing vs. I_{LOAD} Current

T_A = 25°C, unless otherwise noted.

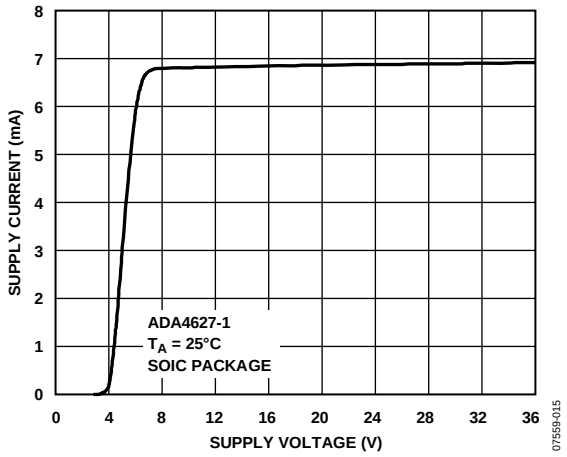

Figure 15. Supply Current vs. Supply Voltage

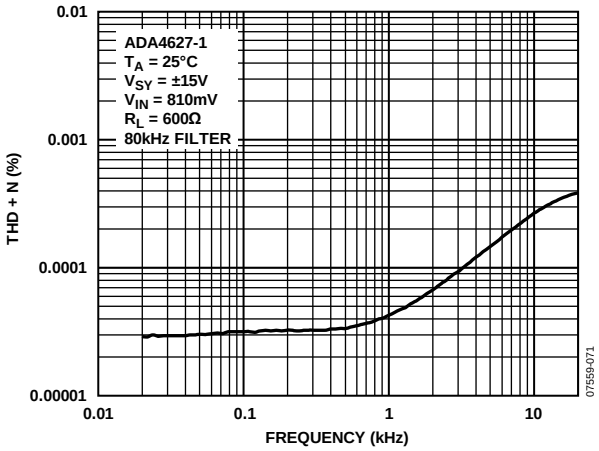

Figure 18. THD + N vs. Frequency

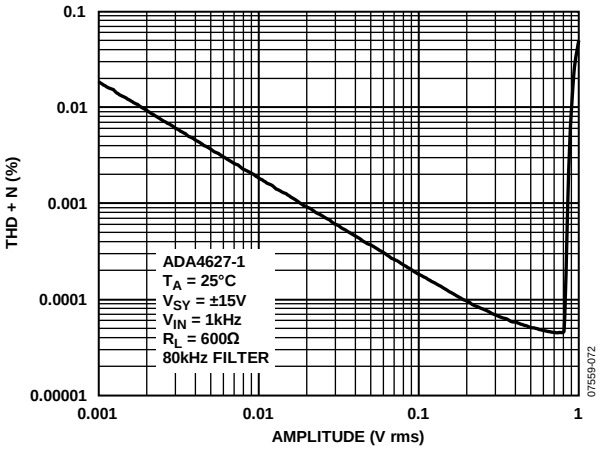

Figure 16. THD + N vs. V_{IN}

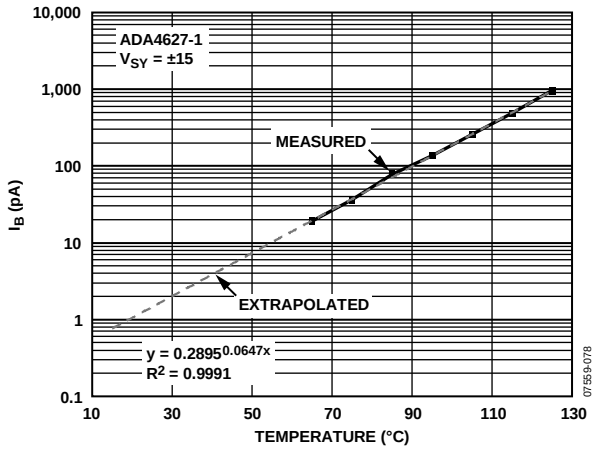

Figure 19. Input Bias Current vs. Temperature

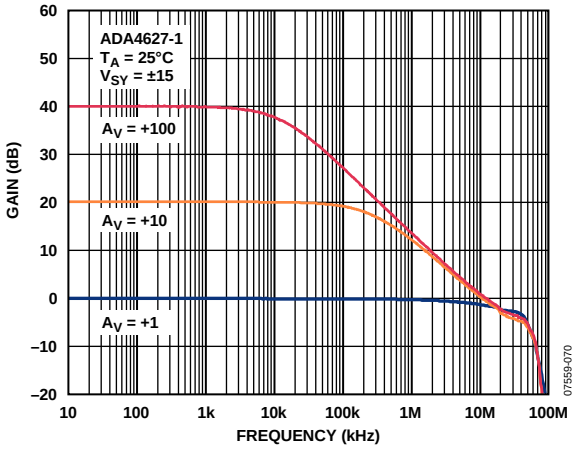

Figure 17. Closed-Loop Gain vs. Frequency

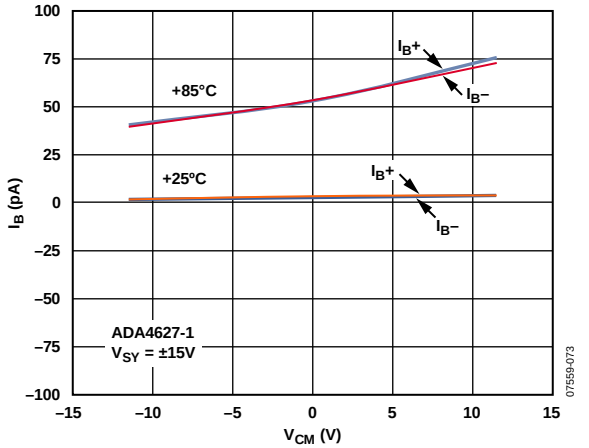

Figure 20. Input Bias Current vs. V_{CM} and Temperature

T_A = 25°C, unless otherwise noted.

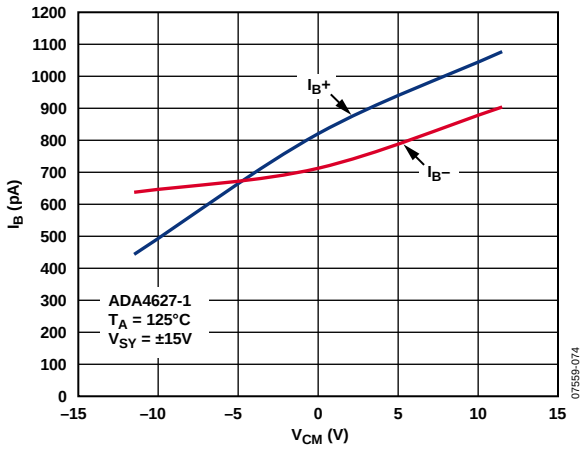

Figure 21. Input Bias Current vs. V_{CM} at 125°C

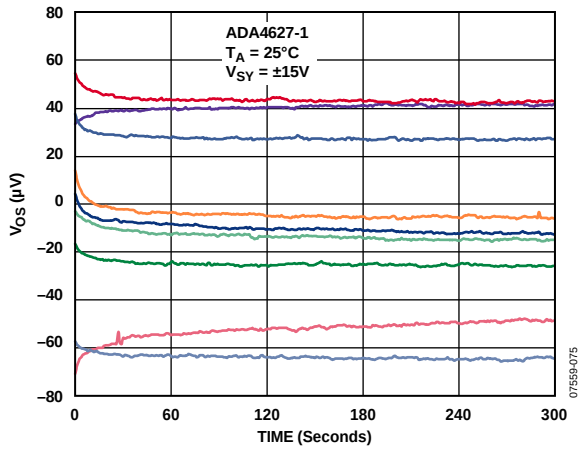

Figure 22. Input Offset Voltage vs. Time

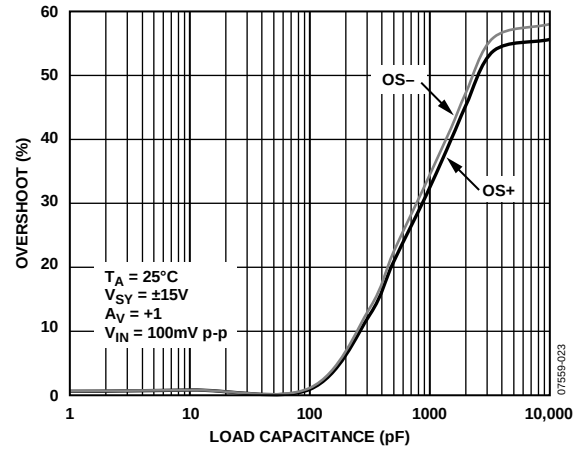

Figure 23. Small Signal Overshoot vs. Load Capacitance

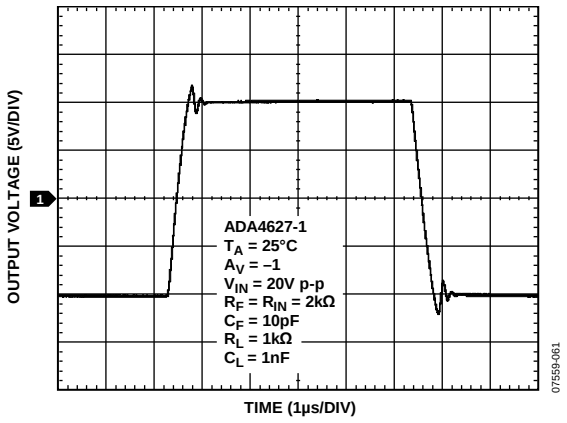

Figure 24. Large Signal Transient Response

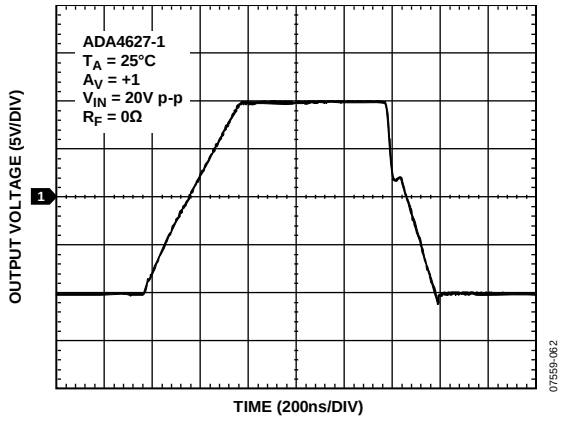

Figure 25. Large Signal Transient Response

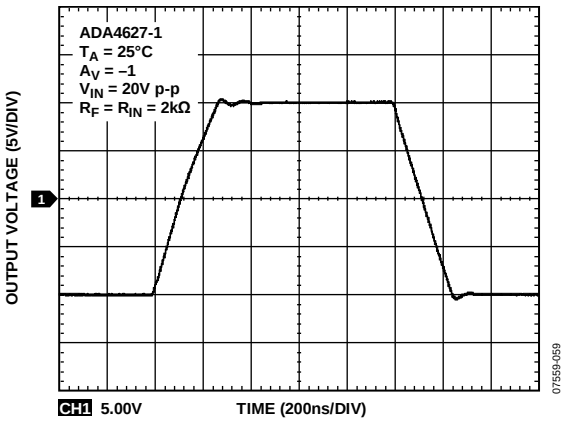

Figure 26. Large Signal Transient Response

T_A = 25°C, unless otherwise noted.

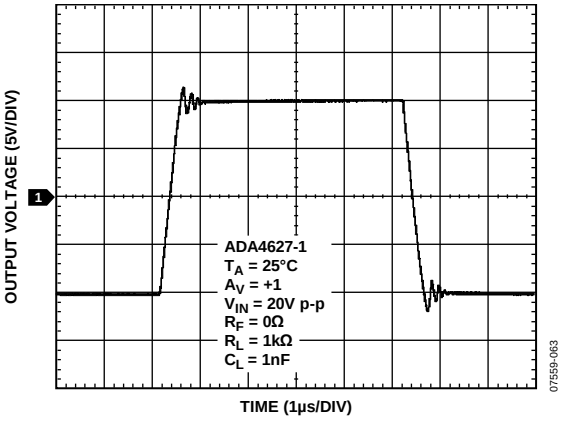

Figure 27. Large Signal Transient Response

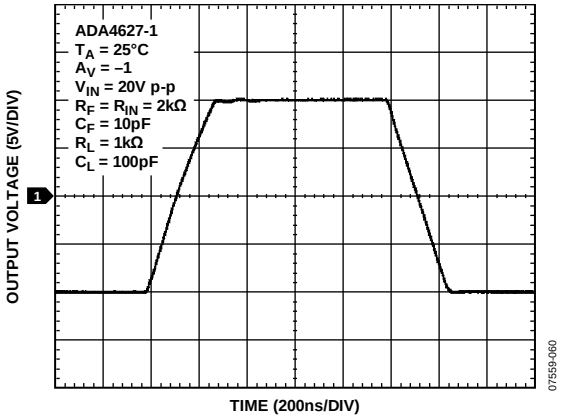

Figure 28. Large Signal Transient Response

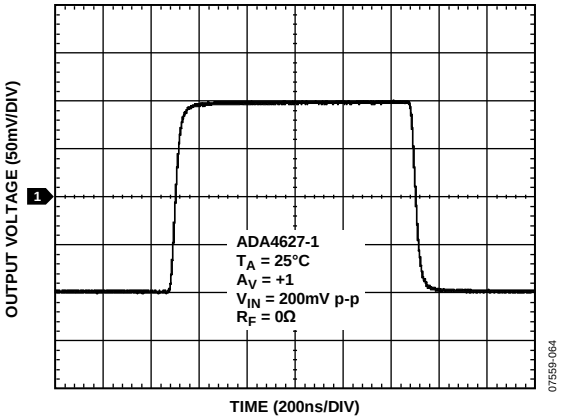

Figure 29. Small Signal Transient Response

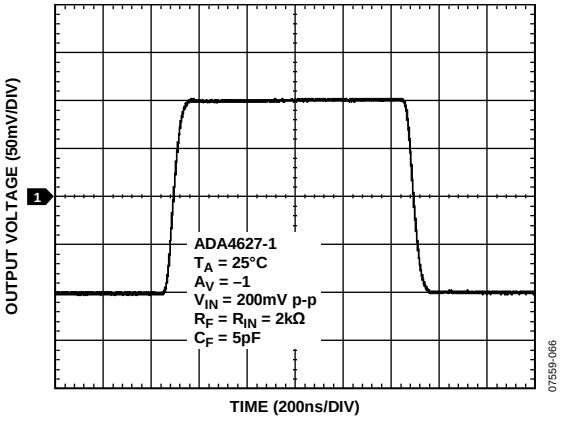

Figure 30. Small Signal Transient Response

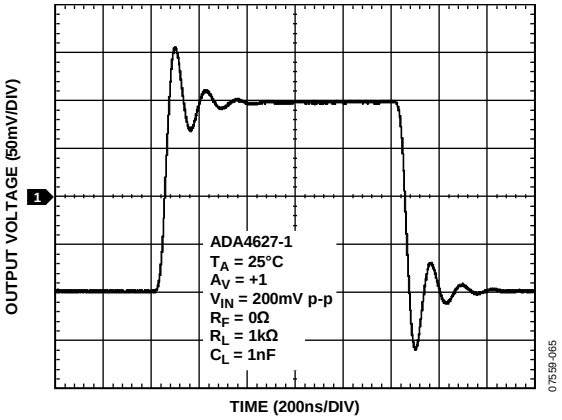

Figure 31. Small Signal Transient Response

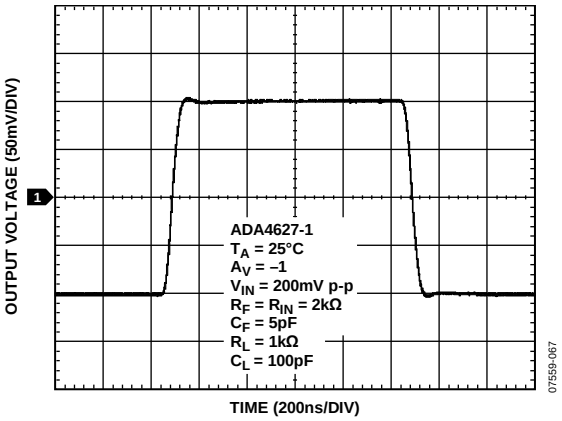

Figure 32. Small Signal Transient Response

T_A = 25°C, unless otherwise noted.

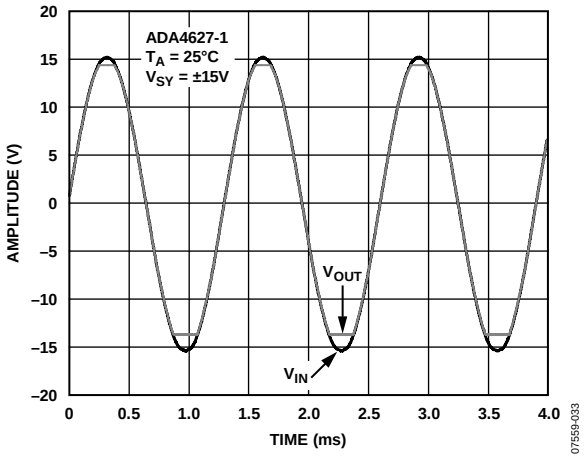

Figure 33. No Phase Reversal

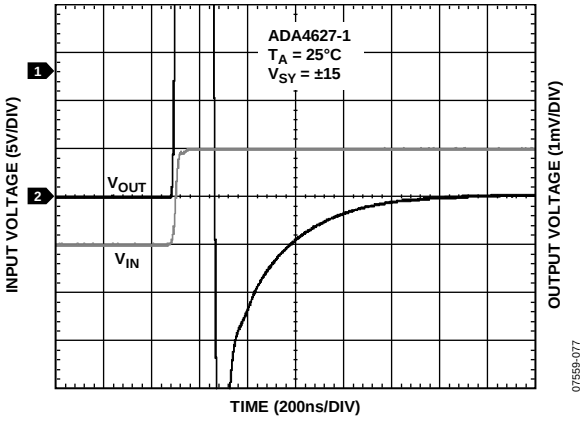

Figure 35. Positive Settling Time to 0.01%

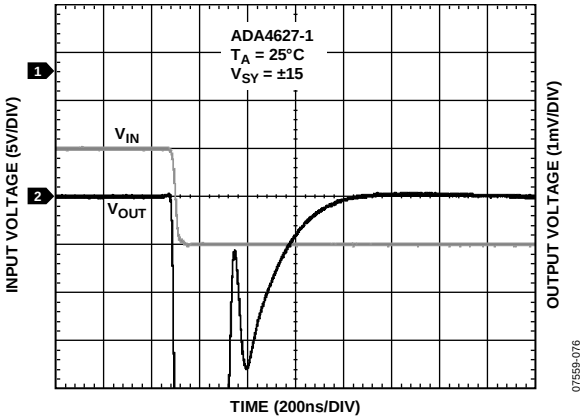

Figure 34. Negative Settling Time to 0.01%

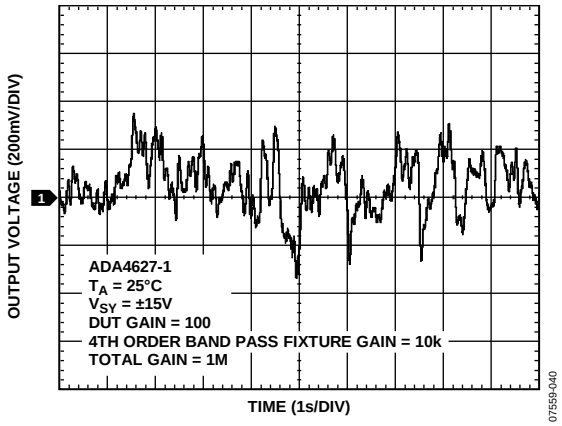

Figure 36. 0.1 Hz to 10 Hz Noise

THEORY OF OPERATION

The ADA4627-1 is a high speed, unity gain stable amplifier with excellent dc characteristics. The typical offset voltage of 70 µV allows the amplifier to be easily configured for high gains without the risk of excessive output voltage errors. The small temperature drift of 2 µV/°C ensures a minimum offset voltage error over the entire temperature range of −40°C to +125°C, making the amplifier ideal for a variety of sensitive measurement applications in harsh operating environments.

INPUT VOLTAGE RANGE

The ADA4627-1 is not a rail-to-rail input amplifier, thus, care is required to ensure that both inputs do not exceed the input voltage range. Under normal negative feedback operating conditions, the amplifier corrects its output to ensure that the two inputs are at the same voltage. However, if either input exceeds the input voltage range, the loop opens and large currents begin to flow through the ESD protection diodes in the amplifier.

These diodes are connected between the inputs and each supply rail to protect the input transistors against an electrostatic discharge event, and they are normally reverse-biased. However, if the input voltage exceeds the supply voltage, these ESD diodes can become forward-biased. Without current limiting, excessive amounts of current may flow through these diodes, causing permanent damage to the device. If inputs are subject to overvoltage, insert appropriate series resistors to limit the diode current to less than 5 mA.

INPUT OFFSET VOLTAGE ADJUST RANGE

The ADA4627-1 SOIC package has offset adjust pins for compatibility with some existing designs. The recommended offset nulling circuit is shown in Figure 37.

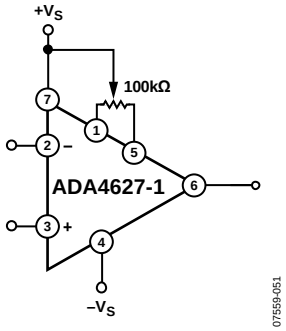

Figure 37. Standard Offset Null Circuit

With a 100 kΩ potentiometer, the adjustment range is more than ±11 mV. However, the V_{OS} temperature drift increases by several µV/°C for every millivolt of offset adjust. The ADA4627-1 has matching thin film resistors that are laser trimmed at two temperatures to minimize both offset voltage and offset voltage drift. The offset voltage at room temperature is less than 0.5 mV, and the offset voltage drift is only a few µV/°C or less, therefore, it is not recommended to use the offset adjust pins, especially for offset adjust of a complete signal chain. Signal chain offset can be addressed with an autozero amplifier used to form a composite amplifier, or if the ADA4627-1 is at an inverting amplifier stage, it can be modified easily to create a summing amplifier where a potentiometer can be added (see Figure 38). The LFCSP package does not have offset adjust pins.

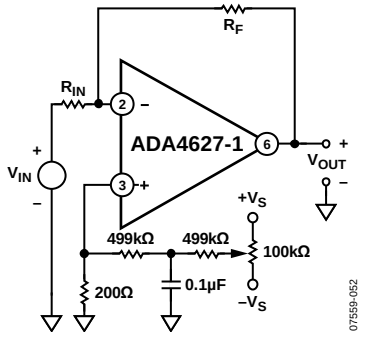

Figure 38. Alternate Offset Null Circuit for Inverting Stage

INPUT BIAS CURRENT

Because the ADA4627-1 has a JFET input stage, the input bias current, due to the reverse-biased junction, has a leakage current that approximately doubles every 10°C. The power dissipation of the part, combined with the thermal resistance of the package, results in the junction temperature increasing 20 to 30 degrees Centigrade above ambient. This parameter is tested with high speed ATE equipment, which does not result in the die temperature reaching equilibrium. This is correlated with bench measurements to match the guaranteed maximum at room temperature in Table 2.

The input current can be reduced by keeping the temperature as low as possible and using a light load on the output.

NOISE CONSIDERATIONS

The JFET input stage offers very low input voltage noise and input current noise. The thermal noise of a 1 kΩ resistor at room temperature is 4 nV/√Hz, thus low values of resistance should be used for dc-coupled inverting and noninverting amplifier configurations. In the case of transimpedance amplifiers (TIAs), current noise is more important.

The ADA4627-1 is an excellent choice for both of these applications. Analog Devices offers a wide variety of low voltage noise and low current noise op amps in a variety of processes optimized for different supply voltage ranges. Refer to Application Note AN-940 for a complete discussion of noise, calculations, and selection tables for more than three dozen low noise, op amp families.

THD + N MEASUREMENTS

Total harmonic distortion plus noise (THD + N) is usually measured with an audio analyzer from Audio Precision, Inc. The analyzer consists of a low distortion oscillator that is swept from the starting frequency to the ending frequency. The

oscillator is connected to the circuit under test, and the output of the circuit goes back to the analyzer.

The analyzer has a tunable notch filter in lock step with the swept oscillator. This removes the fundamental frequency, but allows all of the harmonics and wideband noise to be measured with an integrating voltmeter. However, there is a switchable low-pass filter in series with the notch filter. If the sine wave is at 100 Hz, then the tenth harmonic is still at 1 kHz, thus having a low pass at 80 kHz is not a problem. When the oscillator reaches 20 kHz, the fourth harmonic (80 kHz) is partially attenuated, resulting in a lower reading from the voltmeter. When evaluating THD + N curves from any manufacturer, careful attention should be paid to the test conditions. The difference between an 80 kHz low-pass filter and a 500 kHz filter is shown in Figure 39.

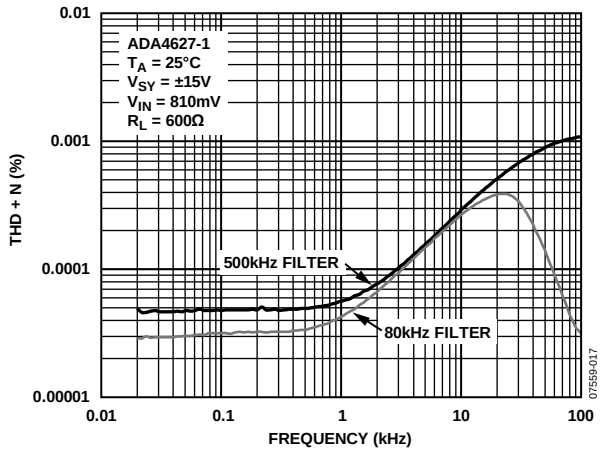

Figure 39. THD + N vs. Frequency

PRINTED CIRCUIT BOARD LAYOUT, BIAS CURRENT, AND BYPASSING

To take advantage of the very low input bias current of the ADA4627-1 at room temperature, leakage paths must be considered. A printed circuit board, with dust and humidity, can have 100 MΩ of resistance over a few tenths of an inch. A 1 mV differential between the two points results in 10 pA of leakage current, more than the guaranteed maximum.

The op amp inputs should be guarded by surrounding the nets with a metal trace maintained at the predicted voltage. In the case of an inverting configuration or transimpedance amplifier, (see Figure 40), the inverting and noninverting nodes can be surrounded by traces held at a quiet analog ground.

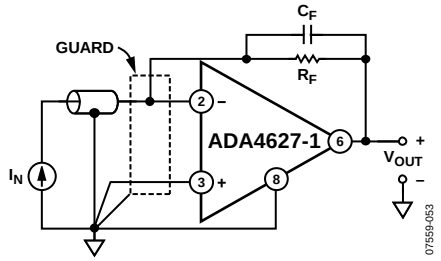

Figure 40. Inverting Amplifier with Guard

For a noninverting configuration, the trace can be driven from the feedback divider, but the resistors should be chosen to offer a low impedance drive to the trace (see Figure 41).

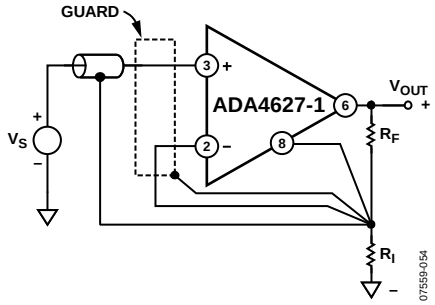

Figure 41. Noninverting Amplifier with Guard

The board layout should be compact with traces as short as possible. For second-order board considerations, such as triboelectric effects and piezoelectric effects, as well as a table of insulating material properties, see the AD549 data sheet.

In some cases, shielding from air currents may be helpful. A general rule of thumb, for op amps with gain bandwidth products higher than 1 MHz, bypass capacitors should be very close to the part, within 3 millimeters. Each supply should be bypassed with a 0.01 µF ceramic capacitor in parallel with a 1 µF bulk decoupling capacitor. The ceramic capacitors should be closer to the op amp. Sockets, which add inductance and capacitance, should not be used.

OUTPUT PHASE REVERSAL

Output phase reversal occurs in some amplifiers when the input common-mode voltage range is exceeded. As common-mode voltage is moved outside the common-mode range, the outputs of these amplifiers can suddenly jump in the opposite direction to the supply rail. This is the result of the differential input pair shutting down, causing a radical shifting of internal voltages that results in the erratic output behavior.

The ADA4627-1 amplifier has been carefully designed to prevent any output phase reversal if both inputs are maintained within the specified input voltage range. If one or both inputs exceed the input voltage range but remain within the supply rails, an internal loop opens and the output varies. Therefore, the inputs should always be a minimum of 3 V away from either supply rail.

DRIVING CAPACITIVE LOADS

Adding capacitance to the output of any op amp results in additional phase shift, which reduces stability and leads to overshoot or oscillation. The ADA4627-1 has a high phase margin and low output impedance, so it can drive reasonable values of capacitance. This is a common situation when an amplifier is used to drive the input of switched capacitor ADCs. For other considerations and various circuit solutions, see the Analog Dialogue article titled *Ask the Applications Engineer-25*, *Op Amps Driving Capacitive Loads*, available at www.analog.com.

OUTLINE DIMENSIONS

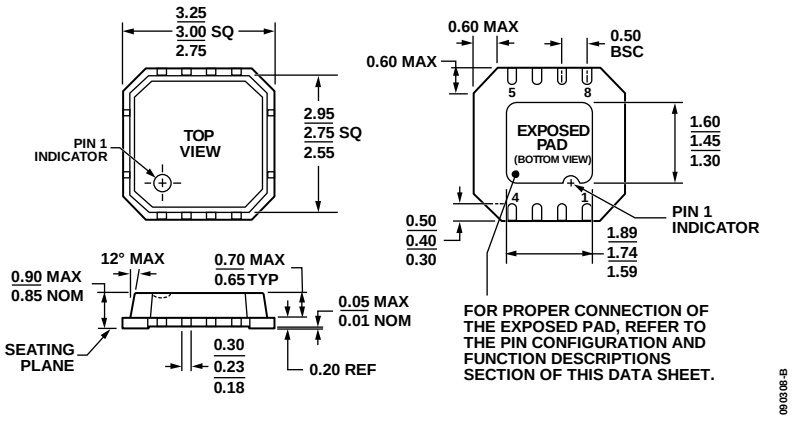

Figure 42. 8-Lead Lead Frame Chip Scale Package [LFCSP_VD]
3 mm × 3 mm Body, Very Thin, Dual Lead
(CP-8-2)
Dimensions shown in millimeters

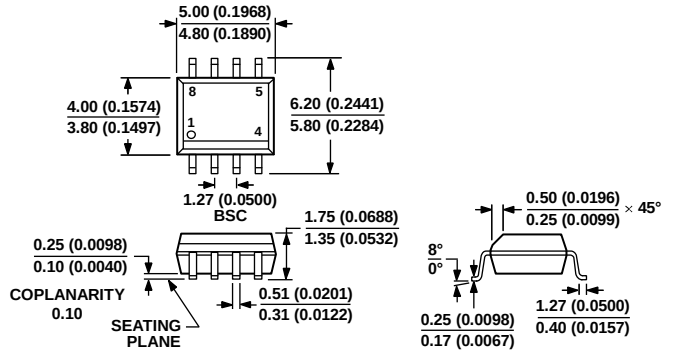

Figure 43. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADA4627-1ACPZ-R2[1]	−40°C to +125°C	8-Lead LFCSP_VD	CP-8-2	A29
ADA4627-1ACPZ-RL[1]	−40°C to +125°C	8-Lead LFCSP_VD	CP-8-2	A29
ADA4627-1ACPZ-R7[1]	−40°C to +125°C	8-Lead LFCSP_VD	CP-8-2	A29
ADA4627-1ARZ[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4627-1ARZ-RL[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4627-1ARZ-R7[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4627-1BRZ[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4627-1BRZ-R7[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4627-1BRZ-RL[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	

[1] Z = RoHS Compliant Part.

NOTES

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