



4.5Ω Quad SPST Analog Switches in UCSP

General Description

The MAX4737/MAX4738/MAX4739 low-voltage, low on-resistance (R_{ON}), quad single-pole/single throw (SPST) analog switches operate from a single +1.8V to +5.5V supply. These devices are designed for USB 1.1 and audio switching applications.

The MAX4737/MAX4738/MAX4739 feature 4.5Ω R_{ON} (max) with 1.2Ω flatness and 0.4Ω matching between channels. These new switches feature guaranteed operation from +1.8V to +5.5V and are fully specified at 3V and 5V. These switches offer break-before-make switching (1ns) with $t_{ON} < 80ns$ and $t_{OFF} < 40ns$ at +2.7V. The digital logic inputs are +1.8V logic compatible with a +2.7V to +3.6V supply.

These switches are packaged in a chip-scale package (UCSP™), significantly reducing the required PC board area. The chip occupies only a 2mm x 2mm area and has a 4 x 4 bump array with a bump pitch of 0.5mm. These switches are also available in a 14-pin TSSOP and a 16-pin thin QFN (4mm x 4mm) package.

Applications

Battery-Operated Equipment
Audio/Video-Signal Routing
Low-Voltage Data-Acquisition Systems
Sample-and-Hold Circuits
Data-Acquisition Systems
Communications Circuits

Features

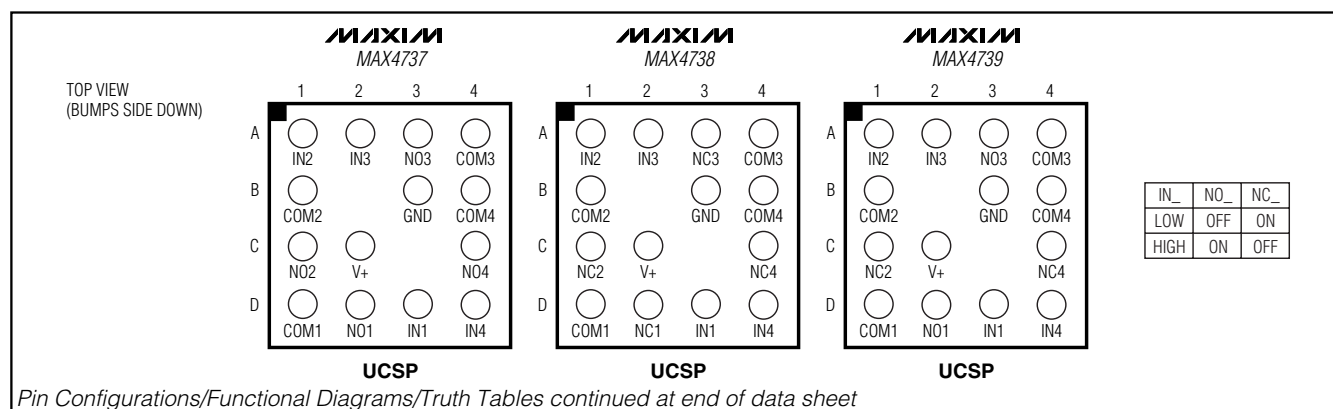
- ◆ USB 1.1 Signal Switching
- ◆ 2ns (max) Differential Skew
- ◆ -3dB Bandwidth: >300MHz
- ◆ Low 20pF On-Channel Capacitance
- ◆ Low R_{ON}
 - 4.5Ω (max) (+3V Supply)
 - 3Ω (max) (+5V Supply)
- ◆ 0.4Ω (max) R_{ON} Match (+3V Supply)
- ◆ 1.2Ω (max) R_{ON} Flatness (+3V Supply)
- ◆ <0.5nA Leakage Current at +25°C
- ◆ High Off-Isolation: -55dB (10MHz)
- ◆ Low Crosstalk: -80dB (10MHz)
- ◆ Low Distortion: 0.03%
- ◆ +1.8V CMOS-Logic Compatible
- ◆ Single-Supply Operation from +1.8V to +5.5V
- ◆ Rail-to-Rail Signal Handling

Ordering Information

PART	TEMP RANGE	PIN/BUMP-PACKAGE	TOP MARK
MAX4737EUD	-40°C to +85°C	14 TSSOP	—
MAX4737ETE	-40°C to +85°C	16 Thin QFN	—
MAX4737EBE-T	-40°C to +85°C	16 UCSP-16	4737
MAX4738EUD	-40°C to +85°C	14 TSSOP	—
MAX4738ETE	-40°C to +85°C	16 Thin QFN	—
MAX4738EBE-T	-40°C to +85°C	16 UCSP-16	4738
MAX4739EUD	-40°C to +85°C	14 TSSOP	—
MAX4739ETE	-40°C to +85°C	16 Thin QFN	—
MAX4739EBE-T	-40°C to +85°C	16 UCSP-16	4739

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Pin Configurations/Functional Diagrams/Truth Tables



4.5Ω Quad SPST Analog Switches in UCSP

ABSOLUTE MAXIMUM RATINGS

(All Voltages Referenced to GND)

V+, IN_	-0.3V to +6.0V
COM_, NO_, NC_ (Note 1)	-0.3V to (V+ + 0.3V)
Continuous Current COM_, NO_, NC_	±100mA
Peak Current COM_, NO_, NC_ (pulsed at 1ms, 10% duty cycle)	±200mA
Continuous Power Dissipation (T _A = +70°C)	
14-Pin TSSOP (derate 6.3mW/°C above +70°C)	500mW
16-Bump UCSP (derate 8.3mW/°C above +70°C)	659mW
16-Pin Thin QFN (derate 25mW/°C above +70°C)	2000mW

ESD Method 3015.7	>2kV
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Bump Temperature (soldering)	
Infrared (15s)	+220°C
Vapor Phase (60s)	+215°C

Note 1: Signals on COM_, NO_, or NC_ exceeding V+ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +2.7V to +3.6V, V_{IH} = +1.4V, V_{IL} = +0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +3.0V, T_A = +25°C, unless otherwise noted.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T _A	MIN	TYP	MAX	UNITS
Analog Signal Range	V _{COM_} , V _{NO_} , V _{NC_}			0		V+	V
ANALOG SWITCH							
On-Resistance (Note 5)	R _{ON}	V+ = 2.7V, I _{COM_} = 10mA; V _{NO_} or V _{NC_} = 1.5V	+25°C		3.0	4.5	Ω
			T _{MIN} to T _{MAX}			5	
On-Resistance Match Between Channels (Notes 5, 6)	ΔR _{ON}	V+ = 2.7V, I _{COM_} = 10mA; V _{NO_} or V _{NC_} = 1.5V	+25°C		0.1	0.4	Ω
			T _{MIN} to T _{MAX}			0.5	
On-Resistance Flatness (Note 7)	R _{FLAT(ON)}	V+ = 2.7V, I _{COM_} = 10mA; V _{NO_} or V _{NC_} = 1.0V, 1.5V, 2.0V	+25°C		0.6	1.2	Ω
			T _{MIN} to T _{MAX}			1.5	
NO_, NC_ Off-Leakage Current (Note 8)	I _{NO_(OFF)} , I _{NC_(OFF)}	V+ = 3.6V, V _{COM_} = 0.3V, 3.3V; V _{NO_} or V _{NC_} = 3.3V, 0.3V	+25°C	-0.5	+0.01	+0.5	nA
			T _{MIN} to T _{MAX}	-1		+1	
COM_ Off-Leakage Current (Note 8)	I _{COM_(OFF)}	V+ = 3.6V, V _{COM_} = 0.3V, 3.3V; V _{NO_} or V _{NC_} = 3.3V, 0.3V	+25°C	-0.5	+0.01	+0.5	nA
			T _{MIN} to T _{MAX}	-1		+1	
COM_ On-Leakage Current (Note 8)	I _{COM_(ON)}	V+ = 3.6V, V _{COM_} = 0.3V, 3.3V; V _{NO_} or V _{NC_} = 0.3V, 3.3V, or floating	+25°C	-1	+0.01	+1	nA
			T _{MIN} to T _{MAX}	-2		+2	

4.5Ω Quad SPST Analog Switches in UCSP

ELECTRICAL CHARACTERISTICS—Single +3V Supply (continued)

(V₊ = +2.7V to +3.6V, V_{IH} = +1.4V, V_{IL} = +0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V₊ = +3.0V, T_A = +25°C, unless otherwise noted.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T _A	MIN	TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS							
Turn-On Time	t _{ON}	V _{NO_} , V _{NC_} = 1.5V; R _L = 300Ω, C _L = 35pF, Figure 1	+25°C	40	80	100	ns
			T _{MIN} to T _{MAX}				
Turn-Off Time	t _{OFF}	V _{NO_} , V _{NC_} = 1.5V; R _L = 300Ω, C _L = 35pF, Figure 1	+25°C	20	40	50	ns
			T _{MIN} to T _{MAX}				
Break-Before-Make Time Delay (MAX4739 Only) (Note 8)	t _{BBM}	V _{NO_} , V _{NC_} = 1.5V; R _L = 300Ω, C _L = 35pF, Figure 2	+25°C	8		1	ns
			T _{MIN} to T _{MAX}				
Skew (Note 8)	t _{SKEW}	R _S = 39Ω, C _L = 50pF, Figure 3	T _{MIN} to T _{MAX}	0.15		2	ns
Charge Injection	Q	V _{GEN} = 2V, R _{GEN} = 0Ω, C _L = 1.0nF, Figure 4	+25°C	5			pC
Off-Isolation (Note 9)	V _{ISO}	f = 10MHz; V _{NO_} , V _{NC_} = 1V _{P-P} ; R _L = 50Ω, C _L = 5pF, Figure 5a	+25°C	-55			dB
		f = 1MHz; V _{NO_} , V _{NC_} = 1V _{P-P} ; R _L = 50Ω, C _L = 5pF, Figure 5a		-80			
Crosstalk (Note 10)	V _{CT}	f = 10MHz; V _{NO_} , V _{NC_} = 1V _{P-P} ; R _L = 50Ω, C _L = 5pF, Figure 5b	+25°C	-80			dB
		f = 1MHz; V _{NO_} , V _{NC_} = 1V _{P-P} ; R _L = 50Ω, C _L = 5pF, Figure 5b		-110			
On-Channel -3dB Bandwidth	BW	Signal = 0dBm, C _L = 5pF, 50Ω in and out, Figure 5a	+25°C	300			MHz
Total Harmonic Distortion	THD	R _L = 600Ω	+25°C	0.03			%
NO_, NC_ Off-Capacitance	C _{NO_(OFF)} , C _{NC_(OFF)}	f = 1MHz, Figure 6	+25°C	9			pF
Switch On-Capacitance	C _{ON}	f = 1MHz, Figure 6	+25°C	15			pF
DIGITAL I/O							
Input Logic High Voltage	V _{IH}		T _{MIN} to T _{MAX}	1.4			V
Input Logic Low Voltage	V _{IL}		T _{MIN} to T _{MAX}			0.5	V
Input Leakage Current	I _{IN}	V ₊ = 3.6V, V _{IN_} = 0 or 5.5V	T _{MIN} to T _{MAX}	-0.1		+0.1	μA

4.5Ω Quad SPST Analog Switches in UCSP

ELECTRICAL CHARACTERISTICS—Single +3V Supply (continued)

(V+ = +2.7V to +3.6V, V_{IH} = +1.4V, V_{IL} = +0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +3.0V, T_A = +25°C, unless otherwise noted.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T _A	MIN	TYP	MAX	UNITS
SUPPLY							
Supply Voltage Range	V+		T _{MIN} to T _{MAX}	1.8		5.5	V
Positive Supply Current	I+	V+ = 5.5V, V _{IN} = 0V or V+	T _{MIN} to T _{MAX}			1	μA

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +4.2V to +5.5V, V_{IH} = +2.0V, V_{IL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +5.0V, T_A = +25°C, unless otherwise noted.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T _A	MIN	TYP	MAX	UNITS
Analog Signal Range	V _{COM} _, V _{NO} _, V _{NC} _		T _{MIN} to T _{MAX}	0		V+	V
ANALOG SWITCH							
On-Resistance (Note 5)	R _{ON}	V+ = 4.2V; I _{COM} _ = 10mA; V _{NO} _ or V _{NC} _ = 3.5V	+25°C		1.7	3.0	Ω
			T _{MIN} to T _{MAX}			3.5	
On-Resistance Match Between Channels (Notes 5, 6)	ΔR _{ON}	V+ = 4.2V; I _{COM} _ = 10mA; V _{NO} _ or V _{NC} _ = 3.5V	+25°C		0.1	0.3	Ω
			T _{MIN} to T _{MAX}			0.4	
On-Resistance Flatness (Note 7)	R _{FLAT(ON)}	V+ = 4.2V; I _{COM} _ = 10mA; V _{NO} _ or V _{NC} _ = 1.0V, 2.0V, 3.5V	+25°C		0.4	1.2	Ω
			T _{MIN} to T _{MAX}			1.5	
NO_, NC_ Off-Leakage Current (Note 8)	I _{NO} (OFF), I _{NC} (OFF)	V+ = 5.5V; V _{COM} _ = 1.0V, 4.5V; V _{NO} _ or V _{NC} _ = 4.5V, 1.0V	+25°C	-0.5	0.01	+0.5	nA
			T _{MIN} to T _{MAX}	-1		+1	
COM_ Off-Leakage Current (Note 8)	I _{COM} _(OFF)	V+ = 5.5V; V _{COM} _ = 1V, 4.5V; V _{NO} _ or V _{NC} _ = 4.5V, 1V	+25°C	-0.5	0.01	+0.5	nA
			T _{MIN} to T _{MAX}	-1		+1	
COM_ On-Leakage Current (Note 8)	I _{COM} _(ON)	V+ = 5.5V; V _{COM} _ = 1.0V, 4.5V; V _{NO} _ or V _{NC} _ = 1.0V, 4.5V, or floating	+25°C	-1	0.01	+1	nA
			T _{MIN} to T _{MAX}	-2		+2	
DYNAMIC CHARACTERISTICS							
Turn-On Time	t _{ON}	V _{NO} _, V _{NC} _ = 3.0V; R _L = 300Ω, C _L = 35pF, Figure 1	+25°C		30	80	ns
			T _{MIN} to T _{MAX}			100	
Turn-Off Time	t _{OFF}	V _{NO} _, V _{NC} _ = 3.0V; R _L = 300Ω, C _L = 35pF, Figure 1	+25°C		20	40	ns
			T _{MIN} to T _{MAX}			50	

4.5Ω Quad SPST Analog Switches in UCSP

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V₊ = +4.2V to +5.5V, V_{IH} = +2.0V, V_{IL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V₊ = +5.0V, T_A = +25°C, unless otherwise noted.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T _A	MIN	TYP	MAX	UNITS
Break-Before-Make Time Delay (MAX4739 Only) (Note 8)	t _{BBM}	V _{NO} _, V _{NC} _ = 3.0V; R _L = 300Ω, C _L = 35pF, Figure 2	+25°C	8		ns	
			T _{MIN} to T _{MAX}	1			
Skew (Note 8)	t _{SKW}	R _S = 39Ω, C _L = 50pF, Figure 3	T _{MIN} to T _{MAX}	0.15	2	ns	
DIGITAL I/O							
Input Logic High Voltage	V _{IH}		T _{MIN} to T _{MAX}	2.0		V	
Input Logic Low Voltage	V _{IL}		T _{MIN} to T _{MAX}		0.8	V	
Input Leakage Current	I _{IN}	V+ = 5.5V, V _{IN} _ = 0V or V+	T _{MIN} to T _{MAX}	-0.1	+0.1	μA	
POWER SUPPLY							
Power-Supply Range	V+		T _{MIN} to T _{MAX}	1.8	5.5	V	
Positive Supply Current	I+	V+ = 5.5V, V _{IN} _ = 0V or V+	T _{MIN} to T _{MAX}		1	μA	

Note 3: UCSP parts are 100% tested at +25°C only, and guaranteed by design over the specified temperature range. TSSOP and thin QFN parts are 100% tested at T_{MAX} and guaranteed by design over the specified temperature range.

Note 4: The algebraic convention used in this data sheet is where the most negative value is a minimum and the most positive value is a maximum.

Note 5: Guaranteed by design for UCSP and thin QFN parts.

Note 6: ΔR_{ON} = R_{ON}(MAX) - R_{ON}(MIN).

Note 7: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Note 8: Guaranteed by design.

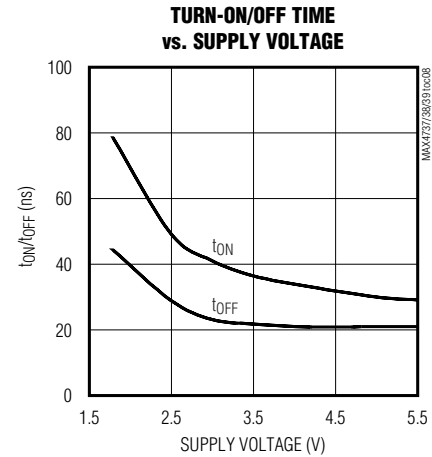
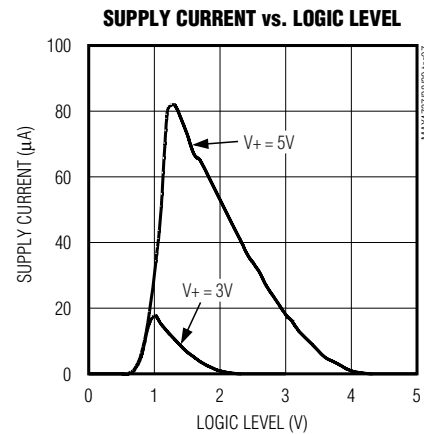
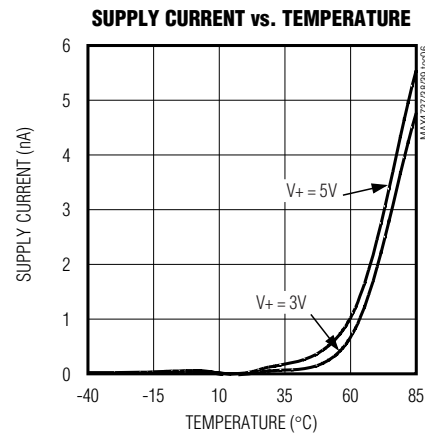
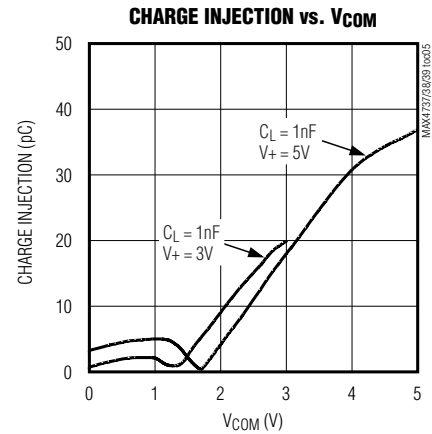
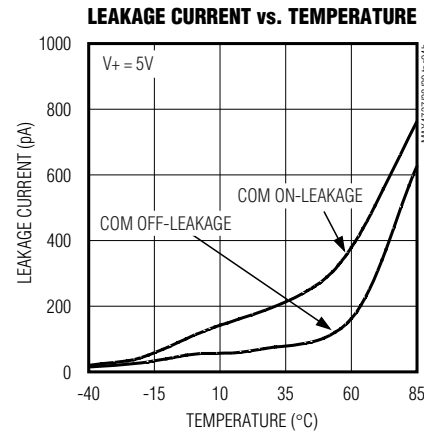
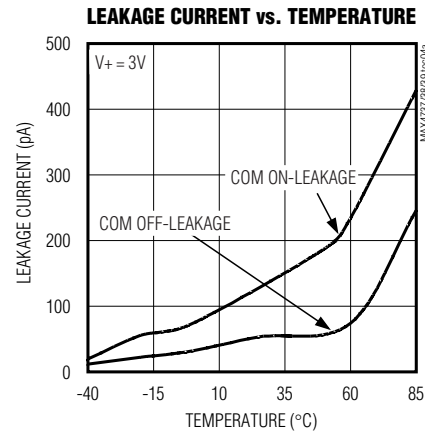
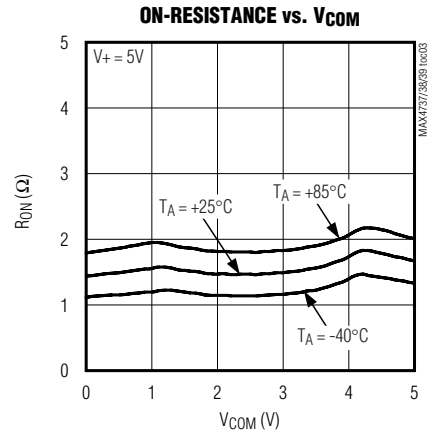
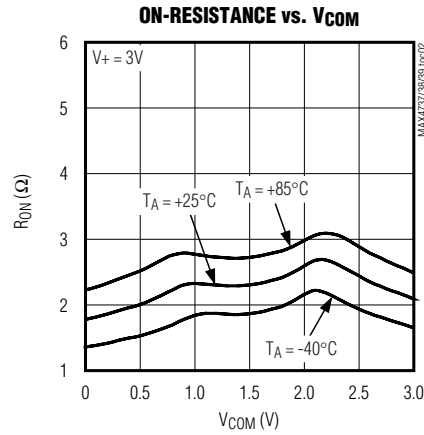
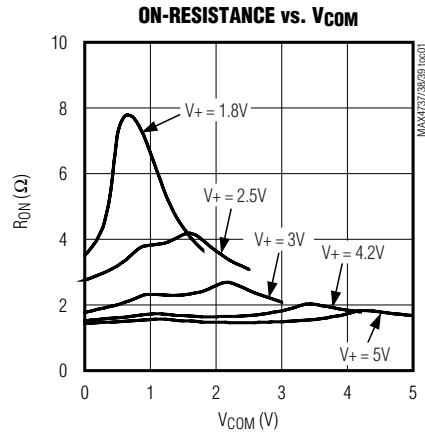
Note 9: Off-Isolation = 20log₁₀ (V_{COM} / V_{NO}), V_{COM} = output, V_{NO} = input to off switch.

Note 10: Between any two switches.

4.5Ω Quad SPST Analog Switches in UCSP

Typical Operating Characteristics

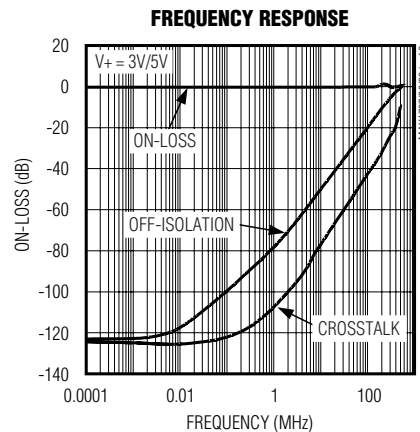
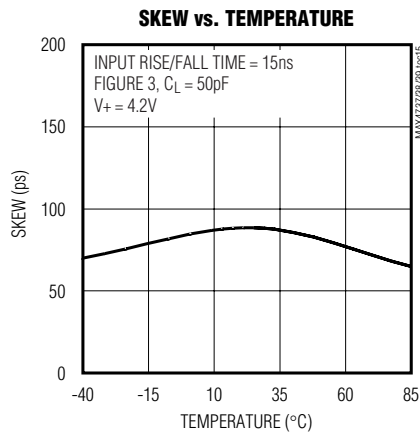
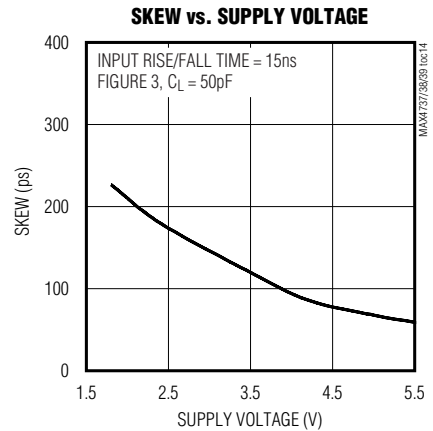
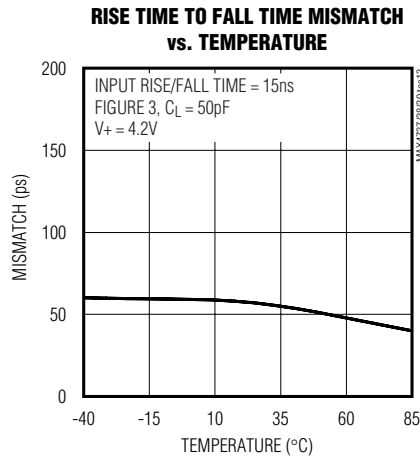
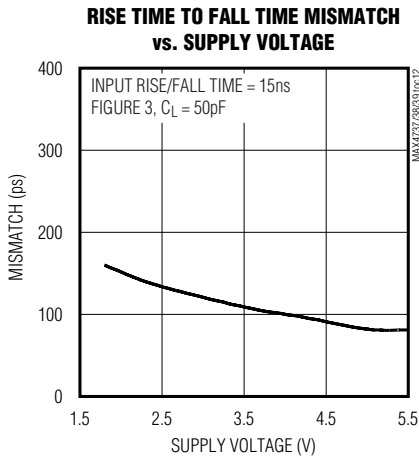
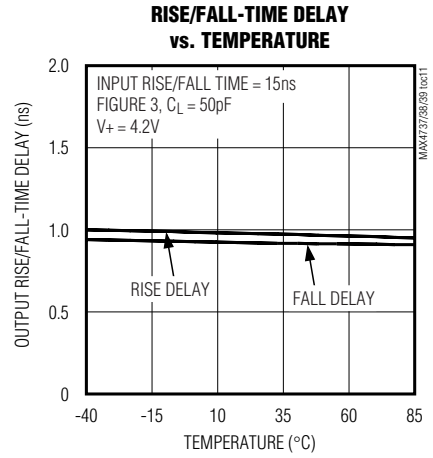
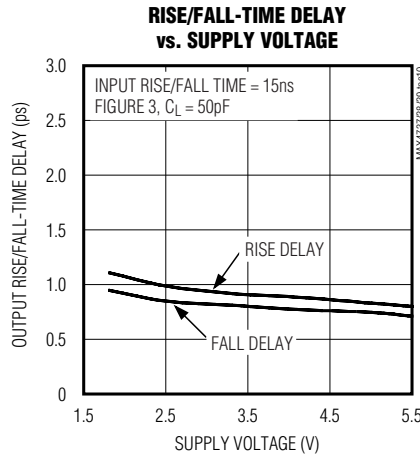
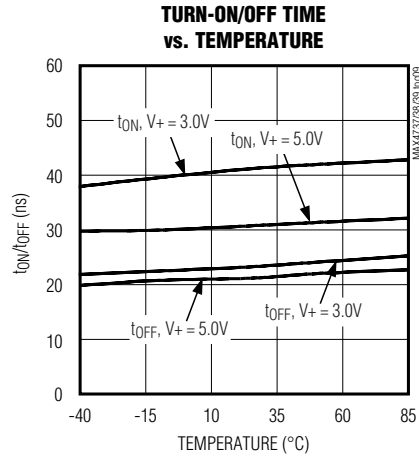
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4.5Ω Quad SPST Analog Switches in UCSP

Typical Operating Characteristics (continued)

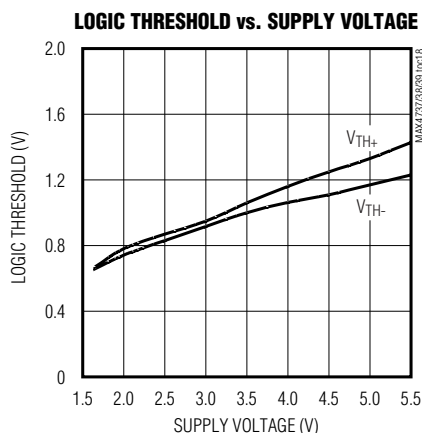
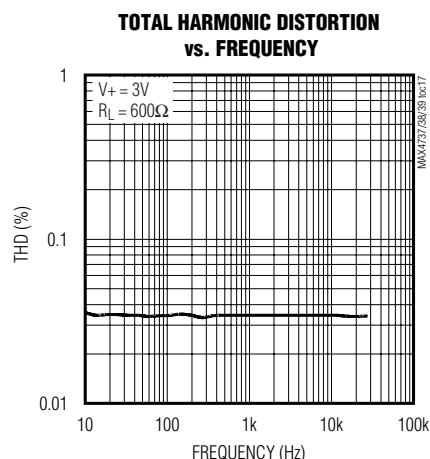
(T_A = +25°C, unless otherwise noted.)



4.5Ω Quad SPST Analog Switches in UCSP

Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)



Pin Description

PIN									NAME	FUNCTION
MAX4737			MAX4738			MAX4739				
UCSP	TSSOP	THIN QFN	UCSP	TSSOP	THIN QFN	UCSP	TSSOP	THIN QFN		
D2	1	15	—	—	—	D2	1	15	NO1	Analog-Switch Normally Open Terminal
—	—	—	D2	1	15	—	—	—	NC1	Analog-Switch Normally Closed Terminal
D1	2	1	D1	2	1	D1	2	1	COM1	Analog-Switch Common Terminal
C1	3	2	—	—	—	—	—	—	NO2	Analog-Switch Normally Open Terminal
—	—	—	C1	3	2	C1	3	2	NC2	Analog-Switch Normally Closed Terminal
B1	4	3	B1	4	3	B1	4	3	COM2	Analog-Switch Common Terminal
A1	5	4	A1	5	4	A1	5	4	IN2	Logic-Control Digital Input
A2	6	5	A2	6	5	A2	6	5	IN3	Logic-Control Digital Input
B3	7	6	B3	7	6	B3	7	6	GND	Ground. Connect to digital ground.
A3	8	7	—	—	—	A3	8	7	NO3	Analog-Switch Normally Open Terminal
—	—	—	A3	8	7	—	—	—	NC3	Analog-Switch Normally Closed Terminal
A4	9	9	A4	9	9	A4	9	9	COM3	Analog-Switch Common Terminal
B4	10	10	B4	10	10	B4	10	10	COM4	Analog-Switch Common Terminal

4.5Ω Quad SPST Analog Switches in UCSP

Pin Description (continued)

PIN									NAME	FUNCTION
MAX4737			MAX4738			MAX4739				
UCSP	TSSOP	THIN QFN	UCSP	TSSOP	THIN QFN	UCSP	TSSOP	THIN QFN		
C4	11	11	—	—	—	—	—	—	NO4	Analog-Switch Normally Open Terminal
—	—	—	C4	11	11	C4	11	11	NC4	Analog-Switch Normally Closed Terminal
D4	12	12	D4	12	12	D4	12	12	IN4	Logic-Control Digital Input
D3	13	13	D3	13	13	D3	13	13	IN1	Logic-Control Digital Input
C2	14	14	C2	14	14	C2	14	14	V+	Positive Analog Supply
—	—	8, 16	—	—	8, 16	—	—	8, 16	N.C.	No Connection. Not internally connected.

Detailed Description

The MAX4737/MAX4738/MAX4739 quad SPST analog switches operate from a single +1.8V to +5.5V supply. The MAX4737/MAX4738/MAX4739 offer excellent AC characteristics, <0.5nA leakage current, less than 1ns differential skew, and 15pF on-channel capacitance. All of these devices are CMOS-logic compatible with V+ to GND signal handling capability.

The MAX4737/MAX4738/MAX4739 are USB-complaint switches that provide 4.5Ω (max) on-resistance and 15pF on-channel capacitance to maintain signal integrity. At 12Mbps (USB full-speed data rate specification), the MAX4737/MAX4738/MAX4739 introduce less than 2ns propagation delay between input and output signals and less than 0.5ns change in skew for the output signals (see Figure 4).

The MAX4737 has four normally open (NO) switches, the MAX4738 has four normally closed (NC) switches, and the MAX4739 has two NO switches and two NC switches.

Applications Information

Digital Control Inputs

The MAX4737/MAX4738/MAX4739 logic inputs accept up to +5.5V regardless of supply voltage. For example, with a +3.3V supply, IN₋ can be driven low to GND and high to +5.5V allowing for mixing of logic levels in a system. Driving the control logic inputs rail-to-rail minimizes power consumption. For a +1.8V supply voltage, the logic thresholds are 0.5V (low) and 1.4V (high); for a +5V supply voltage, the logic thresholds are 0.8V (low) and 2.0V (high).

Analog Signal Levels

Analog signals that range over the entire supply voltage (V+ to GND) are passed with very little change in on-resistance (see *Typical Operating Characteristics*). The switches are bidirectional, so the NO₋, NC₋, and COM₋ pins can be either inputs or outputs.

Power-Supply Bypassing

Power-supply bypassing improves noise margin and prevents switching noise from propagating from the V+ supply to other components. A 0.1μF capacitor connected from V+ to GND is adequate for most applications.

UCSP Applications Information

For the latest application details on UCSP construction, dimensions, tape carrier information, PC board techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to the Application Note: *UCSP—A Wafer-Level Chip-Scale Package* on Maxim's web site at www.maxim-ic.com/ucsp.

4.5Ω Quad SPST Analog Switches in UCSP

Test Circuits/Timing Diagrams

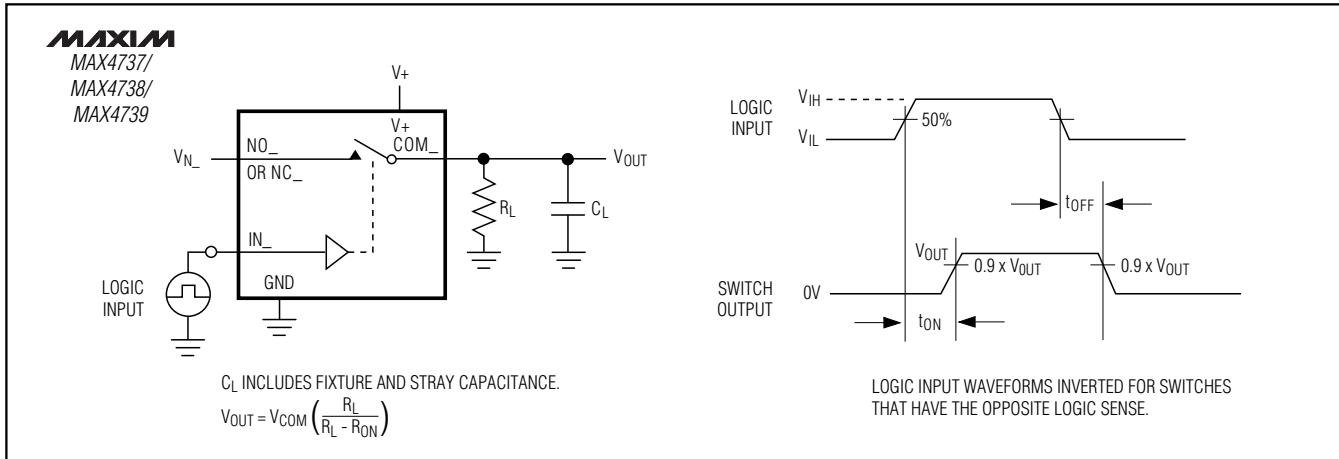


Figure 1. Switching Time

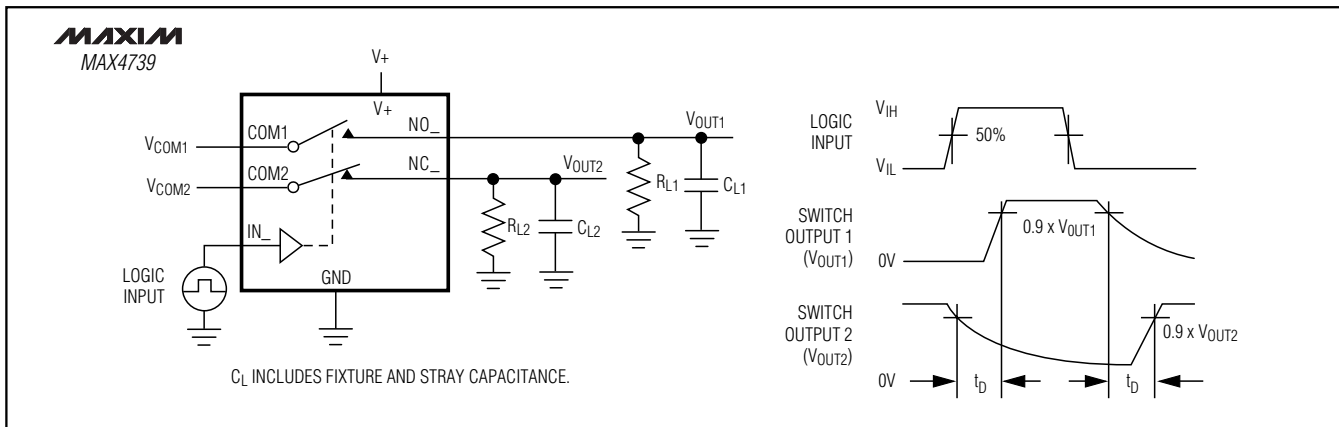


Figure 2. Break-Before-Make Interval

MAX4737/MAX4738/MAX4739

The diagram illustrates the effect of a switch on signal skew and delay. It is divided into two parts: a rising edge transition (top) and a falling edge transition (bottom).

Top Part (Rising Edge):

- Circuit Diagram:** A driver output $TxD+$ is connected to a switch. The switch is controlled by a signal that transitions from low to high. The switch connects the driver to a node A , which is then connected to a node B through a resistor R_S . Node B is connected to a load capacitor C_L .
- Timing Diagrams:**
 - INPUT A:** Shows a rising edge transition from 10% to 90% with a delay t_{r1} .
 - INPUT A-:** Shows a falling edge transition from 90% to 10% with a delay t_{f1} .
 - OUTPUT B:** Shows a rising edge transition from 10% to 90% with a delay t_{r0} .
 - OUTPUT B-:** Shows a falling edge transition from 90% to 10% with a delay t_{f0} .
 - Skew:** The skew between INPUT A and INPUT A- is t_{skew_i} . The skew between OUTPUT B and OUTPUT B- is t_{skew_o} .

Bottom Part (Falling Edge):

- Circuit Diagram:** A driver output $TxD-$ is connected to a switch. The switch is controlled by a signal that transitions from high to low. The switch connects the driver to a node $A-$, which is then connected to a node $B-$ through a resistor R_S . Node $B-$ is connected to a load capacitor C_L .
- Timing Diagrams:**
 - INPUT A:** Shows a rising edge transition from 10% to 90% with a delay t_{r1} .
 - INPUT A-:** Shows a falling edge transition from 90% to 10% with a delay t_{f1} .
 - OUTPUT B:** Shows a rising edge transition from 10% to 90% with a delay t_{r0} .
 - OUTPUT B-:** Shows a falling edge transition from 90% to 10% with a delay t_{f0} .
 - Skew:** The skew between INPUT A and INPUT A- is t_{skew_i} . The skew between OUTPUT B and OUTPUT B- is t_{skew_o} .

Parameters:

- $R_S = 39\Omega$
- $C_L = 50pF$

Delays and Skew:

- $|t_{r0} - t_{r1}|$ DELAY DUE TO SWITCH FOR RISING INPUT AND RISING OUTPUT SIGNALS.
- $|t_{f0} - t_{f1}|$ DELAY DUE TO SWITCH FOR FALLING INPUT AND FALLING OUTPUT SIGNALS.
- $|t_{skew_o}|$ CHANGE IN SKEW THROUGH THE SWITCH FOR OUTPUT SIGNALS.
- $|t_{skew_i}|$ CHANGE IN SKEW THROUGH THE SWITCH FOR INPUT SIGNALS.

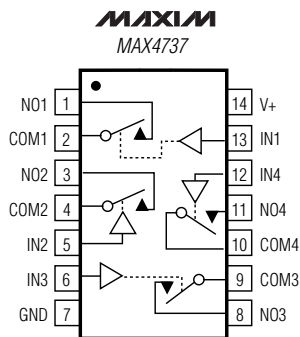
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4.5Ω Quad SPST Analog Switches in UCSP

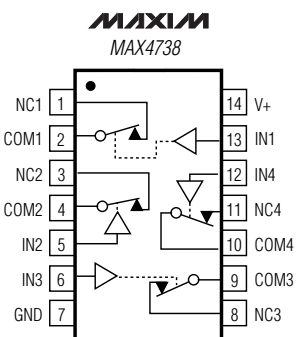
Pin Configurations/Functional Diagrams/Truth Tables (continued)

MAX4737/MAX4738/MAX4739

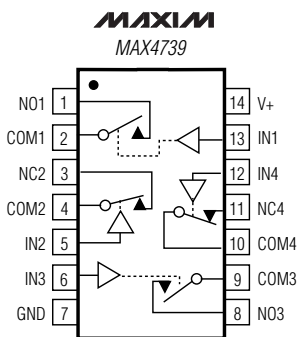
TOP VIEW



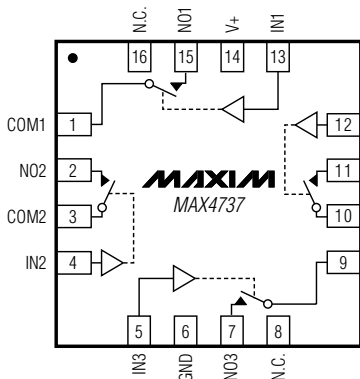
INPUT	SWITCH STATE
LOW	OFF
HIGH	ON



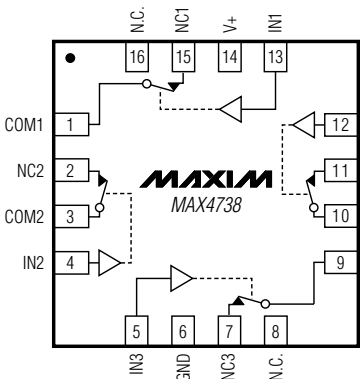
INPUT	SWITCH STATE
LOW	ON
HIGH	OFF



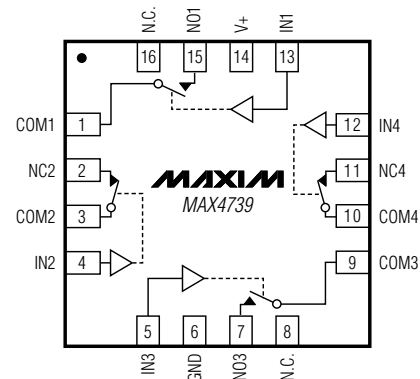
INPUT	NO1, NO3	NC2, NC4
LOW	OFF	ON
HIGH	ON	OFF



INPUT	SWITCH STATE
LOW	OFF
HIGH	ON



INPUT	SWITCH STATE
LOW	ON
HIGH	OFF

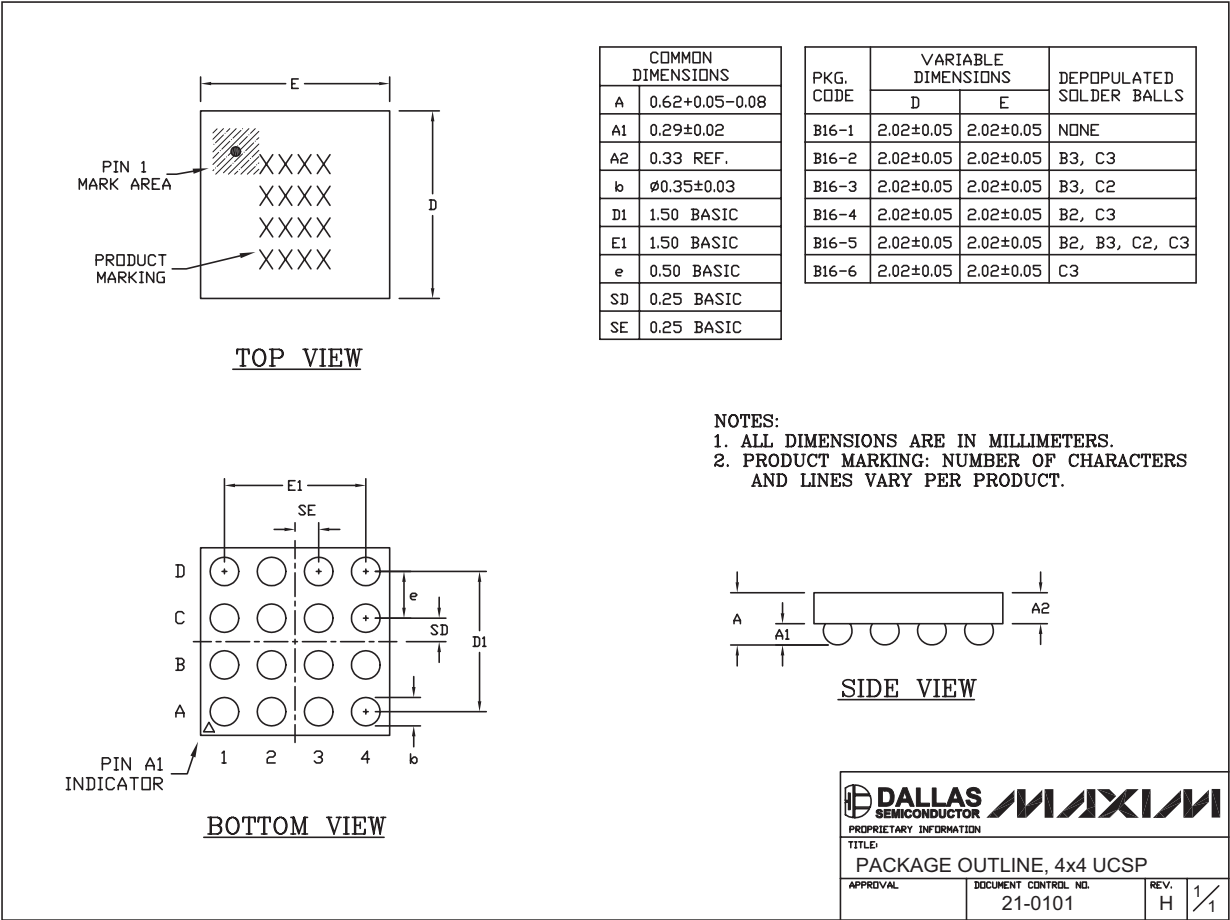


INPUT	NO1, NO3	NC2, NC4
LOW	OFF	ON
HIGH	ON	OFF

4.5Ω Quad SPST Analog Switches in UCSP

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

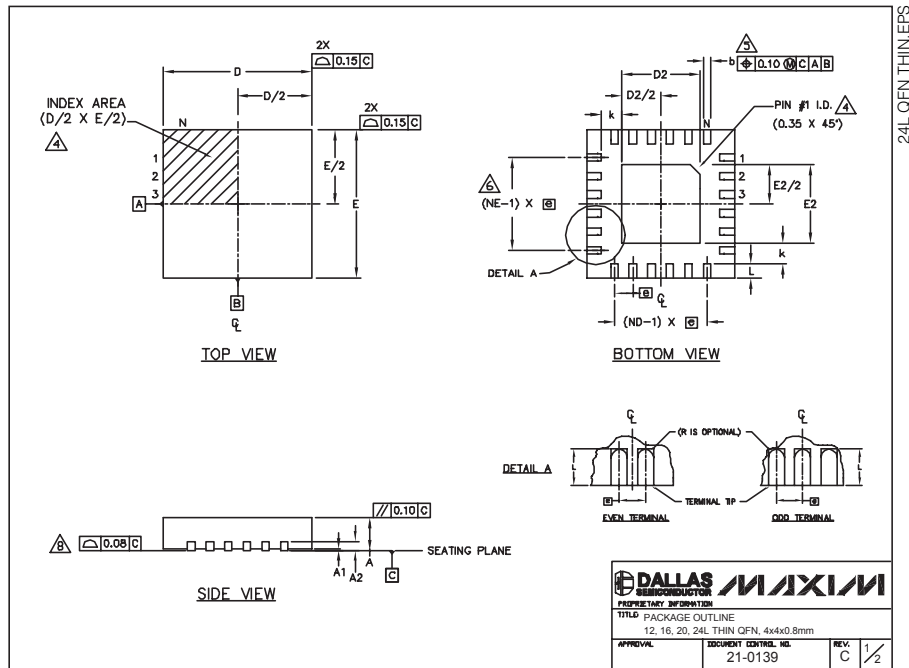


16L UCSP.EPS

4.5Ω Quad SPST Analog Switches in UCSP

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



COMMON DIMENSIONS												
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
AL	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.25	0.30	0.35	0.18	0.23	0.30
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC			0.65 BSC			0.50 BSC			0.50 BSC		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16			20			24		
ND	3			4			5			6		
NE	3			4			5			6		
Upper Var.	WGGB			WGGB			WGGB-1			WGGB-2		

EXPOSED PAD VARIATIONS									
PKG CODES	D2			E2			DOWN BONDS ALLOWED		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.			
T1244-2	1.95	2.10	2.25	1.95	2.10	2.25	NO		
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	YES		
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	NO		
T1644-2	1.95	2.10	2.25	1.95	2.10	2.25	NO		
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	YES		
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	NO		
T2044-1	1.95	2.10	2.25	1.95	2.10	2.25	NO		
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	YES		
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	NO		
T2444-1	2.45	2.60	2.63	2.45	2.60	2.63	NO		
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	YES		
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	YES		
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	NO		

NOTES:

- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
- N IS THE TOTAL NUMBER OF TERMINALS.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SFP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
- ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
- DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
- COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
- DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-1, T2444-3 AND T2444-4.

MAXIM

DALLAS SEMICONDUCTOR

PROPRIETARY INFORMATION

TITLE PACKAGE OUTLINE

12, 16, 20, 24L THIN QFN, 4x4x0.8mm

APPROVAL

DOCUMENT CONTROL NO. 21-0139

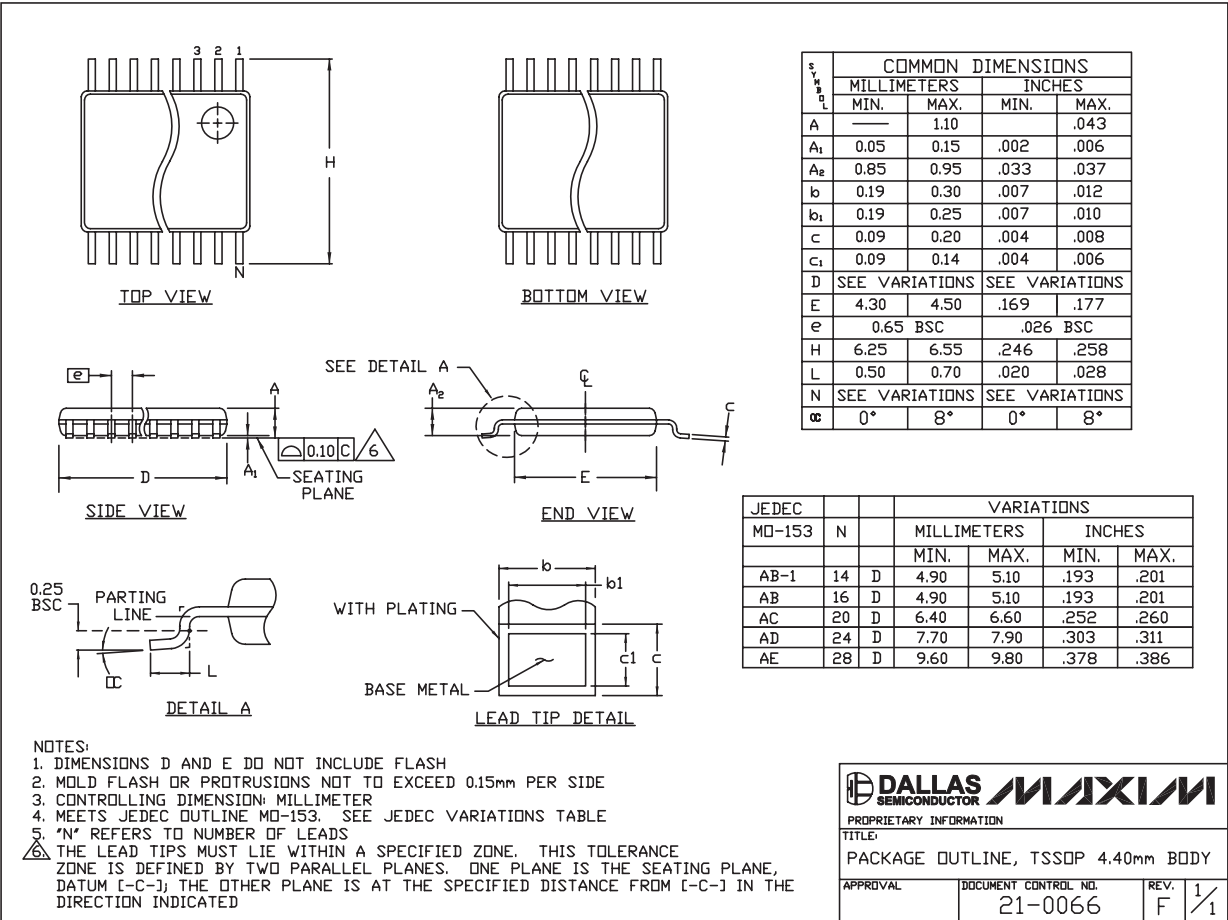
REV. C

2/2

4.5Ω Quad SPST Analog Switches in UCSP

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



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