CS52843

Current Mode PWM Control Circuit

The CS52843 provides all the necessary features to implement off–line fixed frequency current–mode control with a minimum number of external components.

The CS52843 incorporates a new precision temperature–controlled oscillator to minimize variations in frequency. An undervoltage lockout ensures that V_{REF} is stabilized before the output stage is enabled. In the CS52843 turn on is at 8.4 V and turn off at 7.6 V.

Other features include low start–up current, pulse–by–pulse current limiting, and a high–current totem pole output for driving capacitive loads, such as gate of a power MOSFET. The output is low in the off state, consistent with N–channel devices.

Features

- Optimized for Off–Line Control
- Internally Temperature Compensated Oscillator
- V_{REF} Stabilized before Output Stage is Enabled
- Very Low Start–Up Current 300 μA (typ)
- Pulse–by–Pulse Current Limiting
- Improved Undervoltage Lockout
- Double Pulse Suppression
- 2.0% 5.0 Volt Reference
- High Current Totem Pole Output

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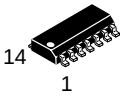
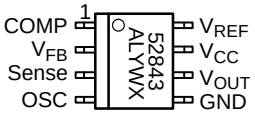
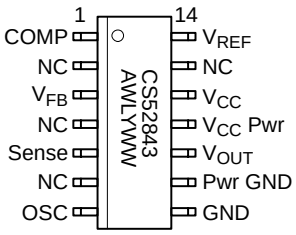
SO–8
D SUFFIX
CASE 751



SO–14
D SUFFIX
CASE 751A

PIN CONNECTIONS AND MARKING DIAGRAMS





A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
CS52843ED8	SO–8	95 Units/Rail
CS52843EDR8	SO–8	2500 Tape & Reel
CS52843ED14	SO–14	55 Units/Rail
CS52843EDR14	SO–14	2500 Tape & Reel

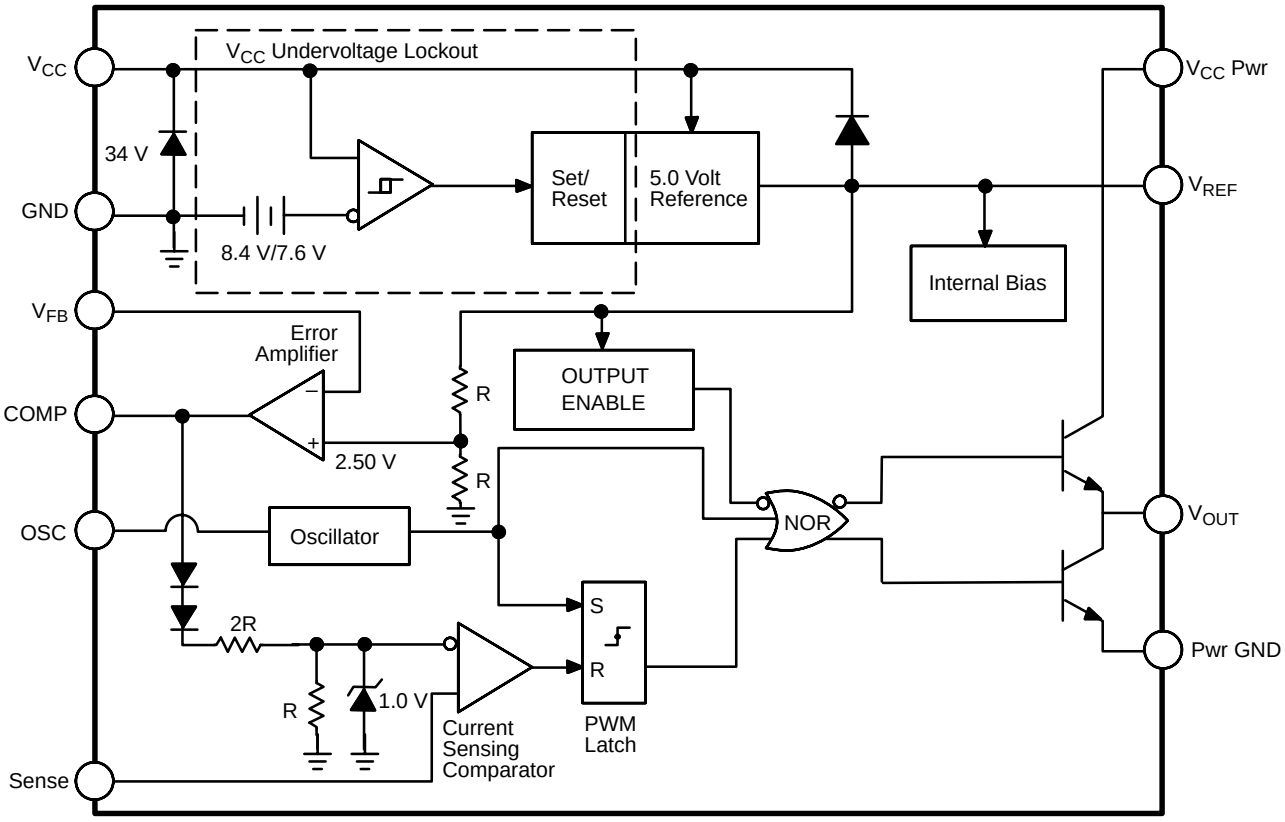


Figure 1. Block Diagram

MAXIMUM RATINGS*

Rating	Value	Unit
Supply Voltage (I_{CC} < 30 mA)	Self Limiting	–
Supply Voltage (Low Impedance Source)	30	V
Output Current	±1.0	A
Output Energy (Capacitive Load)	5.0	μJ
Analog Inputs (V_{FB}, V_{SENSE})	–0.3 to 5.5	V
Error Amp Output Sink Current	10	mA
Lead Temperature Soldering: Reflow: (SMD styles only) (Note 1)	230 peak	°C

1. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS (–40°C ≤ T_A ≤ 85°C; V_{CC} = 15 V (Note 2.); R_T = 680 Ω; C_T = 0.022 μF for triangle mode, R_T = 10 kΩ; C_T = 3.3 nF sawtooth mode; unless otherwise specified.)

Parameter	Test Conditions	Min	Typ	Max	Unit
Reference Section					
Output Voltage	T_J = 25°C, I_{REF} = 1.0 mA	4.9	5.0	5.1	V
Line Regulation	12 ≤ V_{CC} ≤ 25 V	–	6.0	20	mV
Load Regulation	1.0 ≤ I_{REF} ≤ 20 mA	–	6.0	25	mV
Temperature Stability	Note 2.	–	0.2	0.4	mV/°C
Total Output Variation	Line, Load, Temp. Note 2.	4.82	–	5.18	V
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz, T_J = 25°C, Note 2.	–	50	–	μV
Long Term Stability	T_A = 125°C, 1000 Hrs. Note 2.	–	5.0	25	mV
Output Short Circuit	T_A = 25°C	–30	–100	–180	mA
Oscillator Section					
Initial Accuracy	Sawtooth Mode, T_J = 25°C, Note 2. Triangle Mode, T_J = 25°C	47 44	52 52	57 60	kHz kHz
Voltage Stability	12 ≤ V_{CC} ≤ 25 V	–	0.2	1.0	%
Temperature Stability	Sawtooth Mode T_{MIN} ≤ T_A ≤ T_{MAX} Triangle Mode T_{MIN} ≤ T_A ≤ T_{MAX}, Note 2.	– –	5.0 8.0	– –	% %
Amplitude	V_{OSC} (peak to peak)	–	1.7	–	V
Discharge Current	T_J = 25°C T_{MIN} ≤ T_A ≤ T_{MAX}	7.3 6.8	8.3 –	9.3 9.8	mA mA
Error Amp Section					
Input Voltage	V_{COMP} = 2.5 V	2.42	2.50	2.58	V
Input Bias Current	V_{FB} = 0 V	–	–0.3	–2.0	μA
A_{VOL}	2.0 ≤ V_{OUT} ≤ 4.0 V	65	90	–	dB
Unity Gain Bandwidth	Note 2.	0.7	1.0	–	MHz
PSRR	12 ≤ V_{CC} ≤ 25 V	60	70	–	dB
Output Sink Current	V_{FB} = 2.7 V, V_{COMP} = 1.1 V	2.0	6.0	–	mA
Output Source Current	V_{FB} = 2.3 V, V_{COMP} = 5.0 V	–0.5	–0.8	–	mA
V_{OUT} HIGH	V_{FB} = 2.3 V, R_L = 15 kΩ to GND	5.0	6.0	–	V
V_{OUT} LOW	V_{FB} = 2.7 V, R_L = 15 kΩ to V_{REF}	–	0.7	1.1	V
Current Sense Section					
Gain	Notes 3 & 4.	2.85	3.0	3.15	V/V
Maximum Input Signal	V_{COMP} = 5.0 V, Note 3.	0.9	1.0	1.1	V
PSRR	12 ≤ V_{CC} ≤ 25 V, Note 3.	–	70	–	dB
Input Bias Current	V_{SENSE} = 0 V	–	–2.0	–10	μA
Delay to Output	T_J = 25°C, Note 2.	–	150	300	ns

2. These parameters, although guaranteed, are not 100% tested in production.

3. Parameter measured at a trip point of latch with V_{FB} = 0.

4. Gain defined as: $A = \frac{\Delta V_{COMP}}{\Delta V_{SENSE}}$; $0 \le V_{SENSE} \le 0.8$ V

ELECTRICAL CHARACTERISTICS (continued) (–40°C ≤ T_A ≤ 85°C; V_{CC} = 15 V (Note 2.); R_T = 680 Ω; C_T = 0.022 μF for triangle mode, R_T = 10 kΩ; C_T = 3.3 nF sawtooth mode; unless otherwise specified.)

Parameter	Test Conditions	Min	Typ	Max	Unit
Output Section					
Output Low Level	I_{SINK} = 20 mA I_{SINK} = 200 mA	– –	0.1 1.5	0.4 2.2	V V
Output High Level	I_{SOURCE} = 20 mA I_{SOURCE} = 200 mA	13 12	13.5 13.5	– –	V V
Rise Time	T_J = 25°C, C_L = 1.0 nF, Note 5.	–	50	150	ns
Fall Time	T_J = 25°C, C_L = 1.0 nF, Note 5.	–	50	150	ns
Output Leakage	UVLO Active V_{OUT} = 0	–	–0.01	–10	μA
Total Standby Current					
Start–Up Current	–	–	300	500	μA
Operating Supply Current	V_{FB} = V_{SENSE} = 0 V, R_T = 10 kΩ; C_T = 3.3 nF	–	11	17	mA
V_{CC} Zener Voltage	I_{CC} = 25 mA	–	34	–	V
Undervoltage Lockout Section					
Start Threshold	–	7.8	8.4	9.0	V
Min. Operating Voltage	After Turn On	7.0	7.6	8.2	V

5. These parameters, although guaranteed, are not 100% tested in production.

PACKAGE PIN DESCRIPTION

Package Lead Number		Lead Symbol	Function
SO–8	SO–14		
1	1	COMP	Error amp output, used to compensate error amplifier.
2	3	V_{FB}	Error amp inverting input.
3	5	SENSE	Noninverting input to Current Sense Comparator.
4	7	OSC	Oscillator timing network with capacitor to ground, resistor to V_{REF}.
5	8	GND	Ground.
–	9	Pwr GND	Output driver ground.
6	10	V_{OUT}	Output drive pin.
–	11	V_{CC}Pwr	Output driver positive supply.
7	12	V_{CC}	Positive power suppy.
8	14	V_{REF}	Output of 5.0 V internal reference.
–	2, 4, 6, 13	NC	No Connection.

TYPICAL PERFORMANCE CHARACTERISTICS

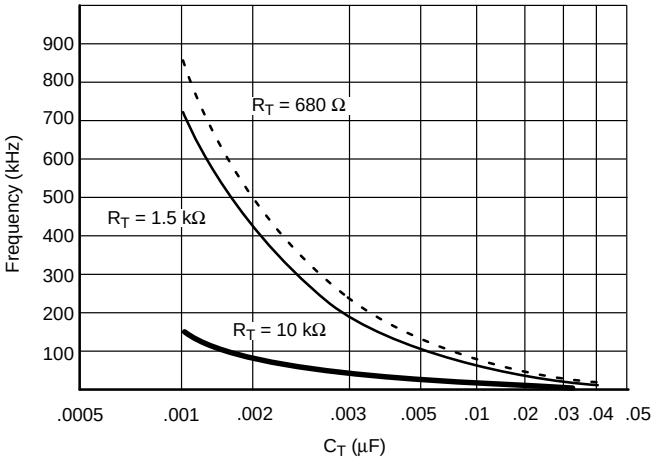


Figure 2. Oscillator Frequency vs C_T

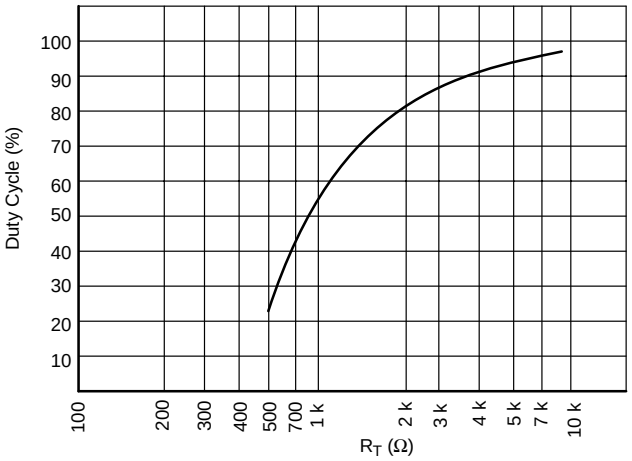


Figure 3. Oscillator Duty Cycle vs R_T

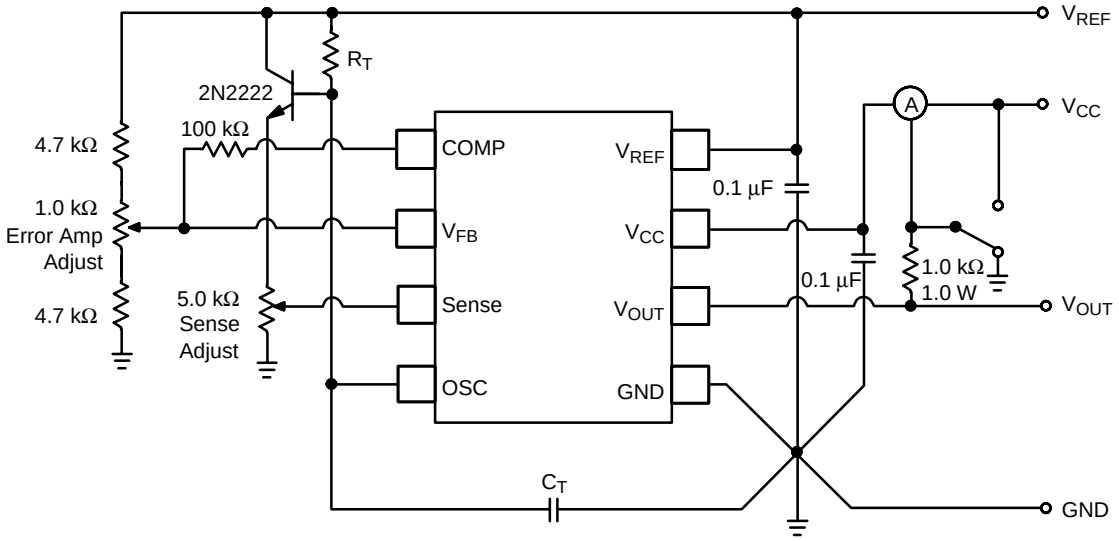


Figure 4. Test Circuit Open Loop Laboratory Test Fixture

CIRCUIT DESCRIPTION

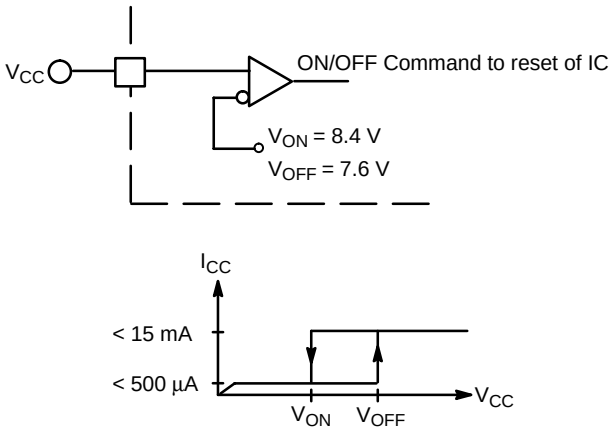


Figure 5. Startup Voltage for the CS52843

Undervoltage Lockout

During Undervoltage Lockout (Figure 5), the output driver is biased to sink minor amounts of current. The output should be shunted to ground with a resistor to prevent activating the power switch with extraneous leakage currents.

PWM Waveform

To generate the PWM waveform, the control voltage from the error amplifier is compared to a current sense signal which represents the peak output inductor current (Figure 6). An increase in V_{CC} causes the inductor current slope to increase, thus reducing the duty cycle. This is an inherent feed–forward characteristic of current mode control, since

the control voltage does not have to change during changes of input supply voltage.

When the power supply sees a sudden large output current increase, the control voltage will increase allowing the duty cycle to momentarily increase. Since the duty cycle tends to exceed the maximum allowed to prevent transformer saturation in some power supplies, the internal oscillator waveform provides the maximum duty cycle clamp as programmed by the selection of oscillator timing components.

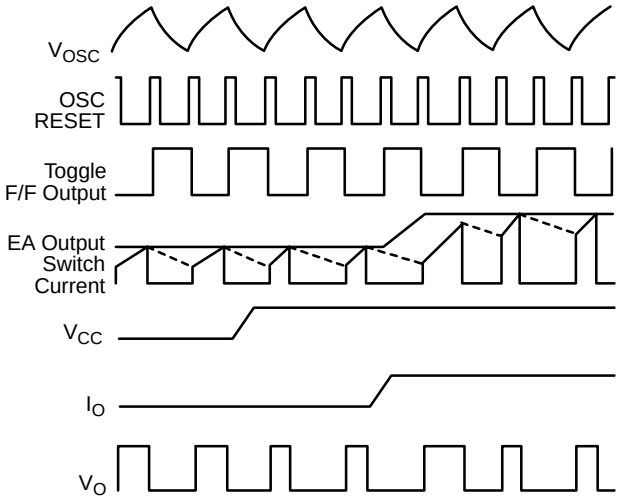


Figure 6. Timing Diagram

Setting the Oscillator

The times t_c and t_d can be determined as follows:

$$t_c = R_T C_T \ln\left(\frac{V_{REF} - V_{LOWER}}{V_{REF} - V_{UPPER}}\right)$$

$$t_d = R_T C_T \ln\left(\frac{V_{REF} - I_d R_T V_{LOWER}}{V_{REF} - I_d R_T - V_{UPPER}}\right)$$

Substituting in typical values for the parameters in the above formulas:

$$V_{REF} = 5.0\ V, V_{UPPER} = 2.7\ V,$$

$$V_{LOWER} = 1.0\ V, I_d = 8.3\ mA$$

then

$$t_c \approx 0.5534 R_T C_T$$

$$t_d = R_T C_T \ln\left(\frac{2.3 - 0.0083 R_T}{4.0 - 0.0083 R_T}\right)$$

For better accuracy R_T should be ≥ 10 kΩ.

Grounding

High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to GND in a single point ground.

The transistor and 5.0 kΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to Sense.

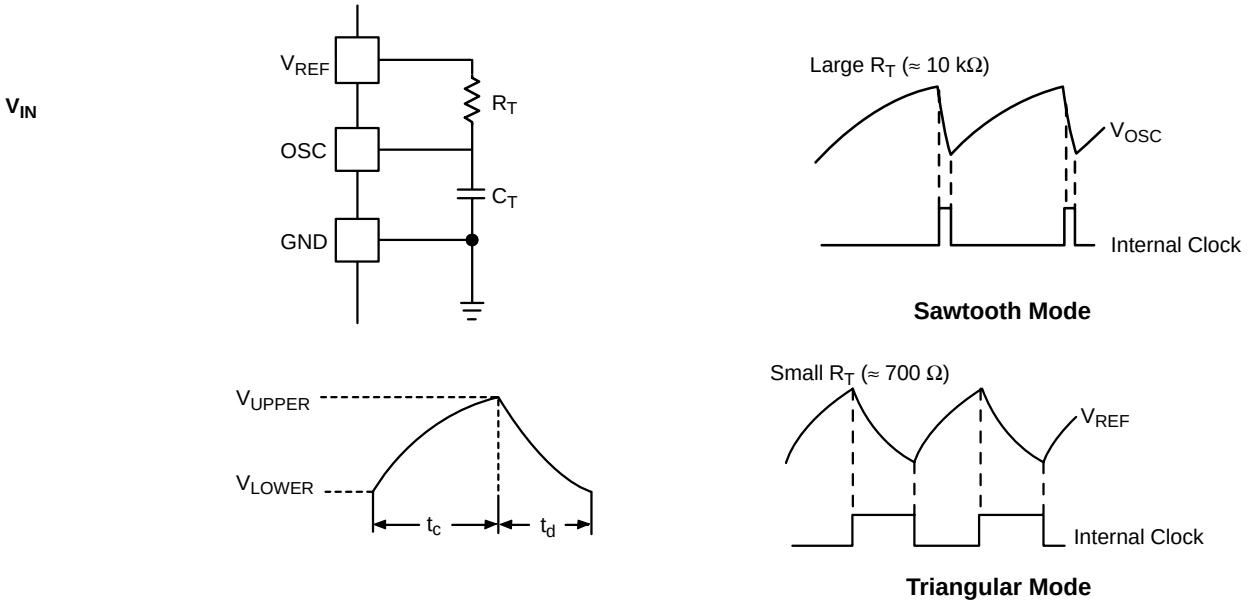
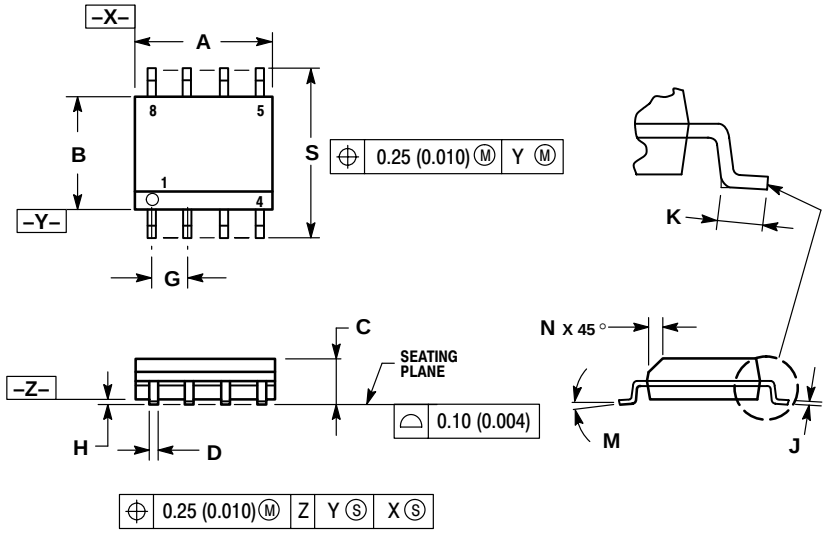


Figure 7. Oscillator Timing Network and Parameters

PACKAGE DIMENSIONS

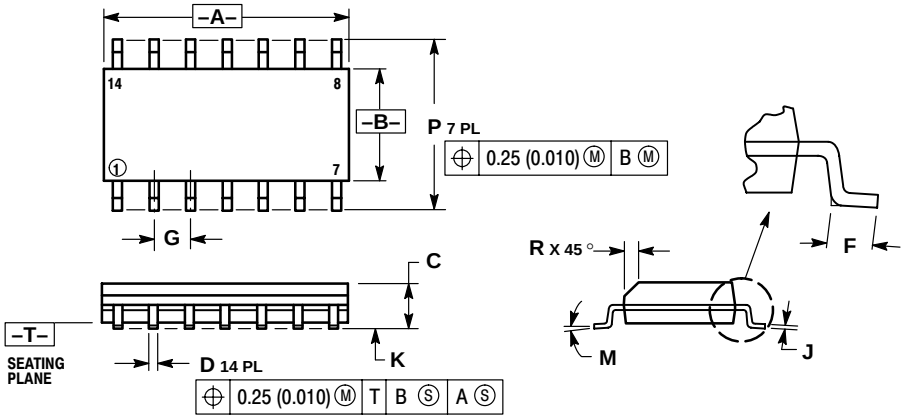
SO–8
DF SUFFIX
CASE 751–07
ISSUE W



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SO–14
D SUFFIX
CASE 751A–03
ISSUE F



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	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

PACKAGE THERMAL DATA

Parameter		SO–8	SO–14	Unit
$R_{\Theta JC}$	Typical	45	30	°C/W
$R_{\Theta JA}$	Typical	165	125	°C/W

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
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