CYM9270
CYM9271A/B
CYM9272A/B
CYM9273

PRELIMINARY

64K x 36 SRAM Module
128K x 36 SRAM Module
256K x 36 SRAM Module
512K x 36 SRAM Module

Features

- **Operates at 50 MHz**
- **Uses 64K x 18 / 128K x 18 or 256K x 18 high performance synchronous SRAMs.**
- **144-position Angled DIMM from Berg p/n 61178**
- **3.3V inputs/data outputs**

Functional Description

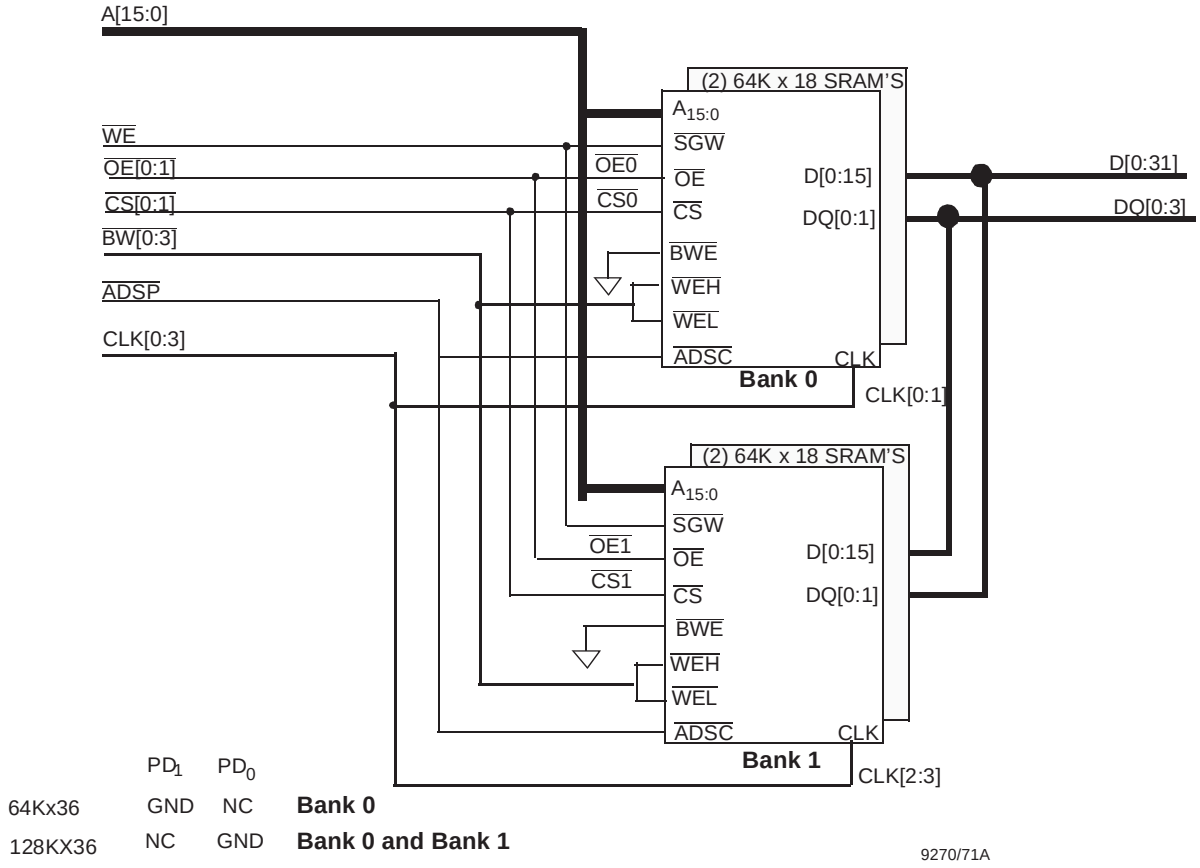
The CYM9270, CYM9271, CYM9272 and the CYM9273 are high-performance synchronous memory modules organized as 64K(9270), 128K(9271), 256K(9272), 512K(9273) by 36 bits. These modules are constructed using either 64K x 18 SRAM's (CYM9270, CYM9271A), 128K x 18 SRAM's (9271B, 9272A) or 256K x 18 SRAM's (9272B, 9273). in plastic surface mount packages on an epoxy laminate board with pins. The modules are designed to be incorporated into large memory arrays.

The modules are configured as single banks or multiple banks depending on the SRAM used to make the module. Separate clock are provided for each of the banks. Separate clocks are provided for each of the SRAM's.

Multiple ground pins and on-board de-coupling capacitors ensure high performance with maximum noise immunity.

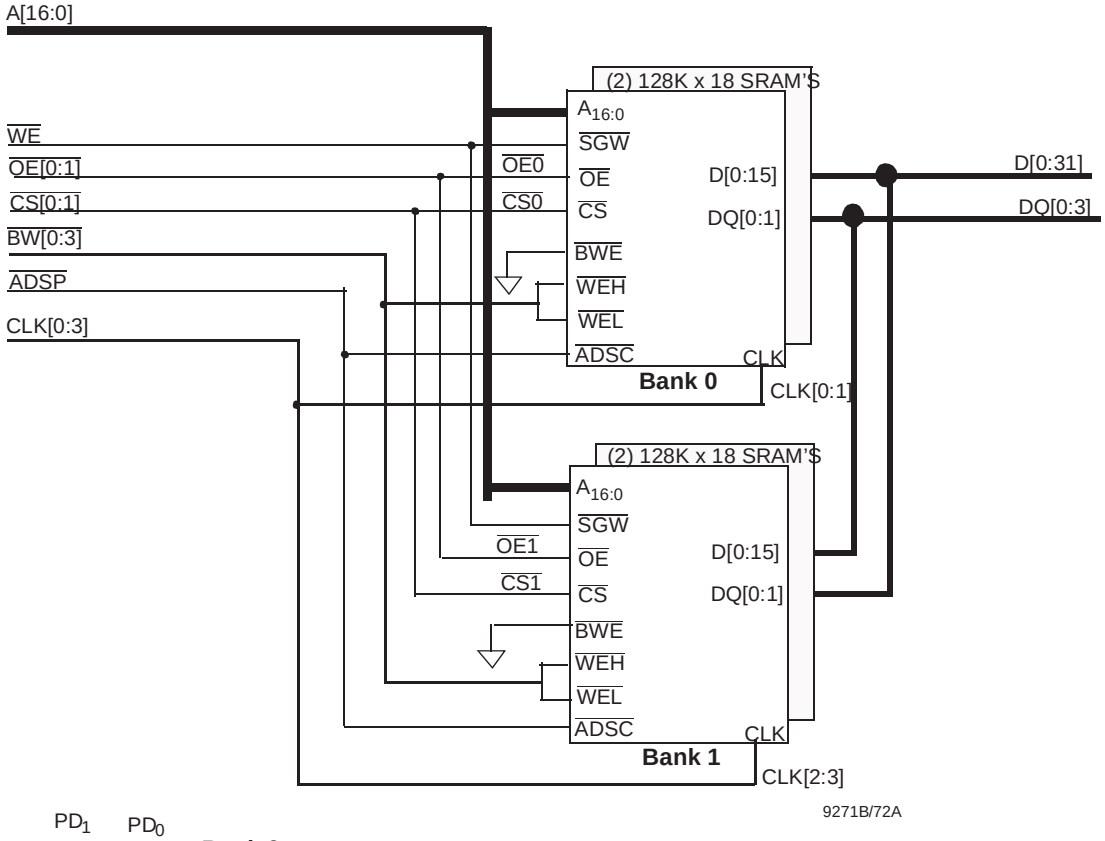
All components on the cache modules are surface mounted on a multi-layer epoxy laminate (FR-4) substrate. The contact pins are plated with 150 micro-inches of nickel covered by 30 micro-inches of gold flash.

Logic Block Diagram - CYM9270/CYM9271A



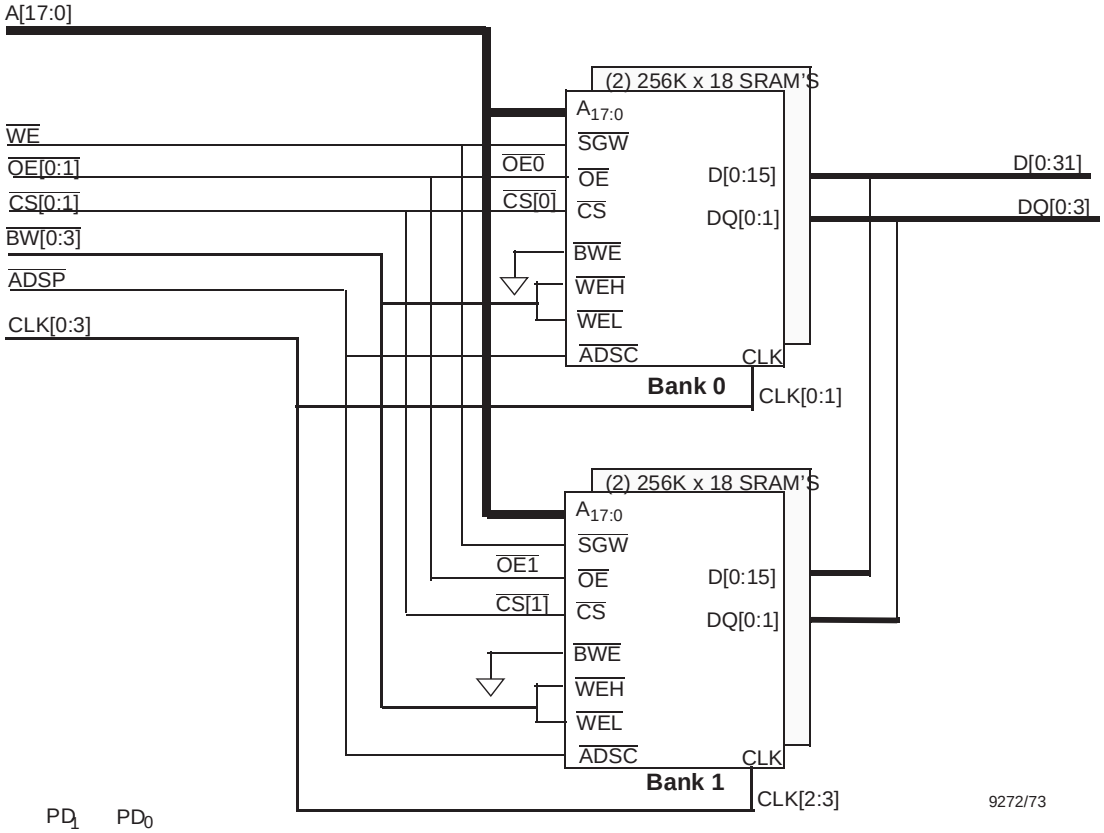
	PD_1	PD_0	
64Kx36	GND	NC	**Bank 0**
128KX36	NC	GND	**Bank 0 and Bank 1**

Logic Block Diagram - CYM9271B/CYM9272A



	PD_1	PD_0	
128Kx36	NC	GND	**Bank 0**
256KX36	GND	GND	**Bank 0 and Bank 1**

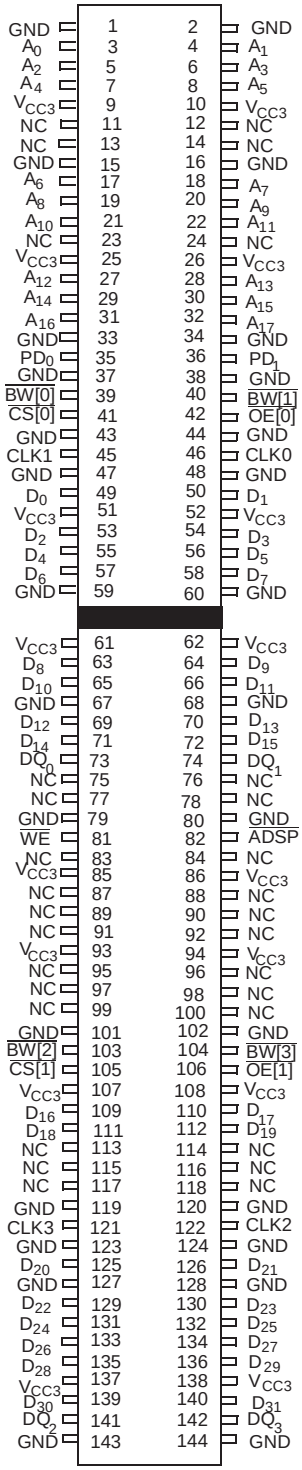
Logic Block Diagram - CYM9272B/CYM9273



	PD_1	PD_0	
256KX36	GND	GND	**Bank 0**
512KX36	NC	NC	**Bank 0 and 1**

PinConfiguration

Dual Read-Out SIMM (DIMM)
Top View



Pin Definitions

Signal	Description
V_{CC3}	3V Supply
GND	Ground
A[17:0]	Addresses from processor
$\overline{ADSP}$	Address strobe from the processor
$\overline{OE}$[1:0]	Output Enables for each of the banks
$\overline{BW}$[0:3]	Byte writes
$\overline{WE}$	Global Write
$\overline{CS}$[1:0]	Chip Select for the two banks.
PD_0-PD_1	Presence Detect output pins
D[31:0]	Data lines from processor
DQ[3:0]	Data Parity lines from processor
CLK[0:3]	Clock lines to the module.
NC	Signal not connected on module
RSVD	Reserved

Presence Detect Pins

	PD_1	PD_0
CYM9270 - 64K x 36	GND	NC
CYM9271 - 128K x 36	NC	GND
CYM9272 - 256K x 36	GND	GND
CYM9273 - 512K x 36	NC	NC

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –55°C to +125°C

Ambient Temperature with Power Applied ..... –0°C to +70°C

3.3V Supply Voltage to Ground Potential..... –0.5V to +4.5V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to +4.6V

DC Input Voltage ..... –0.5V to +4.6V

Output Current into Outputs (LOW)..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Condition	Min.	Max.	Unit
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC}=Min. I_{OH} = –4 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC}=Min. I_{OL} = 8 mA		0.4	V
$I_{cc(9270)}$	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		TBD	mA
$I_{cc(9271)}$	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		TBD(64K) 500(128K)	mA
$I_{CC\ (9272))}$	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		1000(128K) 600(256K)	mA
$I_{CC\ (9273)}$	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		1200(256K)	mA

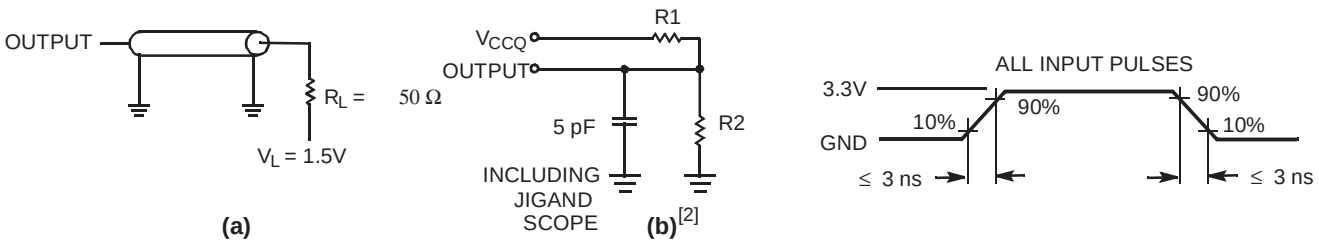
Capacitance[1]

Parameter	Description	Test Conditions	Max.	Max.	Unit
C_A	Address Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	9270	12	pF
			9271	24(64K x 18) 7(128K x 18)	
			9272	14(128K x 18) 10(256K x 18)	
			9273	20(256K x18)	pF
C_I	Control Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	9270	12	pF
			9271	24(64K x 18) 8(128K x 18)	
			9272	16(128K x 18) 10(256K x 18)	
			9273	20(256K x 18)	pF
C_O	Input / Output Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	9270	9	pF
			9271	18(64K x 18) 5(128K x 18)	
			9272	10(128K x 18) 8(256K x 18)	
			9273	16(256K x 18)	pF
C_{CLK}	Clock Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	9270	6	pF
			9271	6(64K x 18) 3(128K x 18)	
			9272	3(128K x 18) 5(256K x 18)	
			9273	5(256K x 18)	pF

Note:

1. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms[3]



Switching Characteristics Over the Operating Range

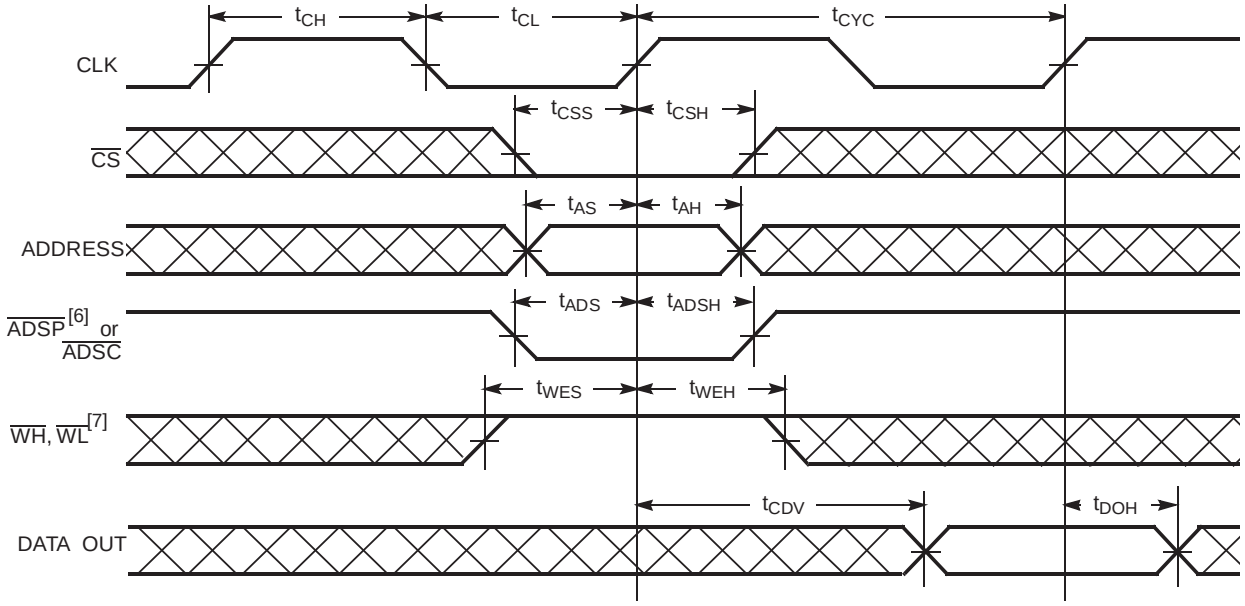
Parameter	Description	CYM9270		CYM9271		CYM9272		CYM9273		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	12		12		12		12		ns
t_{CH}	Clock HIGH	4		4		4		4		ns
t_{CL}	Clock LOW	4		4		4		4		ns
t_{AS}	Address Set-Up Before CLK Rise	3		3		3		3		ns
t_{AH}	Address Hold After CLK Rise	0.5		0.5		0.5		0.5		ns
t_{CDV}	Data Output Valid After CLK Rise		10.3		10.3		10.3		10.3	ns
t_{DOH}	Data Output Hold After CLK Rise	3		3		3		3		ns
t_{WES}	$\overline{WH}$, $\overline{WL}$ Set-Up Before CLK Rise	3.1		3.1		3.1		3.1		ns
t_{WEH}	$\overline{WH}$, $\overline{WL}$ Hold After CLK Rise	0.5		0.5		0.5		0.5		ns
t_{DS}	Data Input Set-Up Before CLK Rise	3.3		3.3		3.3		3.3		ns
t_{DH}	Data Input Hold After CLK Rise	0.5				0.5		0.5		ns
t_{CSS}	Chip Select Set-Up	3.1		3.1		3.1		3.1		ns
t_{CSH}	Chip Select Hold After CLK Rise	0.5		0.5		0.5		0.5		ns
t_{EOZ}[4]	$\overline{OE}$ HIGH to Output High Z		7		7		7		7	ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid	7		7		7		7		ns

Notes:

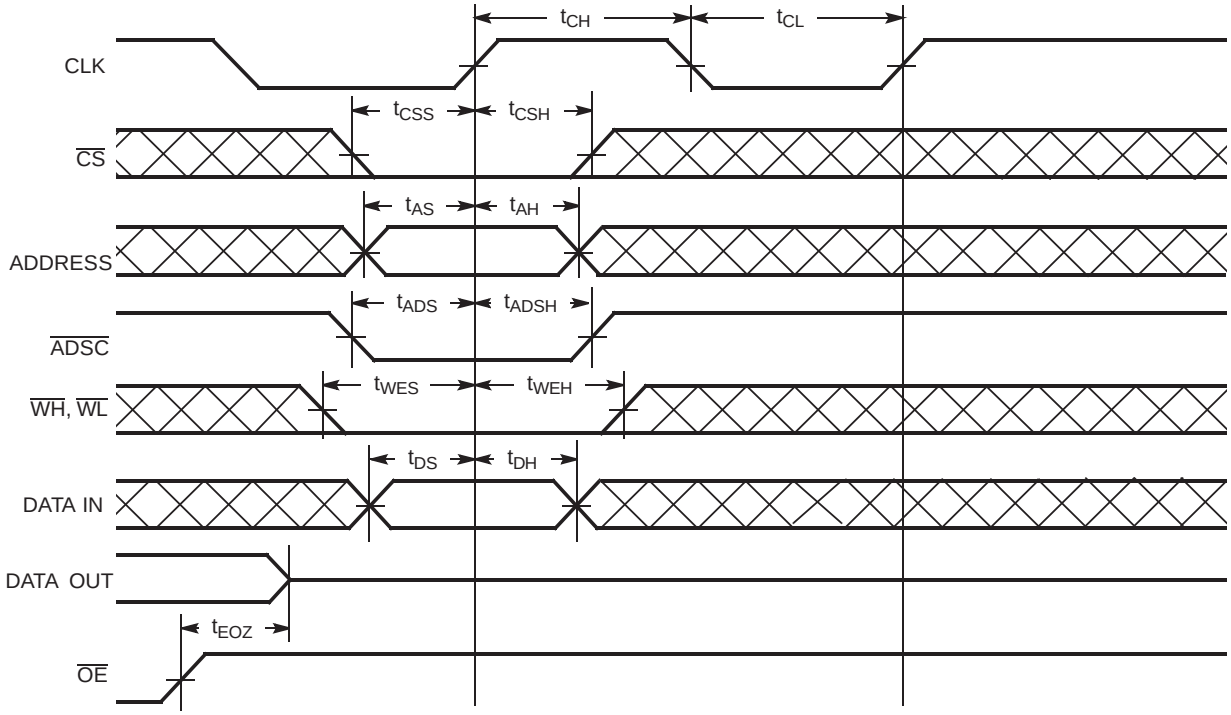
2. Resistor values for V_{CCQ}=3.3V are R1=317Ω and R2=351Ω.
3. Unless otherwise noted, test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and load capacitance. Shown in (a) and (b) of AC test loads. All measurements are at room temperature.
4. t_{EOZ} is specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.

Switching Waveforms

Single Read[5]



Single Write Timing

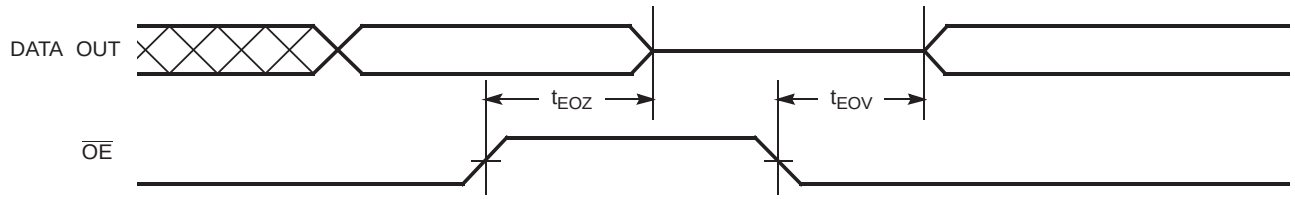


Notes:

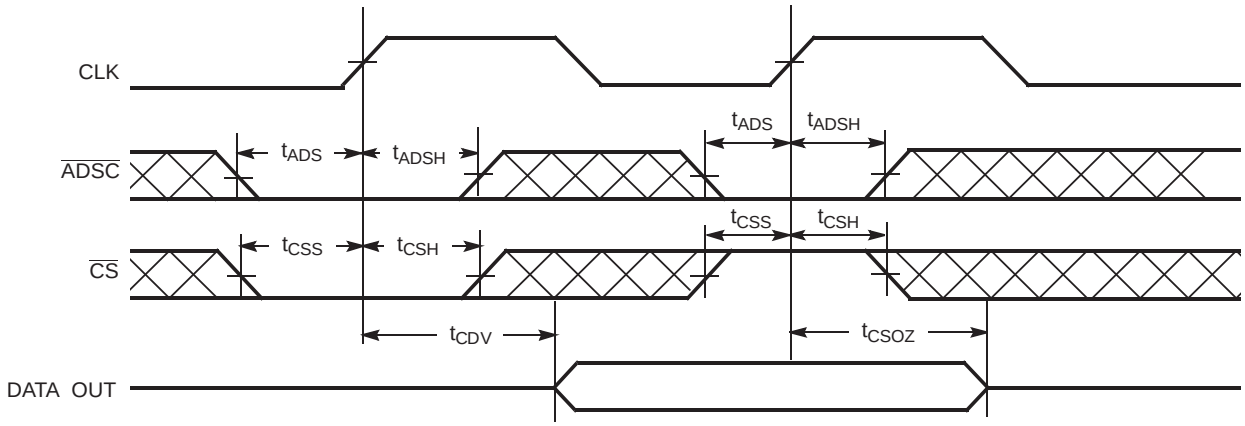
5. OE is LOW throughout this operation.
6. If ADSP is asserted while CS is HIGH, ADSP will be ignored.
7. ADSP has no effect on ADV, WL, and WH if CS is HIGH.

Switching Waveforms (continued)

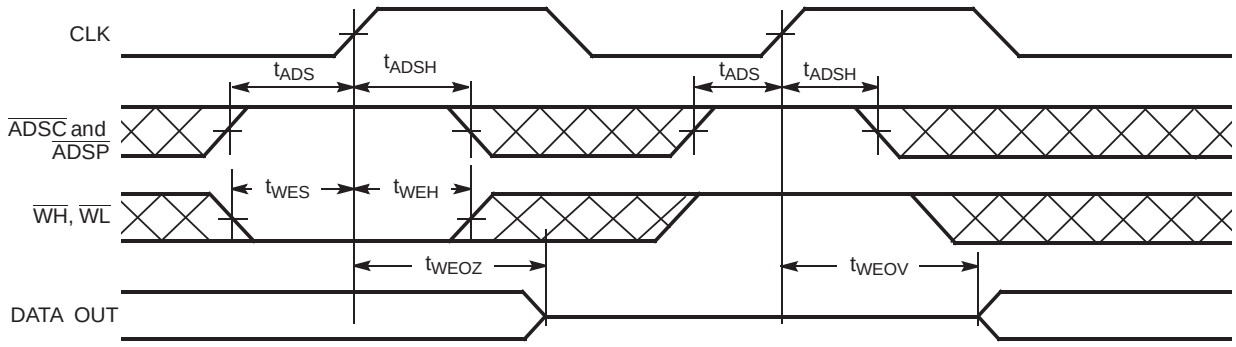
Output (Controlled by $\overline{OE}$)



Output Timing (Controlled by $\overline{CS}$)



Output Timing (Controlled by $\overline{WH}$/ $\overline{WL}$)



Ordering Information

Speed(MHz)	Ordering Code	Package Name	Package Type	Description	Operating Range
50	CYM9270PM-50C	PM45	144-Pin Dual-Readout SIMM	Sync 64K x 36	Commercial
	CYM9271APM-50C	PM46	144-Pin Dual-Readout SIMM	Sync 128K x 36	
	CYM9271BPM-50C	PM45	144-Pin Dual-Readout SIMM	Sync 128K x 36	
	CYM9272APM-50C	PM46	144-Pin Dual-Readout SIMM	Sync 256K x 36	
	CYM9272BPM-50C	PM45	144-Pin Dual-Readout SIMM	Sync 256K x 36	
	CYM9273PM-50C	PM46	144-Pin Dual-Readout SIMM	Sync 512K x 36	

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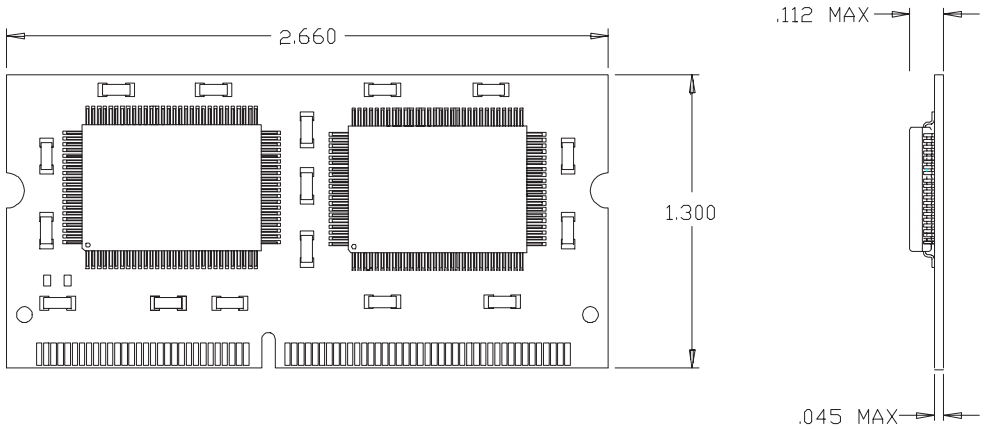
Package Diagrams

144-Pin Single-Sided DIMM PM45



144-Pin Dual-Sided DIMM PM46