32-Channel Serial to Parallel Converter With High Voltage Push-Pull Outputs

Features

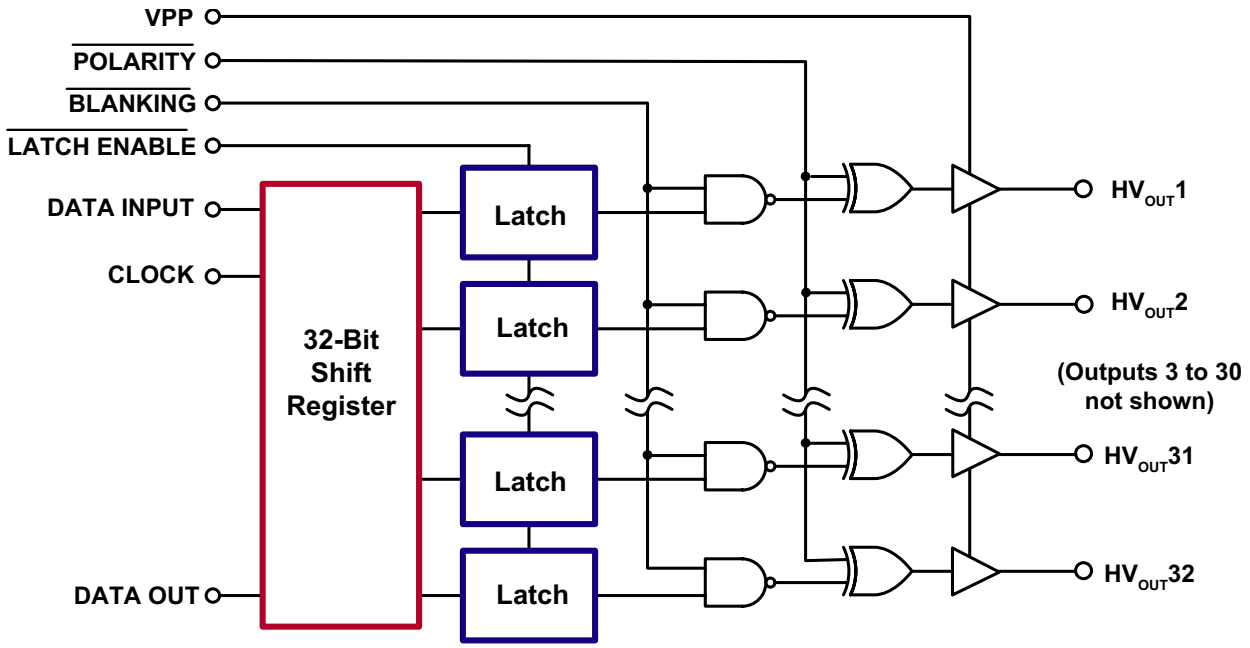
- Processed with HVCMOS® technology
- Output voltages up to 80V
- Low power level shifting
- Shift register speed 8.0MHz
- Latched data outputs
- 5.0V CMOS compatible inputs
- Forward and reverse shifting options
- Diode to V_{PP} allows efficient power recovery

General Description

The HV9708 is a low voltage serial to high voltage parallel converters with push-pull outputs. This device has been designed for use as a driver for AC-electroluminescent displays.It can also be used in any application requiring multiple output, high voltage current sourcing and sinking capabilities such as driving plasma panels, vacuum fluorescent, or large matrix LCD displays. The inputs are fully CMOS compatible.

This device consists of a 32-bit shift register, 32 latches, and control logic to perform the polarity select and blanking of the outputs. $HV_{OUT}1$ is connected to the first stage of the shift register through the polarity and blanking logic. Data is shifted through the shift register on the logic low to high transition of the clock. The HV9708 shifts data in the clockwise direction when viewed from the top of the package. A data output buffer is provided for cascading devices.This output reflects the current status of the last bit of the shift register ($HV_{OUT}32$). Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), $\overline{BL}$ (blanking), or the $\overline{POL}$ (polarity) in-puts. Transfer of data from the shift register to the latch occurs when the $\overline{LE}$ (latch enable) input is high. The data in the latch is stored when $\overline{LE}$ is low.

Block Diagram



Ordering Information

Part Number	Package	Packing
HV9708PJ-G	44-Lead PLCC	27/Tube
HV9708PJ-G M903	44-Lead PLCC	500/Reel

-G denotes a lead (Pb)-free / RoHS compliant package

Absolute Maximum Ratings

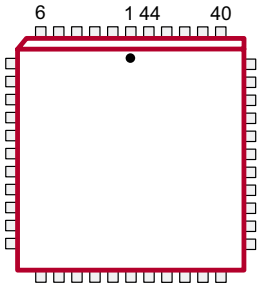
Parameter	Value
Supply voltage, V_{DD}	-0.5V to +7.0V
Supply voltage, V_{PP}	-0.5V to +90V
Logic input levels	-0.5V to V_{DD} +0.5V
Ground current[1]	1.5A
Continuous total power dissipation[2]	1200mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Notes:

1. *Duty cycle is limited by the total power dissipated in the package.*
2. *For operation above 25°C ambient derate linearly to maximum operating temperature at 20mW/°C.*

Pin Configuration



44-Lead PLCC

Product Marking

YY = Year Sealed
WW = Week Sealed
L = Lot Number
A = Assembler ID
C = Country of Origin*
_____ = "Green" Packaging

**May be part of top marking*

Package may or may not include the following marks: Si or

44-Lead PLCC

Typical Thermal Resistance

Package	θ_{ja}
44-Lead PLCC	37°C

Recommended Operating Conditions

Sym	Parameter	Min	Max	Units
V_{DD}	Logic voltage supply	4.5	5.5	V
V_{PP}	High voltage supply	8.0	80	V
V_{IH}	Input high voltage	V_{DD} -0.5	V_{DD}	V
V_{IL}	Input low voltage	0	0.5	V
f_{CLK}	Clock frequency	0	8.0	MHz
T_A	Operating free-air temperature range	-40	+85	°C

Power-Up Sequence

1. Connect ground
2. Apply V_{DD}
3. Set all inputs (Data, CLK, Enable, etc.) to a known state
4. Apply V_{PP}

Power-down sequence should be the reverse of the above.
The V_{PP} should not drop below V_{DD} during operations.

Electrical Characteristics (V_{PP} = 60V, V_{DD} = 5.0V, T_A = 25°C)

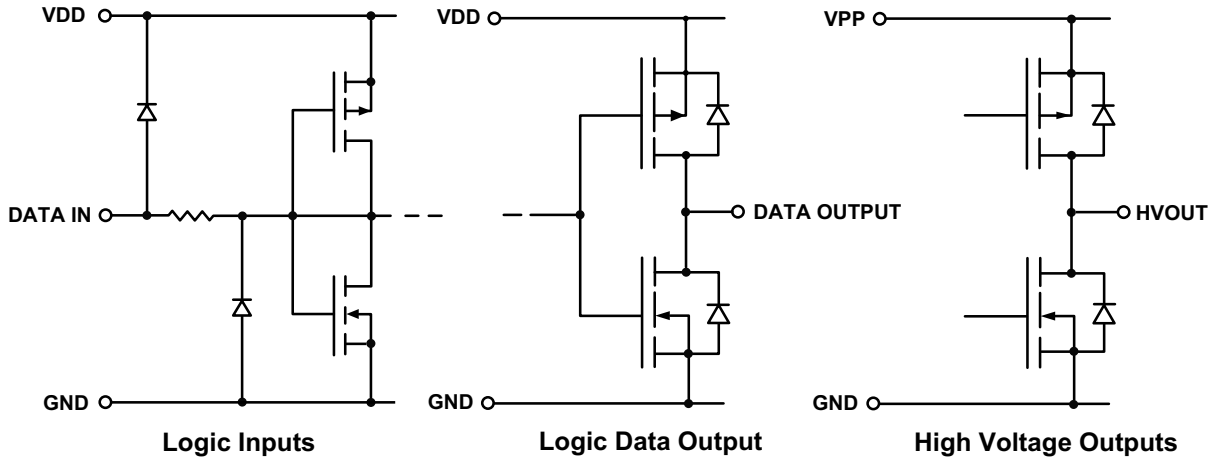
DC Characteristics

Sym	Parameter	Min	Max	Units	Conditions
I_{PP}	V_{PP} supply current	-	100	µA	$HV_{OUTPUTS}$ high to low
I_{DDQ}	I_{DD} supply current (quiescent)	-	100	µA	All inputs = V_{DD} or GND
I_{DD}	I_{DD} supply current (operating)	-	15	mA	V_{DD} = V_{DD} max, f_{CLK} = 8.0 MHz
V_{OH} (Data)	Shift register output voltage	V_{DD} -0.5	-	V	I_O = -100µA
V_{OL} (Data)	Shift register output voltage	-	0.5	V	I_O = 100µA
I_{IH}	Current leakage, any input	-	1.0	µA	Input = V_{DD}
I_{IL}	Current leakage, any input	-	-1.0	µA	Input = GND
V_{OC}	HV output clamp diode voltage	-	-1.5	V	I_{OC} = -5.0mA
V_{OH}	HV output when sourcing	52	-	V	I_{OH} = -20mA, 0 to 70°C
V_{OL}	HV output when sinking	-	4.0	V	I_{OL} = 5.0mA, 0 to 70°C

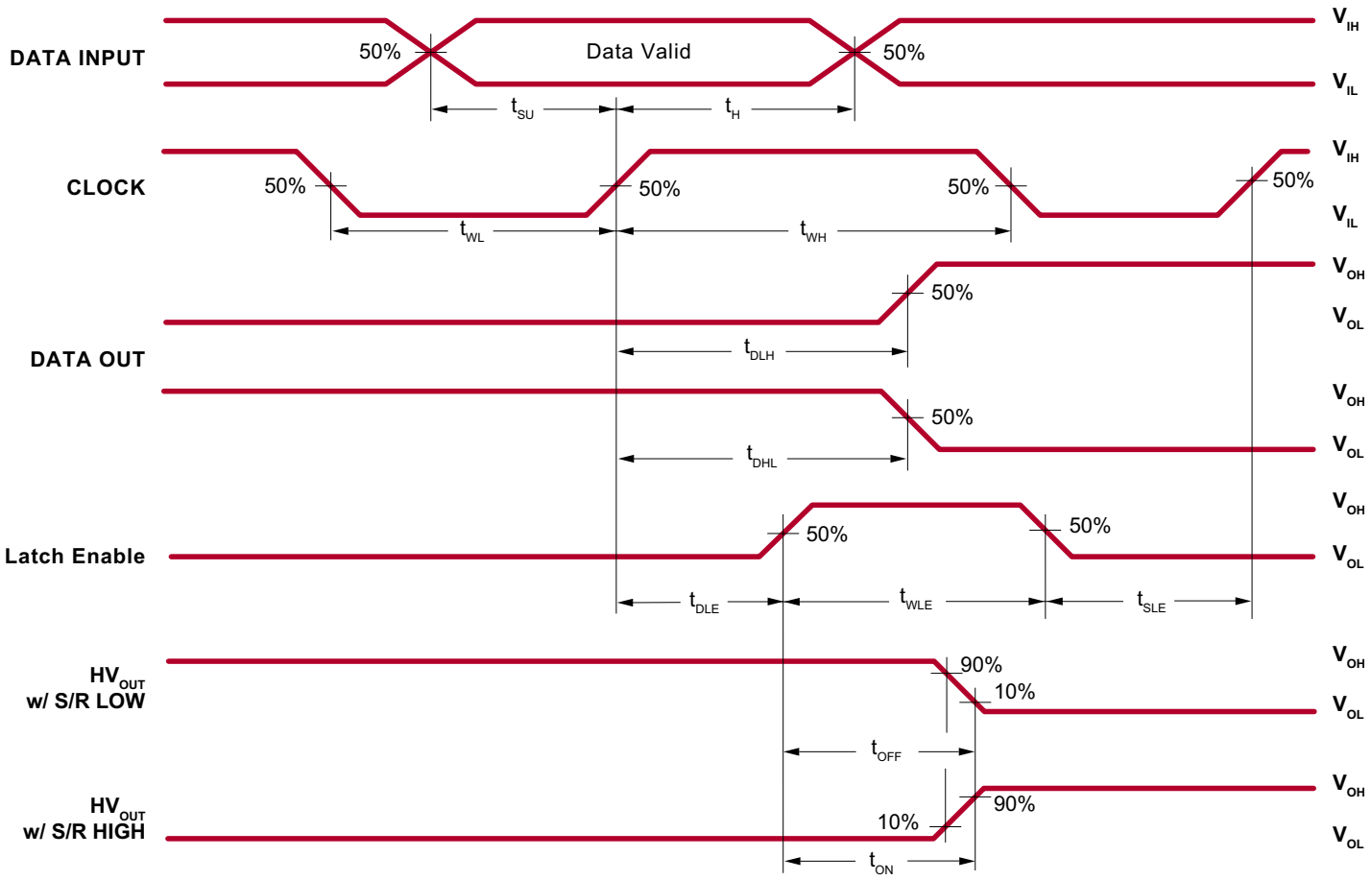
AC Characteristics

Sym	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency	-	8.0	MHz	---
t_{WL} or t_{WH}	Clock width, high or low	62	-	ns	---
t_{SU}	Setup time before CLK rises	25	-	ns	---
t_H	Hold time after CLK rises	10	-	ns	---
t_{DLH} (Data)	Data output delay after L to H CLK	-	110	ns	CL = 15pF
t_{DHL} (Data)	Data output delay after H to L CLK	-	110	ns	CL = 15pF
t_{DLE}	$\overline{LE}$ delay after L to H CLK	50	-	ns	---
t_{WLE}	Width of $\overline{LE}$ pulse	50	-	ns	---
t_{SLE}	$\overline{LE}$ setup time before L to H CLK	50	-	ns	---
t_{ON}	Delay from $\overline{LE}$ to HV_{OUT}, L to H	-	500	ns	---
t_{OFF}	Delay from $\overline{LE}$ to HV_{OUT}, H to L	-	500	ns	---

Input and Output Equivalent Circuits



Switching Waveforms



Function Table

Function	Inputs					Outputs		
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	Shift Reg 1 2...8	HV Outputs 1 2...8	Data Out •
All on	X	X	X	L	L	• •...•	H H...H	•
All off	X	X	X	L	H	• •...•	L L...L	•
Invert mode	X	X	L	H	L	• •...•	$\overline{•}$ $\overline{•...•}$	•
Load S/R	H OR L	↑	L	H	H	H or L •...•	• •...•	•
Load latches	X	X	↑	H	H	• •...•	• •...•	•
	X	X	↑	H	L	• •...•	$\overline{•}$ $\overline{•...•}$	•
Transparent latch mode	L	↑	H	H	H	L •...•	L •...•	•
	H	↑	H	H	H	H •...•	H •...•	•

Notes:

H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition

• = dependent on previous stage's satte before the last CLK or last $\overline{LE}$ high.

Pin Description

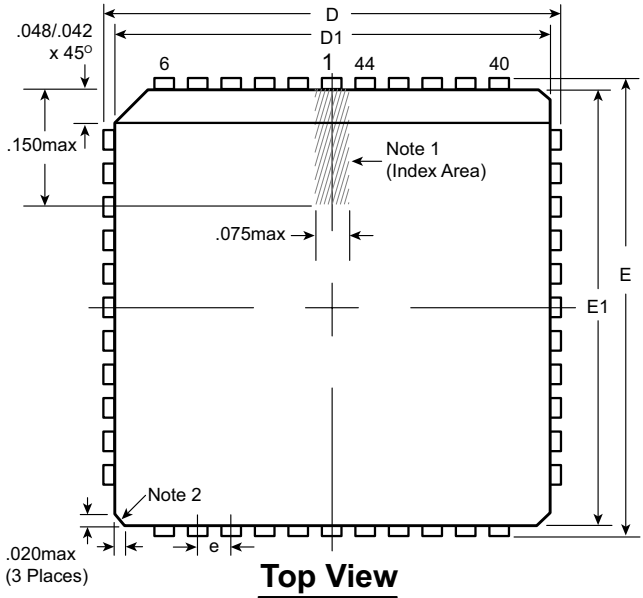
Pin	Function	Function
1	$HV_{OUT}17$	High voltage outputs. High voltage push-pull outputs, which, depending on controlling low voltage data, can drive loads either to a GND, or to V_{PP} rail levels.
2	$HV_{OUT}16$	
3	$HV_{OUT}15$	
4	$HV_{OUT}14$	
5	$HV_{OUT}13$	
6	$HV_{OUT}12$	
7	$HV_{OUT}11$	
8	$HV_{OUT}10$	
9	$HV_{OUT}9$	
10	$HV_{OUT}8$	
11	$HV_{OUT}7$	
12	$HV_{OUT}6$	
13	$HV_{OUT}5$	
14	$HV_{OUT}4$	
15	$HV_{OUT}3$	
16	$HV_{OUT}2$	
17	$HV_{OUT}1$	
18	Data Out	Serial data output Data output for cascading to the data input of the next device.
19	N/C	No connect.
20	N/C	
21	$\overline{\text{Polarity}}$	---
22	CLK	Data shift register clock. Input are shifted into the shift register on the positive edge of the clock.
23	GND	Logic and high voltage ground.
24	VPP	High voltage power rail.
25	VDD	Low voltage logic power rail.
26	$\overline{\text{Latch Enable}}$	Latch enable input. When $\overline{\text{LE}}$ is high, shift register data is transferred into a data latch. When $\overline{\text{LE}}$ is low, data is latched, and new data can be clocked into the shift register.
27	Data In	Serial data input. Data needs to be present before each rising edge of the clock.

Pin Description *(cont.)*

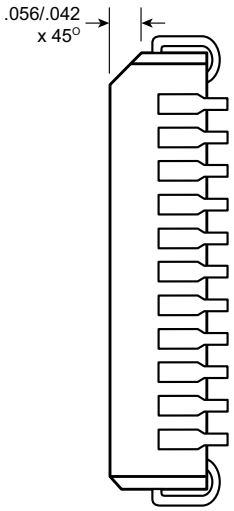
Pin	Function	Function
28	$\overline{\text{Blanking}}$	---
29	N/C	No connect.
30	$HV_{OUT}32$	High voltage outputs. High voltage push-pull outputs, which, depending on controlling low voltage data, can drive loads either to a GND, or to V_{PP} rail levels.
31	$HV_{OUT}31$	
32	$HV_{OUT}30$	
33	$HV_{OUT}29$	
34	$HV_{OUT}28$	
35	$HV_{OUT}27$	
36	$HV_{OUT}26$	
37	$HV_{OUT}25$	
38	$HV_{OUT}24$	
39	$HV_{OUT}23$	
40	$HV_{OUT}22$	
41	$HV_{OUT}21$	
42	$HV_{OUT}20$	
43	$HV_{OUT}19$	
44	$HV_{OUT}18$	

44-Lead PLCC Package Outline (PJ)

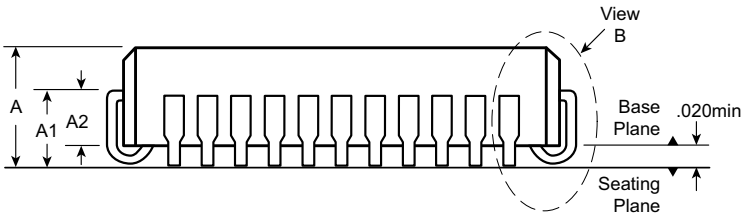
.653x.653in body, .180in height (max), .050in pitch



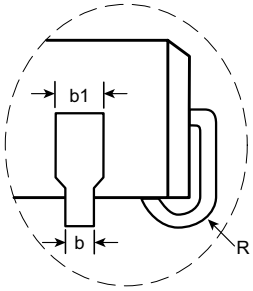
Top View



Vertical Side View



Horizontal Side View



View B

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Actual shape of this feature may vary.*

Symbol		A	A1	A2	b	b1	D	D1	E	E1	e	R
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.685	.650	.685	.650	.050 BSC	.025
	NOM	.172	.105	-	-	-	.690	.653	.690	.653		.035
	MAX	.180	.120	.083	.021	.036†	.695	.656	.695	.656		.045

JEDEC Registration MS-018, Variation AC, Issue A, June, 1993.
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
Supertex Doc. #: *DSPD-44PLCCPJ, Version F031111.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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